National Institute of Technology Karnataka, Surathkal

EC498 - Major Project

A 2.4 GHz Delta Sigma based Fractional Phase Locked Loop for Wireless Communication Applications

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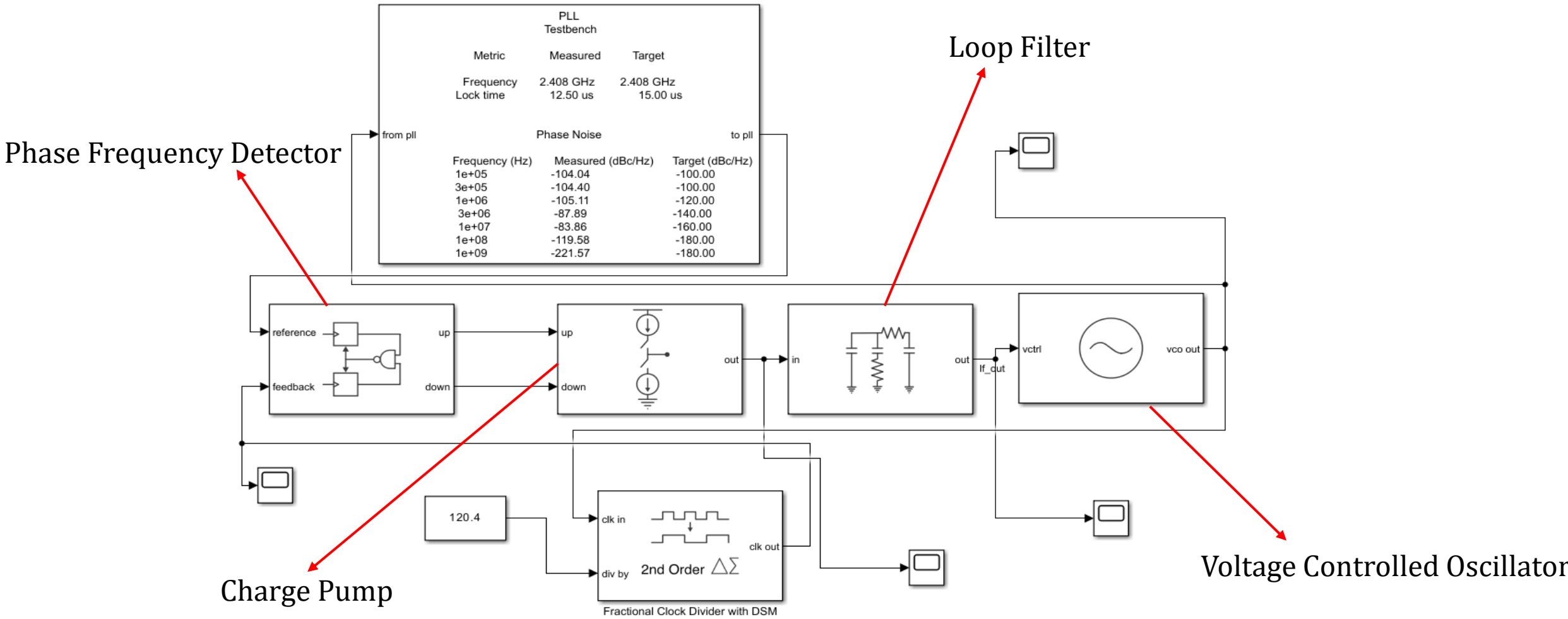
Problem Statement

- To design a 2.4 GHz Delta Sigma based Fractional PLL for frequency synthesis for wireless communication applications. The typical buildings blocks of the PLL are the **Phase Frequency Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillator** and **frequency Divider.**
- Since the Integer N PLLs have a limitation with respect to tuning resolutions, thus the need for fractional N PLL arises. Traditional Fractional N PLLs have very high fractional spurs and hence delta sigma modulation can be used to compensate for these spurs. A **2nd Order Delta Sigma Modulator based Fractional divider** will be designed which will push the energy of the fractional spurs at lower frequencies to higher frequency bands.

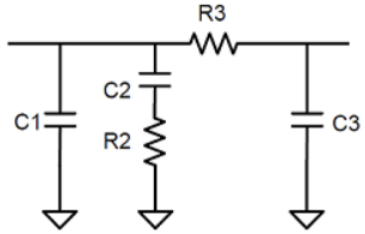
Block Diagram



Design Targets and Objectives

- Technology file: 65 nm CMOS Technology
- Target Frequency band: 2.4GHz to 2.48 GHz
- Fref: 20 MHz , Fout: 2.408 GHz, Divider Ratio of M=120.4, lock time of 15 u sec. Center frequency accuracy : 100KHz.
- Supply Voltage = 1.2V
- Voltage Controlled Oscillator (LC Oscillator)
  - Kvco = 100 MHz/V (MOS Varactors for fine tuning and Capacitor banks for coarse tuning)
  - Free running frequency = 2.4 GHz
- LC Oscillator : higher oscillation frequencies (not limited by propagation delay), lower phase noise, lower tuning range, large area because of integrated inductors.
- Loop filter
  - 3rd Order Passive Filter
  - Phase Margin = 45 degrees.
  - Loop bandwidth = 0.2MHz. (trade off between loop bandwidth and lock time)

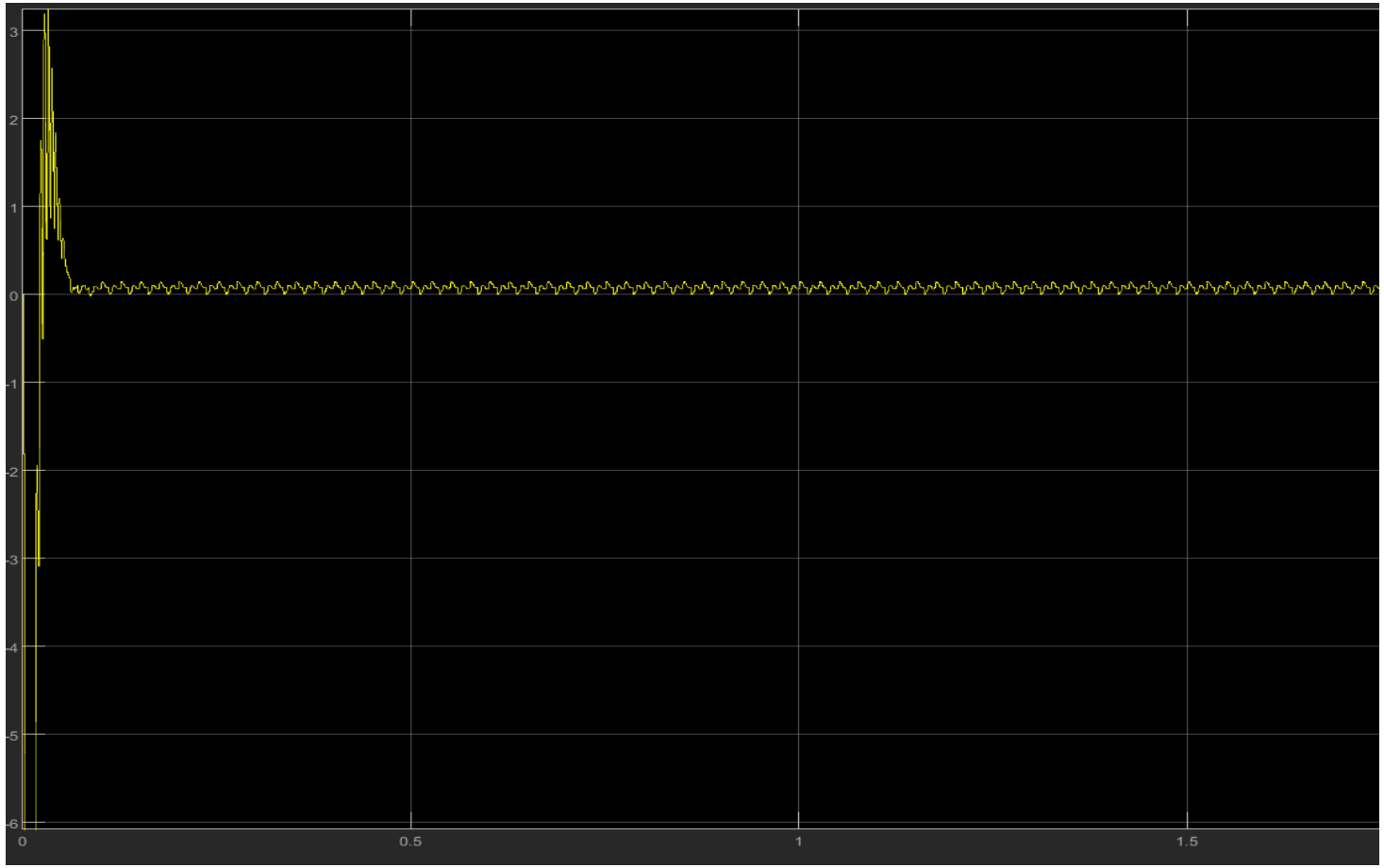
    C1 = 10.9 pF, C2 = 120 pF, C3 = 0.784 pF, R2= 16k ohm, R3 = 204k ohm.
- Charge Pump current : 100 uA.
- 2nd Order Delta Sigma Modulator based Fractional Divider.



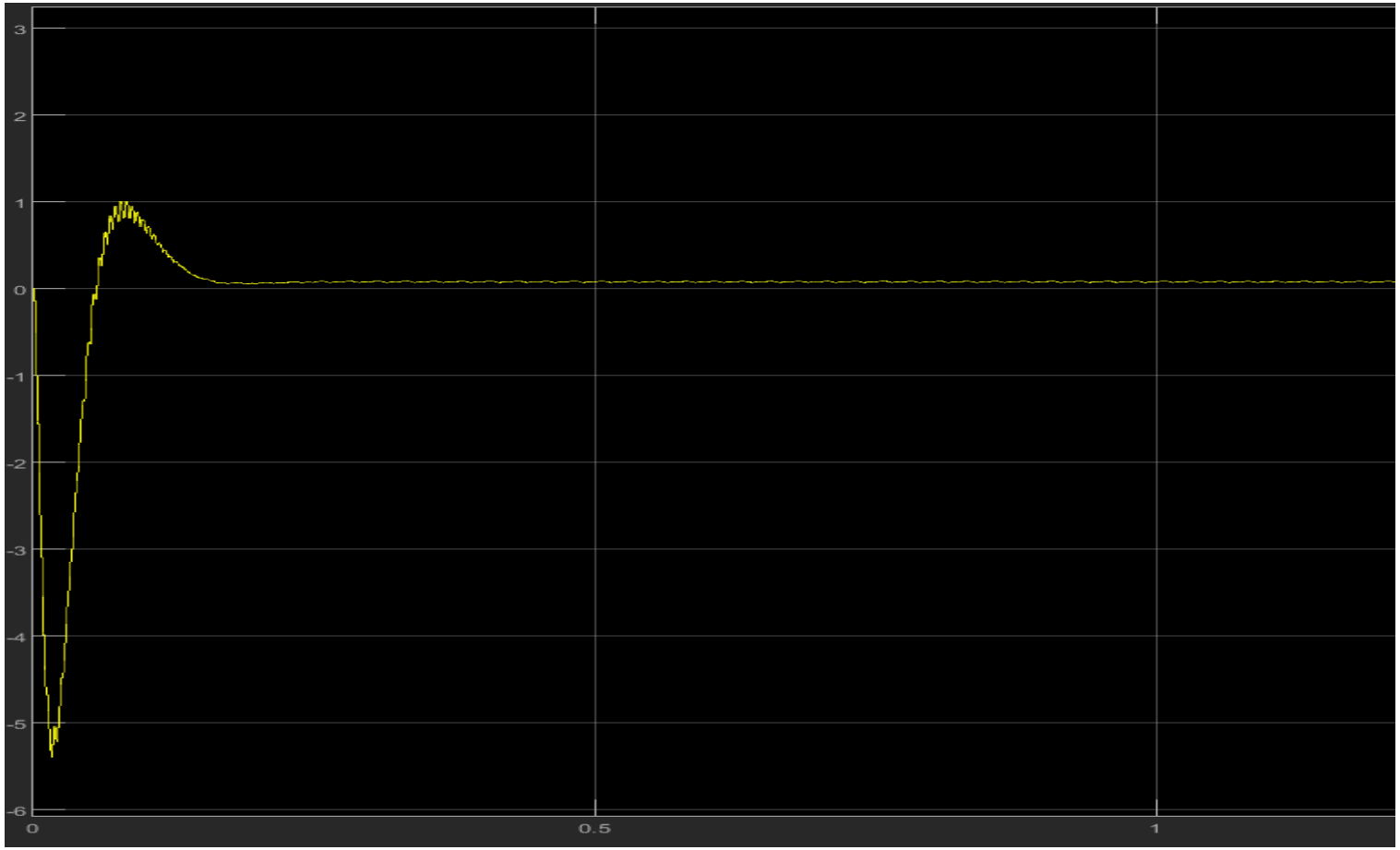
Preliminary Results

Plots of Control Voltage of the VCO with time for various Loop bandwidths

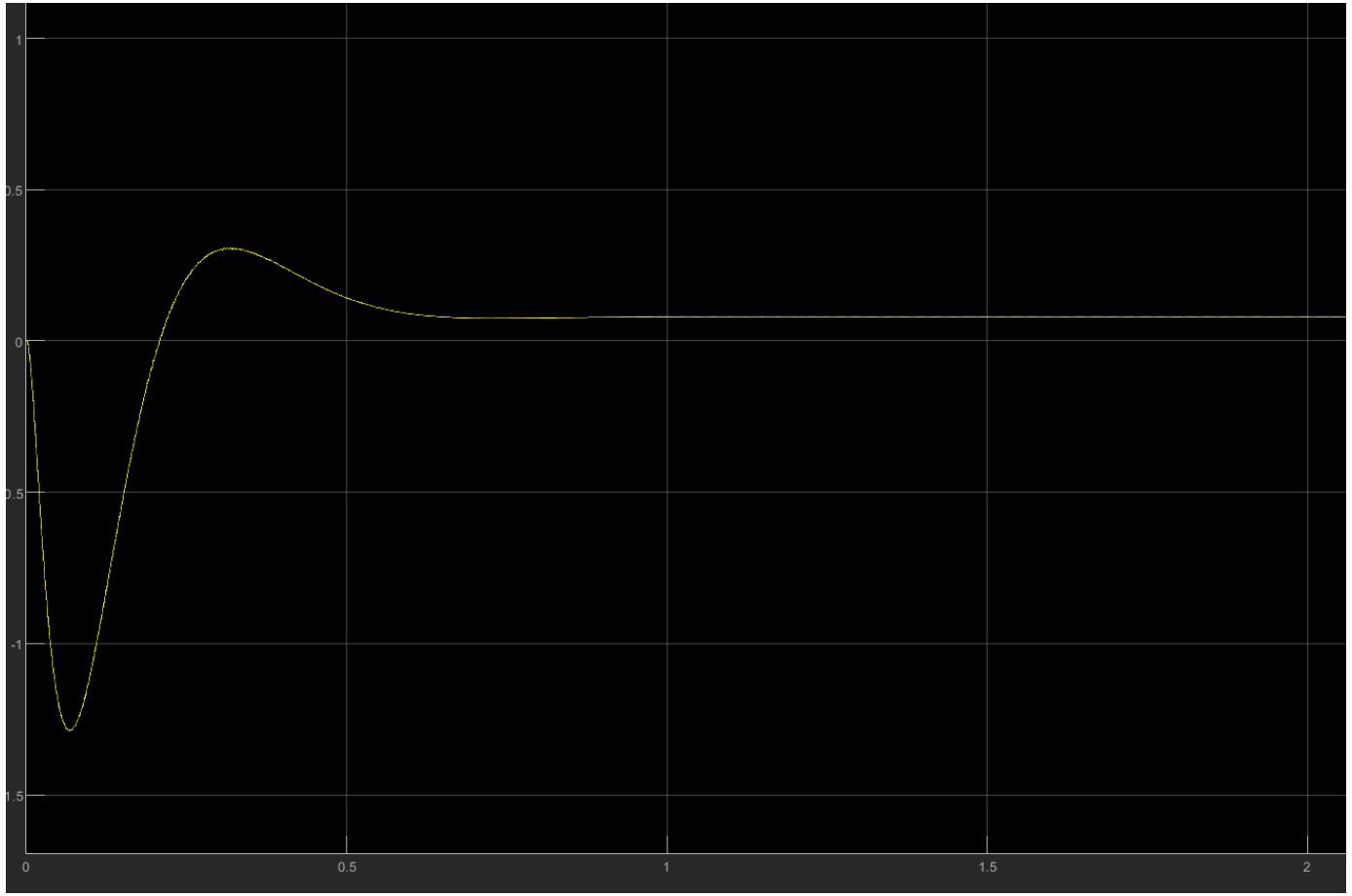
i) Loop Bandwidth = 2MHz, no lock



ii) Loop Bandwidth = 0.8 MHz

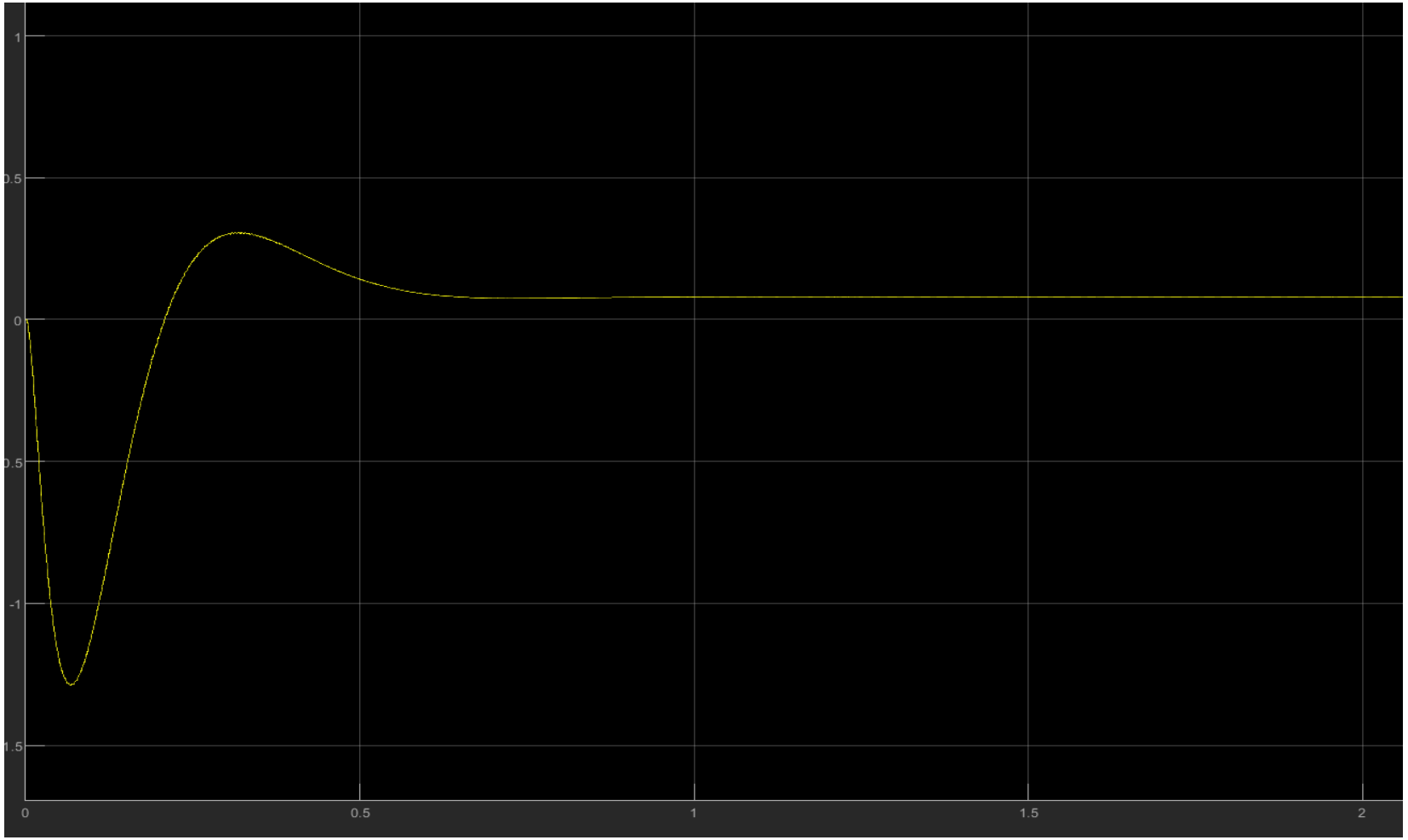


iii) Loop Bandwidth = 0.2 MHz (finalized for the project)

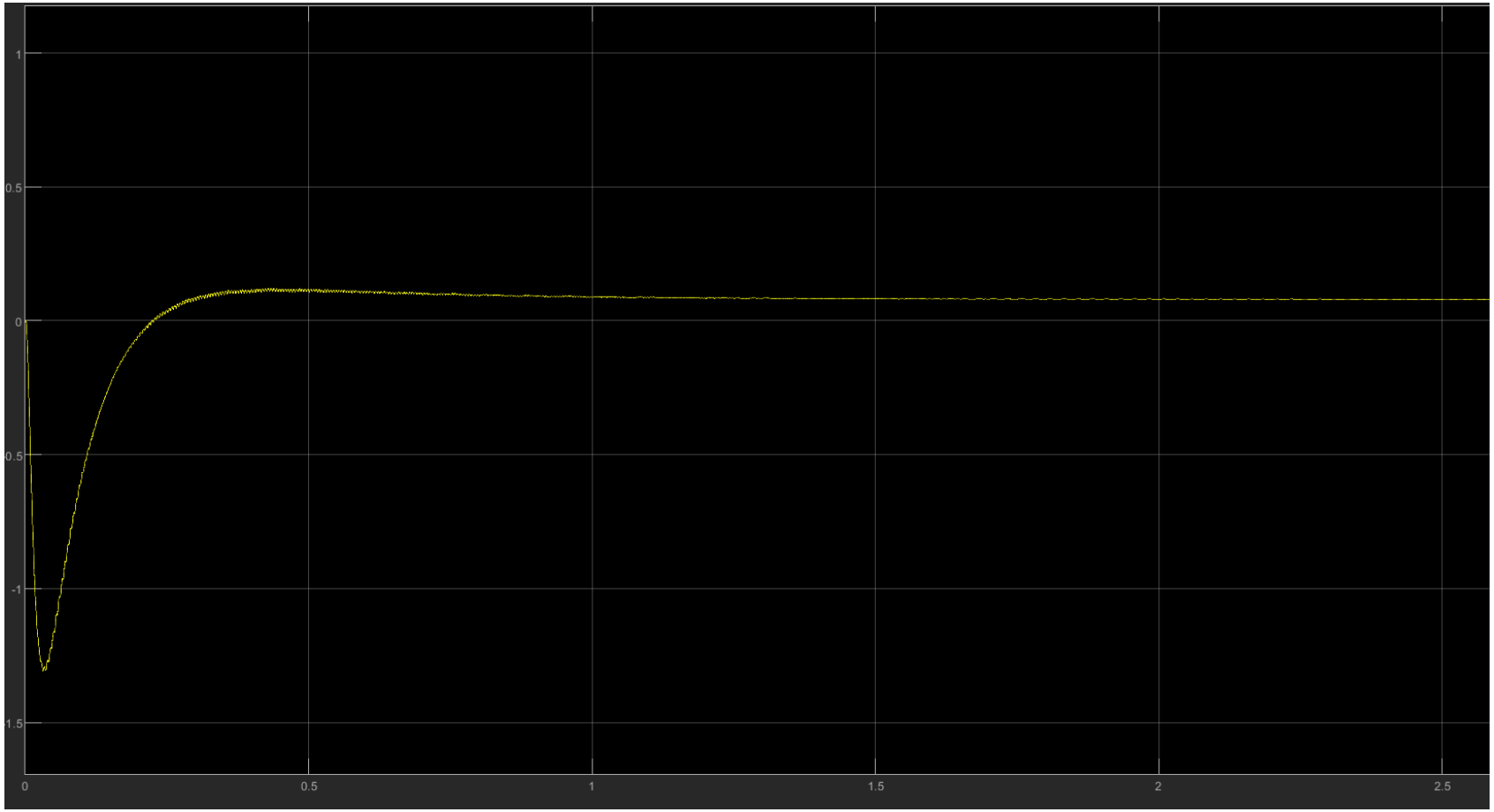


Plots of Control Voltage of the VCO with time for various Phase Margins

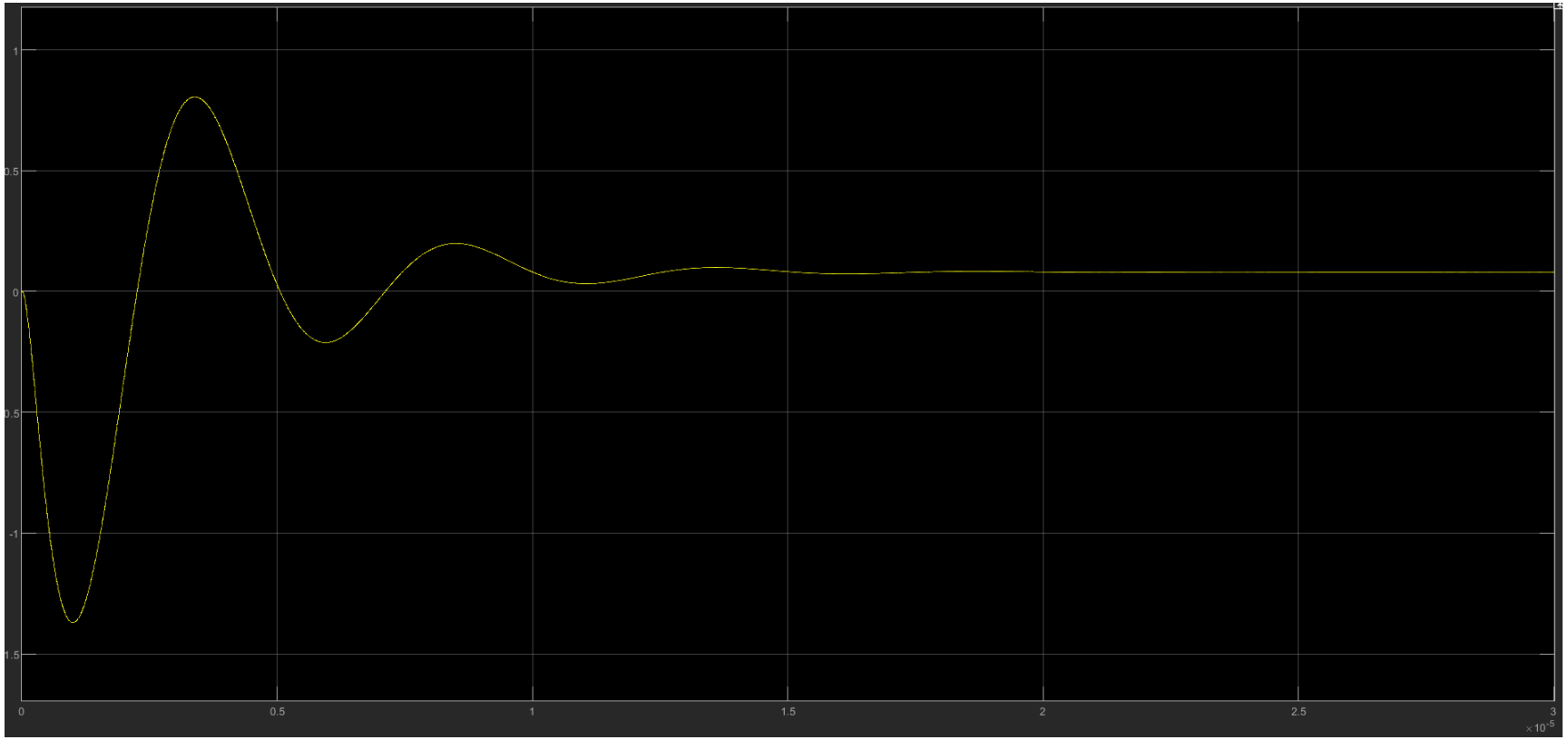
i) PM = 45 Degrees(finalized for the project)



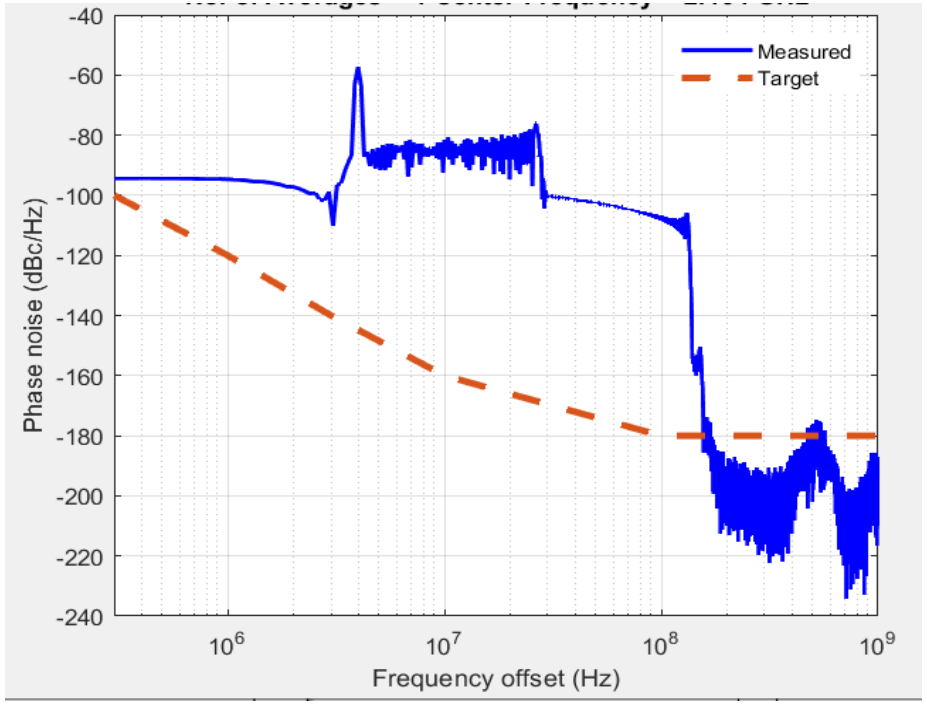
ii) PM = 70 Degrees



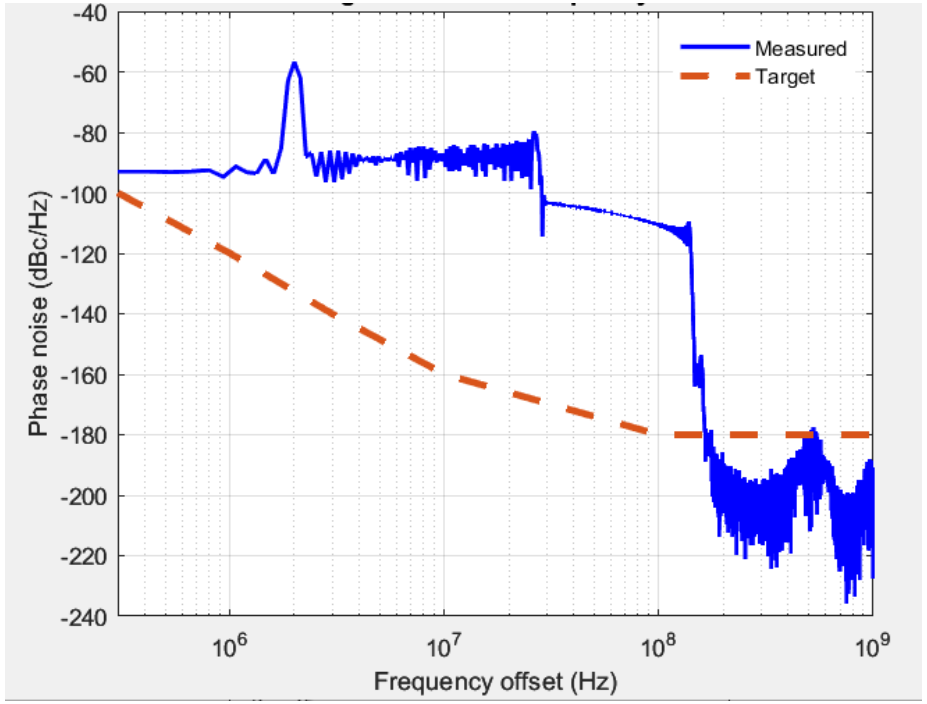
iii) PM = 25 Degrees



Phase Noise Plots – 2nd order Delta Sigma Modulator



Center frequency = 2.408 GHz
-95 dBc/Hz at 1 MHz Offset



Center frequency = 2.416 GHz
-95 dBc/Hz at 1 MHz Offset

TimeLine

Pre Midsem: (1st Week of March)

- Fractional Divider Design (7 weeks):
  - 2nd Order Delta Sigma Modulator
  - Integer Dividers

Post Midsem (2nd Week of April): (6 weeks)

- Integrating the DSM based Fractional Divider with the existing VCO ,PFD and Charge Pump architecture by modifying the parameters of the VCO,PFD and Charge Pump and making minor changes in the loop as per the design specifications.
  - LC Based VCO
  - Phase Frequency Detector (Dead Zone, Blind Zone free)
  - Charge Pump + Loop Filter (Low mismatch charge pumps)

References

- [1]. B. Razavi, Design of CMOS Phase Locked Loops.
- [2] Delta-Sigma Fractional N Phase Locked Loops – Ian Galton.
- [3] P. K. Hanumolu, M. Brownlee, K. Mayaram, and U.-K. Moon, "Analysis of charge-pump phase-locked loops," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 51, no. 9, pp. 1665–1674, Sep. 2004
- [4] B. Razavi, ''The delta-sigma modulator [a circuit for all seasons],'' IEEE Solid State Circuits Mag., vol. 8, no. 2, pp. 10–15, Jun. 2016.
- [5] R. Gu, and S. Ramaswamy, "Fractional-N phase locked loop design and applications", IEEE International Conference on ASIC, pp. 327-332, Oct. 2007.
- [6] S. Pamarti, L. Jansson, and I. Galton, "A wideband 2.4-GHz delta-sigma fractional-N PLL with 1-Mb/s in-loop modulation," IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 49–62, Jan. 2004
- [7] Fractional/ Integer-N PLL – Technical Brief – Texas Instruments
- [8] Phase Locked Loops (PLL) Fundamentals – Ian Collins – Analog Devices
- [9] Delta Sigma PLLs raise the standard for Performance – Application Brief – Texas Instruments

Guide's Approval

Major Project Proposal Inbox ×

Rohan Mallya . <rohanmallya.191cv240@nitk.edu.in>
to Laxminidhi, ADITHI

Respected Sir
We have attached the Major Project proposal below. Kindly approve the same.
Sincerely
Rohan Mallya

One attachment • Scanned by Gmail

Laxminidhi T.
to me, ADITHI

Suggestions-
1. Include some references
2. No space before comma, full stop etc.
Space should be after.

After necessary corrections you can submit.

Regards
Laxminidhi T.