Computer Architecture: unassessed tutorial exercises

Exercise 5.1

The following is a sequence of address references given as word addresses:

1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17

Show the hits, misses and final cache contents for a two-way set associative cache with one-word blocks and a *total size* of 16 words.

Assume LRU replacement.

Exercise 5.2

Show how to configure a twelve-block cache as

(i) direct mapped,

(ii) three-way set associative,

(iii) fully associative.

Suggest a disadvantage of increasing the degree of associativity.

Consider three caches, each consisting of six one-word blocks. Cache D is direct mapped, Cache S is two-way associative, and Cache F is fully associative. Least Recently Used replacement policy is used.

For each of these caches, given the sequence of block addresses

0, 6, 0, 8, 6,

(i) show the cache content after each block access,

(ii) count the number of hits and misses.