PAPER C113

INTRODUCTION TO COMPUTER ARCHITECTURE

Wednesday 6 May 2020, 11:00
Duration: 80 minutes
Post-processing time: 30 minutes
Answer TWO questions

While this time-limited remote assessment has not been designed to be open book, in the present circumstances it is being run as an open-book examination. We have worked hard to create exams that assesses synthesis of knowledge rather than factual recall. Thus, access to the internet, notes or other sources of factual information in the time provided will not be helpful and may well limit your time to successfully synthesise the answers required.
Where individual questions rely more on factual recall and may therefore be less discriminatory in an open book context, we may compare the performance on these questions to similar style questions in previous years and we may scale or ignore the marks associated with such questions or parts of the questions. In all examinations we will analyse exam performance against previous performance and against data from previous years and use an evidence-based approach to maintain a fair and robust examination. As with all exams, the best strategy is to read the question carefully and answer as fully as possible, taking account of the time and number of marks available.

Paper contains 2 questions

Section A

1a The MIPS Rating of a processor is given by how many million instructions it can execute per second. Provide a formula for computing the MIPS Rating of a processor based on its CPI.

Note: "MIPS" in this question does not refer to the MIPS instruction set architecture.

b If processor P1 has a clock rate p times that of processor P2, a MIPS Rating q times that of processor P2, and an instruction count r times that of processor P2 for a given collection of programs, and p, q and r are all larger than one, which processor is faster and by how much?

c The MFLOP Rating of a processor is given by how many million floating-point operations it can execute per second. If processor P3 has a higher MIPS Rating than processor P4, would P3 also have a higher MFLOPS Rating than P4? Explain your answer.

The three parts carry, respectively, 30%, 40%, and 30% of the marks.

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Section B

2 a *Assembly.*

i) *Loops.* Consider the following x86-64 assembly code function with -O optimisation flag:

```
foo:
        movq    %rsi, %rcx
        cmpq    $1, %rdx
        jle     .L4
        movl    $0, %r8d
        movl    $1, %eax
.L3:
        movq    %rdi, %r9
        andq    %rax, %r9
        orq     %r9, %r8
        salq    %cl, %rax
        cmpq    %rax, %rdx
        jg      .L3
.L1:
        movq    %r8, %rax
        ret
.L4:
        movl    $0, %r8d
        jmp     .L1
```

Fill in the blanks in the following `foo` function. You may only use the variable names `x`, `n`, `limit`, `mask` and `result`, not register names.

```
long foo(long x, long n, long limit)
{
    long mask;
    long result = _____;
    for (_____; _____; _____) {
        _____;
    }
    return _____;
}
```

ii) *Accessing Modes.* Assume the following values are stored at the given memory addresses and registers:

Address	Value
0x104	0xAB
0x108	0xDE
0x10C	0xFF
0x110	0x3

Register	Value
%rax	0x2
%rdx	0x108
%rcx	0x3

Array access. Suppose a_q, the address of an integer array Q, and an integer index i are stored in registers `%rdx` and `%rcx` respectively. For each of the following expressions, give its type (int or int*), an expression for its value or if you can, its value, and an assembly code implementation. The result should be stored in register `%rax` if it is a pointer and register element `%eax` if it has data int type.

Expression	Type	Operand Value	Assembly code
Q[3*2-4]			
Q[i*3-2]			
Q+6+i			
&Q[i+2]			

b *Memory Hierarchy.* Assume a system memory with 32MB of main memory and 64KB of cache with 16 bytes block size. The cache uses an LRU (least recently used) policy for eviction and initially is empty.

i) Give the number of cache lines and show how the main memory address is partitioned if the cache is: full associative, direct-mapped and 8-way set-associative.

ii) If the following sequence of addresses is sent to the cache, **0, 12, 16, 20, 32**. What is the miss rate? Show your working.

The two parts carry, respectively, 60% and 40% of the marks.