FINAL

IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

# EXAMINATIONS 2018

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute*

# PAPER C112

# HARDWARE

Friday 18th May 2018, 10:00
Duration: 80 minutes

*Answer ALL TWO questions*

Paper contains 2 questions
Calculators not required

1 Four Mode Counter Circuit

A counter is to work in four modes determined by two input bits as follows.

- When the input is (0,0) the counter goes through the sequence 0,3,2,1,0,3,2,1, $\cdots$
- When the input is (0,1) the counter goes through the sequence 1,2,0,1,2,0, $\cdots$
- When the input is (1,0) the counter goes through the sequence 1,3,0,1,3,0, $\cdots$
- When the input is (1,1) the counter goes through the sequence 3,2,3,2, $\cdots$

a i) Draw the state transition diagram that corresponds to the above specification.

ii) Construct a state transition table for the counter in the format given below. Use "don't care" values wherever possible.

| $I_1$ | $I_0$ | This State | $Q_1$ | $Q_0$ | Next State | $D_1$ | $D_0$ |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | | | |
| 0 | 0 | 1 | 0 | 1 | | | |
| 0 | 0 | 2 | 1 | 0 | | | |
| 0 | 0 | 3 | 1 | 1 | | | |
| 0 | 1 | | | | | | |
| 0 | 1 | | | | | | |
| 0 | 1 | | | | | | |
| 0 | 1 | | | | | | |
| 1 | 0 | | etc | | | | |

b Design the state sequencing logic that implements the above table. (You do not need to draw the circuit)

c Given that the counter state is to be shown on a seven segment display, design the output logic that will provide the signal for the lower right vertical segment of the display.

d Determine whether your circuit will work correctly for all possible changes of the inputs. There is no need to change your design if it could fail under certain conditions.

*The four parts carry equal marks.*

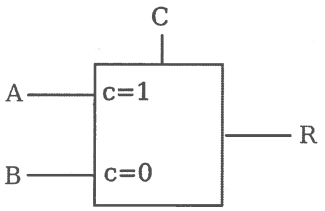
2a A 1-bit full subtractor circuit is defined by the following truth table:

| $A$ | $B$ | $P$ | $D$ | $B$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

Derive equations for D (the difference) and B (the borrow) starting from the canonical minterm form and simplifying them as far as possible.

b Using a functional block of a 1-bit full subtractor (based on your design of the previous part) design a four bit subtractor circuit. Explain under what circumstances a "Payback-In" in would be required.

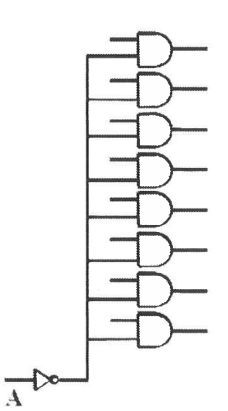
c A 2-input 1-bit multiplexer is represented by the following functional block:



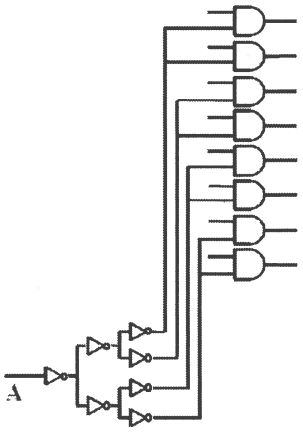

Design a circuit for this 2-input 1-bit multiplexer using only two input NAND gates.

d Show how a 2-input NAND gate could be made using only two 2-input 1-bit multiplexers.

e The figure below shows two possible implementations for an enable circuit for an eight bit multiplexer. Which circuit will have the fastest response to a change in the input A? Explain your answer.




**Implementation 1**




**Implementation 2**

*The five parts carry equal marks.*