Computer Architecture: unassessed tutorial exercises

Exercise 6.1

With a 32-bit virtual address, 4 kilobyte pages, and 4 bytes per page table entry, calculate:

(a) the number of page table entries,

(b) the size of the page table.

Exercise 6.2

(a) Give one advantage and one disadvantage for:

- a direct-mapped cache,
- a fully-associative cache.

(b) Explain how an n-way set-associative cache works. What is the effect of increasing n on the size and the speed of the cache?

(c) Provide a diagram of an n-way set-associative cache, dealing with p-bit addresses, which contains m blocks. How many bits are there in a tag for this cache?

(d) Provide a diagram of a direct-mapped cache, dealing with p-bit addresses, which contains m blocks, and each block contains n words. How many bits are there in a tag for this cache?