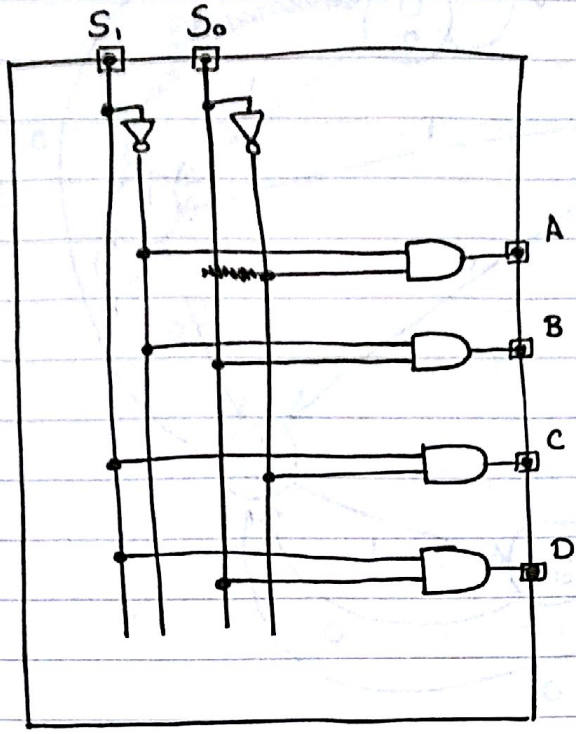
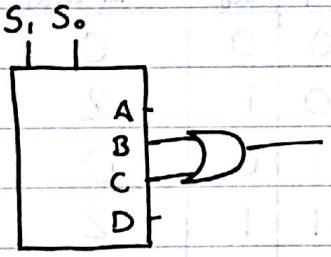
2013

1) a)

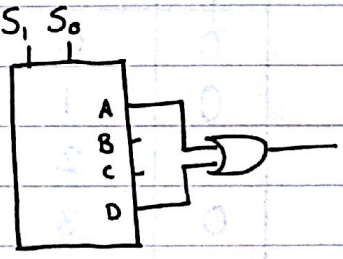


b) i)



XOR

ii)



XNOR

c)

A	B	G	E
0	0	0	1
0	1	0	0
1	0	1	0
1	1	0	1

$G = A \cdot B'$

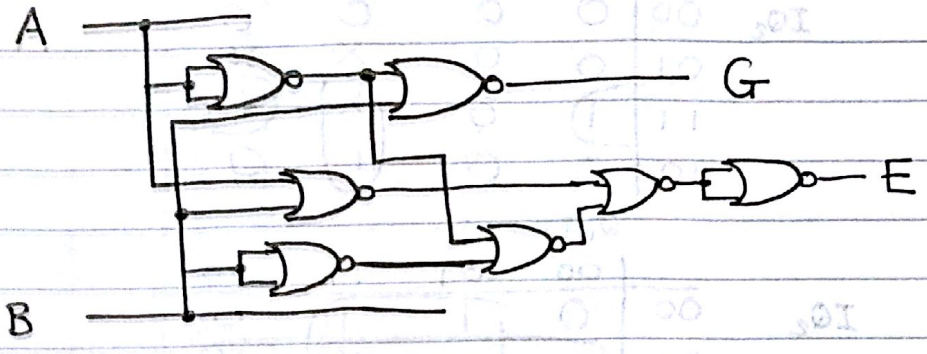
$= (A' + B)'$

$= ((A+A)' + B)'$

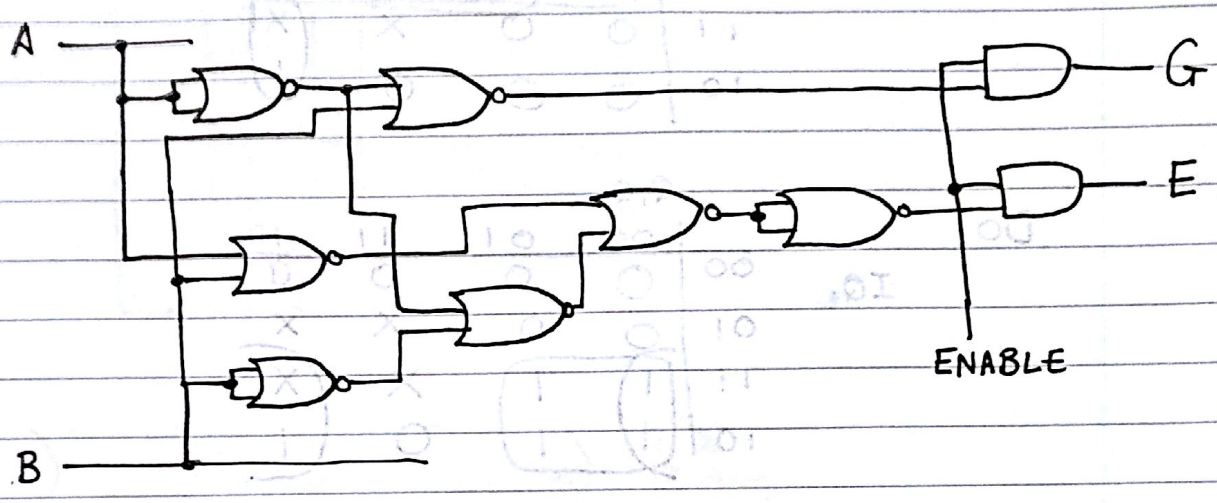
$E = A' \cdot B' + A \cdot B$

$= (A+B)' + (A'+B')'$

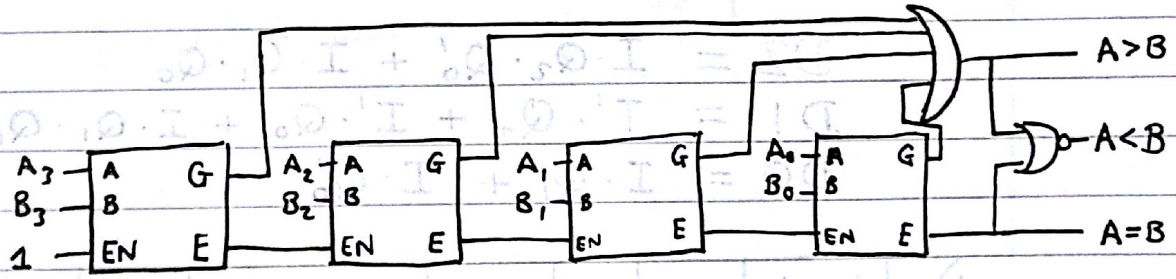
$= (((A+B)' + ((A+A)' + (B+B)')')')'$



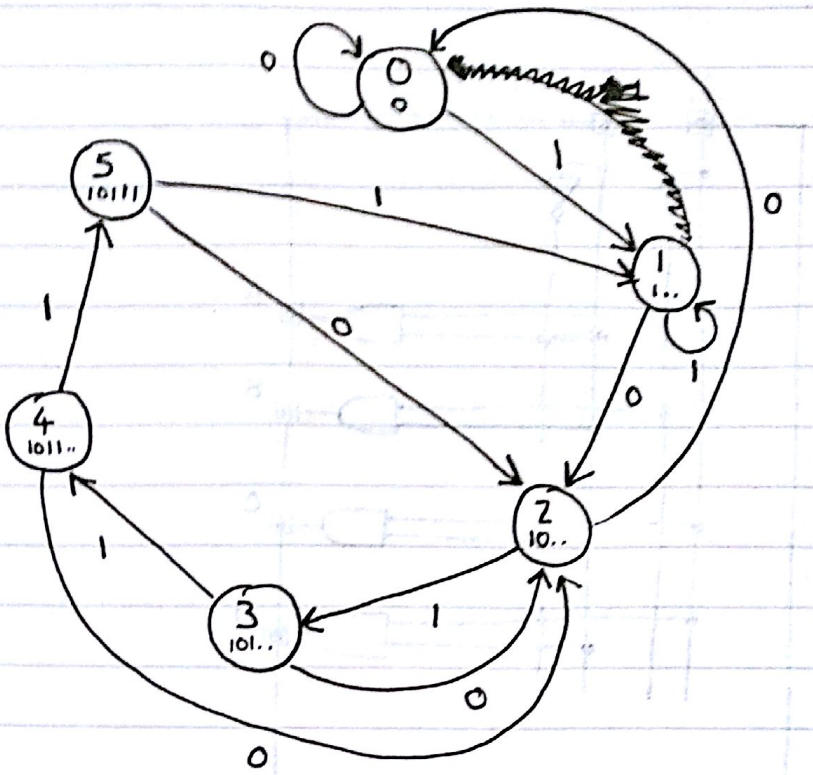
d)



e)



2) a)



b)

Input	This State	Q_2	Q_1	Q_0	Next State	D2	D1	D0
0	0	0	0	0	0	0	0	0
0	1	0	0	1	2	0	1	0
0	2	0	1	0	0	0	0	0
0	3	0	1	1	2	0	1	0
0	4	1	0	0	2	0	1	0
0	5	1	0	1	2	0	1	0
0		1	1	0	X	X	X	X
0		1	1	1	X	X	X	X
1	0	0	0	0	1	0	0	1
1	1	0	0	1	1	0	0	1
1	2	0	1	0	3	0	1	1
1	3	0	1	1	4	1	0	0
1	4	1	0	0	5	1	0	1
1	5	1	0	1	1	0	0	1
1		1	1	0	X	X	X	X
1		1	1	1	X	X	X	X

D2

IQ_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	X	X
11	1	0	X	X
10	0	0	1	0

D1

IQ_2 \ Q_1Q_0	00	01	11	10
00	0	1	1	0
01	1	1	X	X
11	0	0	X	X
10	0	0	0	1

D0

IQ_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	X	X
11	1	1	X	X
10	1	1	0	1

$$D2 = I \cdot Q_2 \cdot Q_0' + I \cdot Q_1 \cdot Q_0$$
$$D1 = I' \cdot Q_2 + I' \cdot Q_0 + I \cdot Q_1 \cdot Q_0'$$
$$D0 = I \cdot Q_1' + I \cdot Q_0'$$

d)

Input	Q_2	Q_1	Q_0	Next State	D2	D1	D0
0	1	1	0	2	0	1	0
0	1	1	1	0	0	0	0
1	1	1	0	7	1	1	1
1	1	1	1	4	1	0	0

If the circuit starts in one of the unassigned states, it will fall into one of the known states straight away. The circuit will, however, think it is part way through the sequence unless some kind of reset is added.

e) $O = Q_2 \cdot Q_1' \cdot Q_0$