Computer Architecture: Unassessed exercise 3

Exercise 3.1

(a) For a given program, 10% of the code is responsible for 90% of the execution time. A co-proceesor is used to speed up this 10% of the code by k times; what is the overall speedup?

(b) A Field Programmable Gate Array (FPGA) is an elecctronic device which contains programmable logic blocks connected together by programmable interconnections.

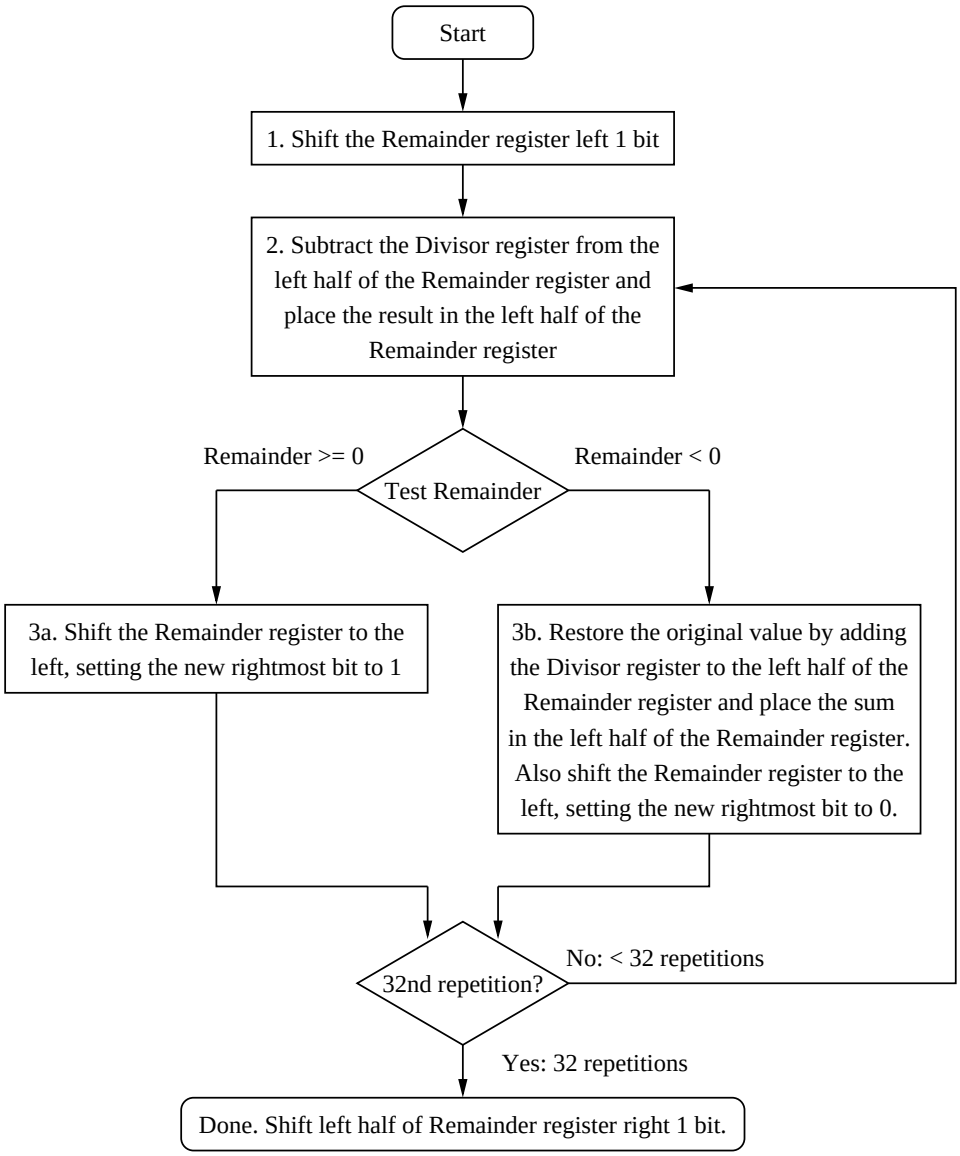
A new FPGA is obtained by replacing a fraction α of the area of the original FPGA by new elements which are p times faster and q times smaller. Assuming that computation is distributed uniformly across an FPGA, how much faster and smaller overall is the new FPGA campared with the original one?

Exercise 3.2

The division algorithm described in the textbook (see figure on the next page) is called *restoring division*, since each time the result of subtracting the divisor from the dividend is negative, the divisor has to be added back to the dividend to restore the original value.

Recall that shift left is the same as multiplying by two. Let us look at the value of the left half of the *Remainder*, starting from step 3b and then go to step 2. This involves computing the value (*Remainder* + *Divisor*) $\times$ 2 - *Divisor*, which is created from restoring the *Remainder* by adding the *Divisor*, shifting the sum left, and then subtracting the *Divisor*. Simplifying, we obtain the value *Remainder* $\times$ 2 + *Divisor*.

Based on this observation, develop a non-restoring division algorithm using the notation in the figure that does not add the *Divisor* to the *Remainder* in step 3b. Show that your algorithm works by dividing the binary number 00000111 by 0010.



The restoring division algorithm described in the course textbook.