

Figure 1 shows a 3x3 grid of Petri nets. The top row has a Petri net with one place 'P' and one transition 'R' leading to a place 'Q'. The middle row has a Petri net with one place 'P' and one transition 'R' leading to a place 'Q', which then leads to a place 'S'. The bottom row has a Petri net with one place 'P' and one transition 'R' leading to a place 'Q', which then leads to a place 'S', which then leads to a place 'T'. The labels R, R+, R1R2, and R1 R2 are placed above the corresponding Petri nets.

with  $\epsilon$  (curr pos of parser).  $X$   
 (mid-way),  $X \rightarrow ABC$   
 do whole rule). Use LR(0) items  
 (progress of parser through rule).

$B$   $\xrightarrow{\text{new}} X \rightarrow AB \cdot C$

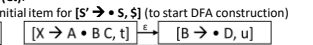
each rule  $B \rightarrow \cdot D$  add  $\epsilon$  trans:  
 $\epsilon$   $\xrightarrow{\text{new}} B \rightarrow \cdot D$

**Making LR(0) Parser:**

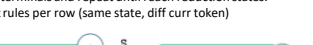
- CFG  $\rightarrow$  LR(0) items
- Items  $\rightarrow$  NFA
- NFA  $\rightarrow$  DFA
- Generate parsing table from DFA

If there is more than one action for a cell in an LR(0) table, the grammar is not LR(0).

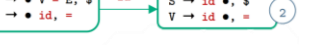
by a string derivable from  $Ct$ ,  $B$  is followed by  $Ct$  if the string  $B$  is followed by  $Ct$  in  $(Ct)$ .



one box and expand all non-terminals into their initial diff symbols – remember above about changing terminals and repeat until reach reduction states.



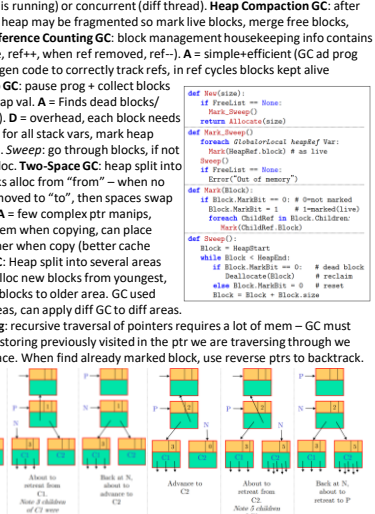
→ • S, \$ (0) → S' → S •, \$ (1)



→  $V \bullet = E, \$$

**Semantic Analysis:** checks statically at compile time if the prog is semantically valid within lang rules. Provides info for next phases

**Garbage Collection:** ensures alloc vars are de-alloc'd when no longer used. Reqs: correctness (don't dealloc live data), performance (fast + low mem overhead to red impact on prog performance), compiler supported (c must provide info for which vars point to heap and pointers in each block via special subroutines for GC or as part of type desc for obj data). Can be run 1-shot (pause





**Feasible Path:** a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z

**Infeasible CFG path:** a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z

**Caller/Callee Saved:** Caller: c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z  
Callee: a, b, c, d, e, f, g, h, i, j, k, l, m, n, o, p, q, r, s, t, u, v, w, x, y, z

D = can require static anal (calling virtual/overloaded fns)

**Optimisations:** Use LL info (Instr types, ISA, order of Instrs)

we get lower. E.g. *Instr Sched*: in pipelined arch, instrs to allow parallel processing. D = requires some code through assembly in order, looking for obvious cases that can be reordered (e.g. basic blocks of code that are followed by load of same location). Very easy to impl (phase ordering problem – what order should ops be a)

Local	Local	Global	Global
Basic Blocks	Basic blocks (single entry exit points) (e.g. expression evaluation on the level of instructions)	Global	Optimisation on the scale of whole procedure
Fast+Easy to Validate		Intraprocedural	Optimisation over the whole program
Global Procedures		Intraprocedural Whole Program	
slow, very complex + rare			

**Interference Graphs from Live Range sets** from each block to construct instrs from each block to construct instrs

$\{(T0, \{T0, T1, T2, T3\}), (T3, \{T1, T1, T0, T2, T3, T4\}), (T4, \{T2, \{T1, T2, T0, T3, T4\})\}$ . Then on

Infesible Pattern: a, b, f, g – valid in graph but  
 become difficult with many call sites.  
 callees saves regs it is using to preserve them  
 (callee can't clobber). *Callee*: callee saves regs it  
 needs to use. Both can end up saving redundant  
 info as they don't know which regs the other  
 will use (esp problem in separate compilation of  
 code). Some make reg preservation decisions  
 upfront, others define *Application Binary  
 Interface* to ensure linked lib calls save right regs.  
**Intel's Law**: every 2 years, density of transistors  
 gets integrated circuits doubles. This is slowing down  
 exponentially. More optimised compilers are now the  
 way forward for progress.

ins) requires type info). **Low-level** (ins) to output. Note can use HL info as can't impact processing speed so reorder dependency anal. **Peephole Optimisation**: scan opt. Can catch some worst cases (e.g. store smallest, just consider 2 adj insns). **D** = applied to get best res?

Runs quickly and easy to validate.

Can have worse than  $O(n)$  (Linear) complexity given  $n$  represents instructions, basic blocks or variables.

Rare and hard to avoid excessive compile times.

Use the LiveOut reference graph:

$\{T_0, T_3, T_2, T_1, T_4\}$   
 $\{T_3, T_4, T_2, T_1\}$

graph colouring :)

Uses/G of prior Defines Iterative

1. Find
2. Iter T
3. Rest
4. new Live
5. Stop

Improvement

To reduce defs de anal. T

no stor

Don't

**Back Edges:** edge from a node to its ancestor. **Natural LCA**  $(n, h)$  is the set of nodes on the path from  $n$  to  $h$  which are dominated by  $h$ , and for which does not contain header node  $h$ .

- **loops:** given set  $S$  of nodes which
  - **loop:** there is a single header
    - there is a path from  $h$  to any  $x \in S$ .
    - $S$ . There is a path from any  $x \in S$  to  $h$  (and no others in  $S$ ).
  - All non-loop nodes can only reach  $h$  (and no others in  $S$ ).
- **node  $d$  dominates  $n$**  if every path from the start to  $n$  goes through  $d$  (every edge to itself). To find nodes which dominate:
  - node: 1. Set  $Dom$  to set of all nodes (as below) as start
  - loop: 2. Once sets stop changing
  - $n \rightarrow h$  where  $h$  dominates  $n$  as header
    - **loop:** natural loop of a back-edge
    - $S$  s.t.: all nodes  $x \in S$  are dominated by  $h$
    - all  $x$  there is a path  $x \rightarrow h$
    - $h$ . This represents a loop with header  $h$

want to know what each pointer var in the program in the code corresponds to an allocation site (there are the alloc occurred). The  $\text{PointsIn}(n)$  for a node  $n$  is the set of all allocation sites that point to  $n$  before the node is allocated. The effect of each instr on the points-to set is  $\text{pointsIn}(n)$  and  $\text{PointsOut}(n)$ . After new dest reg may be modified.

$$\text{pointsIn}(n) = \bigcup_{p \in \text{pred}(n)} \text{pointsOut}(p)$$

$\text{effect}(\text{pointsIn}(n), \text{instruction}_n)$   
 $\text{t} \rightarrow \text{CFGNode} \rightarrow \text{PointsToSet}$   
 $\text{Cmp r1 r2}) = \text{pts}$   
 $\text{Egt label}) = \text{pts}$   
 $\text{New n r}) = \text{pts} \cup \{r, \text{id}\}$   
 $\text{Mov r1 r2}) =$   
 $\text{pts} \cup \text{union}(\{r1, r2\} \cap \{r1, id\} < \text{pts})$   
 $\text{r2 pts} = \{r1, r2\} \cap \{r1, id\} < \text{pts}, r1 = r2$

$\text{atsIn}(6) = \{(D0,1),(D3,2)\}$   
 $\text{atsOut}(6) = \{(D0,1),(D3,1),(D3,2)\}$