IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2015

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
BEng Honours Degree in Mathematics and Computer Science Part I
MEng Honours Degree in Mathematics and Computer Science Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C113=MC113

ARCHITECTURE

Friday 8 May 2015, 10:00
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators required

Section A (Use a separate answer book for this Section)

1 a The P1 processor has 32-bit instructions and 16 registers. All instructions have an 8-bit opcode field. Memory address takes up 2 bytes, and each piece of data stored at a memory location takes up 4 bytes.

Each arithmetic instruction, such as an addition or a subtraction instruction, has three register fields specifying the source and the destination registers, and the remaining bits are not used. The memory load instruction and the memory store instruction each has a register field and a memory address field; the remaining bits are not used.

Show the format of an arithmetic instruction and the memory load instruction, indicating the number of bits in each field, including the fields that are not used.

b A program has three assignment statements:

```
C = A + B; D = A - B; E = A + C;
```

Provide the P1 processor instructions for the above program, and calculate:

i) the number of bytes that all the instructions take up,

ii) the total number of bytes transferred between processor and memory,

given that the variables `A`, `B`... are initially stored in the memory.

c The P2 processor has 64-bit instructions and no registers. All instructions have an 8-bit opcode field. Memory address takes up 2 bytes, and each piece of data stored at a memory location takes up 4 bytes. Each arithmetic instruction, such as an addition or a subtraction instruction, has three fields specifying the source and the destination memory addresses, and the remaining bits are not used.

Show the format of an arithmetic instruction for P2, indicating the number of bits in each field, including the fields that are not used.

d Provide the P2 processor instructions for the program in Part b, and repeat the two calculations in Part b.

e Which processor has smaller size for the instructions implementing the program in Part b? Which processor requires fewer memory accesses, given by the total number of bytes transferred between processor and memory? Provide an explanation if the answers to the above two questions are different.

The five parts carry, respectively, 20%, 25%, 10%, 25% and 20% of the marks.

Section B (Use a separate answer book for this Section)

2a Explain briefly **three** different modes of memory addressing for the Intel 64 architecture and their usage in assembly language.

b Using IEEE Single Precision format, convert the following hexadecimal numbers **CC800000** and **CC8800000** into binary and decimal. Show your work clearly.

c Express the following decimal number **-525.25** in binary and hexadecimal using the IEEE Single Precision Format. Show your working clearly. (If you need extra bits in the calculation, use rounding rather than truncation for calculating your result). Is the IEEE representation accurate?

d Translate the **fun** routine in the following program into **commented** Intel 64 assembly language:

```
void fun (int x)
{
  int y, z;

  z = 13;
  y = x * y;
  if (x == 2)
    y = 7;
  else
    z = x + y;
  while (x > 0)
    z = z + x;
    x--;
}

int main ()
{
  int l = 8;
  fun(l);
}
```

Your solution **must not** use global variables, must save and restore registers correctly and assume 64-bit `int`s.

The four parts carry, respectively, 10%, 20%, 20%, and 50% of the marks.