IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2017

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C112

HARDWARE

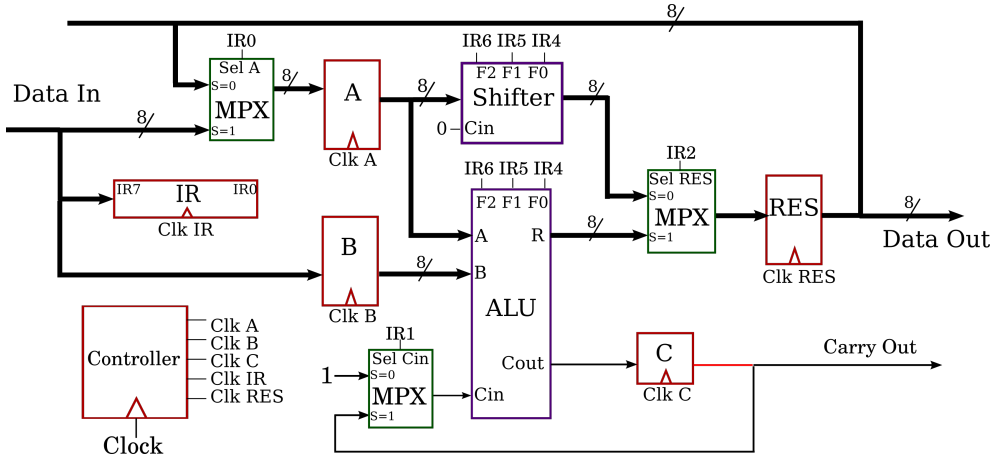
Wednesday 10 May 2017, 10:00
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators not required

1 The Manual Processor

An 8-bit manual processor has the following block diagram. (This is a slightly improved design from the one used in the lectures)



The functions of the ALU and the shifter are defined by the values of their function select bits (F2, F1, F0) according to the following table:

Selection Bits	000	001	010	011	100	101	110	111
ALU Function	0	B-A	A-B	A plus B	A xor B	A+B	A.B	-1
Shifter Function	Unchanged	Rotate left	Shift left C=0	Shift left C=Cin	Rotate Right	Shift Right C=0	Shift Right Cin=I[7]	Shift Right C=Cin

The controller makes the processor go through a fixed cycle of five states in which the following clock gates are applied:

State	Clock
1	CLKIR
2	CLKA
3	CLKB and CLKC
4	CLKIR
5	CLKRES and CLKC

a Draw the circuit of the multiplexer connected to Cin on the ALU, and explain why it is needed.

b Explain, with appropriate block diagrams, how the shifter circuit can be built using multiplexers.

c An average instruction (AVE) is to be designed which will compute the average of two numbers. It will require two cycles through the five states of the controller defined in the table above. The numbers to be averaged will be read from the *Data In* lines during states 2 and 3 of the first processor cycle. You can assume that arithmetic overflow will not occur when they are added together.

Determine the register transfers that will be carried out during each state of the two processor cycles, by constructing a table in the following form showing which registers are loaded and from where. Indicate the purpose of each register transfer.

State	Source	Destination	Purpose
1	Data In	IR	The first instruction byte is loaded
2	Data In	A	The first number is loaded into register A
3			
4			
5			
1			
2			
3			
4			
5			

d Find the contents of the instruction register in states 2 and 5 of both the processor cycles for the AVE instruction. Use don't care values where you can.

The four parts carry equal marks.

2 A Sequence Recognition Circuit

A circuit is to read a bit sequence (synchronised to a clock which is also provided) and produce an output of 1 whenever the bit combination 100111 is recognised. The sequences may be overlapped. The bits arrive with the most significant first.

a Draw the finite state machine diagram of the circuit, naming your states as follows:

A	received 0
B	received 1
C	received 10
D	received 100
E	received 1001
F	received 10011
G	received 100111

b Construct a state transition table in the format given below based on your answer to part a.

Input	This State	Q2	Q1	Q0	Next State	D2	D1	D0
0	A	0	0	0				
0	B	0	0	1				
0	C	0	1	0				
0	D	0	1	1				
0	E	1	0	0				
0	F	1	0	1				
0	G	1	1	0				
0								
1								
etc								

c Design the state sequencing logic that implements the above table. (You do not need to draw the circuit)

d Design the output logic.

e Determine what will happen to the circuit if it goes into the unused state ($Q_2 = Q_1 = Q_0 = 1$) when it is switched on.

The five parts carry equal marks.