IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2016

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
BEng Honours Degree in Mathematics and Computer Science Part I
MEng Honours Degree in Mathematics and Computer Science Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C113=MC113

ARCHITECTURE

27 April, 2016, 1000
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators required

Section A (Use a separate answer book for this Section)

1 a An 8-bit processor P has a single register R with the following instructions, where n is a 4-bit number included as part of the instruction:

operation	bit 7–4	bit 3–0	meaning
load	0001	n	load the value of the memory location at the address n into R
store	0011	n	store the value of R into the memory location at the address n
add	0000	n	compute the sum of n and the value of R, and place the value of the sum in R
jump	0010	not used	unconditional jump to the instruction in memory whose address is specified by R

Describe the above four instructions using a suitable Register Transfer Language.

b In addition to the register R, the datapath for P in Part a also has a program counter PC, an instruction register IR, an instruction memory IM situated between the PC and IR, an incrementer INC for incrementing the PC, an ALU with inputs from R and from a sign-extension circuit SX, and the ALU output connected to the ALUout register. There is a data memory DM with a data input from ALUout and address input from selected bits of IR. There are also two multiplexors controlling information flow. The ALU can add its two inputs, or select one of its inputs and pass it to the output.

Provide a diagram showing how these components are connected together for the processor P. The diagram does not need to include the control unit.

c Provide a state diagram showing the appropriate register transfer actions in each state for a control unit controlling the multi-cycle datapath in Part b. For example, one of the states may contain the register transfer action IR = IM[PC].

The three parts carry, respectively, 20%, 40%, 40% of the marks.

Section B (Use a separate answer book for this Section)

2a Consider the assembler code for a function `void foo(){int a,b; ...}`. Explain two ways of how the values of the local variables `a` and `b` can be stored for use in `foo`.

b Using IEEE Single Precision format, convert the following hexadecimal numbers **C1110000** into binary and decimal. Show your work clearly.

c Express the following decimal number **-666.75** in binary and hexadecimal using the IEEE Single Precision Format. Show your working clearly. (If you need extra bits use rounding rather than truncation for calculating your result).

d Translate the **rex** routine in the following program into **commented** Intel 64 assembly language:

```
int rex (int a,b,c) {
  int d,e;
  a = 3; b = 2;
  d = 2*(b-c);
  while (d != 0) do {
    if (d > 0) {
      d = d-1
    } else {
      d = d+1
    }
    e = rex(d,a,c)
  }
  return d;
}

int main () {
  int a = 8; int b = 7; int c = 6;
  a = rex(a,b,c);
}
```

Your solution **must not** use global variables, must save and restore registers correctly and assume 64-bit `int`s.

The four parts carry, respectively, 10%, 20%, 20%, and 50% of the marks.