

(12)

- cycle 1: $IR = Mem[PC], PC = PC + 4$

- cycle 2: $A = \text{Mem}[\text{zero-ext}(IR_7 - 13)]$
 - cycle 3: $B = \text{Mem}[\text{zero-ext}(IR_0 - 6)]$
- } Assuming Memory's output can be the input to A and B

- cycle 4: $ALV_{Out} = A - B$

- cycle 5: $\text{Mem}[\text{zero-ext}(\text{IR}_{0-6})] = \text{ALUOut}$

JIN instruction:

- cycle 1: $IR = Mem[PC]$, $PC = PC + 4$

- cycle 2: if $N=1$: $PC = \text{zero-ext}(IR_{0-13})$


$$PC = PC + 4$$

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if op == 1
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$$A = \text{Mem}[\text{sign-ext}(R_7, 13)]$$

$$B = \text{Mem}[\text{sign-ext}(1R_{0-6})]$$

$$ALV_{out} = A - B$$
$$\text{Mem}[\text{sign-ext}(IR_{0-6})] = ALU_{\text{out}}$$

STATE 4

STATE 1: MemRead = 1, AddrFromIR = 1, Awrite = 1

STATE 2: MemRead = 1, AddrFromIR = 0, Bwrite = 1

STATE 4: MemWrite = 1, AddrFromIR = 0

$$(2b) \quad 128 \text{ MB} = 128 \cdot 2^{20} \text{ B} = 2^7 \cdot 2^{20} \text{ B} = 2^{27} \text{ B}$$

$$\text{CACHE SIZE} = 64 \text{ KB} = 64 \cdot 2^{10} \text{ B} = 2^6 \cdot 2^{10} \text{ B} = 2^{16} \text{ B}$$

$$(i) \quad \# \text{ CACHE LINES} = \frac{\text{CACHE SIZE}}{\text{LINE SIZE}} = \frac{2^{16} \text{ B}}{2^4 \text{ B}} = 2^{12} \text{ lines}$$

(ii) Since the cache is direct-mapped, there is exactly one line per set. Hence $\# \text{ CACHE LINES} = \# \text{ SETS}$.

A memory address for this cache is partitioned as:

$$\# \text{ OFFSET BITS} = \log_2(\text{LINE SIZE}) = 4 \text{ bits}$$

$$\# \text{ SET INDEX} = \log_2(\# \text{ SETS}) = \log_2(\# \text{ CACHE LINES}) = 12 \text{ bits}$$

$$\# \text{ TAG BITS} = 27 - 12 - 4 = 11 \text{ bits}$$

(Recall that the division is

TAG	SET INDEX	OFFSET
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(2a) (i) We access array A at index %rdx. Hence rdx must have the form:

$$\%rdx = i \cdot N + j$$

From line 4 we know that:

$$\%rdx = j + 4i$$

Putting things together we have: $N = 4$

Same reasoning for B.

%rdi = index to which we access B \Rightarrow %rdi matches the pattern:

$$\%rdi = j \cdot Q + i$$

Also:

$$\%rdi = \%rdi + \%rax = \%rdi + 5 \cdot \%rsi = i + 5 \cdot j$$

Hence: $Q = 5$

Since arrays are stored in consecutive chunks of memory, we can deduce M from the addresses in which the first elements of the arrays are stored (last 2 lines of the assembly code).

Assuming 48 and 80 are in decimal notation, A is 32 bytes in total. Therefore the number of elements in A is $\frac{32}{\text{sizeof(int)}} = 8$. Since $N = 4$ we must have $M = 2$ because $M \cdot N = 8$ elements.

However, we cannot determine P because we don't know how much memory has been allocated for array B.

```
(ii) int half_increment (int x) {  
    int result = x;  
    if ( x == 0 ) {  
        return result;  
    } else {  
        result = div (&x, 2);  
        return result + x;  
    }  
}
```