Computer Architecture: answers to unassessed tutorial exercises

Exercise 5.1

The references are as follows:

Reference	Block Number	Hit or Miss
1	1	M
4	4	M
8	0	M
5	5	M
20	4	M
17	1	M
19	3	M
56	0	M
9	1	M
11	3	M
4	4	H
43	3	M
5	5	H
6	6	M
9	1	H
17	1	H

The final state of the cache is:

Block No.	Bank 1 Address	Bank 2 Address
0	8	56
1	9	17
2		
3	43	11
4	4	20
5	5	
6	6	
7		

Exercise 5.2

Configure a twelve-block cache as

(i) direct mapped: 12 sets, set 0–11, each set has a single block with tag and data.

(ii) three-way set associative: 4 sets, set 0–3, each set has 3 blocks.

(iii) fully associative: 1 set with 12 blocks.

Disadvantage of increasing the degree of associativity: the cache may become larger and slower because of increased hardware complexity and a greater search space.

Let X denote an empty cache location. Given the sequence of block addresses 0, 6, 0, 8, 6, for Cache D:

(i) M_0XXXXX, M_6XXXXX, M_0XXXXX, M_0XM_8XXX, M_6XM_8XXX

(ii) 0 hit, 5 misses

For Cache S:

(i) M_0XXXXX, M_0M_6XXXX, M_0M_6XXXX, $M_0M_6XXM_8X$, $M_0M_6XXM_8X$

(ii) 2 hits, 3 misses

For Cache F:

(i) M_0XXXXX, M_0M_6XXXX, M_0M_6XXXX, $M_0M_6M_8XXX$, $M_0M_6M_8XXXX$

(ii) 2 hits, 3 misses