IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2019

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C113

ARCHITECTURE

Thursday 9th May 2019, 14:00
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators required

Section A (Use a separate answer book for this Section)

1a What is the size, in number of bits, of a Read Only Memory (ROM) which has an *i*-bit input and a *j*-bit output?

b A datapath containing *n* control signals is designed to support a set of instructions with an *m*-bit opcode. The control unit for this datapath takes the opcode of an instruction as its input, and produces the appropriate values for the control signals. There are 2^s states in the state diagram for this control unit, and the control signals depend only on the state and are independent of the inputs to the control unit.

The first implementation, C1, of the control unit consists of a single ROM and a register. Provide a diagram for C1, labelling the size of its components and wires. What is the size of the ROM in C1?

c The second implementation, C2, of the control unit for the datapath in Part b consists of two ROMs, one covering the control signals while the other covering the state of the control unit. Provide a diagram for C2, labelling the size of its components and wires. What is the total size of the ROMs in C2?

d The third implementation, C3, of the control unit for the datapath in Part b consists of a microsequencer with three ROMs, one covering the control signals while the other two are involved in the address selection logic. Provide a diagram for C3, labelling the size of its components and wires. What is the total size of the ROMs in C3?

The four parts carry, respectively, 10%, 30%, 30%, and 30% of the marks.

Section B (Use a separate answer book for this Section)

2a *Assembly.* Consider the following x86-64 assembly function:

```
loop:
        leal    (%rdi,%rdi,4), %eax
        leal    (%rsi,%rax,2), %eax
        leal    0(,%rax,4), %edx
        cmpl    %edx, %esi
        jge     .L1
        leal    (%rdi,%rdi,2), %edx
.L3:
        addl    %edx, %eax
        cmpl    $-2, %esi
        jl      .L3
.L1:
        rep ret
```

Fill in the blanks in the corresponding `loop` function. You may only use the variable names `a`, `b`, `x` and `y`, register names are not allowed.

```
int loop(int a, int b){
    int x, y;
    y = _____;
    for (_____; _____; _____) {
        _____;
    }
    return _____;
}
```

b *Floating point encoding.* Consider a five-bit floating point representation based on the IEEE floating point format, with one sign bit, three exponent bits ($k = 3$) and one fraction bit ($n = 1$). The exponent bias is 3. For the arithmetic operations, recall that the rule with IEEE format uses "round to even" rounding. Fill in the missing entries in the table below:

Description	Binary	M	E	Value
positive infinity		—	—	$+\infty$
	`01101`			
smallest number > 0				
one				1.0
$4.0 - 0.75$				
$2.0 + 3.0$				

c *Memory Hierarchy.* For the code below, assume that we are working with a 128-byte cache that is 2-way associative with 32-byte cacheline. Also assume to start with a cold cache and that the array A is cache-aligned (i.e., A[0] is loaded in the first slot of a cacheline in the first set). All other variables are held in registers. The given code is parameterized with m = 16 and n = 2. For the code below

```
float A[32], t = 0;
for (int i = 0; i < m; i++)
   for (int j = 0; j < n; j++)
      t += A[j*m + i];
```

answer the following questions:

i) How many floats can the cache hold? Assume a float is 8 bytes in size.

ii) How many sets does the cache have?

iii) What is the miss rate?

iv) What kind of misses occur?

v) Does the code exhibit any spatial or temporal locality with respect to accesses to A and the cache?

The three parts carry, respectively, 30%, 30%, and 40% of the marks.