IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

# EXAMINATIONS 2016

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute*

## PAPER C112

## HARDWARE

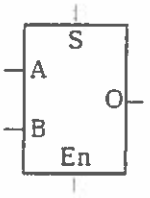
Monday 9 May 2016, 10:00
Duration: 80 minutes

*Answer ALL TWO questions*

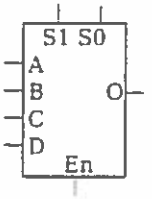
Paper contains 2 questions
Calculators not required

1 Functional Design

a Using only 2-input NAND gates, design a circuit for a 2 input one bit multiplexer with an "enable" input. If the enable input is at logic 1 the circuit behaves as a normal multiplexer, if it is at logic 0 the circuit output is zero.




b Use two of the multiplexer circuits of part a, and as many 2-input NOR gates as you need to design a four input one-bit multiplexer with an enable input.




c Show how one multiplexer, without an enable input, and one inverter could be connected up to operate as a two input NOR gate.

d A one bit comparator is a circuit with two one-bit inputs $A$ and $B$ and two one-bit outputs $G$ (greater) and $E$ (equal). Output $G$ is set to 1 if and only if $A$ is greater than $B$, output $E$ is set to 1 if and only if $A = B$.

Complete the two columns in the table below defining the circuit behaviour and design and draw the circuit using NOR gates only.

| $A$ | $B$ | $G$ | $E$ |
|---|---|---|---|
| 0 | 0 | | |
| 0 | 1 | | |
| 1 | 0 | | |
| 1 | 1 | | |

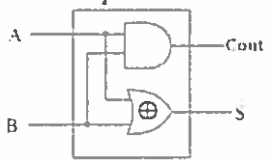
e Modify the circuit designed in part d to provide an enable input. If the enable input is 1 then the circuit behaves as in part d but if the enable input is zero then the output is zero.

*The five parts carry equal marks.*

2 Computer Arithmetic

a A half adder is defined by the following Boolean equations and circuit:

$$S = A \oplus B$$
$$Cout = A \cdot B$$




i) Show how two half adders and one OR gate can be connected to make a full adder which includes a carry input ($Cin$).

ii) Show how four full adders can be connected up to make a four-bit full adder with a carry input ($Cin$) and a carry output ($Cout$).

b Design a four-bit two's complement subtractor, with a carry input and a carry output, using four full adders and some inverter gates. (Note that the the carry input is provided to allow high precision integer arithmetic to be performed, and will be set to 1 when the least significant bits of the binary numbers are being processed.)

c Design a simple four bit ALU circuit which has a single one-bit function select input $F$, two four-bit inputs $A$ and $B$, a one-bit carry input ($Cin$) and a one-bit carry output ($Cout$). If $F = 0$ the output of the ALU is A+B+Cin, if $F = 1$ the output of the ALU is A-B-Cin. You can use the circuits you designed in parts a and b, a four-way two-input multiplexer and a single-way two-input multiplexer as functional blocks in your circuit.

d Using four AND gates and two half adders design a two bit multiplier with inputs $A_1$ $A_0$ and $B_1$ $B_0$ and outputs $O_3$ $O_2$ $O_1$ and $O_0$.

e Show how to connect up four of the two bit multipliers designed in part d, together with three four bit adders to make a four bit multiplier.

*The five parts carry equal marks.*