IMPERIAL COLLEGE LONDON

EXAMINATIONS 2022

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER COMP40005S

INTRODUCTION TO COMPUTER ARCHITECTURE

Tuesday 30 August 2022, 10:00
Writing time: 80 minutes
Upload time: 25 minutes

Answer ALL TWO questions

Open book assessment

This time-limited remote assessment has been designed to be open book. You may use resources which have been identified by the examiner to complete the assessment and are included in the instructions for the examination. You must not use any additional resources when completing this assessment.

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Paper contains 2 questions

1a Using only inverters and fulladders, provide a diagram of a 4-bit subtractor for numbers in two's complement representation.

b Use a diagram to show how the circuit in Part a can be modified to become a 4-bit programmable adder/subtractor. At each cycle when a control input is zero, this circuit performs addition; when the control input is one, the circuit performs subtraction.

c Explain what sign extension means for numbers in unsigned representation and in two's complement representation. Provide circuit diagrams of sign extension circuits for these two number representations.

d Provide a circuit diagram of a sign extension circuit that can deal with both unsigned number representation and two's complement number representation, given that in every cycle a control signal indicates which representation is used.

The four parts carry equal marks.

2a *Assembly* Consider the following x86-64 optimised assembly function:

```
increment:
        movl    $0, %eax
        testq   %rdi, %rdi
        jle     .L8
        subq    $24, %rsp
        leaq    0(,%rdi,8), %rax
        leaq    (%rdi,%rdi,4), %rdx
        addq    %rdx, %rdx
        cmpq    %rdx, %rax
        jge     .L3
.L4:
        addq    $1, %rax
        cmpq    %rdx, %rax
        jne     .L4
        leaq    -1(%rdi,%rdx), %rax
        movq    %rax, 8(%rsp)
.L3:
        leaq    8(%rsp), %rdi
        call    apply_threshold
        movq    8(%rsp), %rax
        addq    $24, %rsp
        ret
.L8:
        ret
```

Fill in the blanks in the following `increment` function. You may only use the variable names `x`, `y` and `result`, not register names.

```
long increment(long x){
    if( ________)
      return ________;
    ________;
    for(______;______;_____)
        ________________;
    ________________;
   return _____________;
}
```

b *Memory Hierarchy.* A certain byte addressable memory system has 13 bits wide. Memory accesses are to 1-byte word. The cache is 2-way set associative (two lines), has 8-sets and the Blocks are 4 Bytes in size. The contents of the cache are as follows:

Set index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	07	1	32	9F	04	DD	07	1	25	DF	1F	D8
1	B5	0	45	2B	E4	ED	47	0	5A	09	67	AD
2	C3	1	0B	32	03	4D	02	1	DD	7E	34	DB
3	67	1	FF	CC	57	BC	AB	0	EB	1C	FB	FD
4	70	0	89	24	FB	1E	70	1	CD	2C	A2	7D
5	BC	1	33	FA	64	09	DE	0	23	7B	4B	6D
6	45	0	AF	12	34	56	23	1	11	CE	66	CD
7	8A	1	EE	08	2A	D8	04	1	05	D2	99	88

The first Tag, Valid bit and Byte 0-3 correspond to Line 0 and the second Tag, Valid bit and Byte 0-3 correspond to Line 1. Provide the format of 0x0E12 and 0x16A4 addresses. Indicate the fields and bits that would be used to determine the block offset, set index and tag of each address in hexadecimal format. Also, indicate the cache entry for these two addresses, i.e. if a cache hit or miss occurs in each of the two address. If a cache hit occurs, provide the cache byte returned. Therefore, for 0x0E12 and 0x16A4 addresses provide:

- Block offset bits (0x), Index bits (0x) and Tag bits (0x)
- Is a hit or miss?
- Cache byte returned if it is a hit.

The two parts carry, respectively, 75% and 25% of the marks.