IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

# EXAMINATIONS 2019

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

*This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute*

## PAPER C112

## HARDWARE

Friday 17th May 2019, 14:00
Duration: 80 minutes

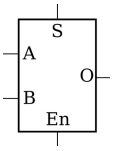
*Answer ALL TWO questions*

Paper contains 2 questions
Calculators not required

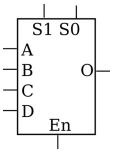
**Section A (Use a separate answer book for this Section)**

1 Functional Design and Computer Arithmetic

a Using only four 2-input NAND gates and two 2-input NOR gates, design a circuit for a 2-input one bit multiplexer with an "enable" input. If the enable input is at logic 1, the circuit behaves as a normal multiplexer, if it is at logic 0, the circuit output is zero.

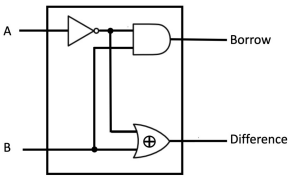



b Using only two of the multiplexer circuits of part a, two 2-input NAND gates, and two 2-input NOR gates, design a four input one-bit multiplexer with an enable input.




c A half subtractor is defined by the following Boolean equations and circuit:

$$Difference = A \oplus B$$
$$Borrow = \bar{A} \cdot B$$




i) Show how two half subtractors and one OR gate can be connected to make a full subtractor which includes a payback input ($Cin$).

ii) Show how two full subtractors can be connected up to make a two-bit full subtractor with a carry input ($Cin$) and a carry output ($Cout$). The carry input is provided to allow high precision integer arithmetic to be performed.

d As an alternative to the above approach, design a two-bit two's complement subtractor, with a carry input and a carry output, using two full adders and some NAND gates. Each full adder is thereby defined as follows, where $Cin$ is the carry input, and $Cout$ is the carry output:

$$Sum = A \oplus B \oplus Cin$$
$$Cout = Cin \cdot (A \oplus B) + A \cdot B$$

e Design a simple two bit ALU circuit which has a single one-bit function select input $F$, two two-bit inputs $A$ and $B$, and a one-bit carry output ($Cout$). If $F = 0$, the output of the ALU is $A - B$; if $F = 1$, the output of the ALU is $A + B$. You can use the circuits in parts c and d, a two-way two-input multiplexer, and a single-way two-input multiplexer as functional blocks in your circuit.

*The five parts carry equal marks.*

**Section B (Use a separate answer book for this Section)**

2 Combinational Circuit Design and feedback

a Using Boolean algebra, simplify the following Boolean expression to its simplest form (fewest number of literals):

$E = A' \cdot B' \cdot (A' + B) \cdot (B' + B),$

where $\cdot$, $+$, and $'$ represent "AND", "OR" and "NOT" operations respectively. Please show the sequence of your steps and state the reduction rules used explicitly.

b i) Draw the schematic logic circuit for a basic SR-Latch 1-bit memory unit.

ii) Briefly describe what your circuit does and derive its truth table.

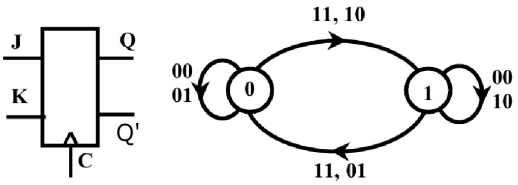
iii) What is the difference between synchronous and asynchronous logic circuits?

iv) Is the 1-bit SR-Latch a synchronous or asynchronous logic circuit?

v) If the input (R,S) to your circuit of part b(i) changes from (1,0) to (1,1) explain what will happen to the output.

vi) If the input to your circuit of part b(i) changes from (0,0) to (1,1) explain what will happen to the output.

c The J-K flip flop, commonly used in hardware design, is a circuit with two inputs labelled J and K, and complementary Q and Q′ outputs. It is defined by the following finite state machine, where the inputs are shown as tuples (J,K).




i) From the finite state machine construct the state transition table of the J-K flip-flop.

ii) Design a circuit for the J-K flip flop using one D-Type flip-flop and whatever other gates you require.

d Explain briefly how spikes can occur in combinational logic circuit outputs.

*The four parts carry, respectively, 20%, 30%, 40%, and 10% of the marks.*