Computer Architecture: tutorial exercise answers

Exercise 3.1

(a) The speedup can be calculated below:

$$\begin{aligned} \text{speedup} &= \text{run time of original / run time of improved} \\ &= 1/((1-0.9)+(0.9/k)) \\ &= 10k/(k+9) \end{aligned}$$

(b) Speed improvement can be calculated:

$$\begin{aligned} &\text{run time of old design / run time of new design} \\ &= 1/((1-\alpha)+(\alpha/p)) \\ &= p/(p-\alpha p+\alpha) \end{aligned}$$

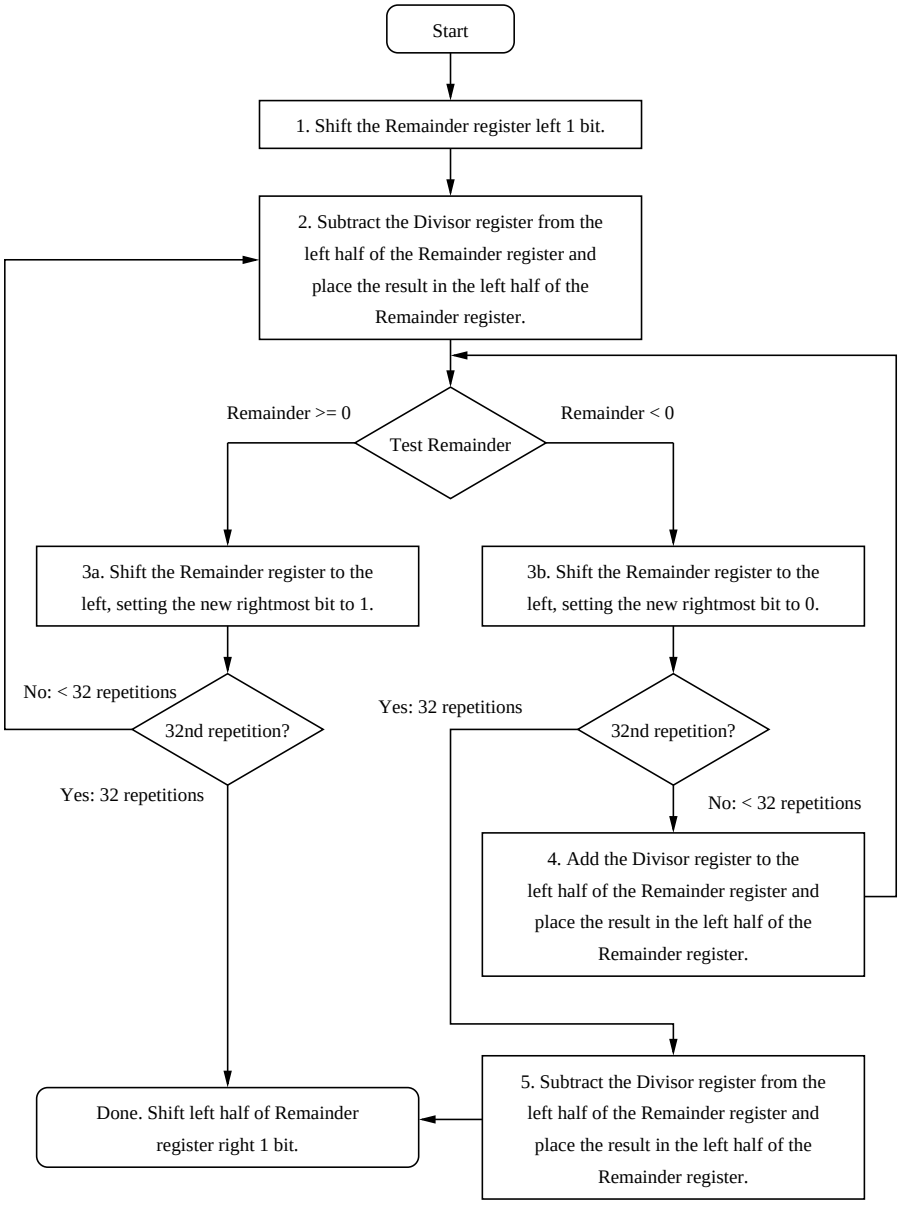
The area improvement can be derived in a similar way to give: $q/(q-\alpha q+\alpha)$.

Exercise 3.2

Note that in this version of the division algorithm, the Remainder register is initialised with the Dividend, and that at the end of the algorithm the Quotient is in the right half of the Remainder register while the left half of the Remainder register holds the actual Remainder.

One possible algorithm is shown on the next page, with an example of the register contents for 00000111 divided by 0010. Note that step 5 is needed if the algorithm finishes in the right hand branch of the algorithm, to correct for the extra addition that is carried out in step 4.

Iteration	Step	Remainder
0	1: R shift left	`00001110`
	2: R = R - Div	`11101110`
1	3b: R shift left	`11011100`
	4: R = R + Div	`11111100`
2	3b: R shift left	`11111000`
	4: R = R + Div	`00011000`
3	3a: R shift left, set LSB	`00110001`
4	2: R = R - Div	`00010001`
	3a: R shift left, set LSB	`00100011`
Done	Left half R shift right	`00010011`


Start
1. Shift the Remainder register left 1 bit.
2. Subtract the Divisor register from the left half of the Remainder register and place the result in the left half of the Remainder register.
Test Remainder
Remainder >= 0
Remainder < 0
3a. Shift the Remainder register to the left, setting the new rightmost bit to 1.
3b. Shift the Remainder register to the left, setting the new rightmost bit to 0.
32nd repetition?
No: < 32 repetitions
Yes: 32 repetitions
32nd repetition?
Yes: 32 repetitions
No: < 32 repetitions
4. Add the Divisor register to the left half of the Remainder register and place the result in the left half of the Remainder register.
5. Subtract the Divisor register from the left half of the Remainder register and place the result in the left half of the Remainder register.
Done. Shift left half of Remainder register right 1 bit.