Part 2

2ai)

Assembly	Type	Expression	Value
leaq 8(%rbx, %rdx, 4) %rax	pointer	*N[2 + 4i]	$X_N + 4i + 8$
movl 12(%rbx, %rdx, 8) %eax	int	N[3 + 8i]	$M[X_{n+} 8i+3]$
leaq 20(%rbx, %rdx, 4) %rax	pointer	*N[5 + 4i]	$X_n + 4i + 20$

ii) x = %rdi , y = %rsi

move x to 12(s)
if x ≤ 0, return 0
else
  move x to ret
  if y ≤ 0, return x
  else
    if %rdi = x + 12
      ret = 0
      increment
      ret = x + 12 return x + 12
    if x > y:
      ~~%rdi = y~~
      ~~%edi << x x << y~~
      return x << y
  else
    %rdi = ~~&x~~ &x
    ret = 0
    increment
    return x

PTO for answer: above is working

2aii)
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if (x <= 0)
    return 0;
if (y >= 0)
    return x;
if (x > y)
    return x << x : x << y;
else
    x = increment (x);
return x;
```

b) 128 MB memory means addresses are 27 bits long.
32-byte block means 5-bit offset.

b.a) Assuming question means "fully" associative.
0-bit index in fully associative.
22 bits tag, 5 bits offset

b.b) Direct Mapped: $(2 \times 1024^2) \div 32 = 65536$ sets
$\log_2(65536) = 16$
$27 - 16 - 5 = 6$
6 bits tag, 16 bits index, 5 bits offset

b.c) 8 blocks per set: $(2 \times 1024^2) \div (8 \times 32) = 8192$ sets
$\log_2(8192) = 13$
$27 - 13 - 5 = 9$
9 bits tag, 13 bits index, 5 bits offset

cont. on Page 4

cont 2b) ~~32 = 10000$_2$~~

~~+~~

~~5 bits long~~

0 = 0.... 0

32 = 0...100000

8 = 0.... 1000

64 = 0... 1000000

no value long enough for associativity of one cache to affect result.

0: Miss, cache is empty

32: Miss, index different to 0

8: Hit, address excluding offset same as 0

32: Hit, same address same as 32 (excluding offset)

64: Miss, address different to 32 or 8 (excluding offset)

~~2~~ 3 miss, 5 requests, Miss Rate: $\frac{3}{5} = 60\%$