IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2017

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
BEng Honours Degree in Mathematics and Computer Science Part I
MEng Honours Degree in Mathematics and Computer Science Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C113=MC113

ARCHITECTURE

Friday 5 May 2017, 14:00
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators required

Section A (Use a separate answer book for this Section)

1 a Give one advanatge and one disadvanatge of:

i) Two's Complement number representation

ii) Sign and Magnitude number representation

b Show how the 10-bit Two's Complement number representation 11001 00110 can be converted into the following:

i) its decimal value

ii) 10-bit Sign and Magnitude representation

iii) 10-bit Excess 250

iv) Octal

c i) What does BCD stands for?

ii) Convert the 10-bit Two's Complement number representation 11001 00100 into BCD, given that the bit pattern 1101 represents the negative sign which is used in describing a negative number.

d An 8-bit processor P has one register R. The instructions of P consist of a 4-bit opcode, and the remaining 4 bits can be used either for a memory address or for a constant value. There are instructions for loading data from memory to R and storing data from R to memory, for loading a constant to R, and for adding and subtracting a value stored in memory from R. There is an instruction for jumping to the instruction at a given memory address if R is negative. Finally, there is an instruction STOP, when the program finishes.

i) Describe the six instructions for P, except the STOP instruction, in a suitable Register Transfer Level (RTL) Language.

ii) Provide the instruction sequence for P to add two 8-bit BCD numbers, with value between 0 and 9, and stored in memory addresses 0 and 1, with the resulting BCD number stored in memory address 2.

The four parts carry, respectively, 20%, 20%, 10% and 50% of the marks.

Section B (Use a separate answer book for this Section)

2a Name at least four different possible sizes/types of (integer) operands in Intel 64 assembler code and briefly describe them. How can one refer to parts of a general register which are of exactly these sizes/types?

b Using IEEE Single Precision format, convert the following hexadecimal numbers **C1D0 0000** and **C1DE 0000** into binary and decimal. Show your work clearly.

c Express the decimal numbers **128** and **-129** using the IEEE Single Precision Format (in binary and hexadecimal). Show your working clearly. (If you need extra bits use rounding rather than truncation for calculating your result).

Describe how to add these two numbers in IEEE format and give the (normalised) result in IEEE format (in binary and hexadecimal).

d Translate the **rec** routine in the following program into **commented** Intel 64 assembly language using the stack for local variables and arguments:

```
int rec (int a,b){
  int c = 1;
  int d = a-b;
  if (d > 0) {
    rec(b,a)
  } else {
    while (a <= b) do {
      a = a+c; c = 2*c;
    }
  }
  return c;
}

int main () {
  int x = 0;
  int y = 2;
  x = rec(x,y);
}
```

Your solution **must not** use global variables, must save and restore registers correctly and assume 64-bit `int`s.

The four parts carry, respectively, 10%, 20%, 20%, and 50% of the marks.