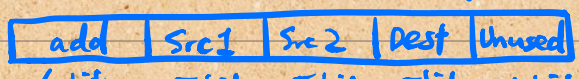
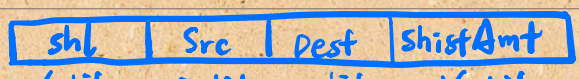
113 2018 Exam

1a. i) load:

add:



shl:



ii) Because different instructions follow different datapath, which may involve different sets of registers. For instance, load may involve Memory Address Register and Memory Data Register, while add may involve only ALU unit and a temporary result register. Those registers need to be updated in different clock cycles one after another, hence different cycle counts.

b. Let the original number be in the register $1.

```
shl  $1, 2, $1     # $1 = 4 · $1_old
add  $1, $1, $1    # $1 = 4 · $1_old + $1_old
```

#cycles = 1 + 2 = 3

When K = 508, the instruction would be:

```
shl  $1, 1, $2
add  $1, $2, $3
shl  $2, 1, $2
add  $3, $2, $3
shl  $2, 1, $2
add  $3, $2, $3
shl  $2, 1, $2
add  $3, $2, $3    # $3 = 63 · $1_pre
shl  $2, 1, $2     # $2 = 64 · $1_pre
add  $3, $2, $1    # $1 = 127 · $1_pre
shl  $1, 2, $1     # $1 = 508 · $1_pre
```

Cycles = 3 · 6 + 1 = 19

c. i) % diff = $\frac{|10-31|}{13/2} = \frac{14}{13}$

ii) % diff = $\frac{|119-101|}{29/2} = \frac{18}{29}$

percentage difference = $\frac{\text{abs. value of diff}}{\text{avg of 2 numbers}}$

2a. i)

Operand	Type	Mem. Address	Value
%rax	register	-	0x2
0x110	memory	0x110	0x3
$0x110	immediate	-	0x110
263(%rax, %rdx)	memory	0x10C	0xFF
0x100(,%rax, 4)	memory	0x108	0x12
(%rcx,%rax, 2)	memory	0x10C	0xFF

ii)

```
int loop(int a, int b, int c){
    int x, y;
    y = b;
    for (x= a+c ; x > 0 ; x--) {
        y++;
    }
    return y;
}
```

b. i) Bias = $2^{k-1} - 1 = 1$

ii) Largest = $2^{2-1} \cdot (1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}) = 3.75$

iii) Smallest Normalized = $2^{1-1} \cdot (1+0) = 1.0$

Smallest possible value = $2^{-1} \cdot (0 + \frac{1}{8}) = 0.0625$

iv) 0 10 100
Sign Exp Mantissa

C. Since there are 8 bytes in one block, the ~~offset~~ has 3 bits. Hence for address 2 and 4, the set index must be the same and no miss would occur. From 8 to 32, every read operation would be a miss (every time the set index is different). Hence hit rate = $\frac{2}{6} = \frac{1}{3}$.

If we increase the block size to 16 bytes, the offset would be 4 bits. Hence, 2, 4, and 8 would all become hits. The only two misses are 16 and 32, hence hit rate = $\frac{3}{6} = \frac{1}{2}$, which has been improved.