IMPERIAL COLLEGE OF SCIENCE, TECHNOLOGY AND MEDICINE

EXAMINATIONS 2015

BEng Honours Degree in Computing Part I
MEng Honours Degrees in Computing Part I
for Internal Students of the Imperial College of Science, Technology and Medicine

This paper is also taken for the relevant examinations for the Associateship of the City and Guilds of London Institute

PAPER C112

HARDWARE

Friday 15 May 2015, 14:00
Duration: 80 minutes

Answer ALL TWO questions

Paper contains 2 questions
Calculators not required

1 A two mode counter with a single bit input has the following specification: When the input is 1 the counter cycles through states 0, 2, 4, 5, 0, 2, 4, 5 etc. When the input is 0 the counter cycles through states 0, 3, 1, 5, 0, 3, 1, 5 etc.

a Draw the transition diagram of a finite state machine that corresponds to the counter specification.

b Compile a state transition table in the format below for a circuit implementation of the counter using three flip flops. Use don't care values wherever possible.

Input	This State	Q2	Q1	Q0	Next State	D2	D1	D0
0	0							
0	1							
0	2							
0	3							
0	4							
0	5							
0								
0								
1								
1								
1								
1								
1								
1								
1								
1								

c Draw Karnaugh maps for D0 D1 and D2 and determine the minimum form of the equations for D0 D1 and D2.

d Determine what will happen to your circuit if it accidentally gets into a state-input combination that is not part of the counting sequence. There is no need to correct it if it doesn't work correctly.

e The counter has two outputs labeled O_1 and O_2. O_1 is set to logic 1 if and only if the state number is odd, and O_2 is set to 1 if and only if the state number is even. Using Karnaugh maps (or otherwise) find the minimum forms of the equations for these two outputs.

The five parts carry equal marks.

2 Binary coded decimal (BCD) digits are commonly used in calculators. Four bits are used to define a digit in the following manner:

Digit	b_3	b_2	b_1	b_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0

Digit	b_3	b_2	b_1	b_0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

The rest of the bit combinations (1010, 1011, 1100, 1101, 1110, 1111) are not used and are invalid BCD digit combinations. Design a circuit for adding BCD digits with carry as follows.

a Draw a Karnaugh map of a circuit which has four inputs (b_3,b_2,b_1,b_0) and one output. The output is 1 if and only if the four-bit input does not represent a valid BCD digit. Find the Boolean equation of the minimum form of the circuit.

b A four bit binary adder is used to add two BCD digits. If the result is a valid BCD digit and the carry is zero, then the result is the correct BCD sum of the inputs. In all other cases the binary sum is not the same as the BCD sum of the two inputs, and in some cases the binary carry is not the same as he BCD carry. Enumerate each possible binary sum for which the binary carry is different from the BCD carry. Show how the circuit you designed in part a, together with a single **OR** gate can be used to produce the correct BCD carry when adding any two BCD digits.

c When using a full binary adder to add two BCD digits, if the BCD carry (found in part b) is 1 then the binary sum will not be same as the BCD sum of the two BCD inputs. Write down three possible examples in which this will happen, and find the four bit binary number which when added to the binary sum will produce the correct BCD sum.

d Draw a block diagram of a complete BCD adder, with carry in and carry out using two four-bit binary adders, the circuit you designed in part b (drawn as a block diagram), and any other gates you require. You can assume that only valid BCD digits are used as input.

e The calculator has a mode which uses octal arithmetic. Octal uses just the digits 0,1,2,3,4,5,6 and 7, and each octal digit is represented by a three bits. For example, 6+5=13 in octal arithmetic. A four-bit adder is to be used to add octal digits. Draw a diagram showing how one stage of the octal sum is implemented for octal inputs A and B, output S and carry in and carry out. Just one four bit adder is required.

The five parts carry equal marks.