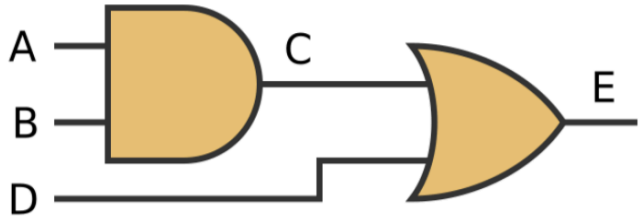
LAB 1



TOTAL 10 nets
10 total faults

and gate collapising and or gate collapsing 4 faults collapse

6 faults remain

(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# cat code.bench
#code
INPUT(1)
INPUT(2)
INPUT(3)

OUTPUT(5)

4 = AND(1,2)
5=OR(4,3)

(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# atalanta -t out1 code.bench
before
after
end initialazition
iLastUndetectedFault=5
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
3 3 3 **
* *
* Welcome to atalanta (version 2.0) *
* *
* Dong S. Ha (ha@vt.edu) *
* Web: http://www.ee.vt.edu/ha *
* Virginia Polytechnic Institute & State University *
* *

```
      ****************************************************

******  SUMMARY OF TEST PATTERN GENERATION RESULTS  ******
1. Circuit structure
   Name of the circuit                  : code
   Number of primary inputs             : 3
   Number of primary outputs            : 1
   Number of gates                      : 2
   Level of the circuit                 : 2

2. ATPG parameters
   Test pattern generation Mode         : RPT + DTPG + TC
   Limit of random patterns (packets)   : 16
   Backtrack limit                      : 10
   Initial random number generator seed : 1767934484

   Test pattern compaction Mode         : REVERSE + SHUFFLE
   Limit of shuffling compaction        : 2
   Number of shuffles                   : 4

3. Test pattern generation results
   Number of test patterns before compaction : 4
   Number of test patterns after compaction  : 4
   Fault coverage                       : 100.000 %
   Number of collapsed faults           : 6
   Number of identified redundant faults    : 0
   Number of aborted faults             : 0
   Total number of backtrackings        : 0

4. Memory used                          : 0.000 MB

5. CPU time
   Initialization                       : 0.017 Secs
   Fault simulation                     : 0.000 Secs
   FAN                                  : 0.000 Secs
   Total                                : 0.017 Secs
(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# ls
atalanta  code.bench  code.test  code.vec  out1



(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# cat out1
* Name of circuit:  code.bench
* Primary inputs :
```

1 2 3

* Primary outputs:
5

* Test patterns and fault free responses:

1: 110 1
2: 010 0
3: 001 1
4: 100 0

—==========

The above was with no redundant faults

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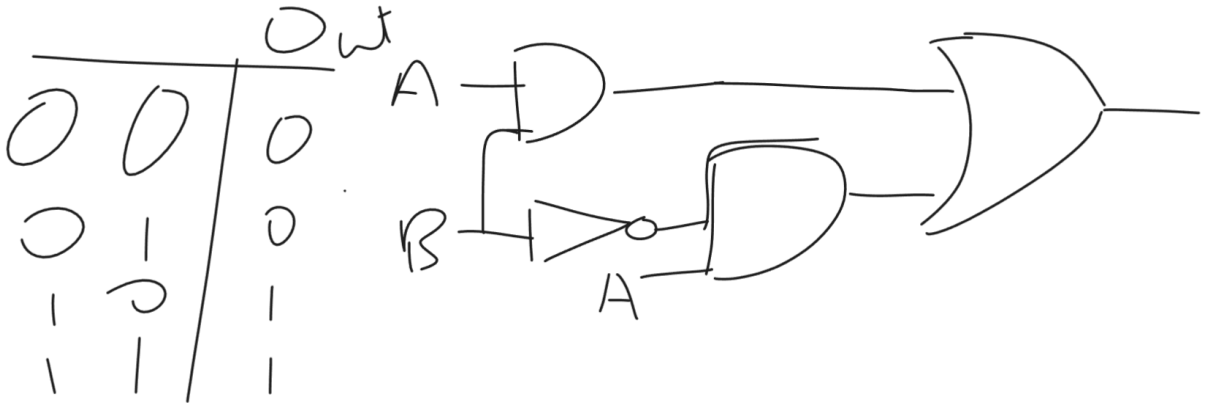
2) AB +AB' =A

B input and gates have redundant faults



(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# cat code2.bench

```
#code2
INPUT(A)
INPUT(B)

OUTPUT(F)

n1 = AND(A, B)
n2 = NOT(B)
n3 = AND(A, n2)
F  = OR(n1, n3)
```

```
(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# atalanta -t out2 code2.bench
before
after
end initialazition
iLastUndetectedFault=11
iLastUndetectedFault=10
iLastUndetectedFault=9
iLastUndetectedFault=8
iLastUndetectedFault=6
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
2 2 2  ******************************************************
       *                                        *
       *        Welcome to atalanta (version 2.0)         *
       *                                        *
       *            Dong S. Ha (ha@vt.edu)              *
       *          Web: http://www.ee.vt.edu/ha           *
       *  Virginia Polytechnic Institute & State University  *
       *                                        *
       ******************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                    : code2
   Number of primary inputs               : 2
   Number of primary outputs              : 1
   Number of gates                        : 4
   Level of the circuit                   : 3

2. ATPG parameters
   Test pattern generation Mode           : RPT + DTPG + TC
   Limit of random patterns (packets)     : 16
   Backtrack limit                        : 10
   Initial random number generator seed   : 1767935506
   Test pattern compaction Mode           : REVERSE + SHUFFLE
   Limit of shuffling compaction          : 2
   Number of shuffles                     : 4

3. Test pattern generation results
   Number of test patterns before compaction : 4
   Number of test patterns after compaction  : 4
   Fault coverage                         : 66.667 %
```

```
   Number of collapsed faults              : 12
   Number of identified redundant faults     : 4
   Number of aborted faults                : 0
   Total number of backtrackings           : 4

4. Memory used                          : 0.000 MB

5. CPU time
   Initialization                       : 0.017 Secs
   Fault simulation                        : 0.000 Secs
   FAN                                  : 0.000 Secs
   Total                                : 0.017 Secs

(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# cat out2
* Name of circuit:  code2.bench
* Primary inputs :
  A B

* Primary outputs:
  F

* Test patterns and fault free responses:

   1: 01 0
   2: 11 1
   3: 10 1
   4: 00 0

(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# atalanta  -t out2 -v code2.bench
before
after
end initialazition
iLastUndetectedFault=11
iLastUndetectedFault=10
iLastUndetectedFault=9
iLastUndetectedFault=8
iLastUndetectedFault=6
iLastUndetectedFault=4
iLastUndetectedFault=3
iLastUndetectedFault=2
2 2 2   ******************************************************
        *                                                    *
        *          Welcome to atalanta (version 2.0)         *
        *                                                    *
```

```
*              Dong S. Ha (ha@vt.edu)              *
*           Web: http://www.ee.vt.edu/ha           *
*  Virginia Polytechnic Institute & State University  *
*                                                  *
****************************************************

******   SUMMARY OF TEST PATTERN GENERATION RESULTS   ******
1. Circuit structure
   Name of the circuit                  : code2
   Number of primary inputs               : 2
   Number of primary outputs              : 1
   Number of gates                      : 4
   Level of the circuit                 : 3

2. ATPG parameters
   Test pattern generation Mode           : RPT + DTPG + TC
   Limit of random patterns (packets)     : 16
   Backtrack limit                      : 10
   Initial random number generator seed   : 1767936060
   Test pattern compaction Mode           : REVERSE + SHUFFLE
   Limit of shuffling compaction          : 2
   Number of shuffles                   : 4

3. Test pattern generation results
   Number of test patterns before compaction : 4
   Number of test patterns after compaction  : 4
   Fault coverage                       : 66.667 %
   Number of collapsed faults             : 12
   Number of identified redundant faults  : 4
   Number of aborted faults               : 0
   Total number of backtrackings          : 4

4. Memory used                          : 0.000 MB

5. CPU time
   Initialization                       : 0.017 Secs
   Fault simulation                       : 0.000 Secs
   FAN                                  : 0.000 Secs
   Total                                : 0.017 Secs
(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# ls
atalanta code.bench code.test code.vec code2.bench code2.test code2.ufaults code2.vec
out1  out2  out2.test
(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin# cat code2.ufaults
n2 /1
```

B->n1 /1
B /1
B /0
(OSS CAD Suite) root@5af7e969d6b9:/usr/local/bin#

^ untestable faults -v