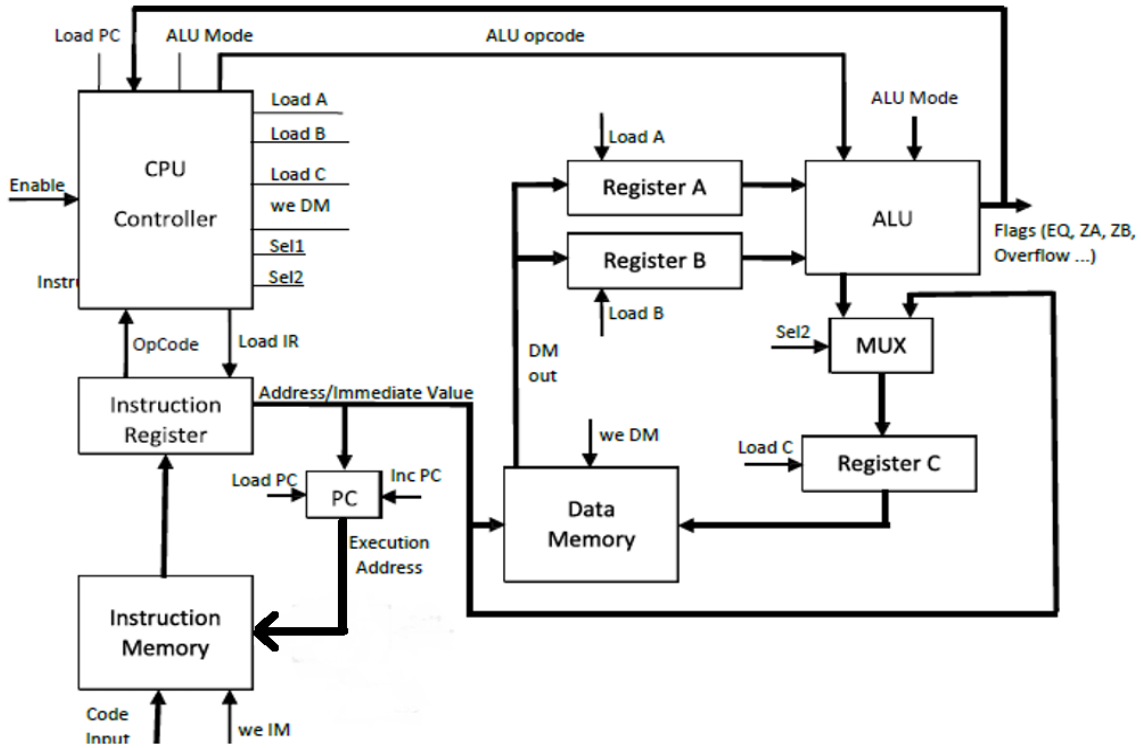
Design of a 16-Bit CPU using VHDL



Mode	Opcode	Operation
0 (AU)	000	A + B
	001	A * B
1 (LU)	000	A AND B
	001	A OR B
	010	A NAND B
	011	A NOR B
	100	NOT A
	101	NOT B
	110	A XOR B
	111	A XNOR B
2 (Shifter)	000	Right Shift A (B times)
	001	Left Shift A (B times)

First, the various components of the CPU were programmed. Next, the control unit was designed using the port mapping techniques. Finally, the CPU was put together at the last stage. The programming was done in VHDL. Testbenches were written for individual components at each stage to verify the functioning.

The components used were:

1. ALU
   a.ArithmeticUnit
   b.LogicUnit
   c. Shifter
2. Data Memory
3. Instruction memory
4. Program Counter
5. Instruction Register
6. Multiplexer
7. Controller
8. CPU

ALU

The ALU was required to perform arithmetic, logical or shift operation based on the opcode recieved. Individual units were first designed followed by the top model.

Data Memory

This unit was mainly used to store the data or immediate value for the registers.

Instruction Memory

The instruction memory will hold the address from the program counter and immediate values.

Program Counter

This unit holds the address of the next instruction to be executed.

Instruction Register

This unit generates OPCODe for the ALU and provides adress or immediate value.

Multiplexer

This unit is used to select the signal to pass through

Controller

This unit incorporates all the units using port mapping technique.

CPU

This design is of the overall unit.