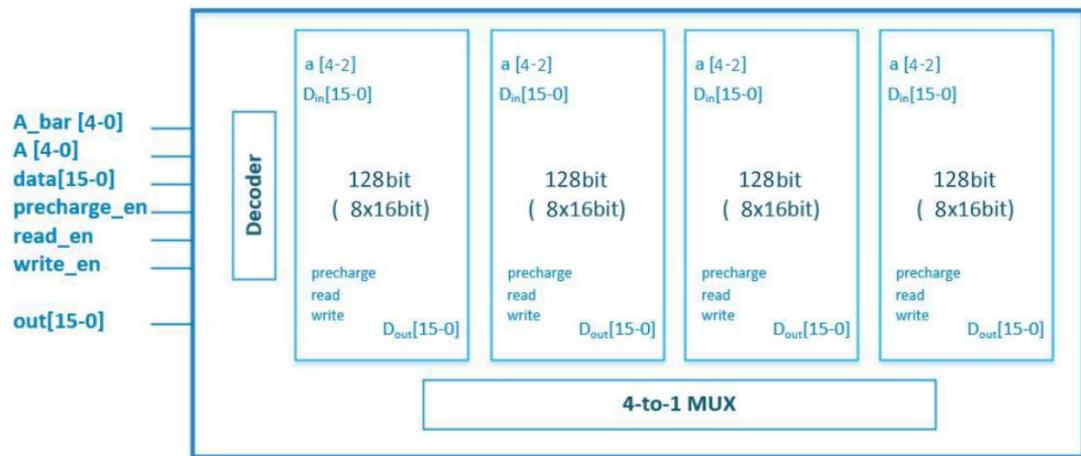


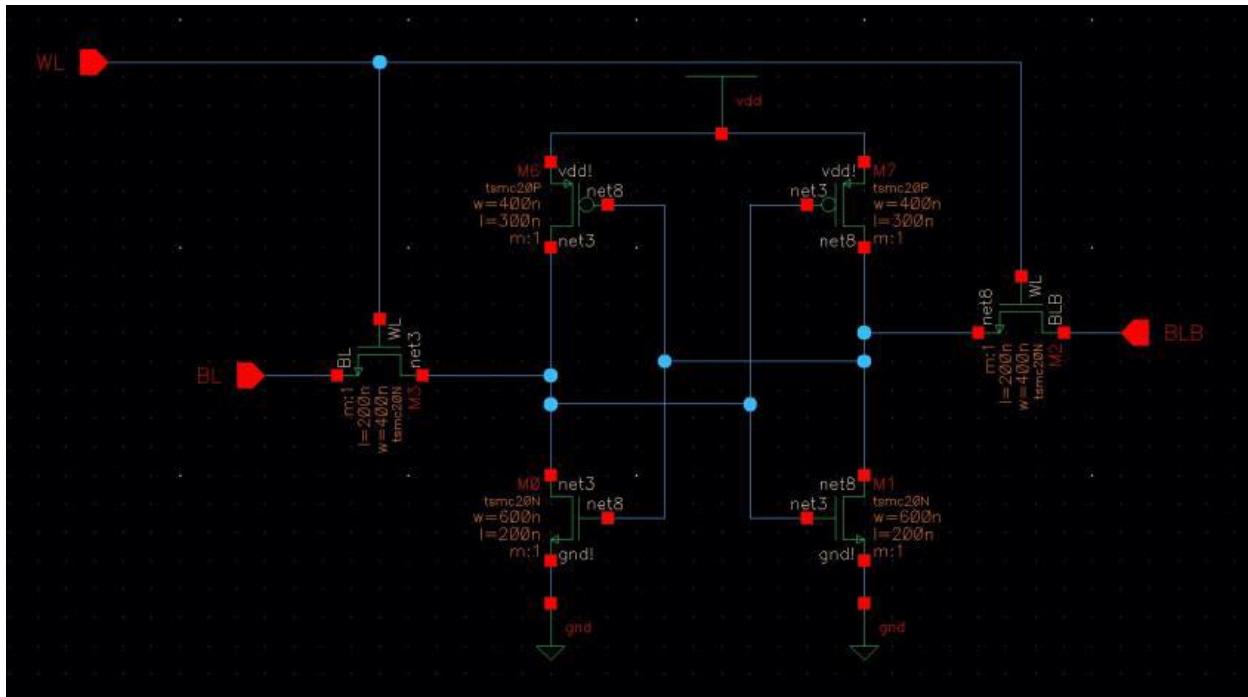
512 Bit SRAM

512 bit Sram is designed using 4 banks of 128-bit each SRAM



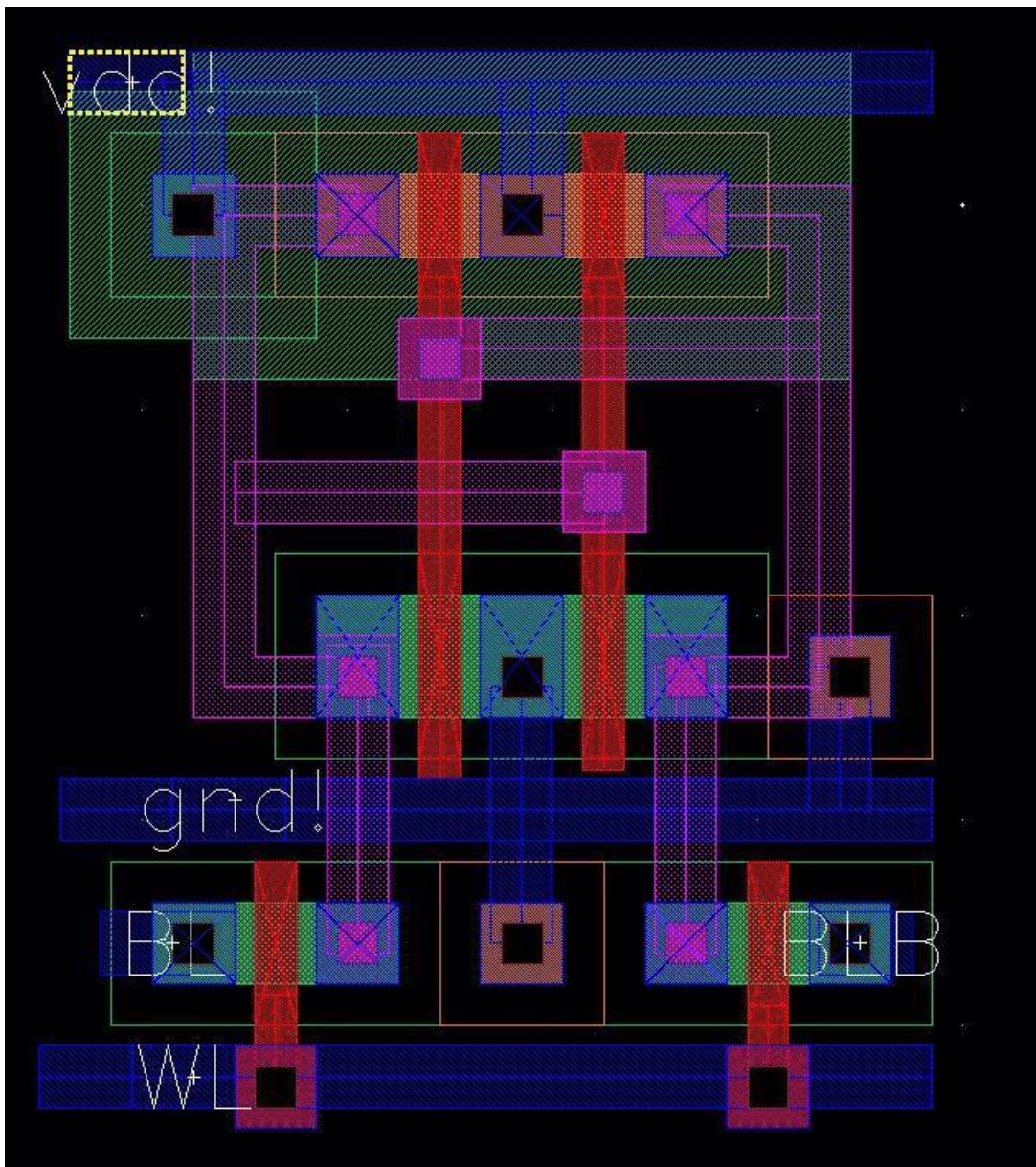
The Sram is designed using the 6T model.

The schematic of the 6T is as shown below.



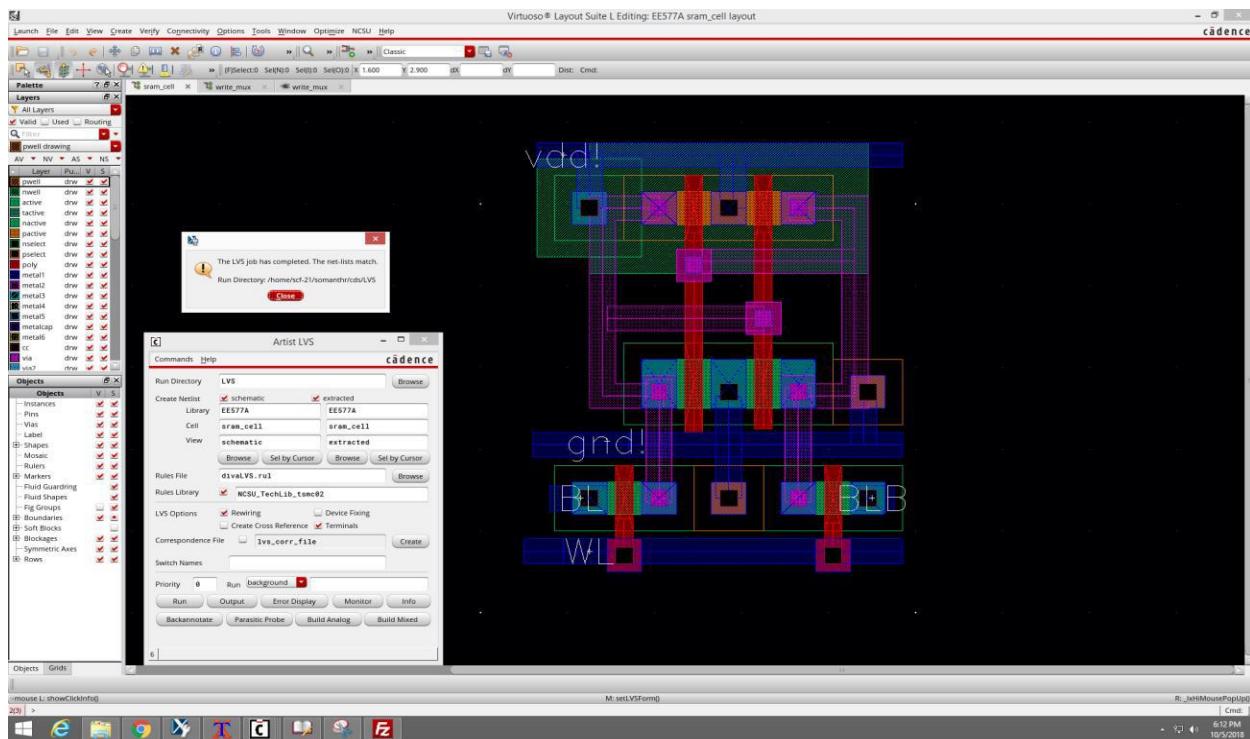
512 Bit SRAM

The layout is as shown below



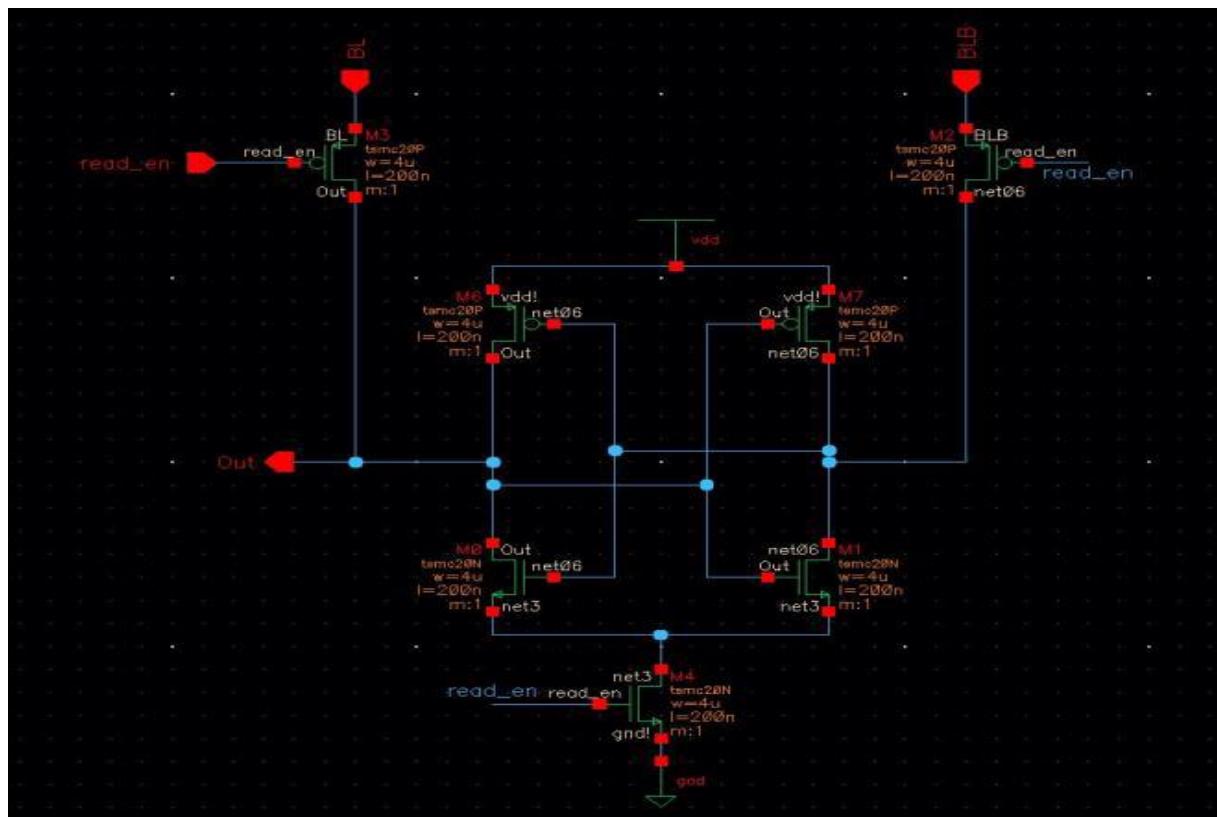
The LVS is done and the snippet is as shown

512 Bit SRAM



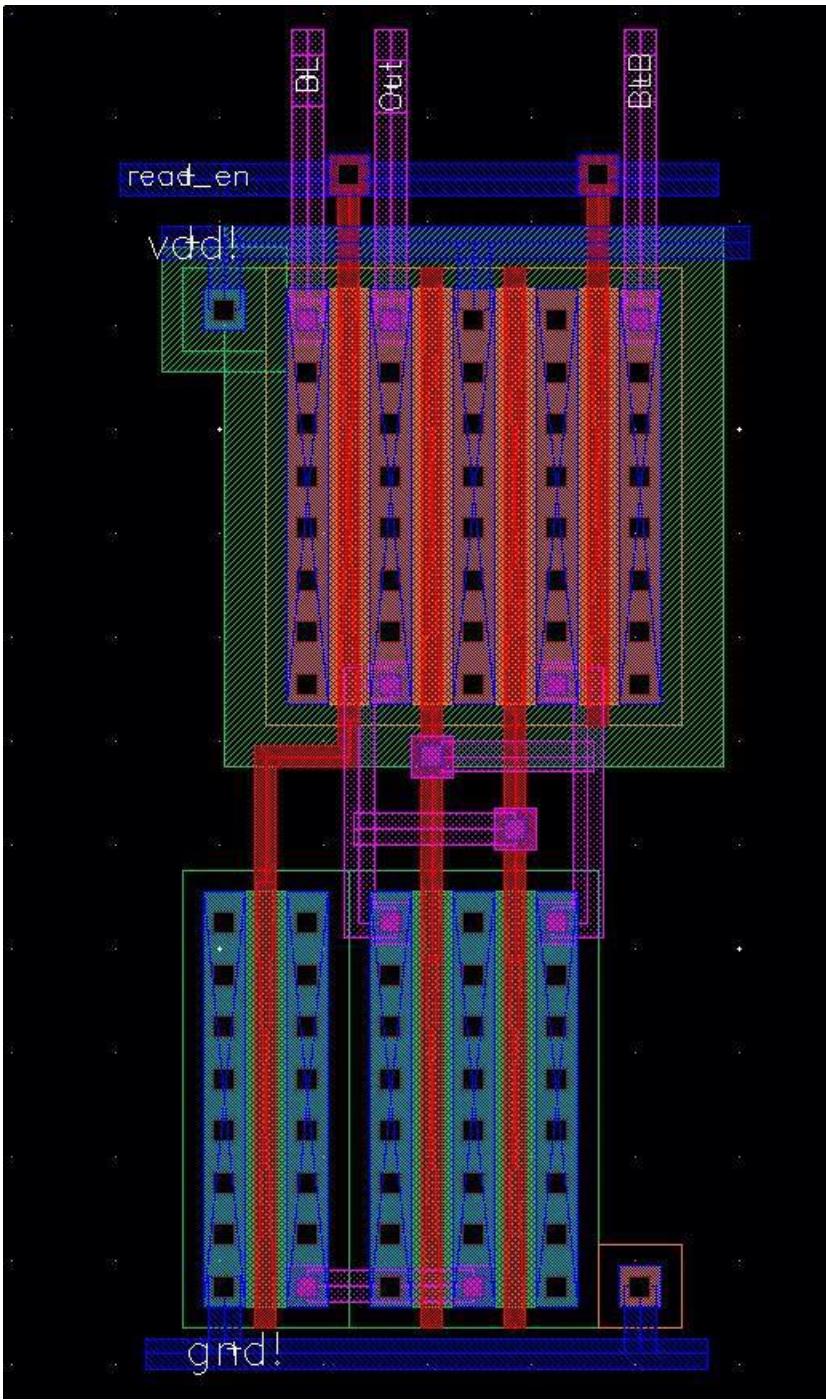
Sense Amplifier is Designed

A sense amplifier is used to read the data by using the bit and bit bar lines as input. It is controlled by a read enable signal. All the transistors in the sense amplifier circuit are sized to have a width of 4um.



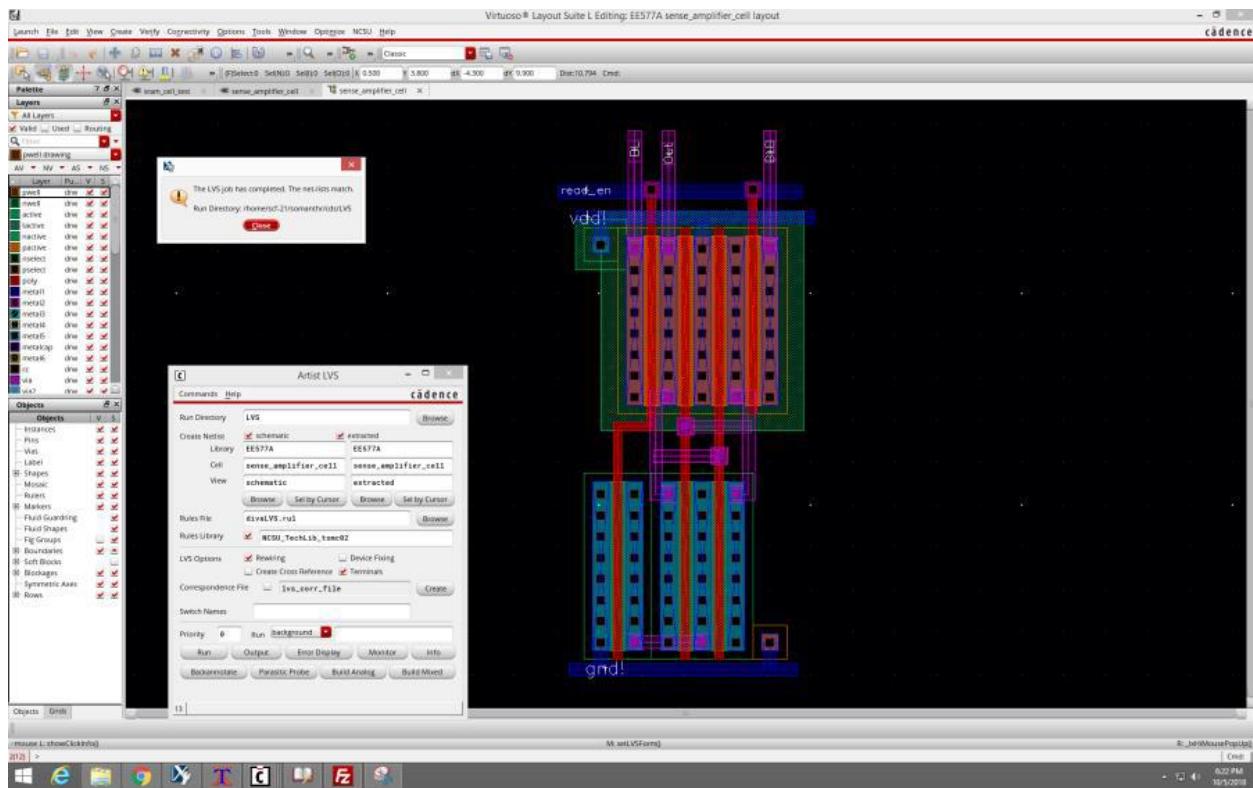
512 Bit SRAM

Layout is as given below



And the LVS is performed

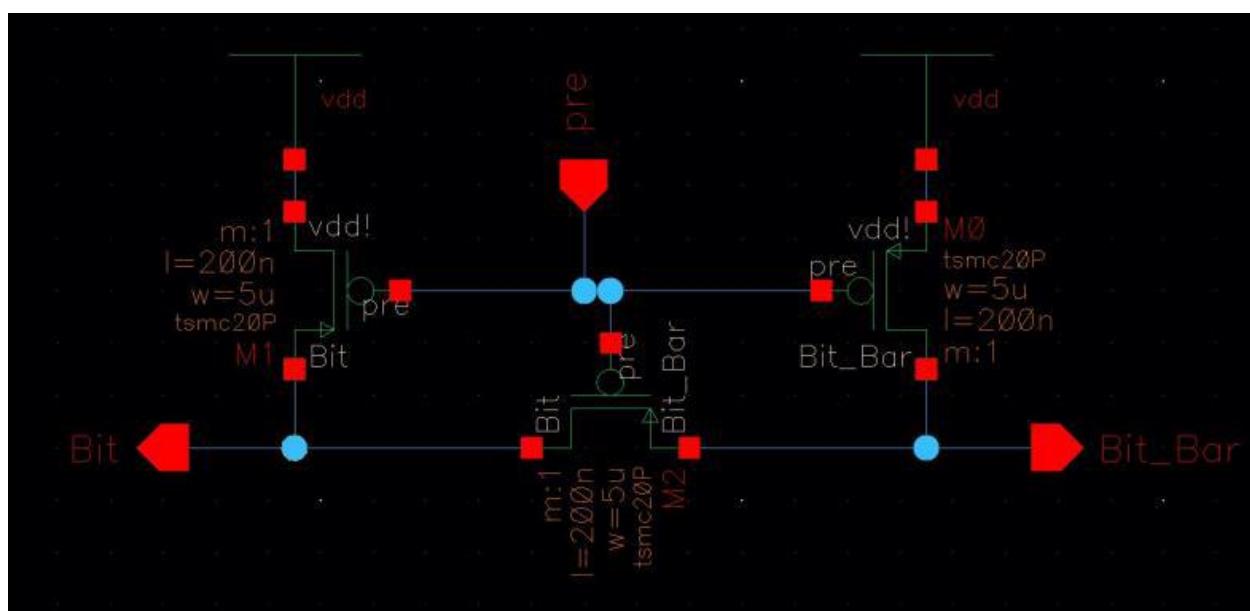
512 Bit SRAM



The Precharge Circuit

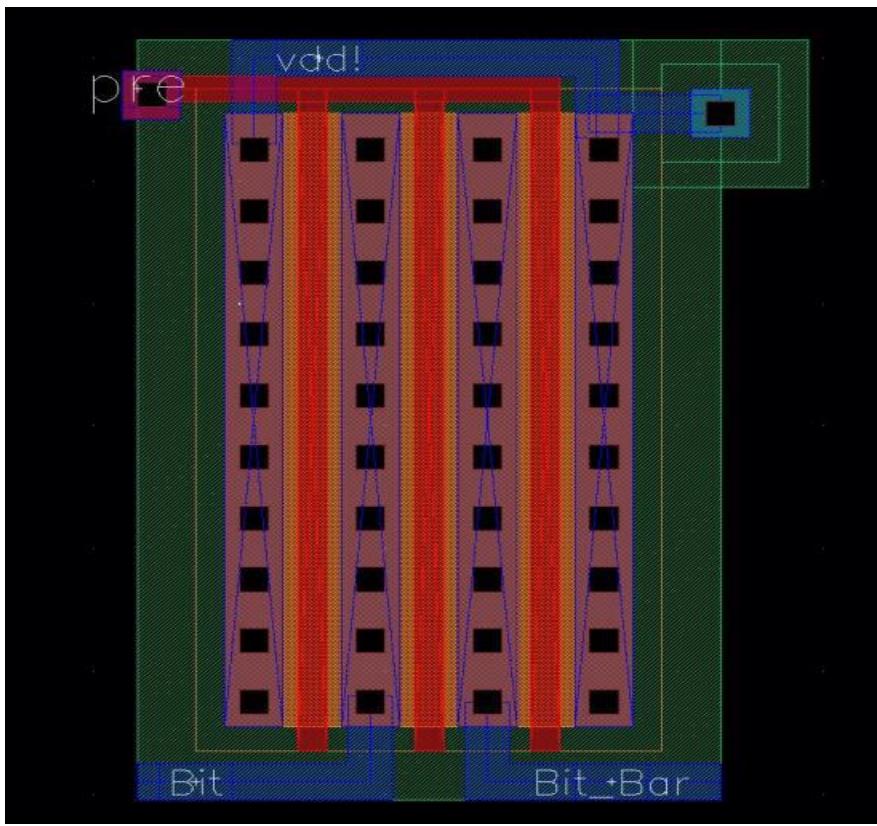
A precharge circuit is used to charge the bit and bit bar lines. A pmos transistor is connected between bit and bit_bar to avoid ΔV difference between the two lines. The transistors are sized to have a width of 5um. Each bank will have 16 such precharge circuits charging up the 16 pairs of bit and bit bar lines of the 16 columns in that bank.

Schematic:

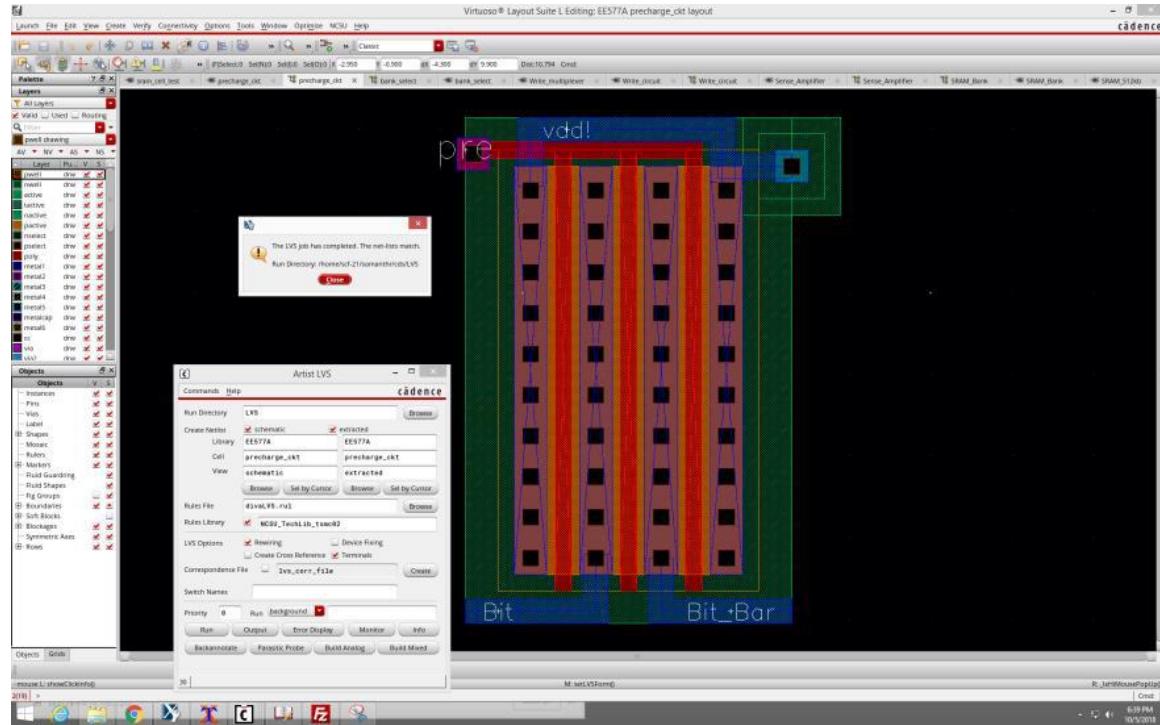


512 Bit SRAM

Layout:



LVS:

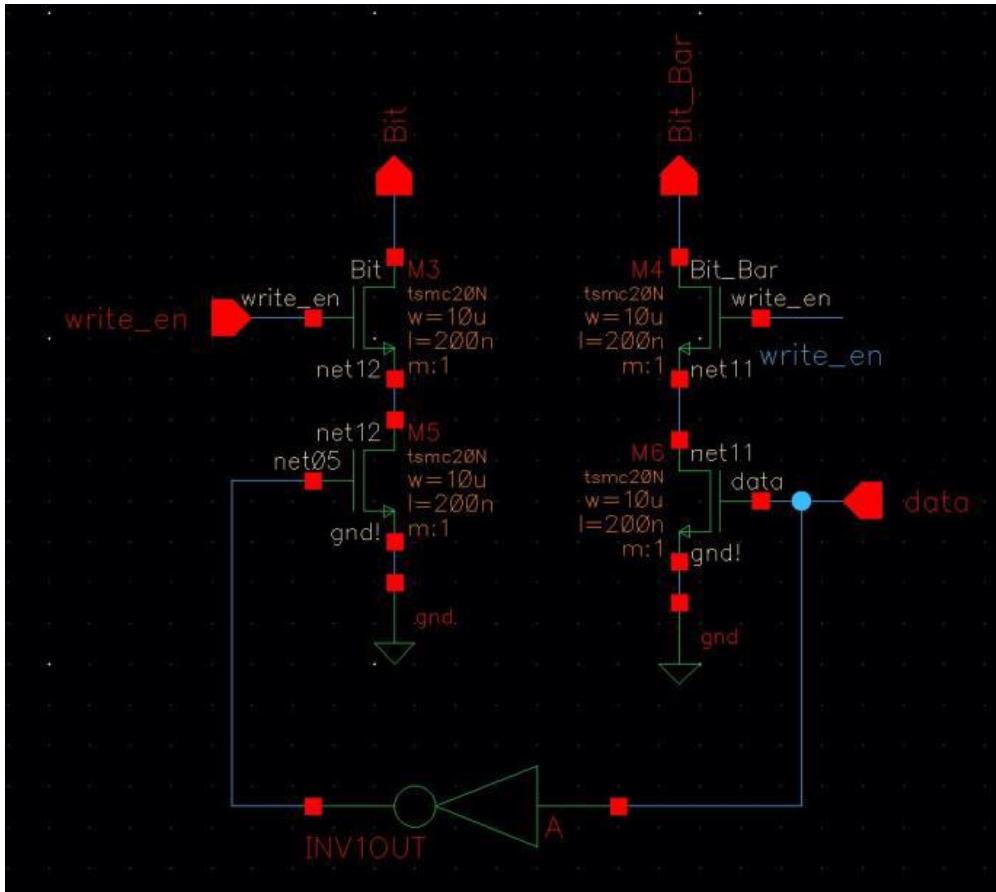


512 Bit SRAM

Write Circuit for 1 cell

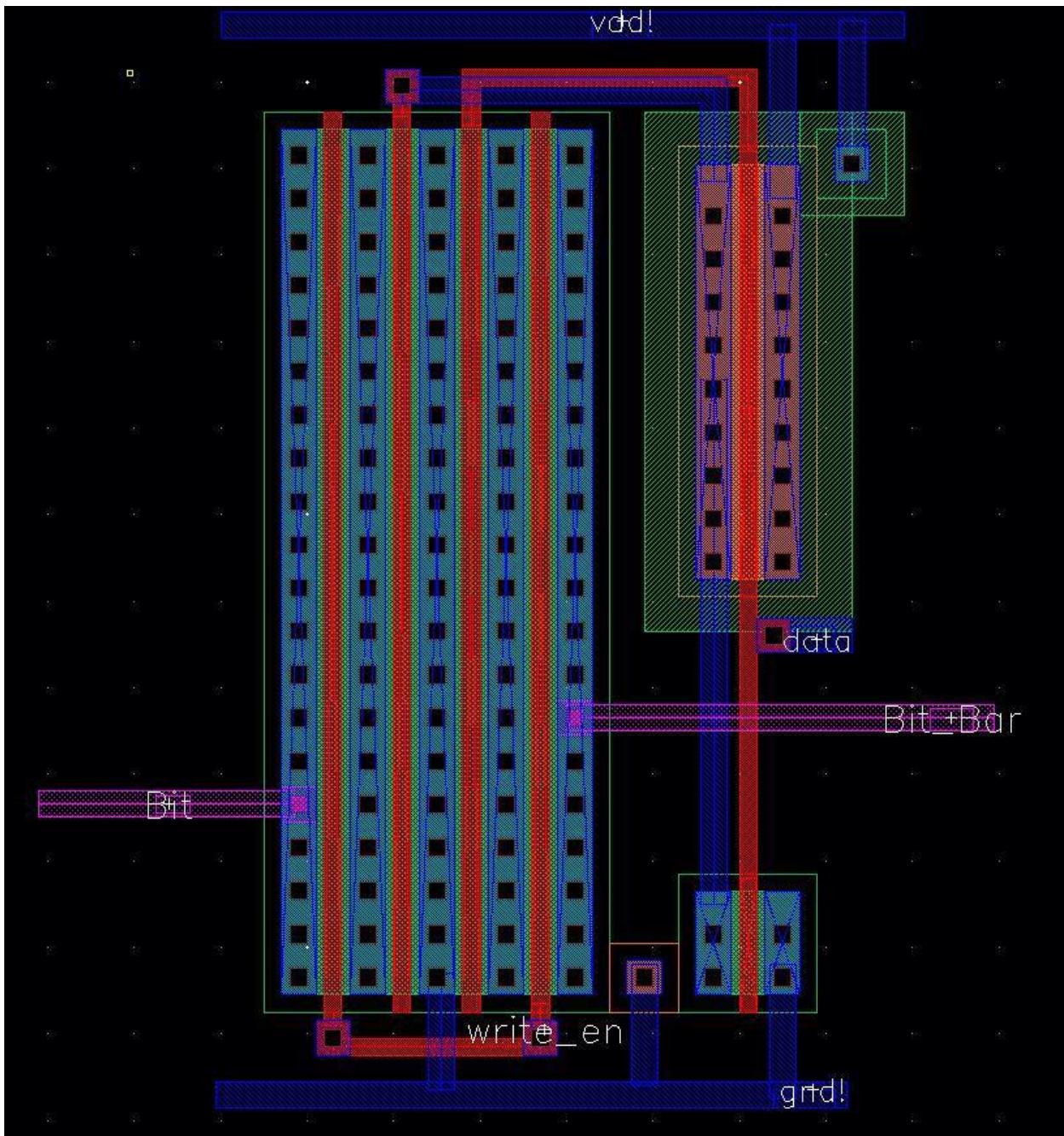
The circuit writes the input data to the SRAM cell through the bit and bit bar lines and it is controlled by the write enable signal. The nmos transistors have width = 10um.

Schematic:



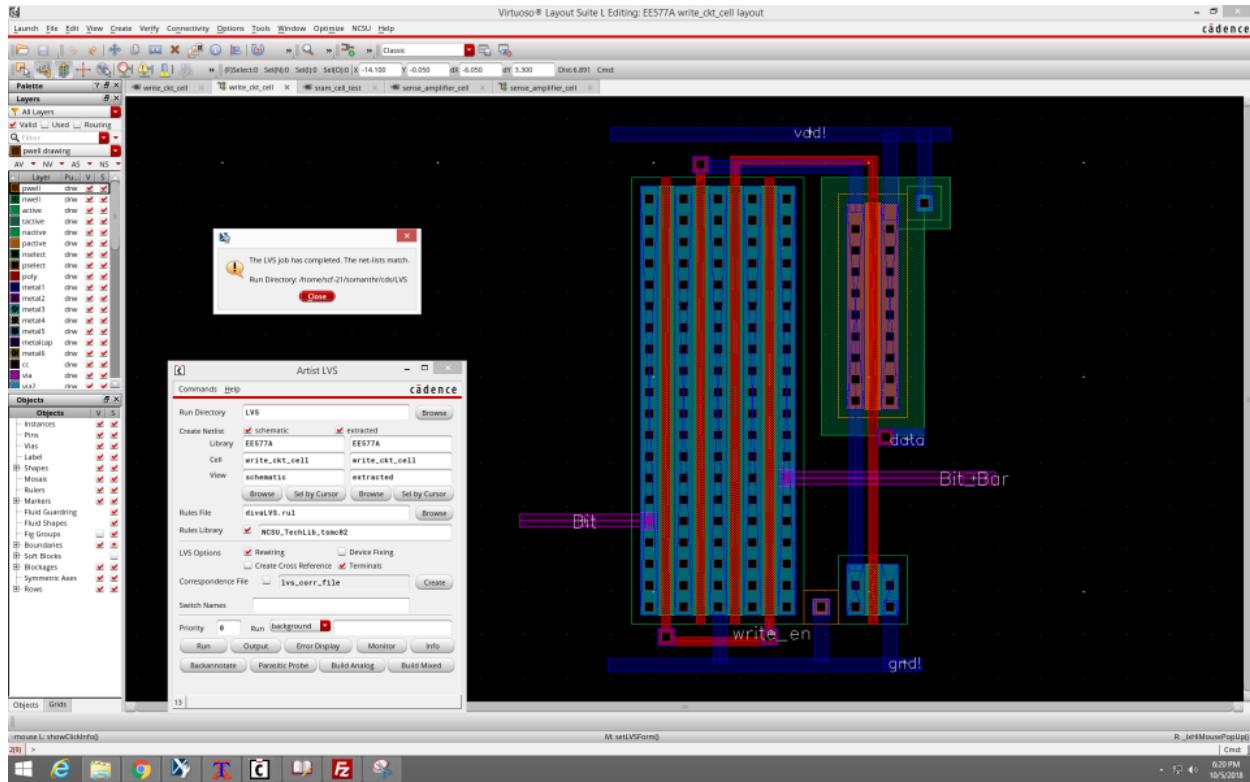
512 Bit SRAM

Layout



LVS:

512 Bit SRAM

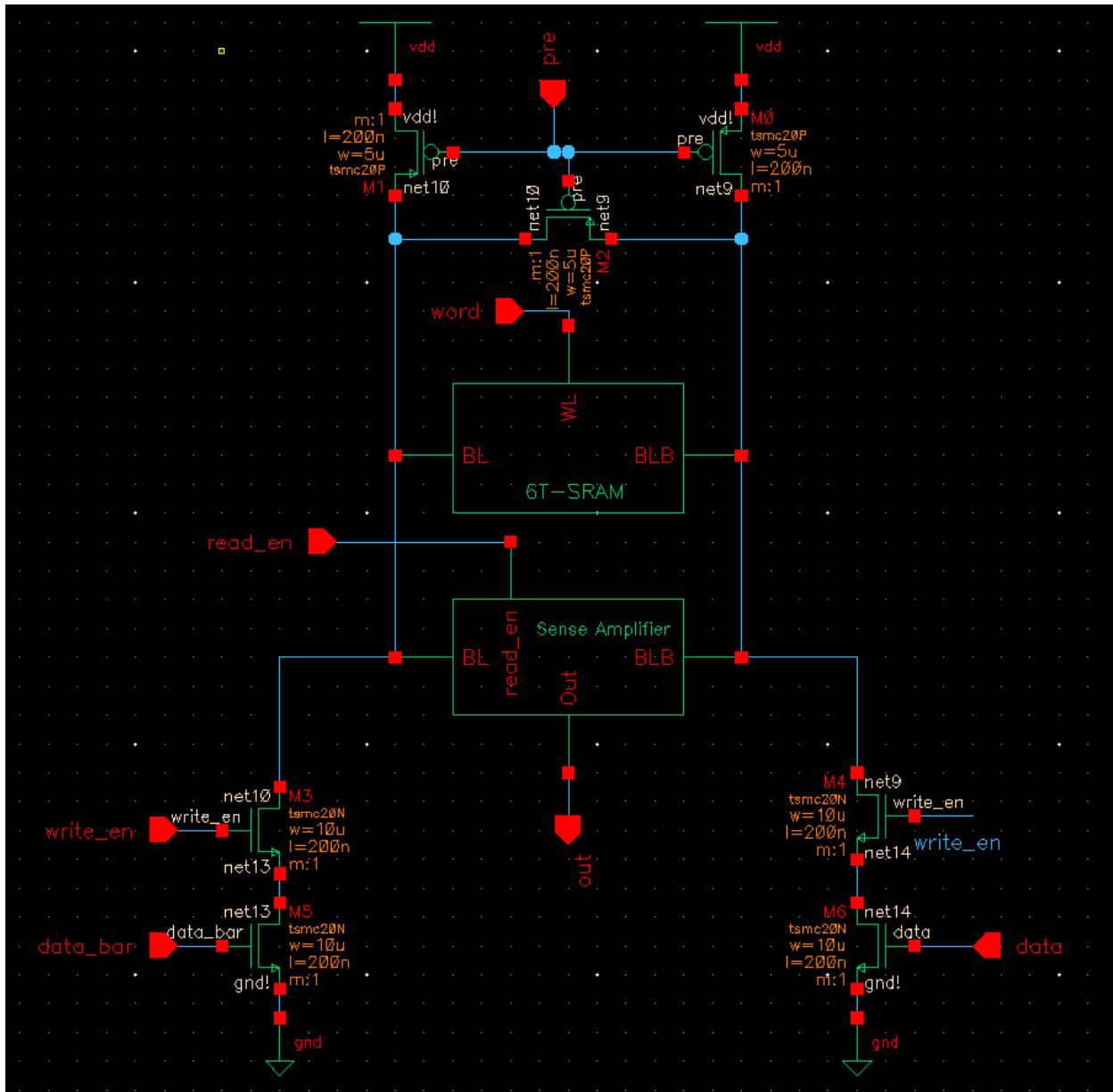


Single SRAM Functionality Test

Precharge circuit, SRAM cell, Sense amplifier and Write circuit are used to build the write data path in order to verify the read and write operation of the single SRAM cell.

Schematic:

512 Bit SRAM

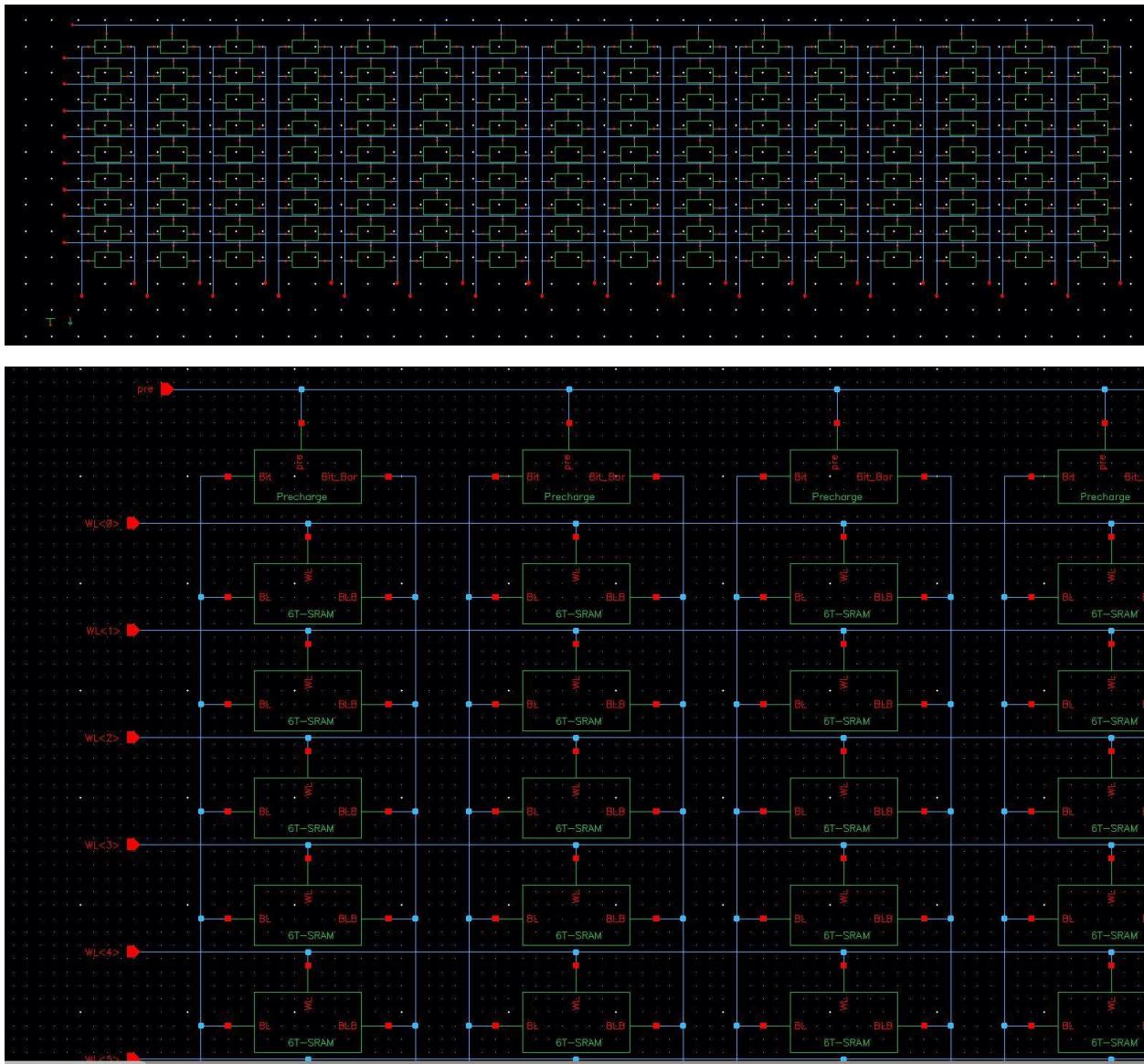


SRAM Bank

A SRAM Bank of 128 bit (8×16) is designed as shown below. It consists of 128 SRAM cells and 16 precharge circuits.

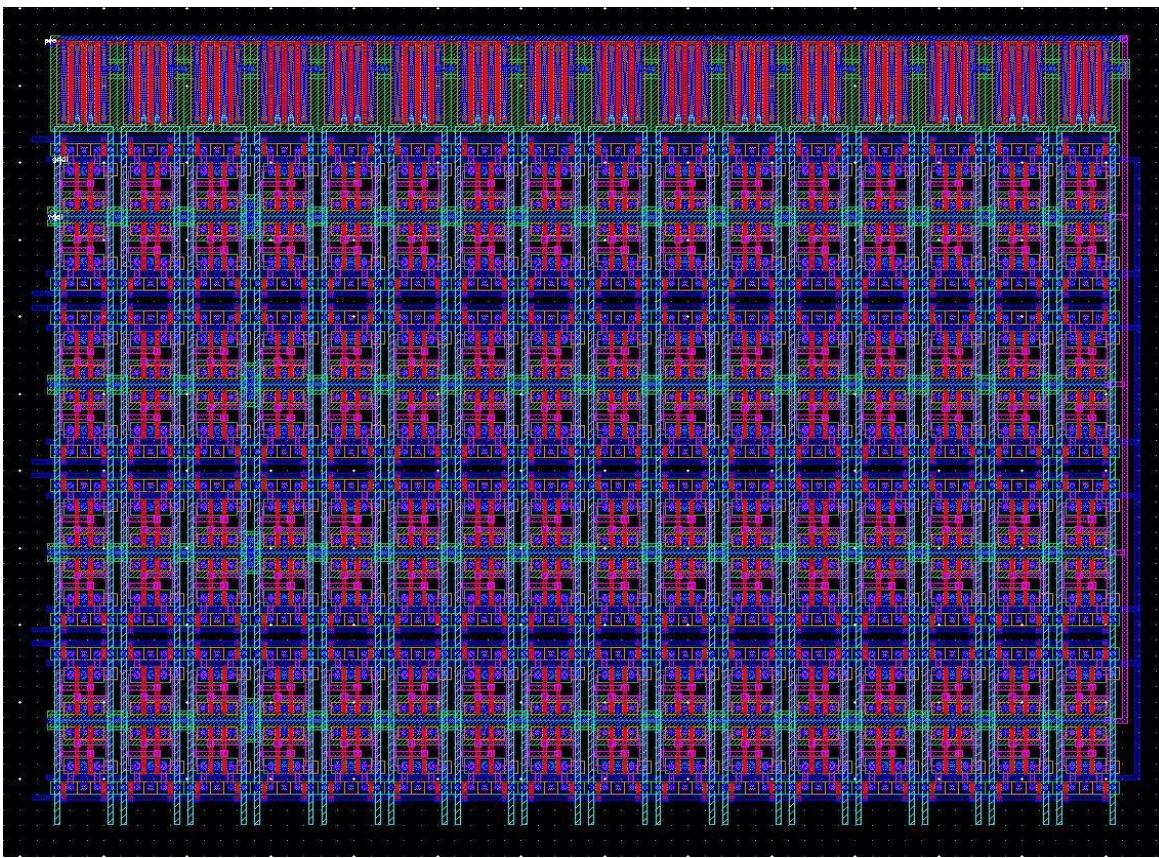
512 Bit SRAM

Schematic:

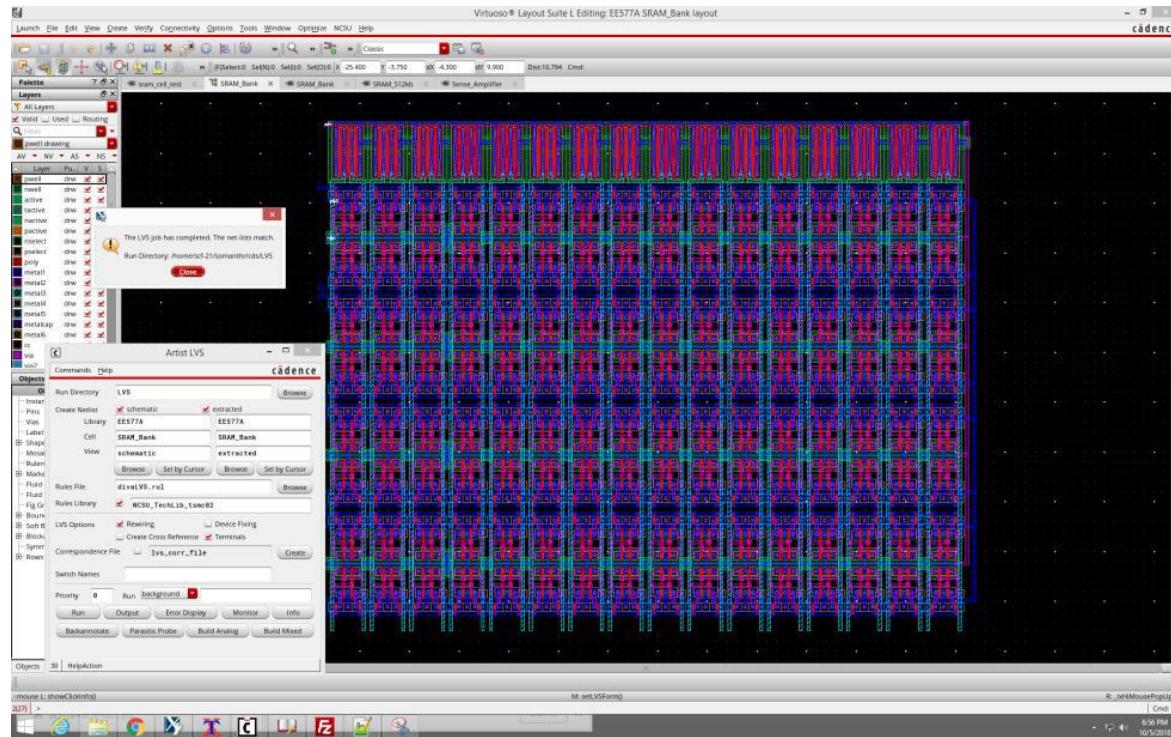


512 Bit SRAM

Layout:



LVS:



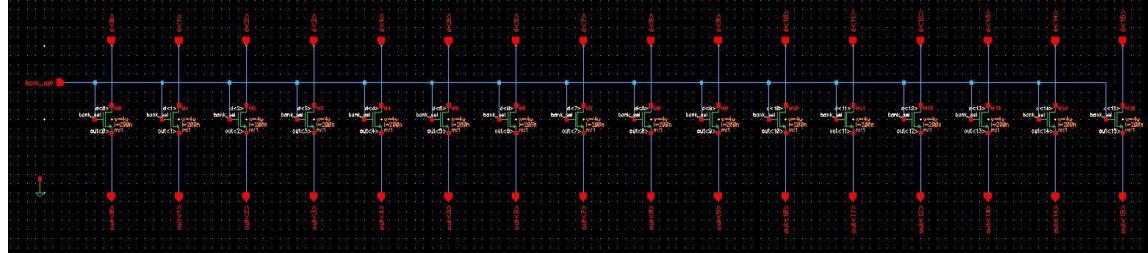
512 Bit SRAM

Write Multiplexer

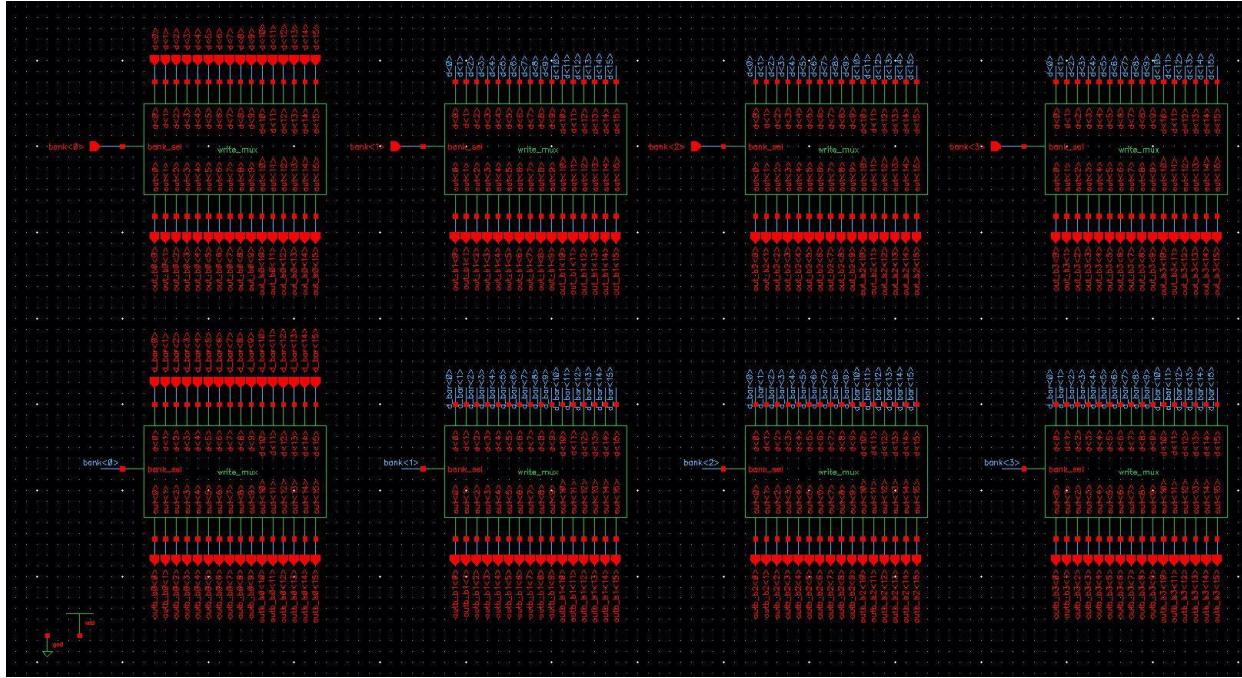
Nmos transistors are used as pass transistors for the write mux.

Schematic:

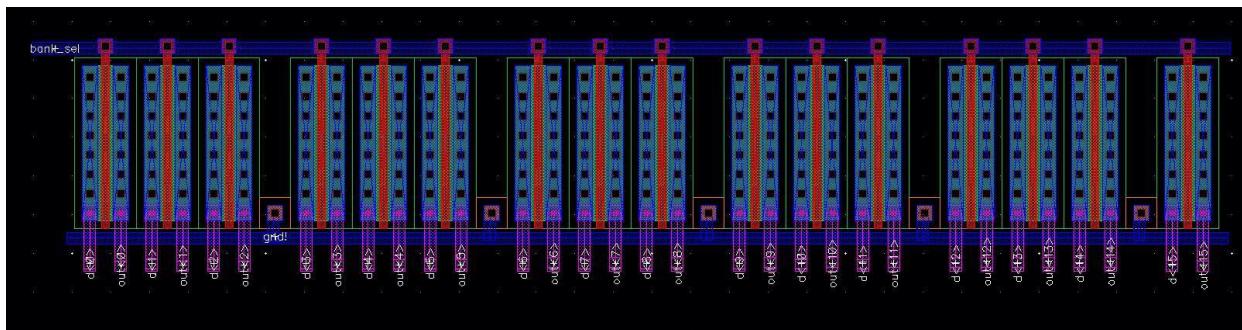
1) 16-bit write multiplexer



2) Write multiplexer for 512 bit SRAM

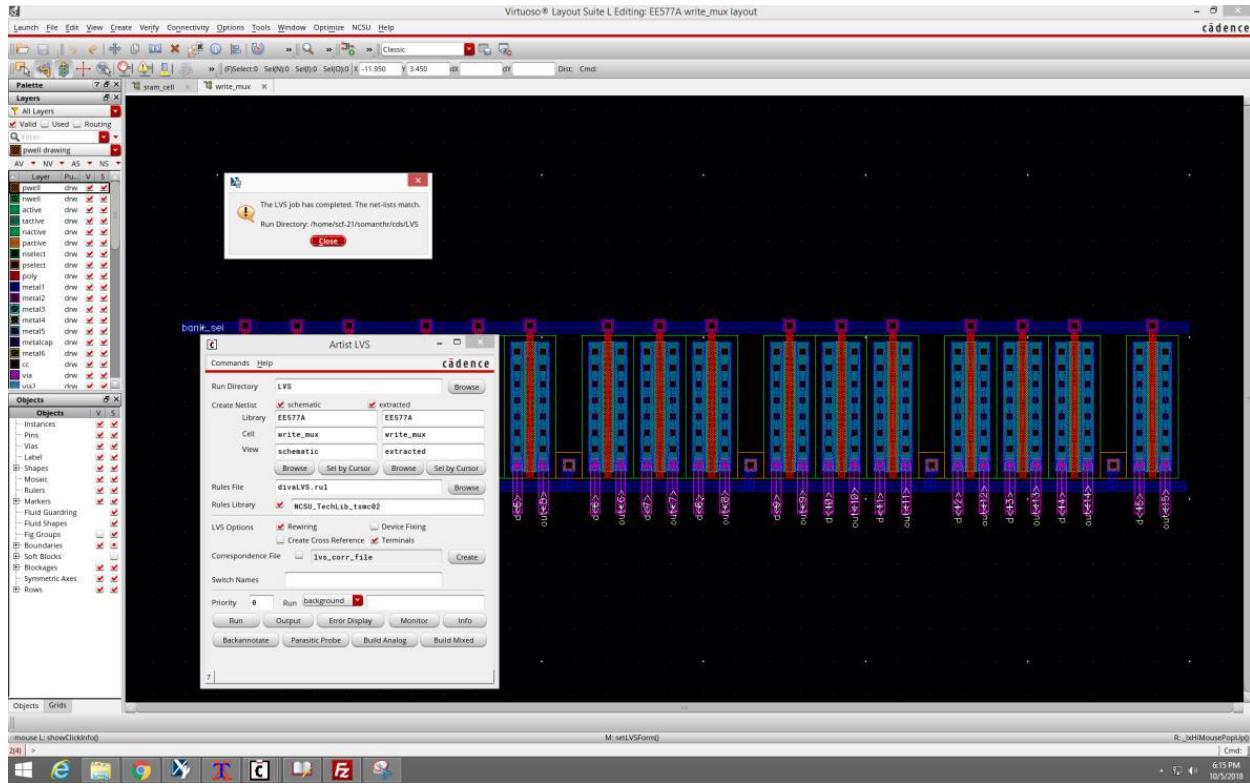


Layout: 16-bit write multiplexer



LVS:

512 Bit SRAM

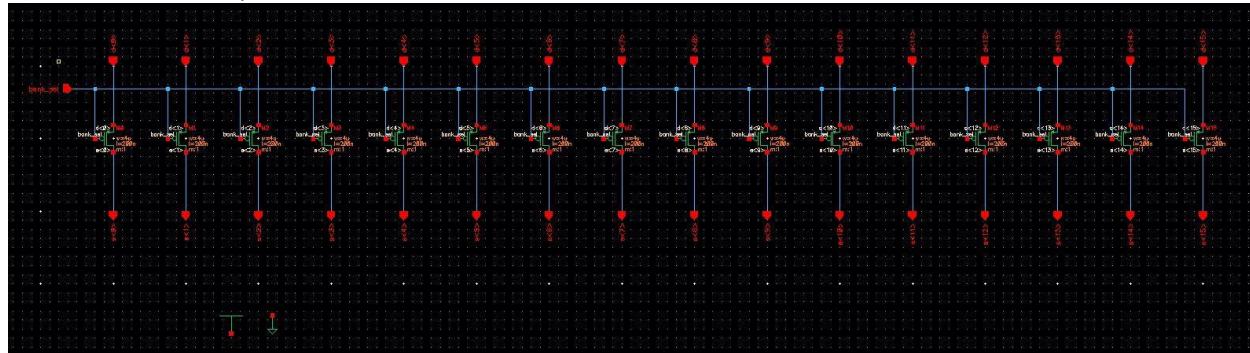


Read Multiplexer

Pmos transistors are used as pass transistors for the read mux.

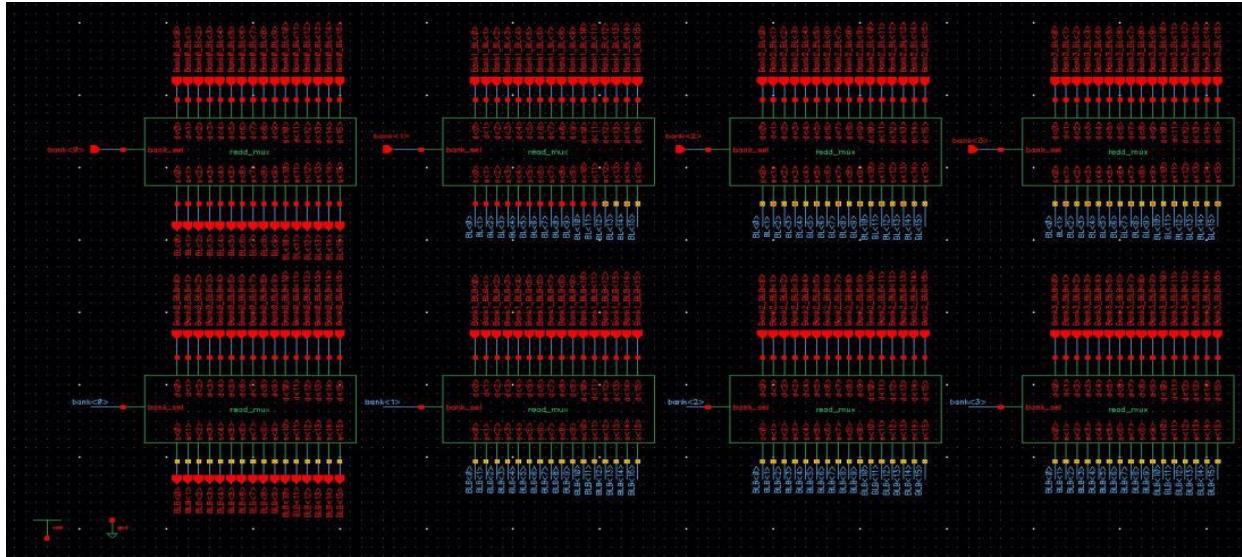
Schematic:

1) 16-bit read multiplexer

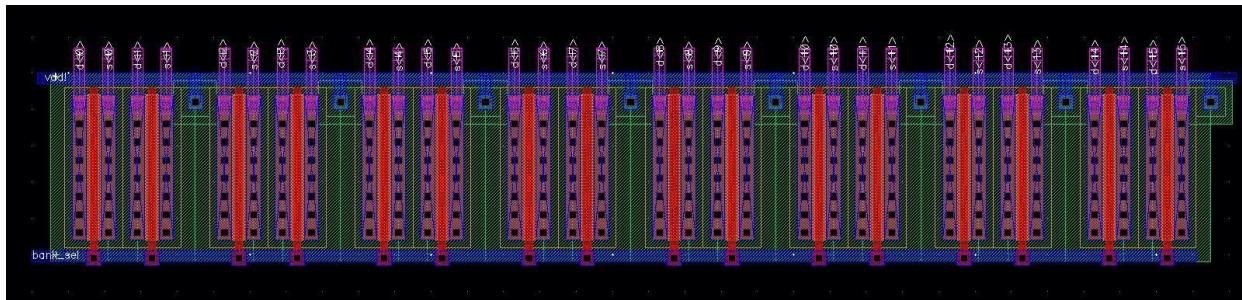


2) Read multiplexer for 512 bit SRAM

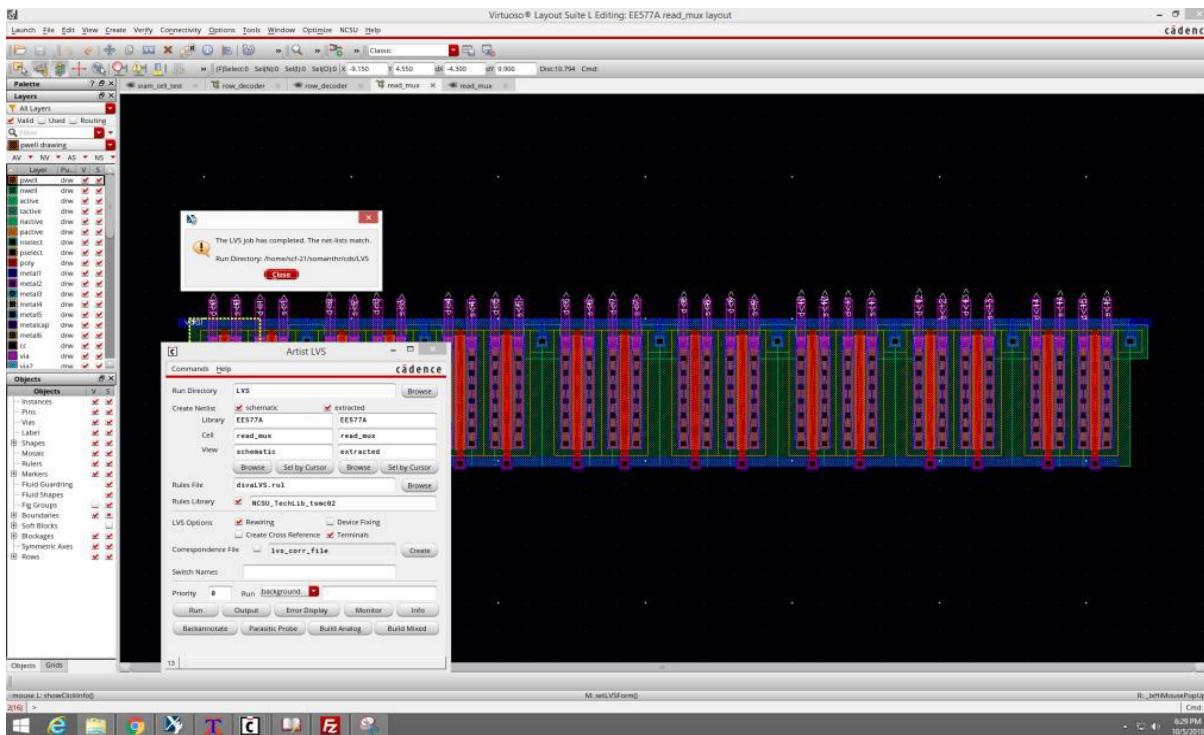
512 Bit SRAM



Layout: 16-bit Read multiplexer



LVS:

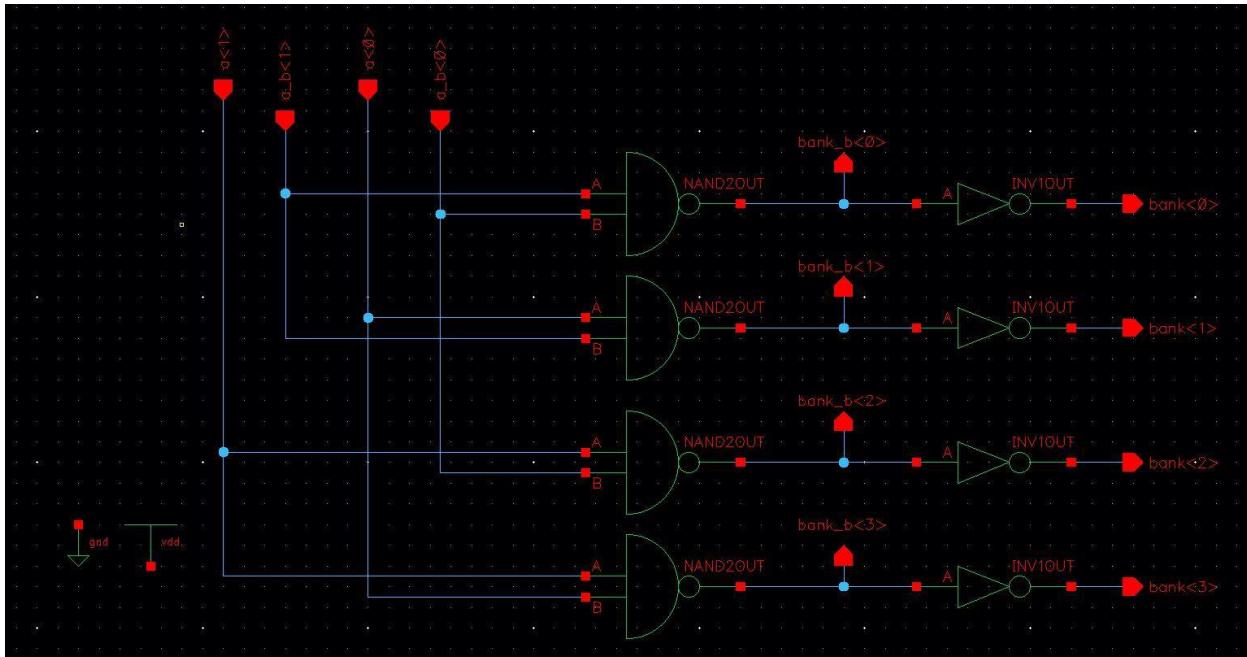


512 Bit SRAM

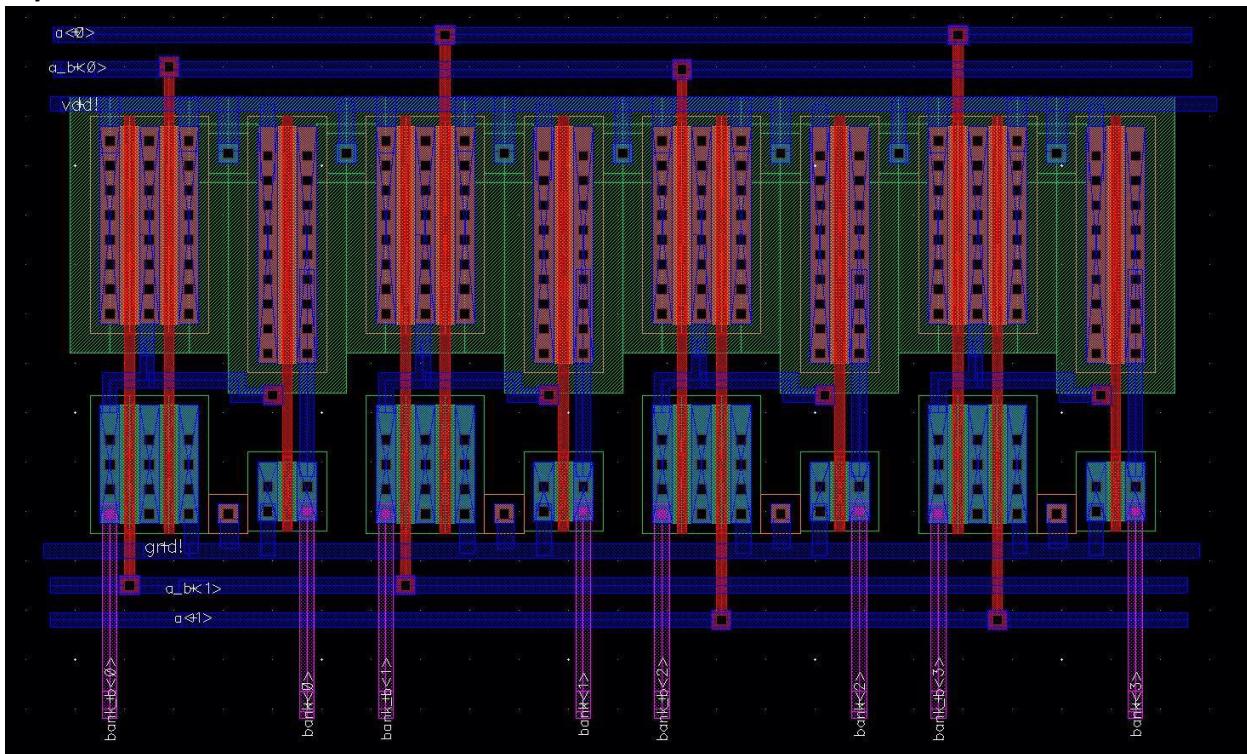
Bank Select

The column Decoder to select the corresponding bank receives the A1 A0 bits and generates 4 select lines to select between the 4 banks (Bank3 – Bank0).

Schematic:

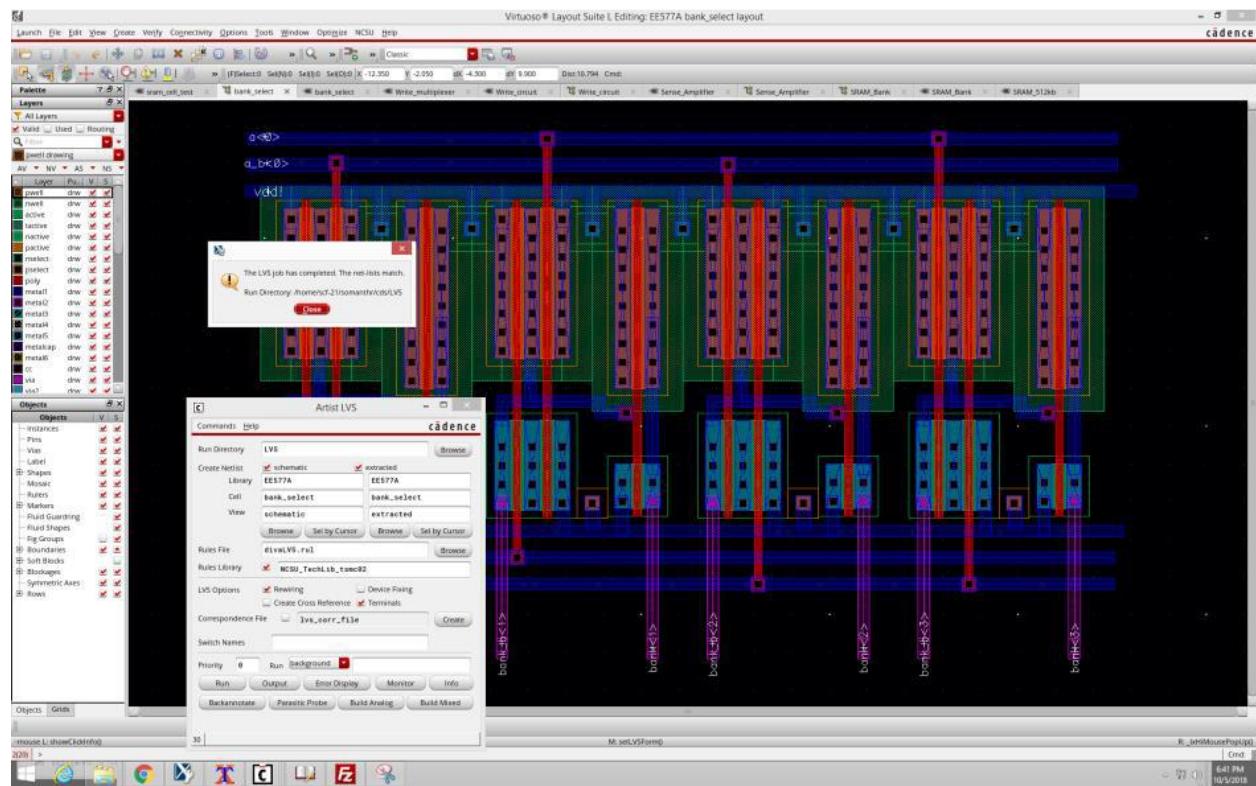


Layout:



512 Bit SRAM

LVS:

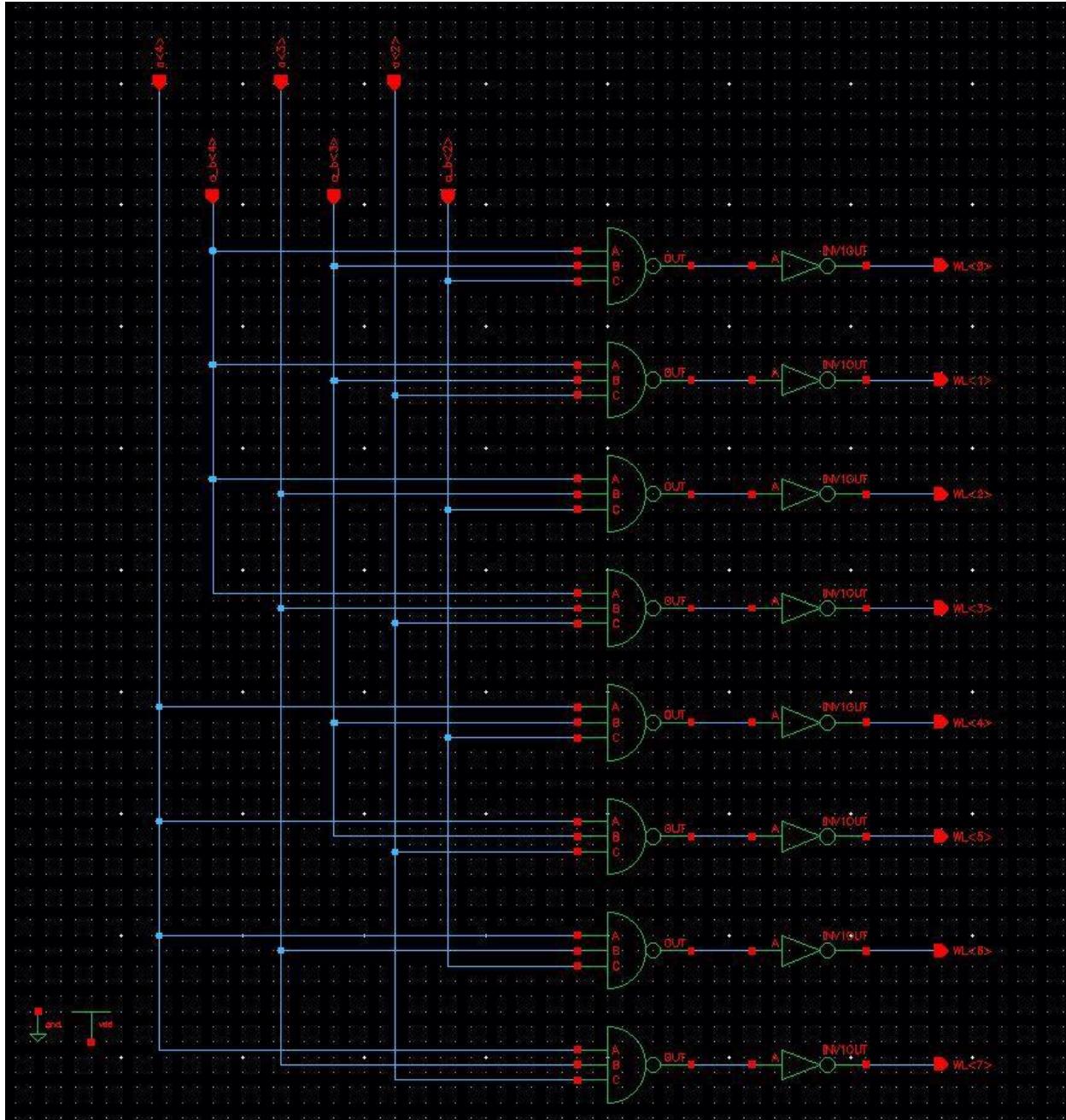


Row Decoder

The row decoder receives the input A4 – A2 Address bits and decodes it to 16 Word Lines each controlling a line of 16 cells in a bank.

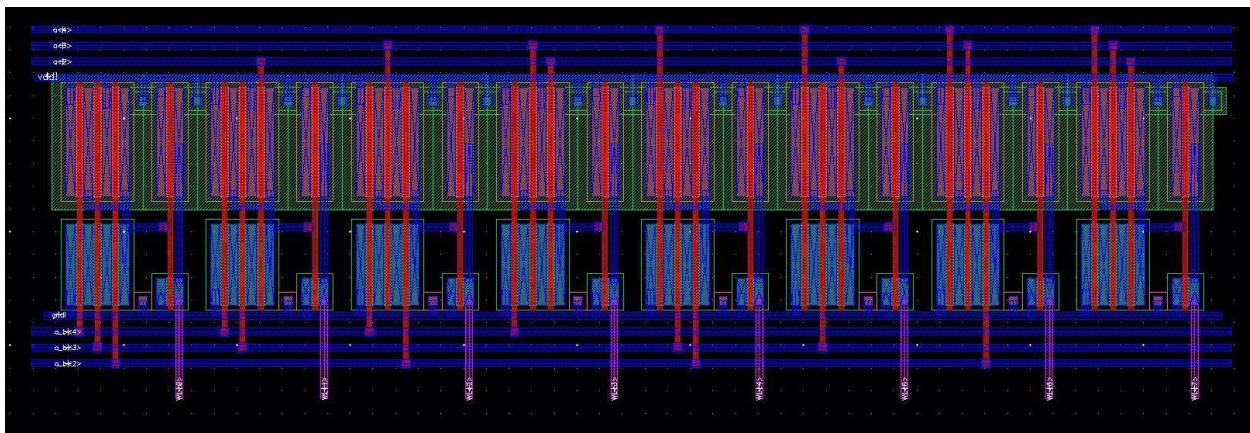
Schematic:

512 Bit SRAM

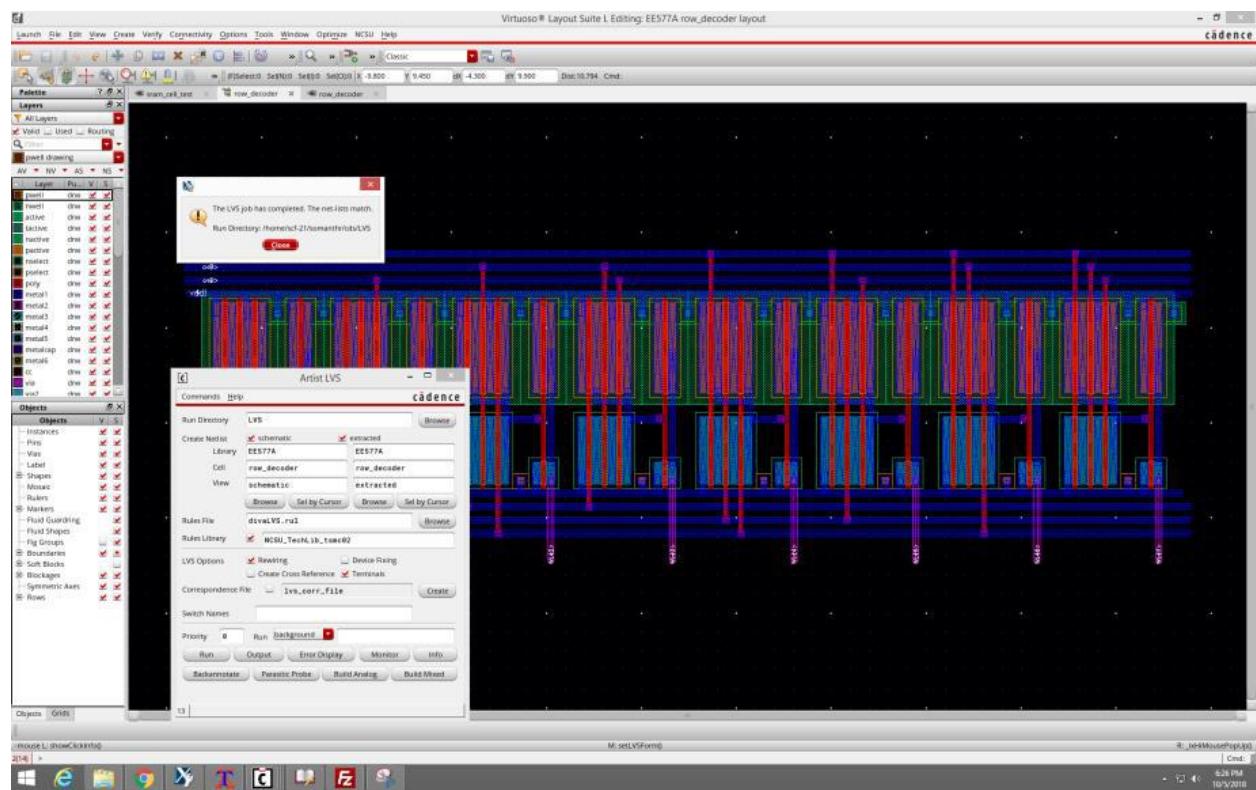


512 Bit SRAM

Layout:

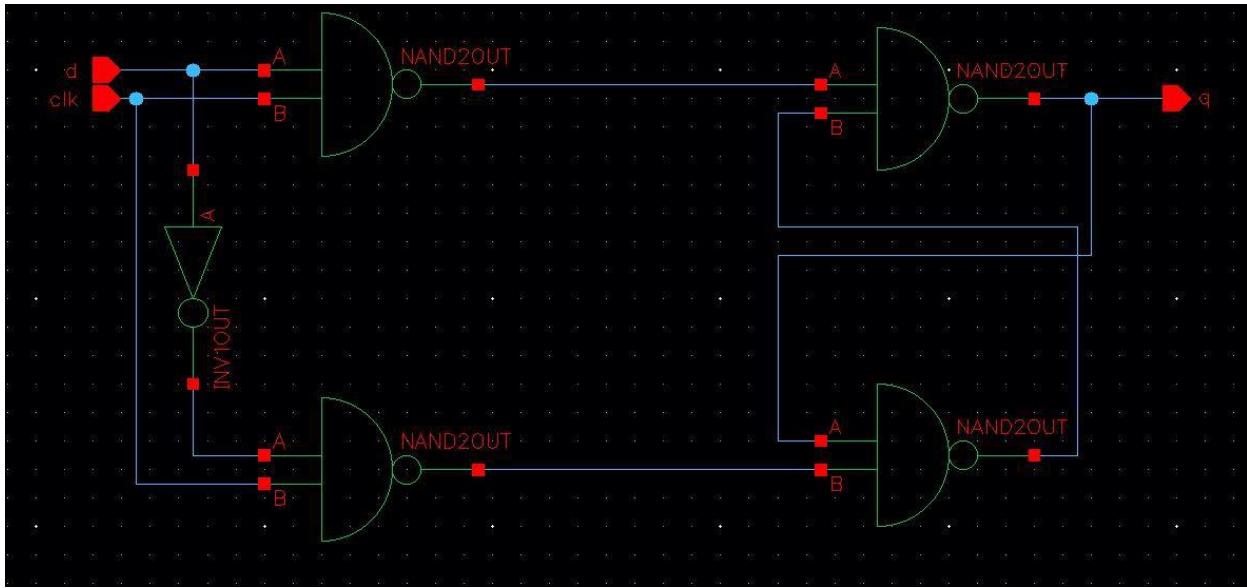


LVS:

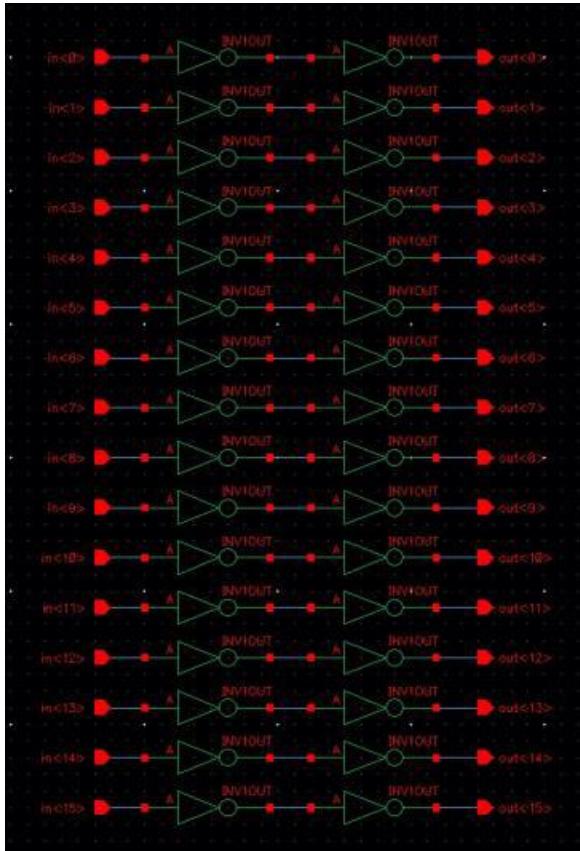


Flip Flop

A D flip-flop is designed as shown below.

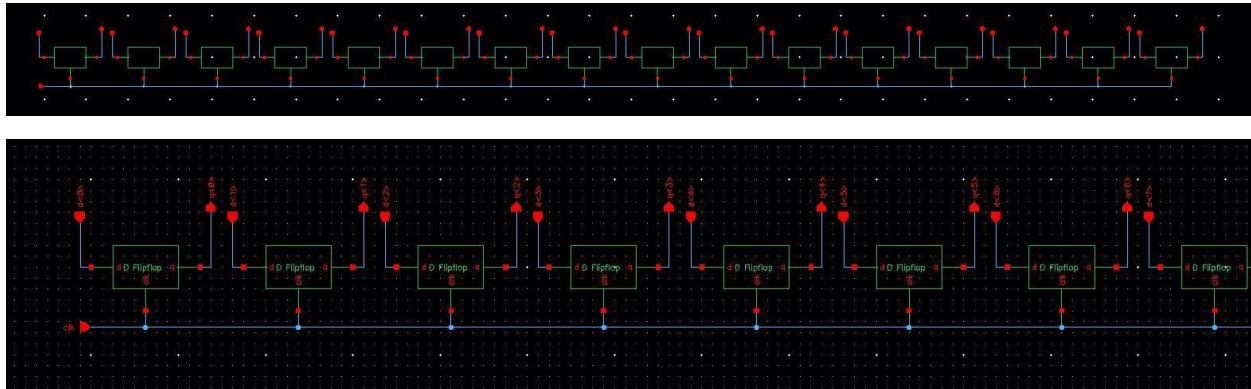


Buffer - A 16-bit buffer is designed using inverters. It is used to provide sufficient delay so that the Register can latch its input.



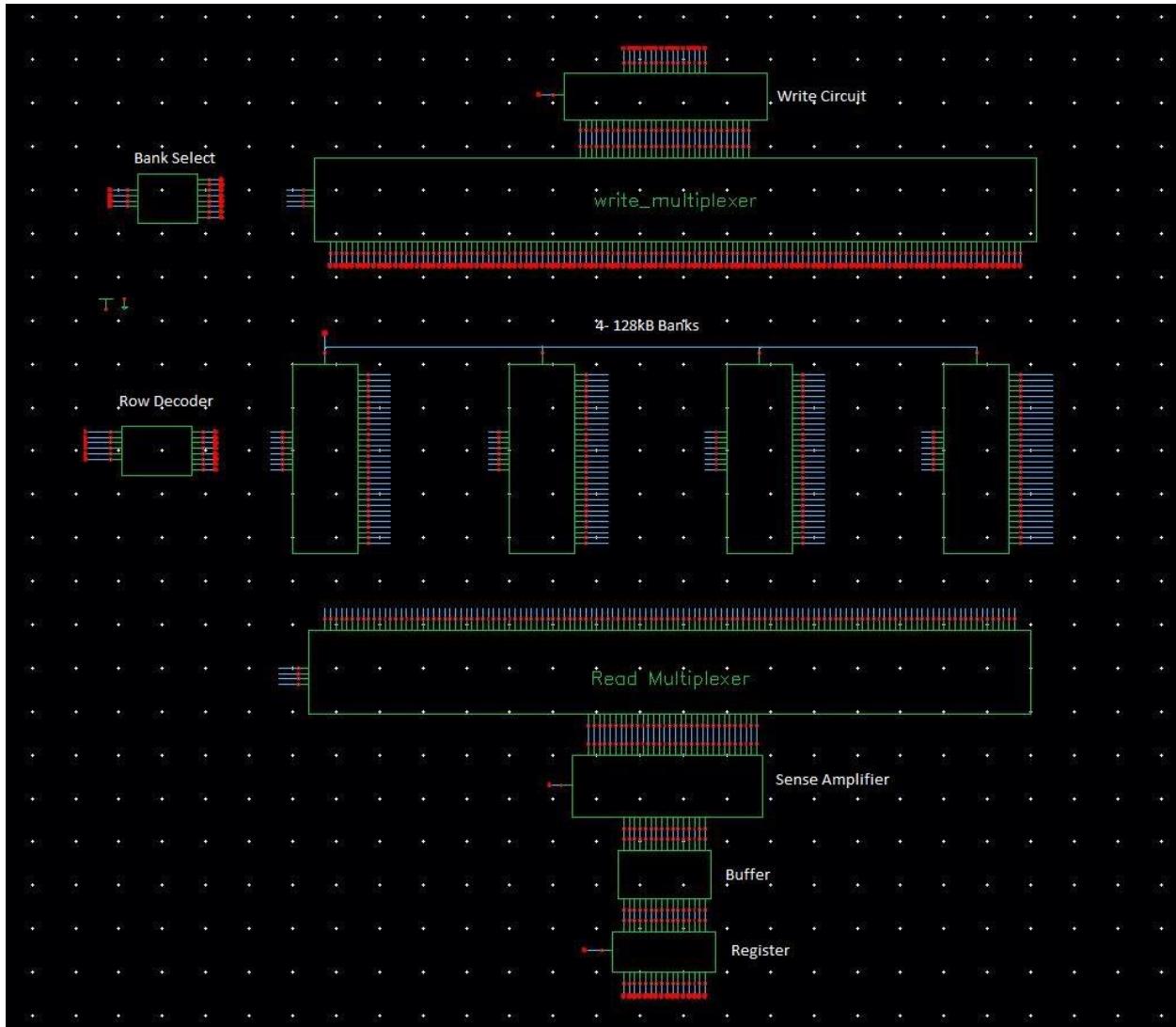
512 Bit SRAM

Register - A 16-bit register is designed using 16 D flip-flops to register the data that is to be read.



512 bit Memory

The schematic for the 512 bit memory with all the components connected is as shown.



512 Bit SRAM

SIMULATION

