CMOS NOR GATE

Adithya Herle P S, Reva University

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Abstract

This paper aims to design a 2-input CMOS NOR Gate. A NOR gate (NOT+OR) is a logic gate which produces output that is true only if all the inputs are false else it produces false output. The CMOS NOR gate circuit as shown in figure.1 consists of pull-up network (i.e. PMOS) in series and pull-down network (i.e. NMOS) in parallel. Number of NMOS and PMOS used depends on the number of inputs for e.g. If I want a 3 input NOR gate then we should use 3 PMOS and 3 NMOS transistors. This paper consists of design and simulation of 2-input CMOS NOR gate followed by simulation results (Waveforms).

1 Reference Circuit Details

The circuit diagram demonstrates the CMOS 2-input NOR gate as shown in Figure.1. The two-input NOR gate uses two PMOS transistors in series between VDD and gate-output, and the complementary circuit of a parallel connection of two NMOS transistors between GND and gate-output as shown in figure.1. Here, first transistor's source terminal is connected to Vdd (high) and lower transistor's (NMOS) drain terminal is connected to Vss (GND). Second PMOS transistor's drain terminal is shorted with both NMOS transistor's source terminal and is given to the output which acts as an output terminal. It behaves complementary to the OR logic. If either input A or B or all are 'high' (1) then at least one of the lower transistors (NMOS) will be saturated, hence producing output 'low' (0). Only in the event of both inputs both inputs being 'low' (0) will both lower transistors (NMOS) be in cutoff mode and both upper transistors (PMOS) be saturated, thus producing output 'high' (1). This behavior defines a NOR Logic function.

2 Reference Circuit

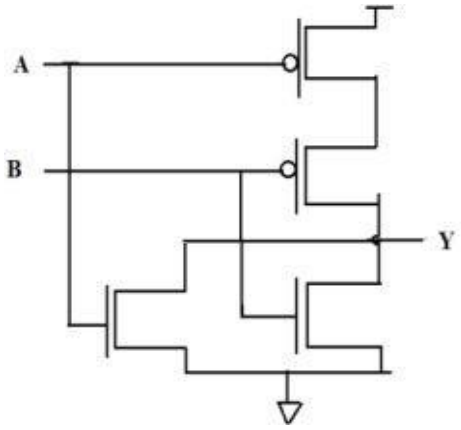

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

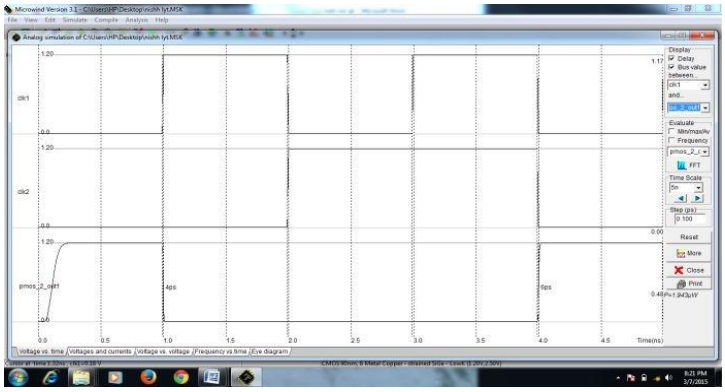

Figure 2: reference waveform.

4 References

[1] Nishali. Layout Design Implementation of NOR Gate. (PDF) Layout Design Implementation of NOR Gate | IJEEE APM - Academia.edu.