

Test Plan

1. Basic memory test: This test tests the functionality of the cache.

Ho to do

1. Write to address.
2. Read from the same.
3. We are not having any data, how to do think on this.
4. Hit\_miss test: This test will make a read and read to **random** address

Output expected

* 1. First Miss
  2. Then Hit
  3. A and b will happen the number of times we write and read.

This test will also do an eviction in back but our test is targeted for testing HIT and Miss so we don’t test LRU in this test.

1. PLRU test: This test will stress the cache lines/sets by making sure all the decisive statements are exercised during the read and write process.

How to do

* 1. Write to same tag bit in random order
  2. Check if you are getting the Least recently used line evicted.
  3. Also check if things are getting evicted possibly in all lines use for loop to do it.

1. MESI FSM test case
2. Write allocate test/write back:
3. Inclusivity test
4. Clear cache test: make all states invalid
5. TAG bits changed what will it do.