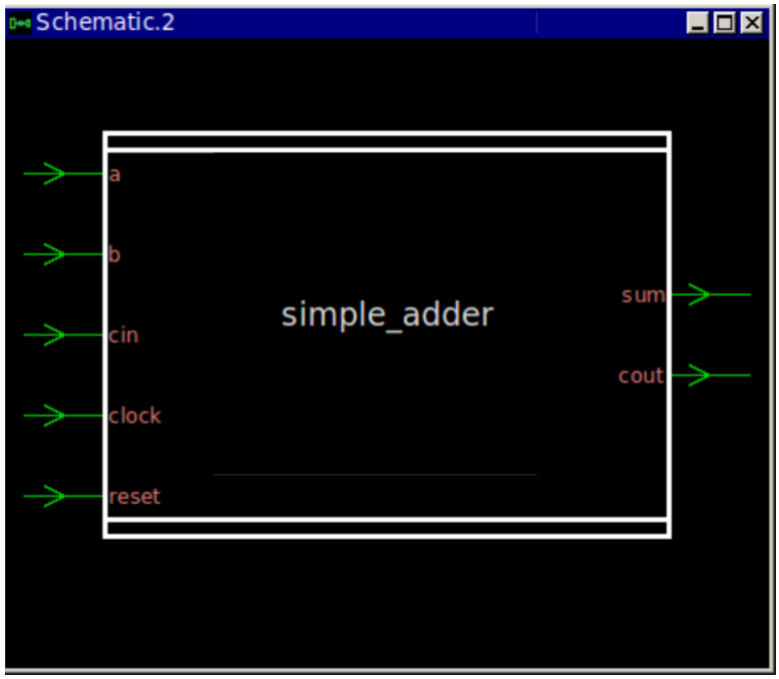
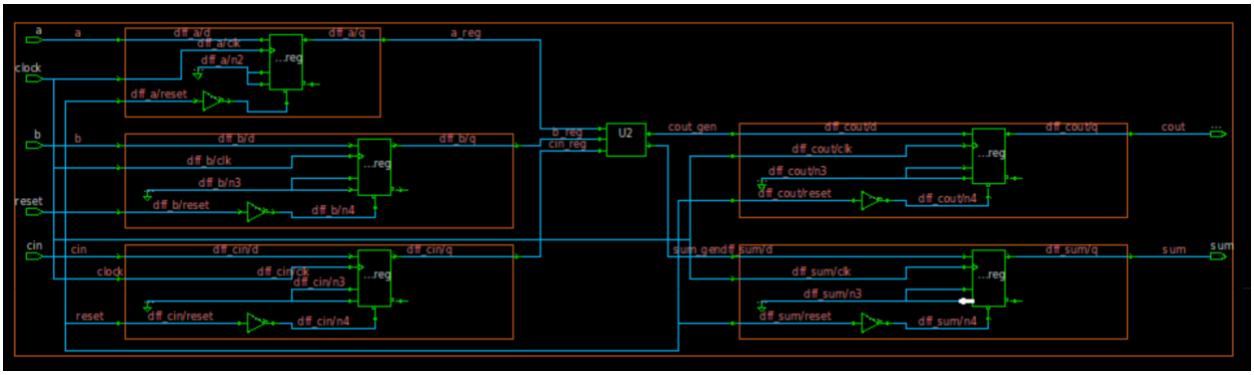
Assignment 1

Adithya Rajagopal

HW_LAB_1_A:

Schematic view for simple_adder.





Assignment 1

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Timing report:

```
dc_shell> report_timing

****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : simple_adder
Version: P-2019.03-SP1-1
Date   : Sun Jan 15 21:31:27 2023
****************************************

Operating Conditions: ss0p95v125c   Library: saed32rvt_ss0p95v125c
Wire Load Model Mode: enclosed

  Startpoint: dff_a/q_reg
              (rising edge-triggered flip-flop clocked by CLK)
  Endpoint: dff_sum/q_reg
            (rising edge-triggered flip-flop clocked by CLK)
  Path Group: CLK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  simple_adder       ForQA                 saed32rvt_ss0p95v125c

  Point                                    Incr       Path
  -----------------------------------------------------------
  clock CLK (rise edge)                    0.00       0.00
  clock network delay (ideal)              0.00       0.00
  dff_a/q_reg/CLK (SDFFARX1_RVT)           0.00       0.00 r
  dff_a/q_reg/Q (SDFFARX1_RVT)             0.20       0.20 f
  dff_a/q (dff_4)                          0.00       0.20 f
  U2/S (FADDX1_RVT)                        0.15       0.35 r
  dff_sum/d (dff_0)                        0.00       0.35 r
  dff_sum/q_reg/D (SDFFARX1_RVT)           0.00       0.35 r
  data arrival time                                   0.35

  clock CLK (rise edge)                   0.50       0.50
  clock network delay (ideal)             0.00       0.50
  dff_sum/q_reg/CLK (SDFFARX1_RVT)        0.00       0.50 r
  library setup time                     -0.12       0.38
  data required time                                 0.38
  -----------------------------------------------------------
  data required time                                 0.38
  data arrival time                                 -0.35
  -----------------------------------------------------------
  slack (MET)                                        0.03


1
dc_shell>
```

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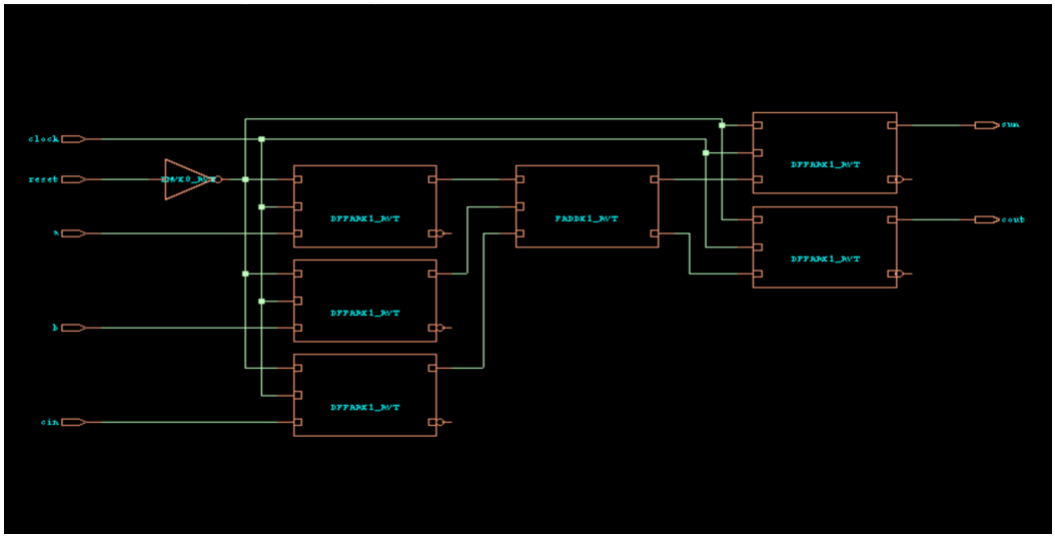
HW_LAB_1_B:

Schematic view



Report timing:

```
@genus:root: 3> report_timing
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.12-s068_1
  Generated on:           Jan 15 2023  11:16:04 pm
  Module:                 simple_adder
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (62 ps) Late External Delay Assertion at pin cout
          Group: CLK
     Startpoint: (R) dff_cout_q_reg/CLK
          Clock: (R) CLK
       Endpoint: (R) cout
          Clock: (R) CLK

                     Capture       Launch
       Clock Edge:+      500            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     500            0

      Output Delay:-     250
     Required Time:=     250
      Launch Clock:-       0
         Data Path:-     188
             Slack:=      62

Exceptions/Constraints:
  output_delay             250             ou_del_2_1

#-------------------------------------------------------
# Delay Arrival    Cell      Flags     Timing Point
#  (ps)   (ps)
#-------------------------------------------------------
      0       0  (arrival)   -       dff_cout_q_reg/CLK
    188     188  DFFARX1_RVT -       dff_cout_q_reg/Q
      0     188  (port)      <<<     cout
#-------------------------------------------------------
```

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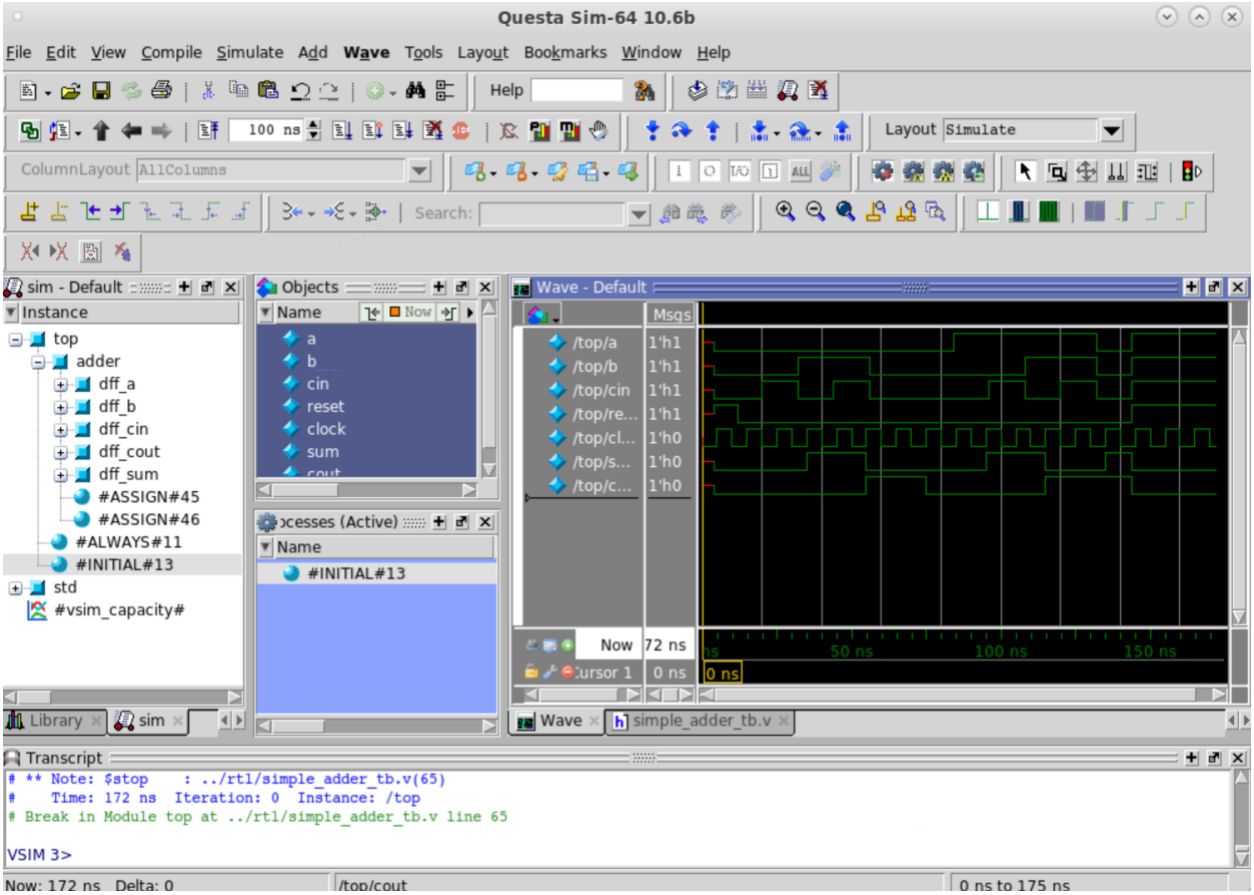
Comparison Table

Constraints	DC	Genus
Cell Count	11	7
Combinational Cell Count	6	2
Sequential Cell Count	5	5
Cell Area	56.92826	41.68
WNS	0	0
TNS	0	0
Violation count	0	0

HW_LAB_1_C:

FE RTL Waveform



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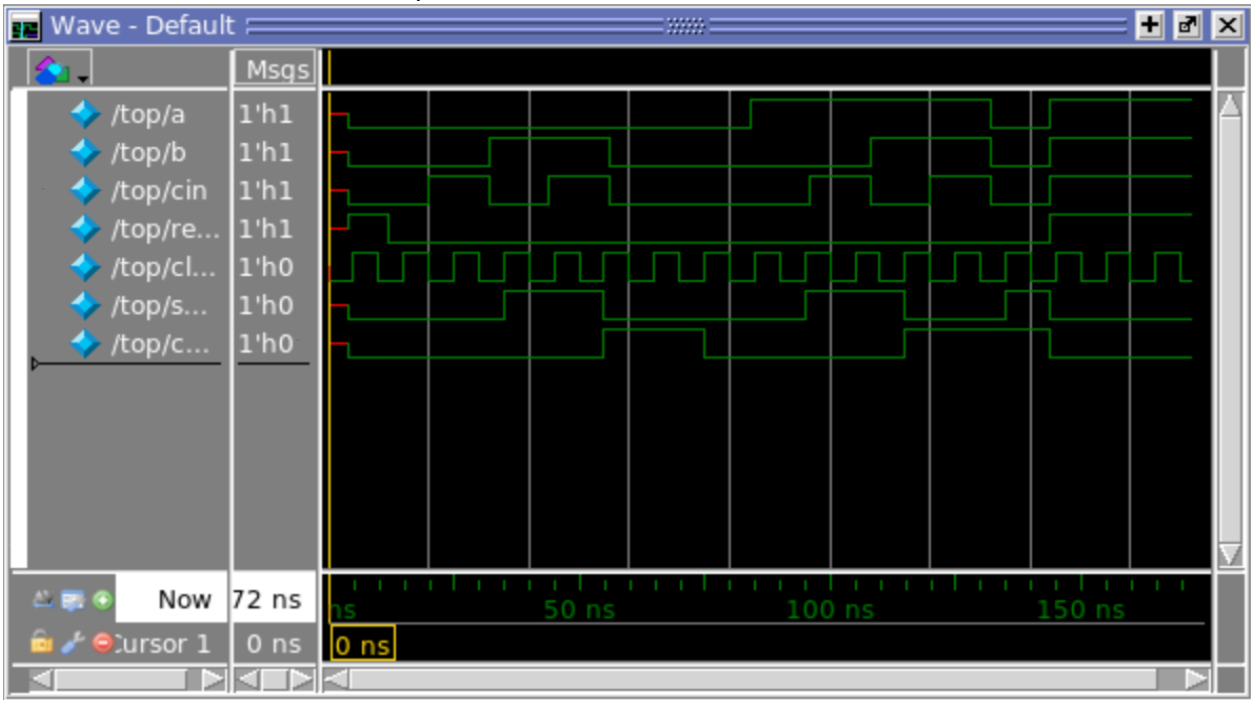
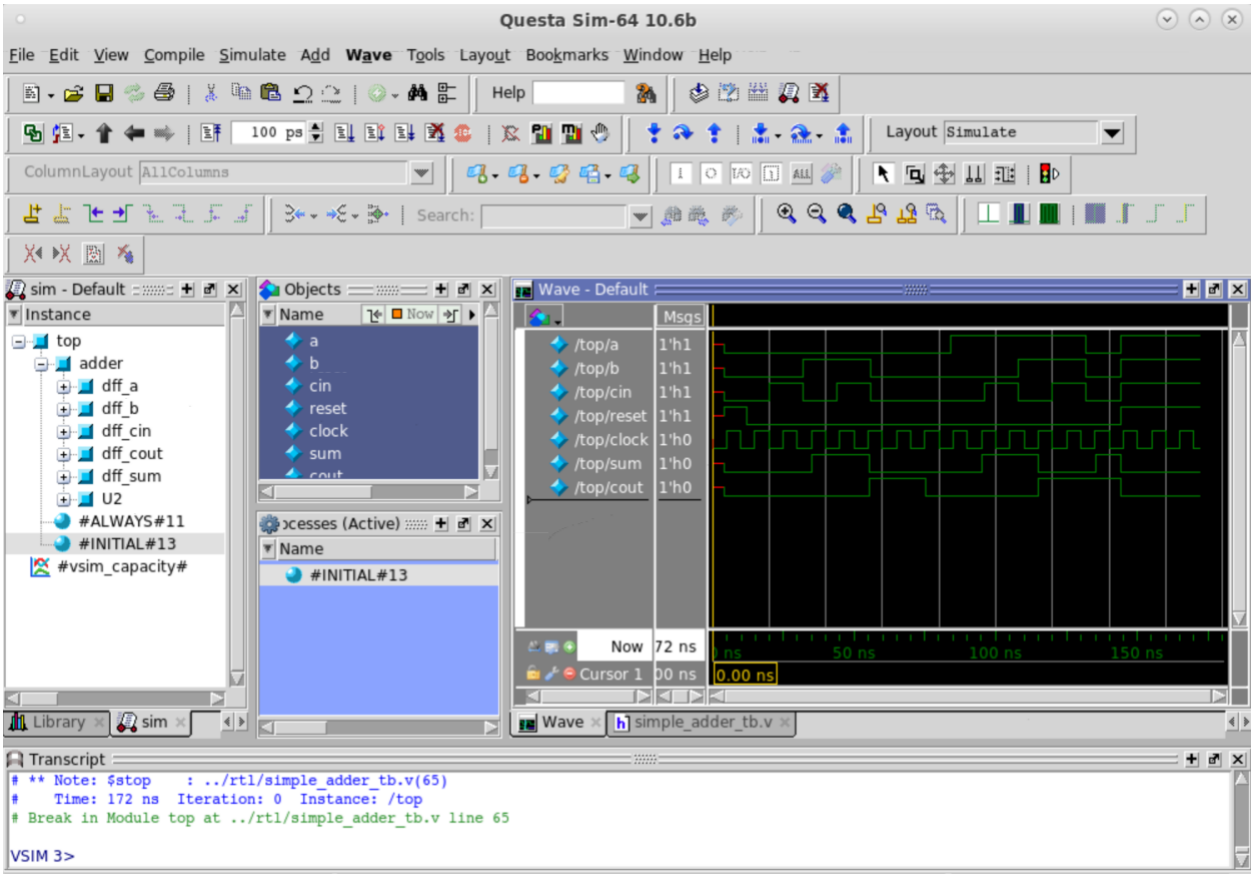
In detail RTL Waveform for comparison,



BE Netlist Waveform



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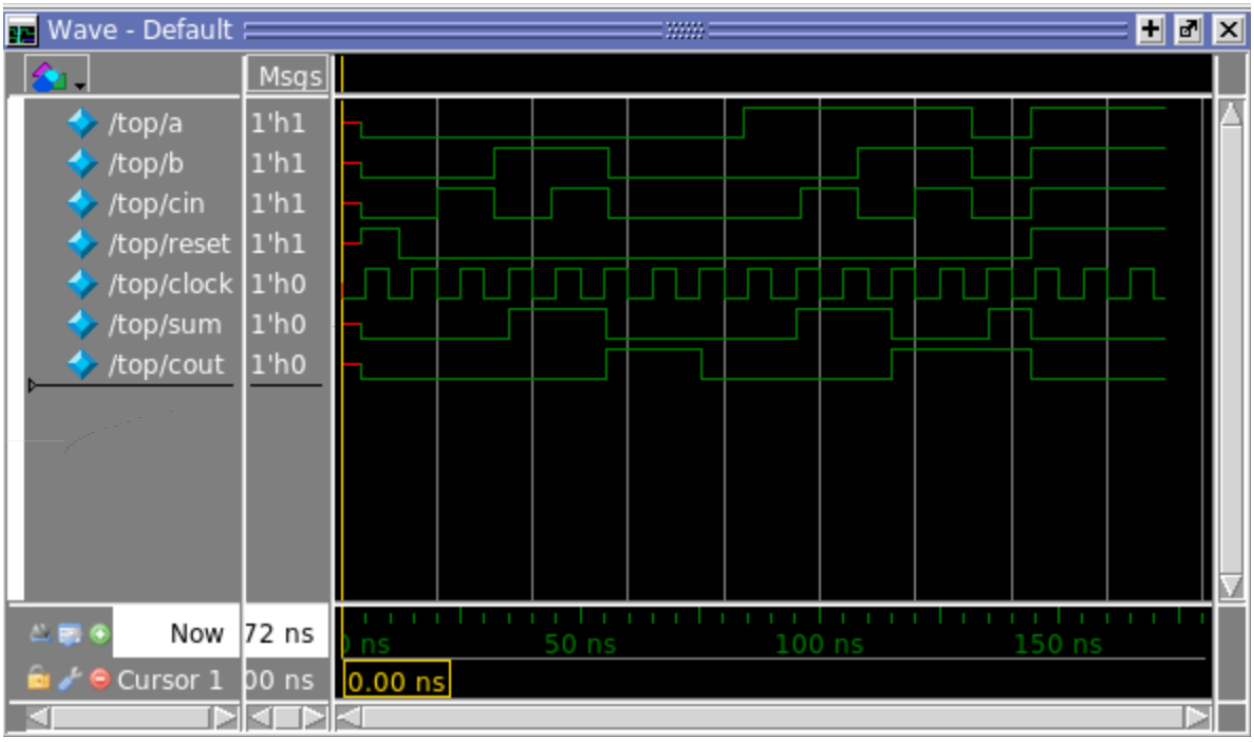
In Detail Waveform for the same



Comparison statement between FE RTL vs BE Netlist

Waveforms are same for both Front end and Back end hence the RTL and generated netlist has same functionality.

Questa Commands

vlib: creates a design library

vmap: Defines the mapping between a logical library name and a directory

vlog: Compiles all the Verilog files

vsim: Starts the VHDL/Questa simulator

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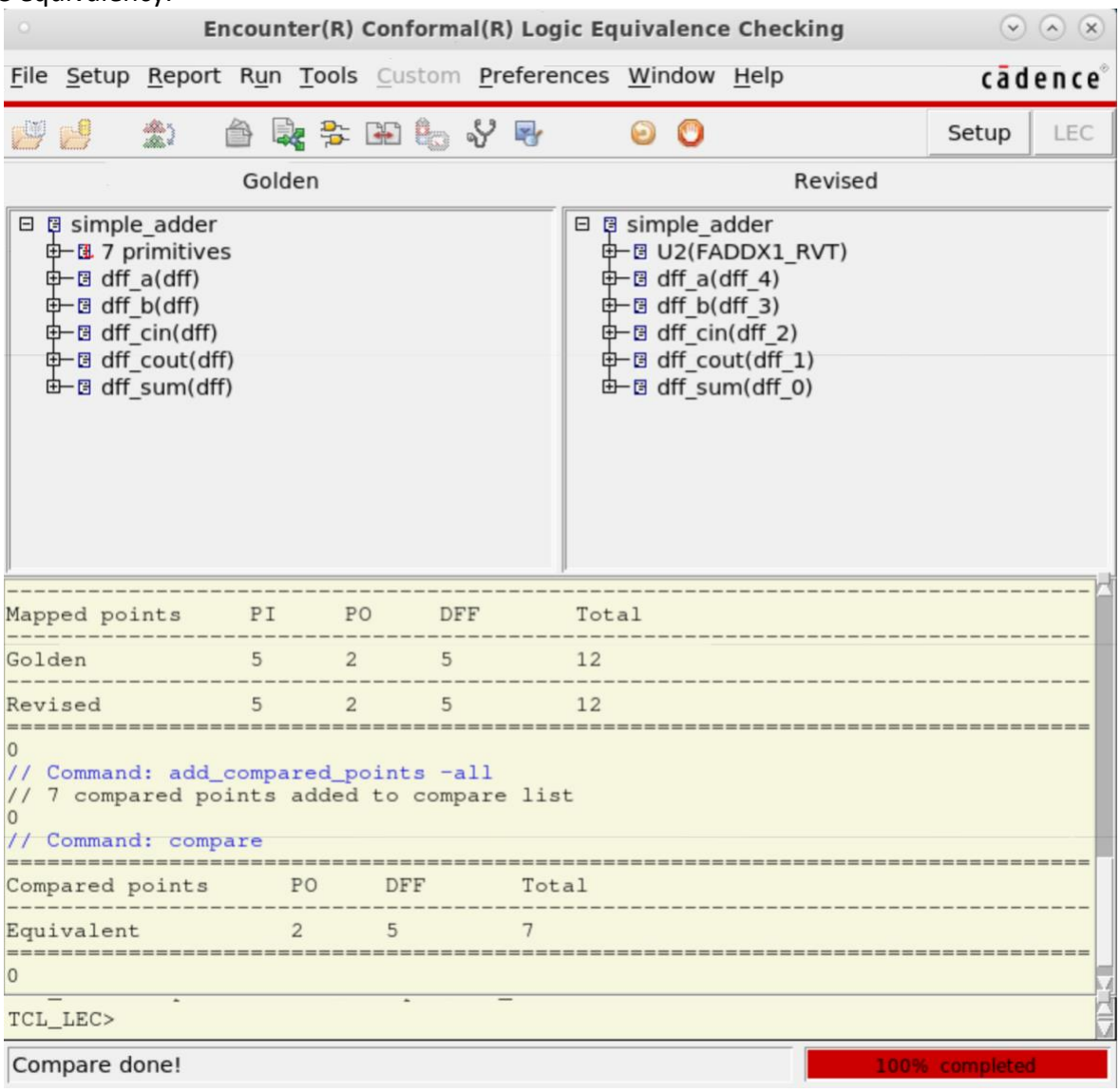
HW_LAB_1_D:

LEC equivalency.



Commands used in LEC:

Commands	**Description**
Lec -dofile	Lec tool is invoked and commands in dofile is executed
Lec -tclmode	Lec tool is invoked in tclmode

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Commands	**Description**
Read_design	Reads the RTL or netlist or library files required for the lec run
Set_system_mode	To switch system modes
Add_compared_points	To specify which mapped points conformal compares.
compare	Compare the points added in the list and tells whether he key points are equivalent or not.

HW_LAB_1_E:

https://github.com/adithyakashyap95/lab1-adit5