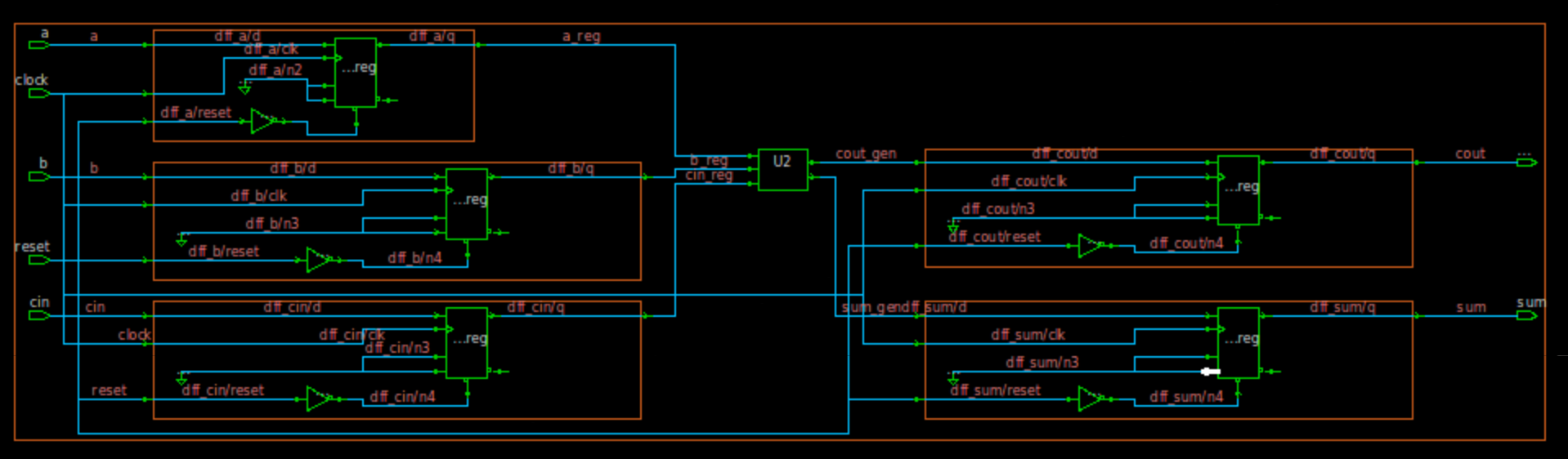
**HW\_LAB\_1\_A:**

Schematic view for simple\_adder.

Graphical user interface

Description automatically generated



**Timing report:**

Text

Description automatically generated

A picture containing graphical user interface

Description automatically generated

**HW\_LAB\_1\_B:**

Schematic view

Diagram

Description automatically generated

**Report timing:**

Text

Description automatically generated

**Comparison Table**

|  |  |  |  |
| --- | --- | --- | --- |
| **Constraints** |  | **DC** | **Genus** |
|  |  |  |  |
| Cell Count |  | 11 | 7 |
| Combinational Cell Count |  | 6 | 2 |
| Sequential Cell Count |  | 5 | 5 |
| Cell Area |  | 56.92826 | 41.68 |
| WNS |  | 0 | 0 |
| TNS |  | 0 | 0 |
| Violation count |  | 0 | 0 |

**HW\_LAB\_1\_C:**

**FE RTL Waveform**

Graphical user interface, application

Description automatically generated

In detail RTL Waveform for comparison,

A screenshot of a computer

Description automatically generated

**BE Netlist Waveform**

Graphical user interface, application

Description automatically generated

In Detail Waveform for the same

A screenshot of a computer

Description automatically generated

**Comparison statement between FE RTL vs BE Netlist**

Waveforms are same for both Front end and Back end hence the RTL and generated netlist has same functionality.

**Questa Commands**

**vlib:** it creates a design library

**vmap:** it defines the mapping between a logical library name and a directory

**vlog:** it compiles all the Verilog files

**vsim:** it starts the VHDL simulator

**HW\_LAB\_1\_D:**

LEC equivalency.

Table

Description automatically generated with medium confidence

**HW\_LAB\_1\_E:**

COPY to GIT and answer other questions