DAY-43

#100DAYSOFRTL

Aim:- Implementation of Full Subtractor using Verilog.

RTL CODE:-

```
///DAY-43
////DATE:-12/02/2024
////Full Subtractor
module FS(input A,B,C,
output b,d);
assign d=A^B^C;
assign b=(~A)&B|B&C|C&(~A);
endmodule
```

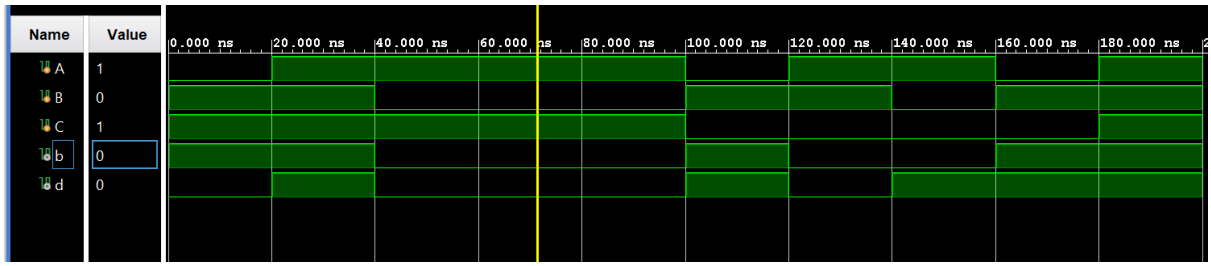
TESTBENCH:-

```
module FS_tb();
reg A,B,C;
wire b,d;
FS uut(A,B,C,b,d);
initial begin
for(int i=0; i<15; i=i+1) begin
A=$random();
B=$random();
C=$random();
#10;
$display("A=%b,B=%b,C=%b,b=%b,d=%b",A,B,C,b,d);
#10;
end
end
initial begin
#200;
$finish();
end
endmodule
```

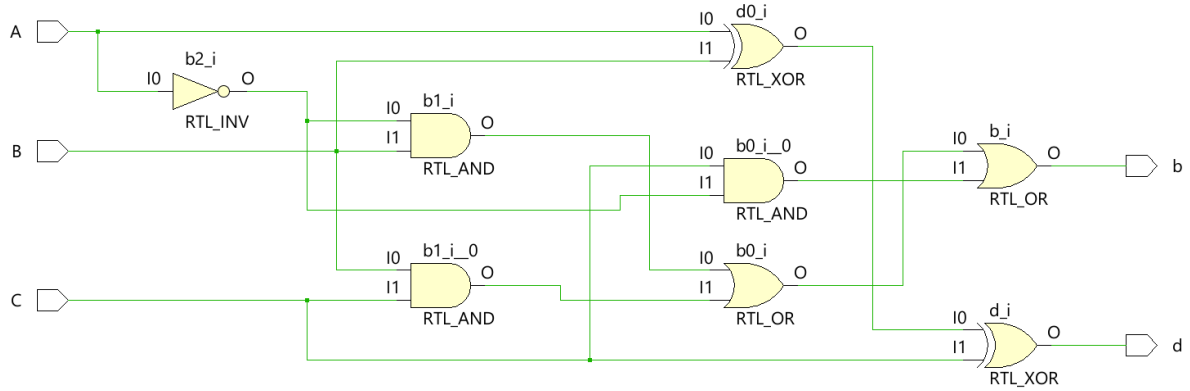
OUTPUT:-

```
A=0,B=1,C=1,b=1,d=0
A=1,B=1,C=1,b=1,d=1
A=1,B=0,C=1,b=0,d=0
A=1,B=0,C=1,b=0,d=0
A=1,B=0,C=1,b=0,d=0
A=0,B=1,C=0,b=1,d=1
A=1,B=1,C=0,b=0,d=0
A=1,B=0,C=0,b=0,d=1
A=0,B=1,C=0,b=1,d=1
A=1,B=1,C=1,b=1,d=1
```

WAVEFORMS:-



SCHEMATIC:-



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