DAY-72

#100DAYSOFRTL

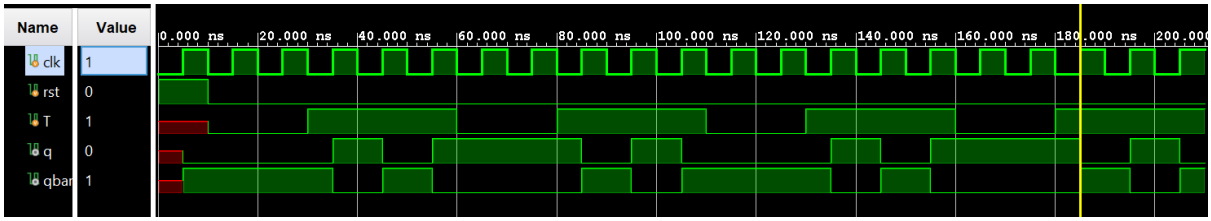
Aim:- Implementation of JK F/F TO T F/F using Verilog.

RTL CODE:-

```
////DATE:-12/03/2024
///DAY-72
////Implementation of JK FF TO T FF
module Day_72_(input clk,rst,T,
output q,qbar);
Jkff jkff(clk,rst,T,T,q,qbar);
endmodule


module Jkff(input clk,rst,J,K,
output reg q, qbar);
always@(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case({J,K})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={2'b10};
2'b11:{q,qbar}<={qbar,q};
default: begin end
endcase
end
end
endmodule
```

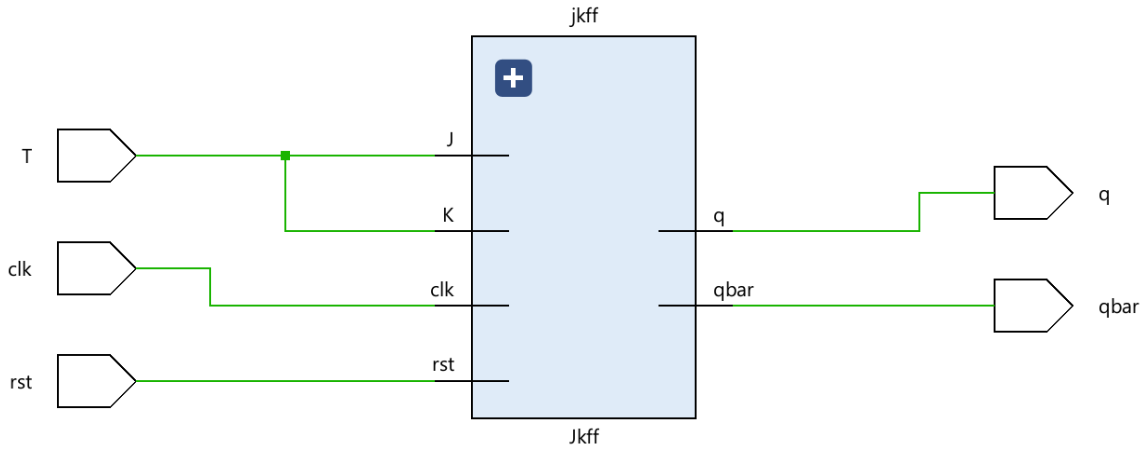
WAVEFORMS:-



TESTBENCH:-

```
module Day_72_tb();
reg clk,rst,T;
wire q,qbar;
Day_72_ uut(clk,rst,T,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
T=0; #20;
T=1; #30;
T=0; #20;
T=1; #30;
T=0; #20;
T=1; #30;
T=0; #20;
T=1; #30;
$finish();
end
endmodule
```

SCHEMATIC:-



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