DAY-73

#100DAYSOFRTL

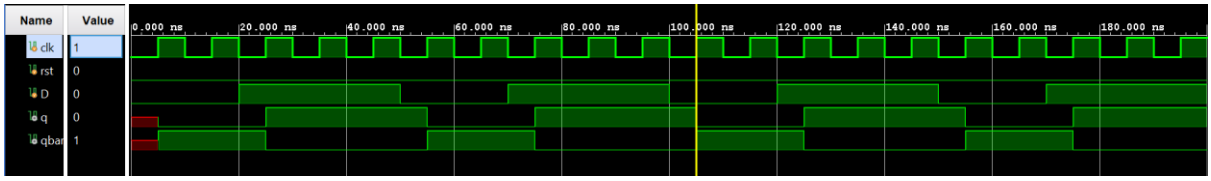
Aim:- Implementation of JK F/F TO D F/F using Verilog.

RTL CODE:-

```
////DATE:-13/03/2024
////DAY-73
////Implementation of JK FF TO D FF
module Day_73(input clk,rst,D,
output q,qbar);
wire w1;
not g1(w1,D);
Jkff1 jkff(clk,rst,D,w1,q,qbar);
endmodule

/// JK flipflop
module Jkff1(input clk,rst,J,K,
output reg q, qbar);
always@(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case({J,K})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={2'b10};
2'b11:{q,qbar}<={qbar,q};
default: begin end
endcase
end
end
endmodule
```

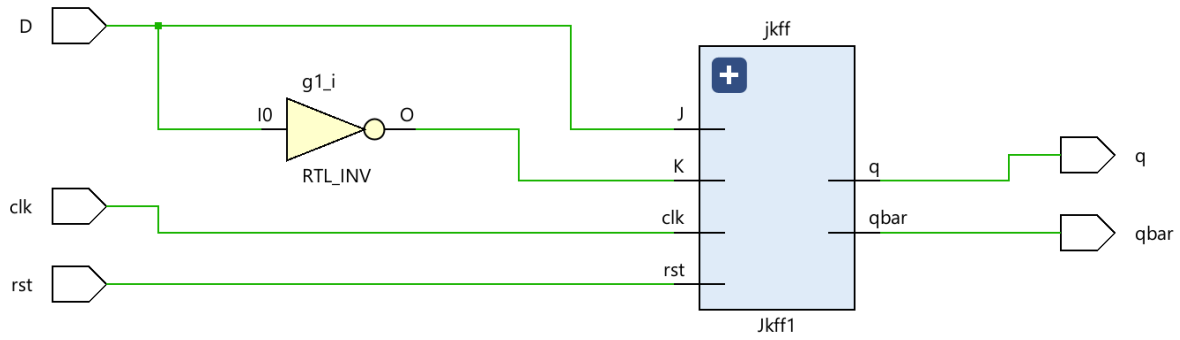
WAVEFORMS:-



TESTBENCH:-

```
module Day_73_tb();
reg clk,rst,D;
wire q,qbar;
Day_73 uut(clk,rst,D,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1;
rst=0;
D=0; #20;
D=1; #30;
D=0; #20;
D=1; #30;
D=0; #20;
D=1; #30;
D=0; #20;
D=1; #30;
$finish();
end
endmodule
```

SCHEMATIC:-



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