DAY-90

#100DAYSOFRTL

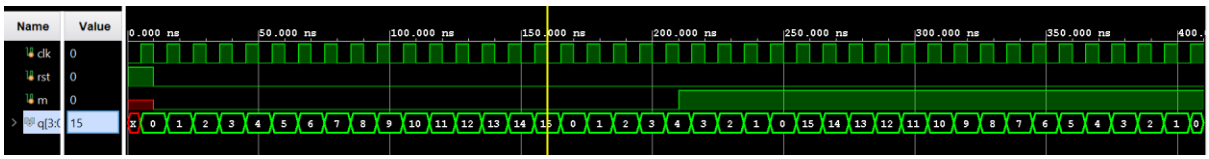
Aim:- Implementation of 4-BIT SYNCHRONOUS Up/Down Counter using T Flipflops.

RTL CODE:-

```
////DATE:-30/03/2024
////DAY-90
////Implementation of 4-Bit Synochronous up/down Counter with control input m using T flipflop
module Day_90(input clk,rst,m, output [3:0] q);
wire w1,w2,w3;
wire [3:0]qbar;
assign w1=(q[0]&q[1]&(~m))|((~q[0])&(~q[1])&(m));///m is a control input 0 for up and 1 for down counting.
assign w2=(q[0]^m);
assign w3=(q[2]&q[1]&q[0]&(~m))|((~q[2])&(~q[1])&(~q[0])& m);
tff t1(clk,rst,1'b1,q[0],qbar[0]);
tff t2(clk,rst,w2,q[1],qbar[1]);
tff t3(clk,rst,w1,q[2],qbar[2]);
tff t4(clk,rst,w3,q[3],qbar[3]);
endmodule

module tff(input clk,rst,T,
output reg q,output qbar);
always@(posedge clk) begin
if(rst)
q<=0;
else begin
case(T)
1'b0:q<=q;
1'b1:q<=~q;
endcase
end
end
assign qbar=(~q);
endmodule
```

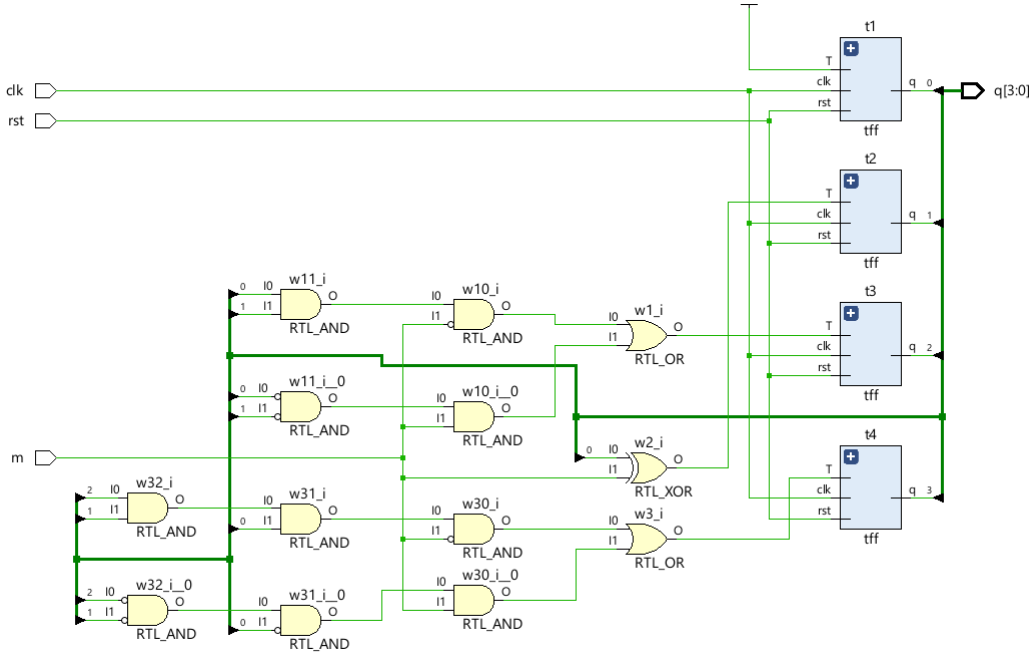
WAVEFORMS:-



TESTBENCH:-

```
module Day_90_tb();
reg clk,rst,m;
wire [3:0]q;
Day_90 uut(clk,rst,m,q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
m=0;
#200;
m=1;
#200;
$finish();
end
endmodule
```

SCHEMATIC:-



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