DAY-29

#100DAYSOFRTL

Aim:- Implementation of 1:32 Demultiplexer Using Verilog.

RTL CODE:-

```
////DATE:-29/01/2024
////Implementation of 1x32 Demux using 1x8 Demux
module Demux1_1x8(input i, input [2:0] Sel,
output reg [7:0] y);
always@(*) begin
case(Sel)
3'b000:y={7'b0,i};
3'b001:y={6'b0,i,1'b0};
3'b010:y={5'b0,i,2'b0};
3'b011:y={4'b0,i,3'b0};
3'b100:y={3'b0,i,4'b0};
3'b101:y={2'b0,i,5'b0};
3'b110:y={1'b0,i,6'b0};
3'b111:y={i,7'b0};
default:begin end
endcase
end
endmodule

module Demux_1x4( input i, input [1:0] Sel,
output reg [3:0] y);
always @(*) begin
case(Sel)
2'b00:y={3'b0,i};
2'b01:y={2'b0,i,1'b0};
2'b10:y={1'b0,i,2'b0};
2'b11:y={i,3'b0};
default:begin end
endcase
end
endmodule

module Demux_1x32(input i,
input [4:0] Sel, output [31:0] y);
wire [3:0] w;
Demux_1x4 C1(i,Sel[4:3],w[3:0]);
Demux1_1x8 C2(w[3],Sel[2:0],y[31:24]);
Demux1_1x8 C3(w[2],Sel[2:0],y[23:16]);
Demux1_1x8 C4(w[1],Sel[2:0],y[15:8]);
Demux1_1x8 C5(w[0],Sel[2:0],y[7:0]);
endmodule
```

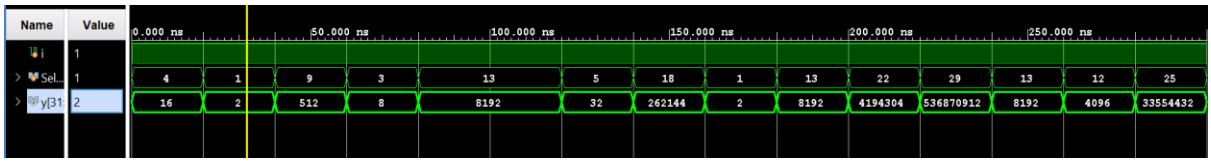
TESTBENCH:-

```
1  module Demux_1x32_tb();
2  reg i;
3  reg [4:0] Sel;
4  wire [31:0] y;
5  Demux_1x32 uut(i,Sel,y);
6  initial begin
7  for(int k=0; k<15; k=k+1) begin
8  i=1;
9  Sel=$random();
10 #10;
11 $display("i=%d,Sel=%d,y=%d",i,Sel,y);
12 #10;
13 end
14 end
15 initial begin
16 #300;
17 $finish();
18 end
19 endmodule
20
```

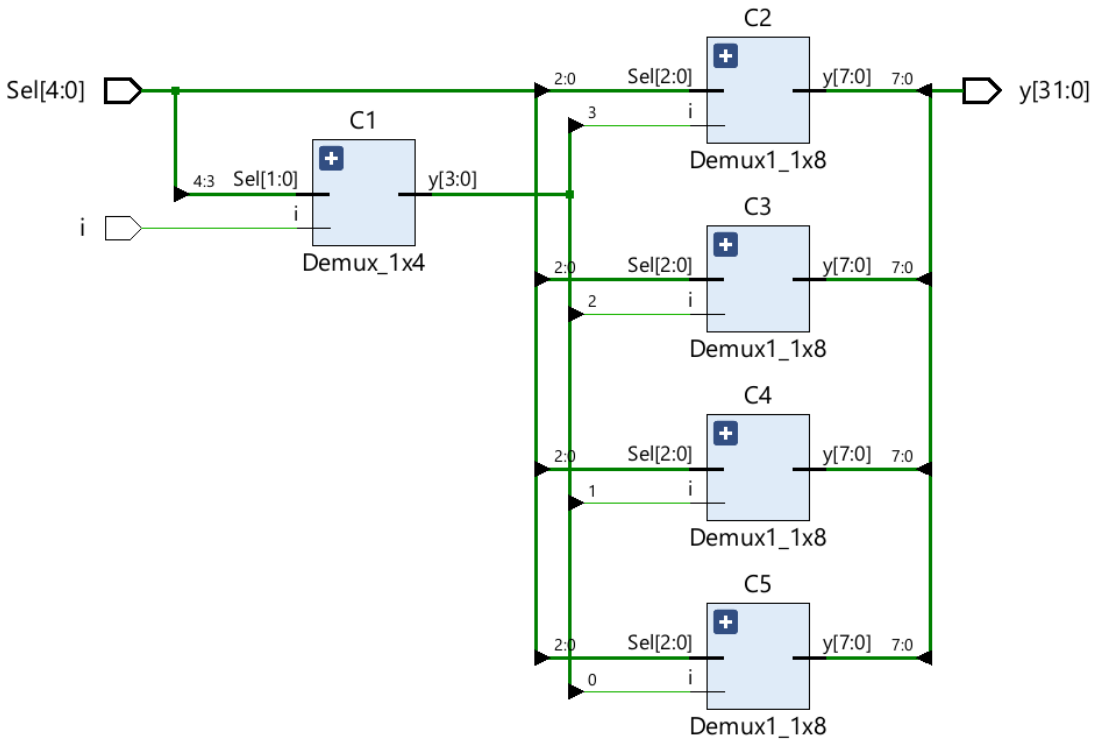
OUTPUT:-

```
i=1,Sel= 4,y=         16
i=1,Sel= 1,y=          2
i=1,Sel= 9,y=        512
i=1,Sel= 3,y=          8
i=1,Sel=13,y=       8192
i=1,Sel=13,y=       8192
i=1,Sel= 5,y=         32
i=1,Sel=18,y=     262144
i=1,Sel= 1,y=          2
i=1,Sel=13,y=       8192
i=1,Sel=22,y=    4194304
i=1,Sel=29,y= 536870912
i=1,Sel=13,y=       8192
i=1,Sel=12,y=       4096
i=1,Sel=25,y=   33554432
```

WAVEFORMS:-



SCHEMATIC:-


C2
Sel[4:0]
2:0
Sel[2:0]
y[7:0]
7:0
y[31:0]
3
i
Demux1_1x8
C1
4:3
Sel[1:0]
y[3:0]
i
i
Demux_1x4
C3
2:0
Sel[2:0]
y[7:0]
7:0
2
i
Demux1_1x8
C4
2:0
Sel[2:0]
y[7:0]
7:0
1
i
Demux1_1x8
C5
2:0
Sel[2:0]
y[7:0]
7:0
0
i
Demux1_1x8

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