DAY-47

#100DAYSOFRTL

Aim:- Implementation of JK Flipflop using Verilog.

RTL CODE:-

```
////DAY-47
////DATE:-16/02/2024
////Implementation of JK-FLIPFLOP
module Day_47(input J,K,rst,clk,
output reg q,qbar);
always@(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case({J,K})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={2'b10};
2'b11:{q,qbar}<={qbar,q};
default: begin end
endcase
end
end
endmodule
```

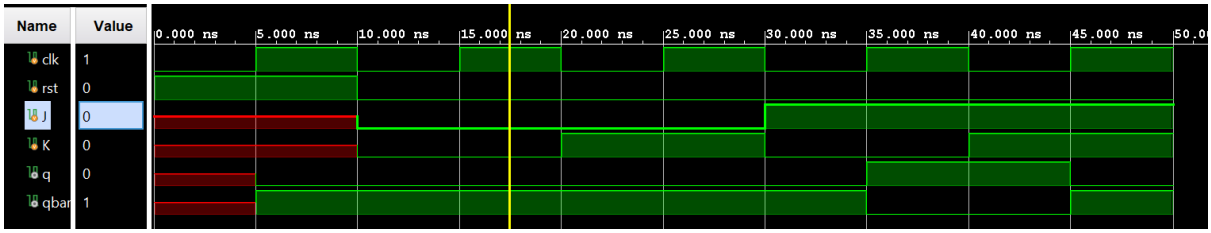
TESTBENCH:-

```
module Day_47_tb();
reg J,K,rst,clk;
wire q,qbar;
Day_47 uut(J,K,rst,clk,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
{J,K}=2'b00; #10;
$display("J=%b,K=%b,q=%b,qbar=%b",J,K,q,qbar);
{J,K}=2'b01; #10;
$display("J=%b,K=%b,q=%b,qbar=%b",J,K,q,qbar);
{J,K}=2'b10; #10;
$display("J=%b,K=%b,q=%b,qbar=%b",J,K,q,qbar);
{J,K}=2'b11; #10;
$display("J=%b,K=%b,q=%b,qbar=%b",J,K,q,qbar);
$finish();
end
endmodule
```

OUTPUT:-

J=0,K=0,q=0,qbar=1
J=0,K=1,q=0,qbar=1
J=1,K=0,q=1,qbar=0
J=1,K=1,q=0,qbar=1

WAVEFORMS:-



SCHEMATIC:-