DAY-56

#100DAYSOFRTL

Aim:- Implementation of Down Counter using Verilog.

RTL CODE:-

```
///DATE:-25/02/2024
///DAY-56
////Implementation of Down Counter
module Day_56(input clk,rst,
output reg [3:0] cnt);
always @(posedge clk) begin
if(rst)
cnt<=4'b1111;
else
cnt<=cnt-1;
end
endmodule
```

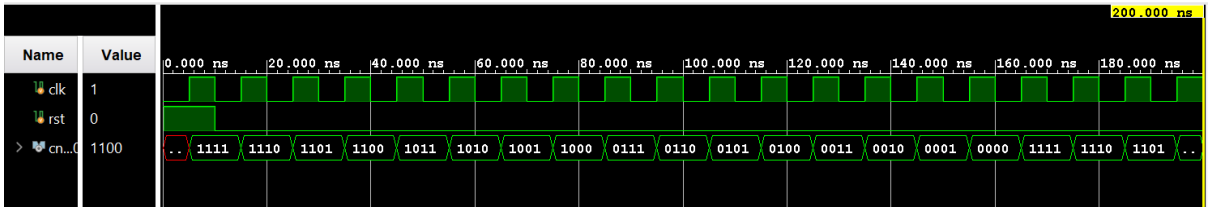
TESTBENCH:-

```
module Day_56_tb();
reg clk,rst;
wire [3:0] cnt;
Day_56 uut(clk,rst,cnt);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
$display("clk=%d,rst=%d,cnt=%d",clk,rst,cnt);
for(integer i=0; i<16; i=i+1) begin
rst=0;
#10;
$display("clk=%d,rst=%d,cnt=%d",clk,rst,cnt);
end
end
initial begin
#200;
$finish();
end
endmodule
```

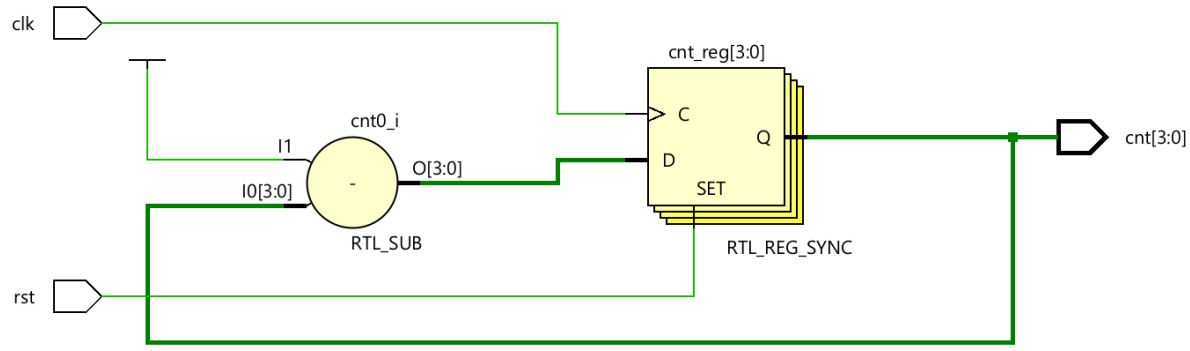
OUTPUT:-

```
clk=1,rst=1,cnt=15
clk=1,rst=0,cnt=14
clk=1,rst=0,cnt=13
clk=1,rst=0,cnt=12
clk=1,rst=0,cnt=11
clk=1,rst=0,cnt=10
clk=1,rst=0,cnt= 9
clk=1,rst=0,cnt= 8
clk=1,rst=0,cnt= 7
clk=1,rst=0,cnt= 6
clk=1,rst=0,cnt= 5
clk=1,rst=0,cnt= 4
clk=1,rst=0,cnt= 3
clk=1,rst=0,cnt= 2
clk=1,rst=0,cnt= 1
clk=1,rst=0,cnt= 0
```

WAVEFORMS:-



SCHEMATIC:-



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