DAY-53

#100DAYSOFRTL

Aim:- Implementation of 2-BIT Cube Generator using Verilog.

RTL CODE:-

```
///DATE:-22/02/2024
////DAY-53
///Implementation of 2-bit Cube generator.
module Day_53(input [1:0] A,
output [4:0] Y);
assign Y[0]=A[0];
assign Y[1]=A[1]&A[0];
assign Y[2]=1'b0;
assign Y[3]=A[1];
assign Y[4]=A[1]&A[0];
endmodule
```

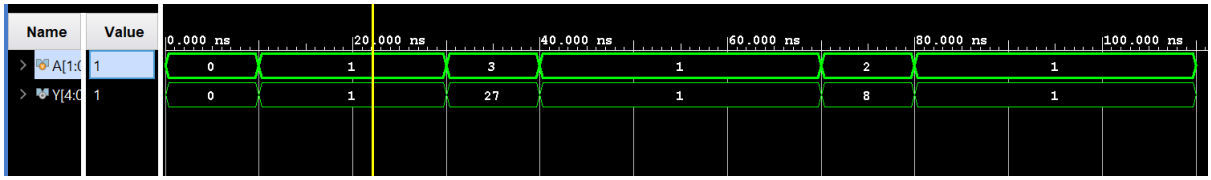
TESTBENCH:-

```
module Day_53_tb();
reg [1:0] A;
wire [4:0] Y;
Day_53 uut(A,Y);
initial begin
for(integer i=0; i<10; i=i+1) begin
A=$random();
#10;
$display("A=%d,Y=%d",A,Y);
//#10;
end
end
initial begin
#110;
$finish();
end
endmodule
```

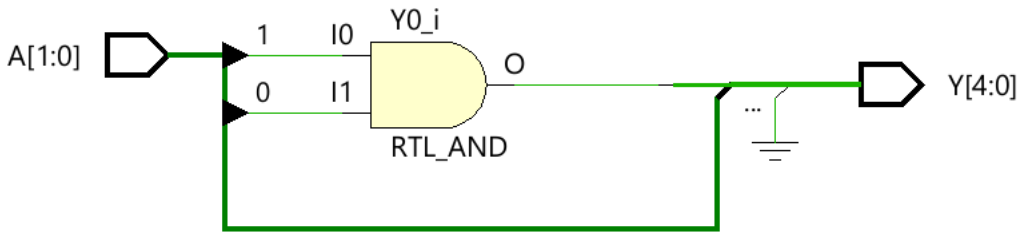
OUTPUT:-

```
A=0,Y= 0
A=1,Y= 1
A=1,Y= 1
A=3,Y=27
A=1,Y= 1
A=1,Y= 1
A=1,Y= 1
A=2,Y= 8
```

WAVEFORMS:-



SCHEMATIC:-



==========