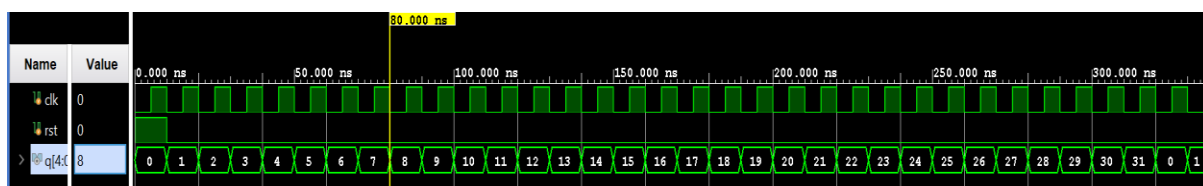# DAY-85

#100DAYSOFRTL

Aim:- Implementation of Asynchronous 5-bit Ripple Up Counter using T FlipFlop.

RTL CODE:-

```verilog
////DATE:-25/03/2024
////DAY-85
////Implementation of Asynchronous 5-bit Ripple Up Counter
module Day_85(input clk,rst, output [4:0] q);
tFF T1(clk,rst,1'b1,q[0]);
tFF T2(q[0],rst,1'b1,q[1]);
tFF T3(q[1],rst,1'b1,q[2]);
tFF T4(q[2],rst,1'b1,q[3]);
tFF T5(q[3],rst,1'b1,q[4]);
endmodule

module tFF(input clk,rst,T, output reg q);
always@(negedge clk) begin
if(rst)
q<=0;
else begin
case(T)
1'b0:q=q;
1'b1:q=~q;
endcase
end
end
endmodule
```
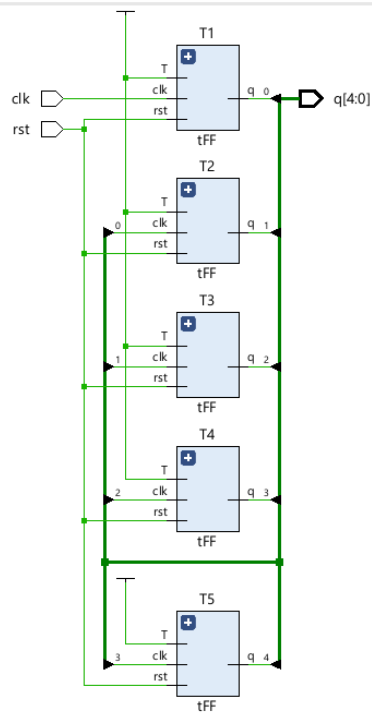
WAVEFORMS:-

TESTBENCH:-

```
module Day_85_tb();
reg clk,rst;
wire [4:0] q;
Day_85 uut(clk,rst,q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
#20;
end
endmodule
```

SCHEMATIC:-