DAY-22

#100DAYSOFRTL

Aim:- Implementation of 8x1 Mux using 2x1 Mux by instantiating in Verilog.

RTL CODE:-

```
////DATE:-22/01/2024
////Implementation of 8X1 MUX using 2X1 MUX
module Mux1_2x1(input [1:0] A,
input Sel, output y);
assign y=Sel?A[1]:A[0];
endmodule

module Day_22(input [7:0] A, input [2:0] Sel,
output y);
wire [5:0] w;
Mux1_2x1 A1(A[1:0],Sel[0],w[0]);
Mux1_2x1 A2(A[3:2],Sel[0],w[1]);
Mux1_2x1 A3(A[5:4],Sel[0],w[2]);
Mux1_2x1 A4(A[7:6],Sel[0],w[3]);
Mux1_2x1 A5(w[1:0],Sel[1],w[4]);
Mux1_2x1 A6(w[3:2],Sel[1],w[5]);
Mux1_2x1 A7(w[5:4],Sel[2],y);
endmodule
```

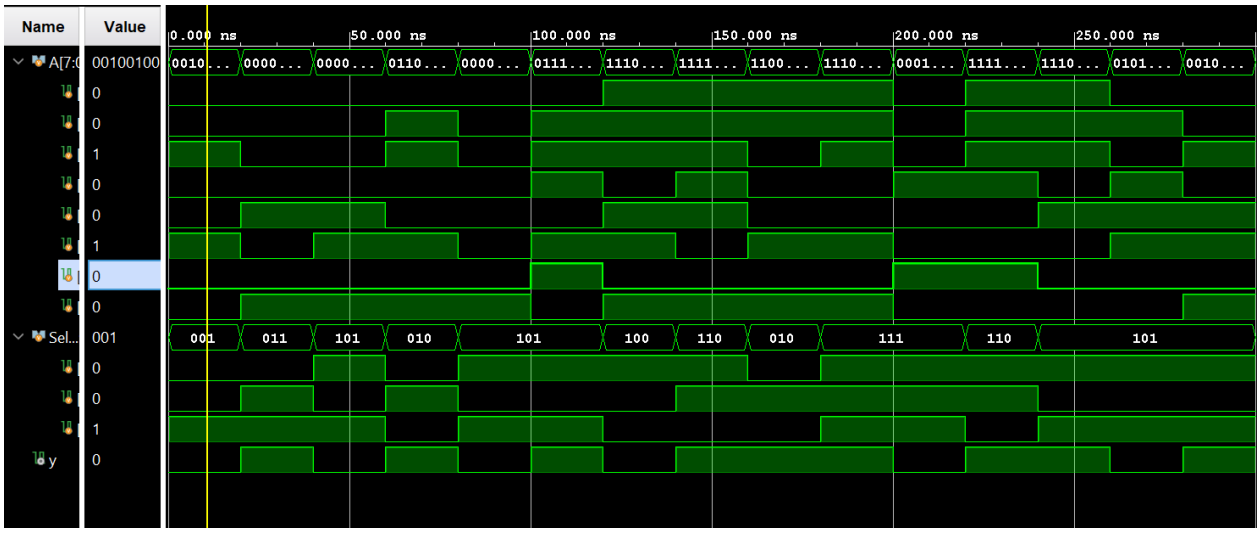
OUTPUT:-

```
A=00100100,Sel=1,y=0
A=00001001,Sel=3,y=1
A=00001101,Sel=5,y=0
A=01100101,Sel=2,y=1
A=00000001,Sel=5,y=0
A=01110110,Sel=5,y=1
A=11101101,Sel=4,y=0
A=11111001,Sel=6,y=1
A=11000101,Sel=2,y=1
A=11100101,Sel=7,y=1
A=00010010,Sel=7,y=0
A=11110010,Sel=6,y=1
A=11101000,Sel=5,y=1
A=01011100,Sel=5,y=0
A=00101101,Sel=5,y=1
```

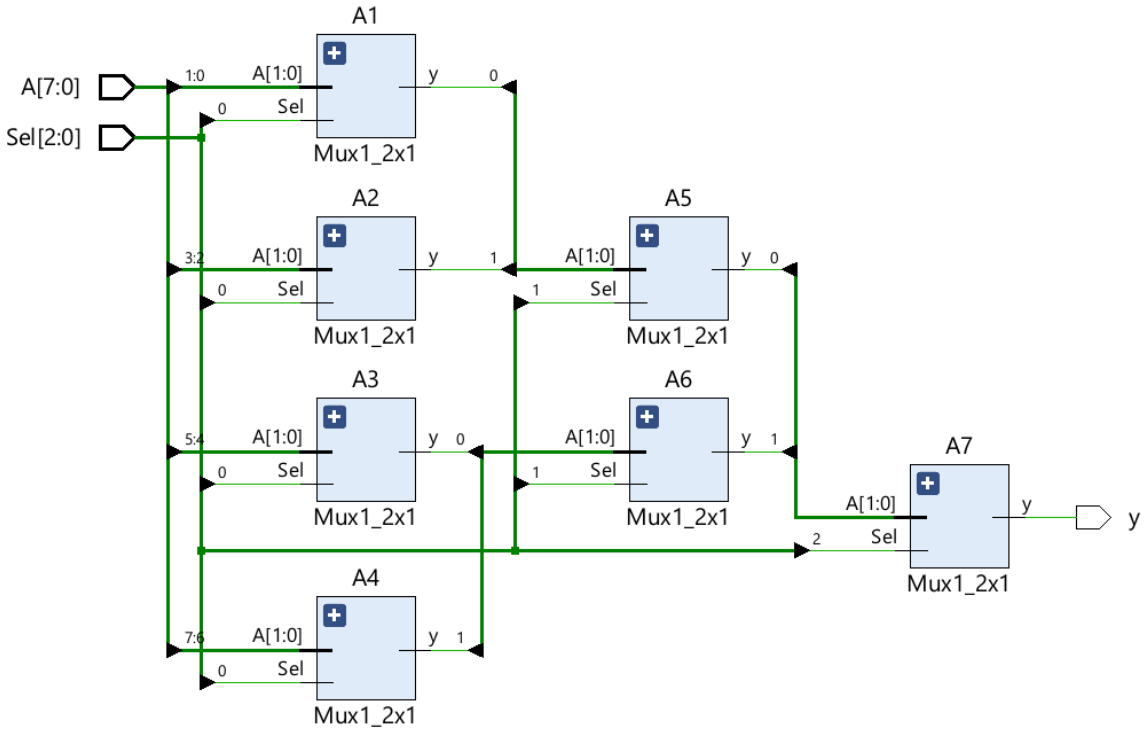
TESTBENCH:-

```
module Day22_tb();
reg  [7:0] A;
reg [2:0] Sel;
wire y;
Day_22 uut(A,Sel,y);
initial begin
for(integer i=0; i<20; i=i+1) begin
A=$random();
Sel=$random();
#10;
$display("A=%b,Sel=%d,y=%d",A,Sel,y);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-


A1
A[7:0]
Sel[2:0]
1:0
A[1:0]
Sel
y
0
Mux1_2x1
A2
3:2
A[1:0]
Sel
y
1
Mux1_2x1
A5
A[1:0]
Sel
y
0
1
Mux1_2x1
A3
5:4
A[1:0]
Sel
y
0
Mux1_2x1
A6
A[1:0]
Sel
y
1
1
Mux1_2x1
A7
A[1:0]
Sel
y
2
Mux1_2x1
y
A4
7:6
A[1:0]
Sel
y
1
Mux1_2x1

==========