DAY-48

#100DAYSOFRTL

Aim:- Implementation of D Flipflop using Verilog.

RTL CODE:-

```
///DAY-48
///DATE:-17/02/2024
////Implementation of D-Flipflop
module Day_48(input D,clk,rst,
output reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case(D)
1'b0:{q,qbar}<={1'b0,1'b1};
1'b1:{q,qbar}<={1'b1,1'b0};
endcase
end
end
endmodule
```

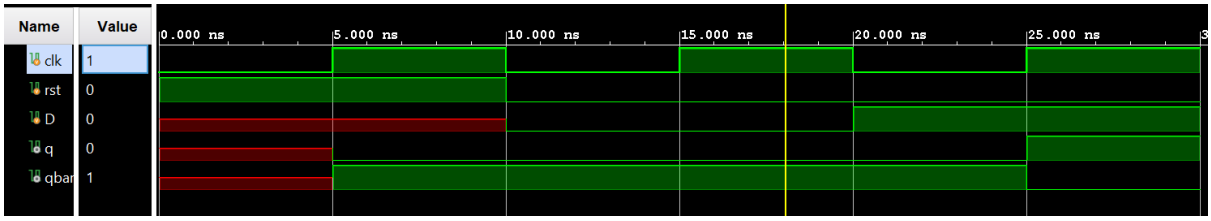
TESTBENCH:-

```
module Day_48_tb();
reg D,clk,rst;
wire q,qbar;
Day_48 uut(D,clk,rst,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
D=0; #10;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
D=1; #10;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
$finish();
end
endmodule
```

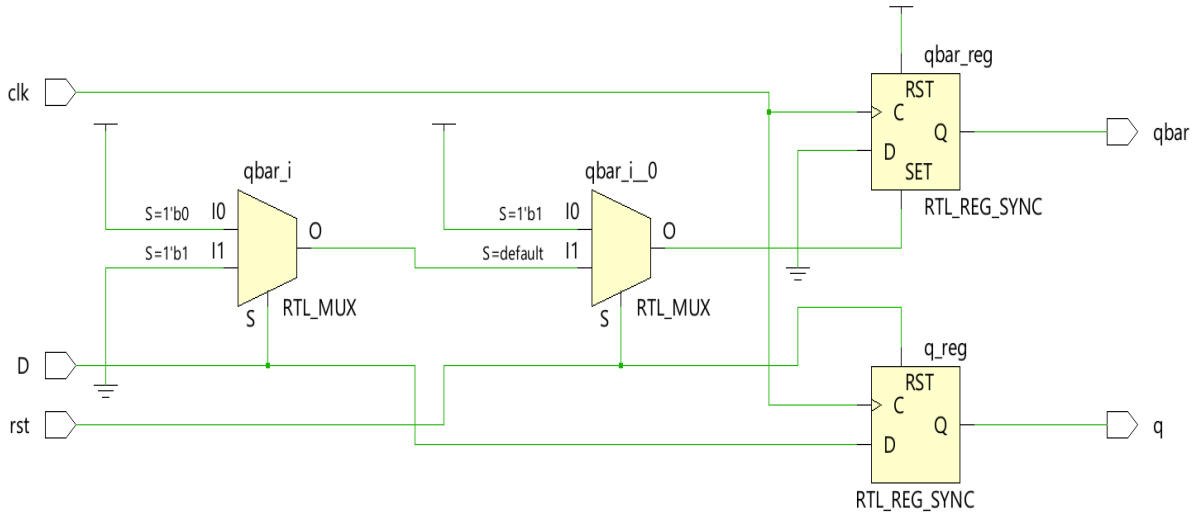
OUTPUT:-

```
D=0,q=0,qbar=1
D=1,q=1,qbar=0
```

WAVEFORMS:-



SCHEMATIC:-



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