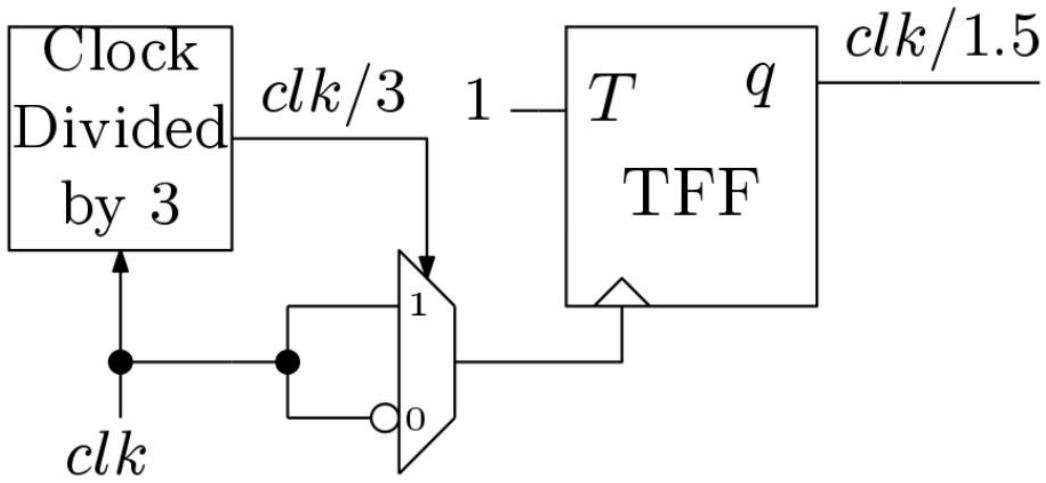
DAY-99

#100DAYSOFRTL

Aim:- Implementation of Frequency Divider by 1.5.



RTL CODE:-

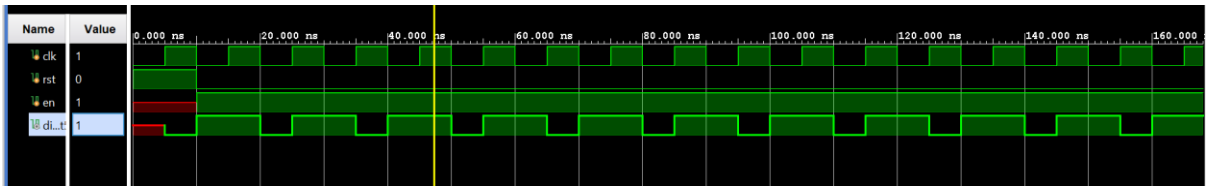
```
////DATE:-08/04/2024
///DAY-99
///Implementation of Frequency Divider by 1.5
module Day_99(input clk,rst,en, output div1point5);
wire div3;
wire w1;
wire w2;
reg [1:0] cnt;
always@(posedge clk) begin
if(rst)
cnt<=2'd0;
else if(en) begin
if(cnt==2'd2)
cnt<=0;
else
cnt<=cnt+1;
end
end
dff dflipflop(clk,rst,cnt[1],w1);
or g1(div3,cnt[1],w1);
Mux_2x1 Mux(clk,(~clk),div3,w2);
TFF T1(w2,rst,1'b1,div1point5);
endmodule
```

```
module dff(input clk,rst, D, output reg q);
always @(negedge clk) begin
if(rst)
q<=0;
else begin
case(D)
1'b0:q<=0;
1'b1:q<=1;
endcase
end
end
endmodule

module Mux_2x1(input A,B,Sel, output y);
assign y=(Sel)?A:B;
endmodule

module TFF(input clk,rst,T, output reg q);
always @(posedge clk) begin
if(rst)
q<=0;
else begin
case(T)
1'b0:q<=q;
1'b1:q<=~q;
endcase
end
end
endmodule
```

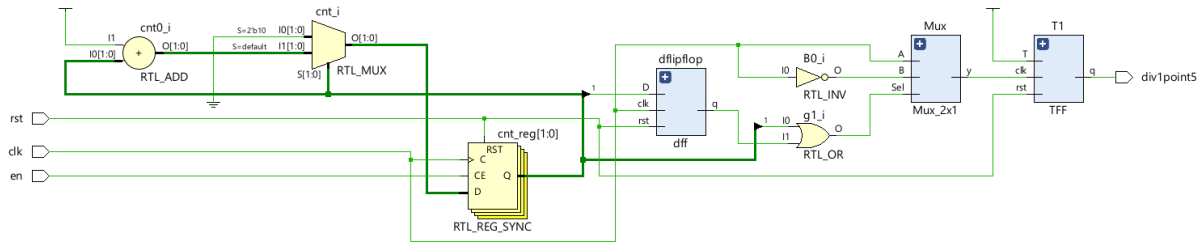
TESTBENCH:-

```
module Day_99_tb();
reg clk,rst,en;
wire div1point5;
Day_99 uut(clk,rst,en,div1point5);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
en=1;
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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