DAY-8

#100DAYSOFRTL

Aim:- Implementation of Full Adder using Half Adders in Gate level Modelling.

RTL CODE:-

```
///DATE:-08/01/2024
////Implementation of FULLADDER using HalfAdder
module HA(input A,B,
output S,C);
wire w1,w2;
xor g1(S,A,B);
and g2(C,A,B);
endmodule

module FAusingHA(input A,B,Cin,
output Sum,Carry);
wire S,C,w3;
HA M1(.A(A),.B(B),.S(S),.C(C));
HA M2(.A(S),.B(Cin),.S(Sum),.C(w3));
or g1(Carry,C,w3);
endmodule
```

TESTBENCH:-

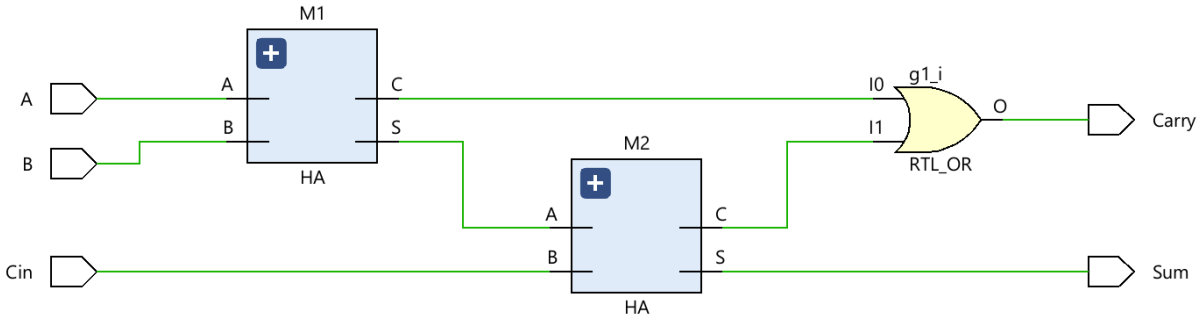
```
module FAusingHA_tb();
reg A,B,Cin;
wire Sum,Carry;
FAusingHA dut(A,B,Cin,
Sum,Carry);
initial begin
A=0;B=0;Cin=0;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=0;B=0;Cin=1;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=0;B=1;Cin=0;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=0;B=1;Cin=1;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=1;B=0;Cin=0;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=1;B=0;Cin=1;
#10;
```

```
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=1;B=1;Cin=0;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
A=1;B=1;Cin=1;
#10;
$display("A=%b,B=%b,C=%b,Sum=%b,Carry=%b",A,B,Cin,Sum,Carry);
$finish();
end
endmodule
```

OUTPUT:-

```
A=0,B=0,C=0,Sum=0,Carry=0
A=0,B=0,C=1,Sum=1,Carry=0
A=0,B=1,C=0,Sum=1,Carry=0
A=0,B=1,C=1,Sum=0,Carry=1
A=1,B=0,C=0,Sum=1,Carry=0
A=1,B=0,C=1,Sum=0,Carry=1
A=1,B=1,C=0,Sum=0,Carry=1
A=1,B=1,C=1,Sum=1,Carry=1
```

SCHEMATIC:-



WAVEFORMS:-