DAY-93

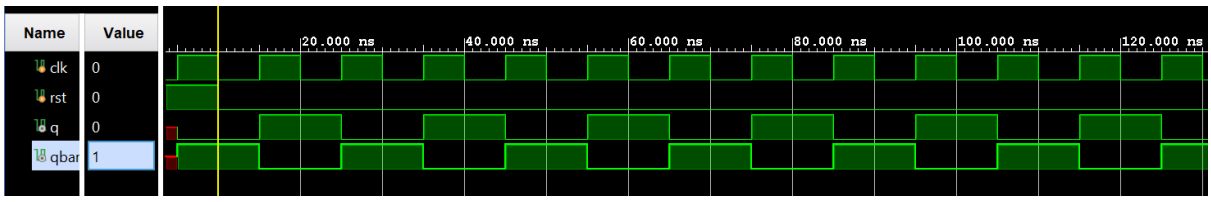
#100DAYSOFRTL

Aim:- Implementation of Clock Divider/Frequency Divider by 2.

RTL CODE:-

```
////DATE:-02/04/2024
////DAY-93
////Implementation of Clock Divider by 2
module Day_93(input clk,rst, output reg q,
output qbar);
always@(posedge clk) begin
if(rst)
q<=0;
else begin
q<=qbar;
end
end
assign qbar=~q;
endmodule
```

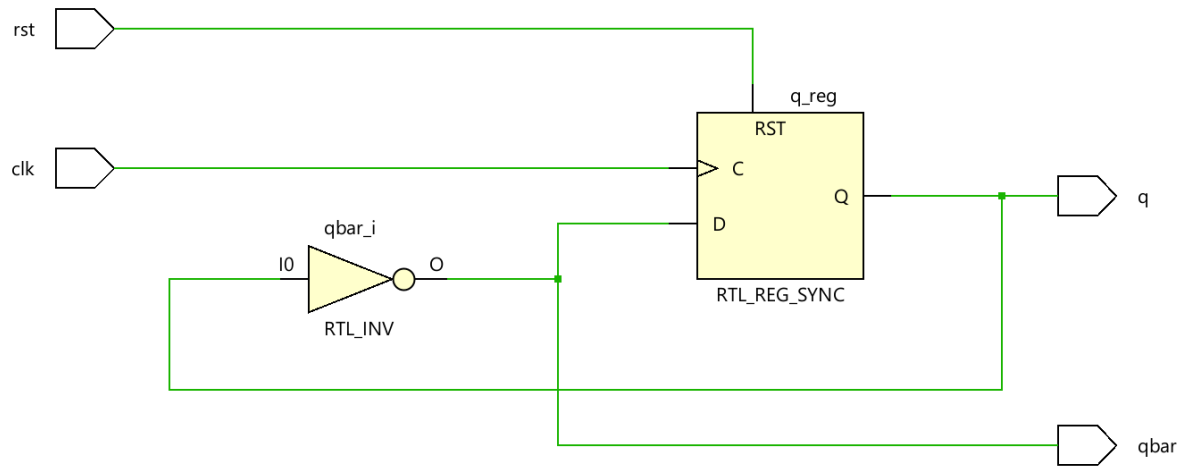
WAVEFORMS:-



TESTBENCH:-

```
module Day_93_tb();
reg clk,rst;
wire q,qbar;
Day_93 uut(clk,rst,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
end
endmodule
```

SCHEMATIC:-



==========