DAY-95

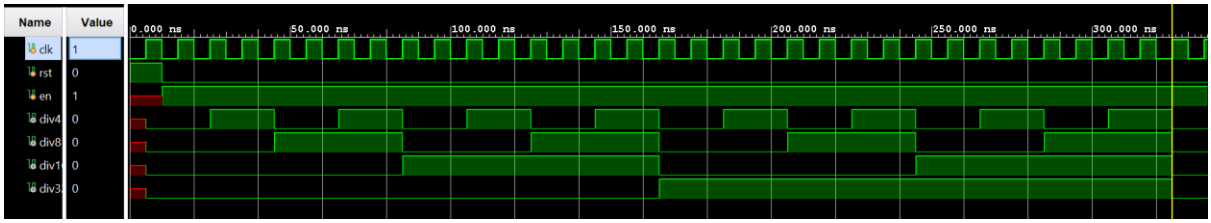
#100DAYSOFRTL

Aim:- Implementation of Implementation of Clock Divider by 2n.

RTL CODE:-

```
///DATE:-04/04/2024
///DAY-95
///Implementation of Clock divider by 2n
module Day_95(input clk,rst,en,
output div4,div8,div16,div32);
reg [4:0] cnt;
always@(posedge clk) begin
if(rst)
cnt<=5'd0;
else if(en) begin
if(cnt==5'd31)
cnt<=0;
else
cnt<=cnt+1;
end
end
assign div4=cnt[1];
assign div8=cnt[2];
assign div16=cnt[3];
assign div32=cnt[4];
endmodule
```

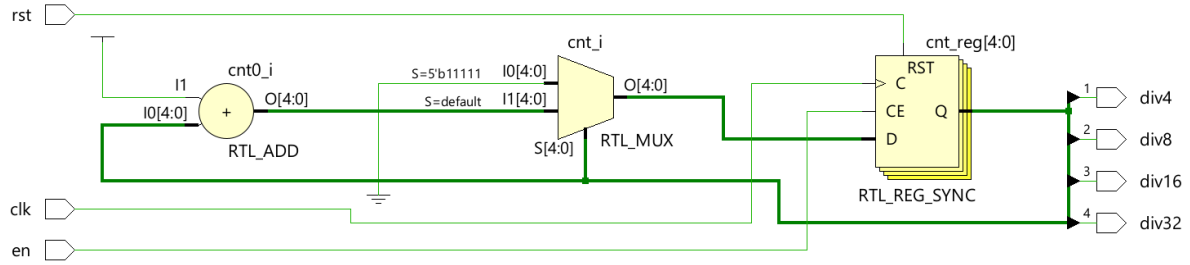
WAVEFORMS:-



TESTBENCH:-

```
module Day_95_tb();
reg clk,rst,en;
wire div4,div8,div16,div32;
Day_95 uut(clk,rst,en,div4,div8,div16,div32);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
en=1;
end
endmodule
```

SCHEMATIC:-



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