DAY-51

#100DAYSOFRTL

Aim:- Implementation of SR-GATED NAND LATCH using Verilog.

RTL CODE:-

```
1  ////DATE:-20/02/2024
2  ///DAY-51
3  ////Implementation of SR Gated NAND Latch
4  module Day_51_Latch(input S,R,EN,
5  output  q,qbar);
6  wire w1,w2;
7  nand g1(w1,S,EN);
8  nand g2(w2,R,EN);
9  nand g3(q,qbar,w1);
10 nand g4(qbar,q,w2);
11 endmodule
12
```

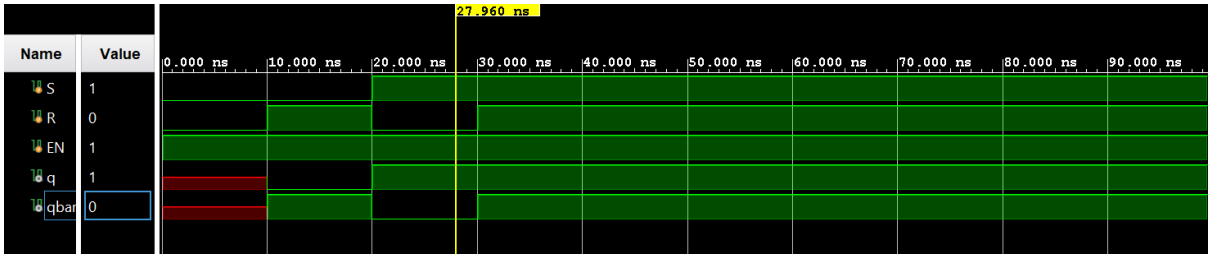
TESTBENCH:-

```
module Day_51_Latch_tb();
reg S,R,EN;
wire q,qbar;///Unit Under Test
Day_51_Latch uut(S,R,EN,q,qbar);
initial begin
EN=1; //#10;
S=0; R=0; #10;
$display("S=%b,R=%b,EN=%b,q=%b,qbar=%b",S,R,EN,q,qbar);
S=0; R=1; #10;
$display("S=%b,R=%b,EN=%b,q=%b,qbar=%b",S,R,EN,q,qbar);
S=1; R=0; #10;
$display("S=%b,R=%b,EN=%b,q=%b,qbar=%b",S,R,EN,q,qbar);
S=1; R=1; #10;
$display("S=%b,R=%b,EN=%b,q=%b,qbar=%b",S,R,EN,q,qbar);
end
initial begin
#100;
$finish();
end
endmodule
```

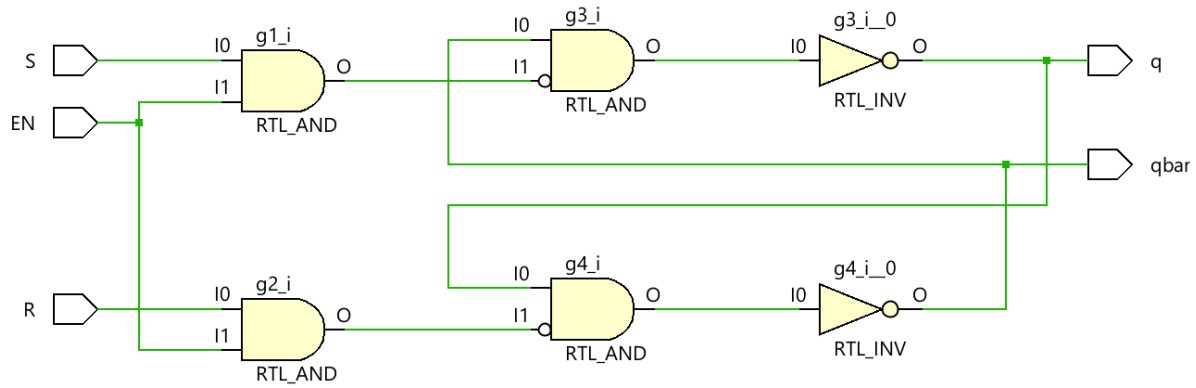
OUTPUT:-

```
S=0,R=0,EN=1,q=x,qbar=x
S=0,R=1,EN=1,q=0,qbar=1
S=1,R=0,EN=1,q=1,qbar=0
S=1,R=1,EN=1,q=1,qbar=1
```

WAVEFORMS:-



SCHEMATIC:-



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