



## DAY-44

### #100DAYSOFRTL

**Aim:-** Finding the Minimum and Maximum of given two numbers using Verilog.

### RTL CODE:-

```
1 //DAY-44
2 //DATE:-13/02/2024
3 //Implementation of MinMax using Verilog
4 module Max_Min(input [3:0] A,B,
5 output reg [3:0] Min,Max );
6 always@(*) begin
7     if(A>B) begin
8         Max=A;
9     end
10    else
11        Max=B;
12    end
13    always@(A or B) begin
14        if(A<B) begin
15            Min=A;
16        end
17        else
18            Min=B;
19        end
20    //assign Max=(A>B)?A:B;
21    //assign Min=(A<B)?A:B;
22 endmodule
23
```

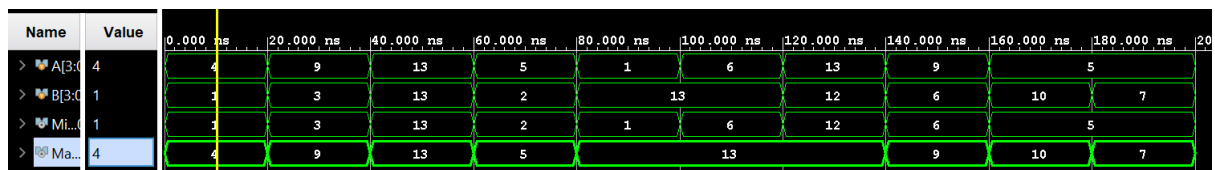
### TESTBENCH:-

```
module Max_Min_tb();
    reg [3:0] A,B;
    wire [3:0] Min,Max;
    Max_Min uut(A,B,Min,Max);
    initial begin
        for(int i=0; i<15; i=i+1) begin
            A=$random();
            B=$random();
            #10;
            $display("A=%d,B=%d,Min=%d,Max=%d",A,B,Min,Max);
            #10;
        end
        initial begin
            #200;
            $finish();
        end
    endmodule
```

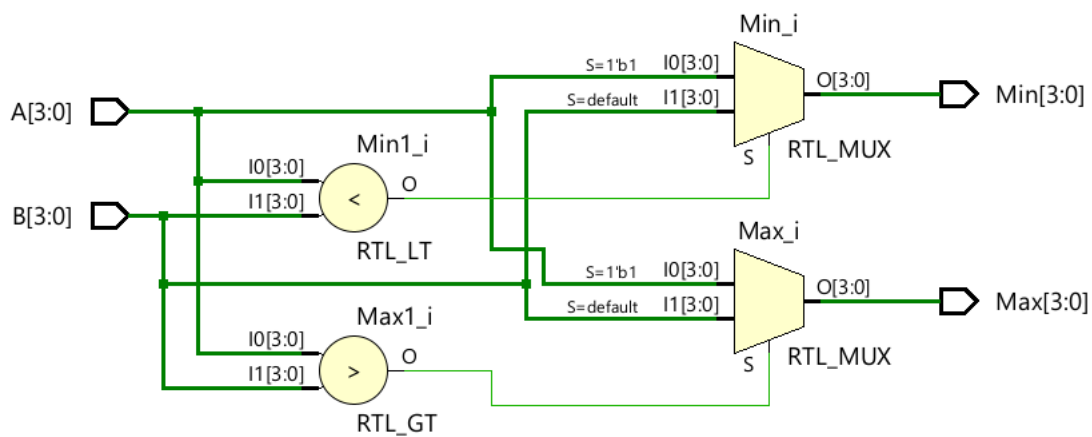
## OUTPUT:-

A= 4,B= 1,Min= 1,Max= 4  
A= 9,B= 3,Min= 3,Max= 9  
A=13,B=13,Min=13,Max=13  
A= 5,B= 2,Min= 2,Max= 5  
A= 1,B=13,Min= 1,Max=13  
A= 6,B=13,Min= 6,Max=13  
A=13,B=12,Min=12,Max=13  
A= 9,B= 6,Min= 6,Max= 9  
A= 5,B=10,Min= 5,Max=10  
A= 5,B= 7,Min= 5,Max= 7

## WAVEFORMS:-



## SCHEMATIC:-



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