DAY-97

#100DAYSOFRTL

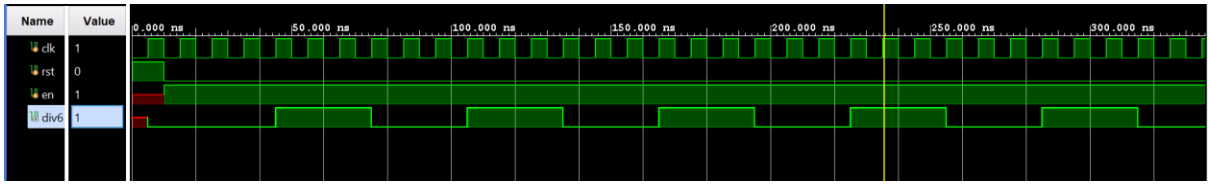
Aim:- Implementation of Clock Divider by 6(F/6).

RTL CODE:-

```
////DATE:-06/04/2024
///DAY-97
///Implementation of Frequency Divider by 5
module Day_97(input clk,rst,en, output div6);
wire w1;
reg [2:0] cnt;
always@(posedge clk) begin
if(rst)
cnt<=3'd0;
else if(en) begin
if(cnt==3'd5)
cnt<=0;
else
cnt<=cnt+1;
end
end
DFf dflipflop(clk,rst,cnt[2],w1);
or g1(div6,w1,cnt[2]);
endmodule

module DFf(input clk,rst, D, output reg q);
always @(posedge clk) begin
if(rst)
q<=0;
else begin
case(D)
1'b0:q<=0;
1'b1:q<=1;
endcase
end
end
endmodule
```

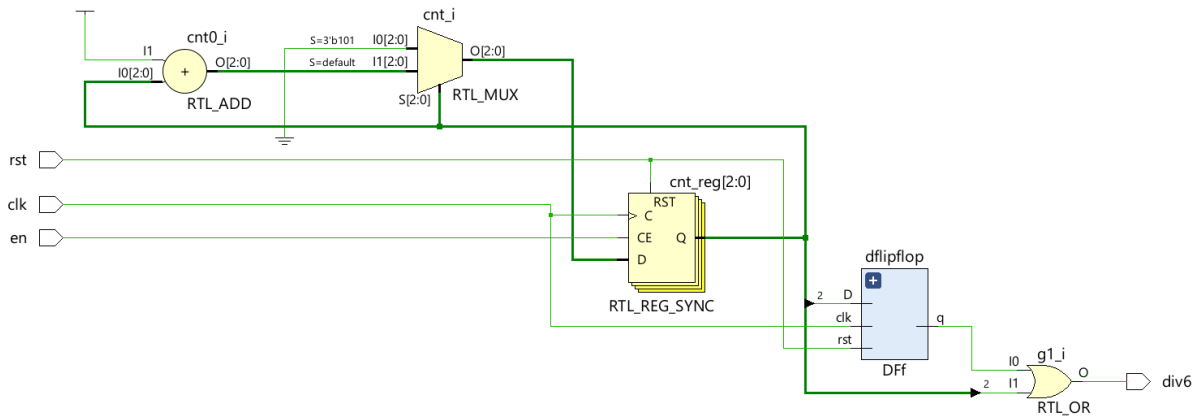
WAVEFORMS:-



TESTBENCH:-

```
module Day_97_tb();
reg clk,rst,en;
wire div6;
Day_97 uut(clk,rst,en,div6);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
en=1;
end
endmodule
```

SCHEMATIC:-



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