DAY-92

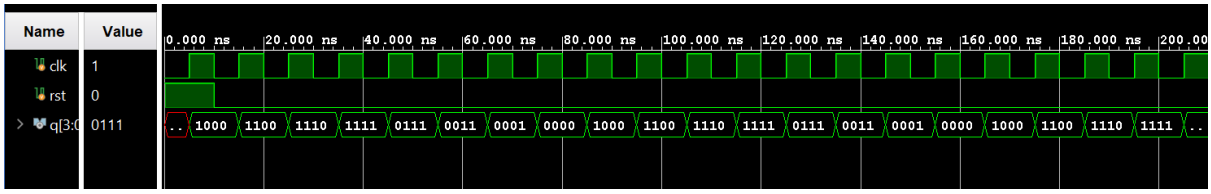
#100DAYSOFRTL

Aim:- Implementation of Johnson Counter/Twisted Ring Counter using Verilog HDL.

RTL CODE:-

```
////DATE:-01/04/2023
////DAY-92
////Implementation of Johnson Counter/Twisted Ring Counter
module Day_92(input clk,rst, output [3:0] q);
reg [3:0] A;
always @(posedge clk) begin
if(rst)
A=4'b1000;
else begin
A={~A[0],A[3:1]};
end
end
assign q=A;
endmodule
```

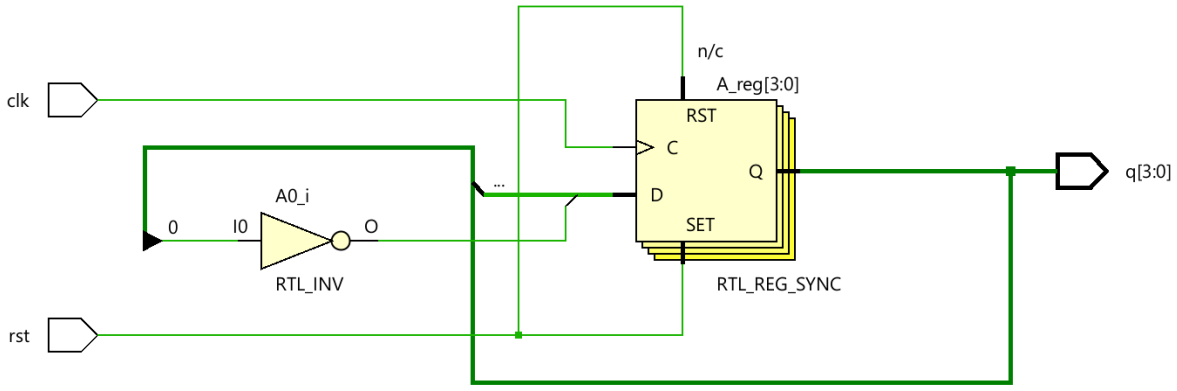
WAVEFORMS:-



TESTBENCH:-

```
module Day_92_tb();
reg clk,rst;
wire [3:0] q;
Day_92 uut(clk,rst,q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
#200;
$finish();
end
endmodule
```

SCHEMATIC:-



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