DAY-54

#100DAYSOFRTL

Aim:- Implementation of Parity Bit Generator using Verilog.

RTL CODE:-

```
////DATE:-23/02/2024
////DAY-54
////Implementation of Parity Bit generator to be added to the data_in
module Day_54(input [7:0] data_in, input En,
output  reg Parity_Bit);
wire w1,w2;
assign w1=^(data_in);
assign w2=~(^(data_in));
always @(*) begin
if(En)
Parity_Bit=~(w2);
else
Parity_Bit=~(w1);
end
endmodule
```

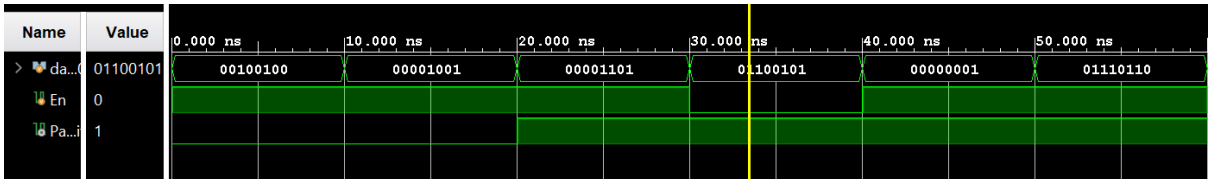
TESTBENCH:-

```
module Day_54_tb();
reg [7:0] data_in;
reg En;
wire Parity_Bit;
Day_54 uut(data_in,En,Parity_Bit);
initial begin
for(integer i=0; i<15; i=i+1) begin
data_in=$random();
En=$random();
#10;
$display("data_in=%b,En=%b,Parity_Bit=%d",data_in,En,Parity_Bit);
end
end
initial begin
#300;
$finish();
end
endmodule
```

OUTPUT:-

```
data_in=00100100,En=1,Parity_Bit=0
data_in=00001001,En=1,Parity_Bit=0
data_in=00001101,En=1,Parity_Bit=1
data_in=01100101,En=0,Parity_Bit=1
data_in=00000001,En=1,Parity_Bit=1
data_in=01110110,En=1,Parity_Bit=1
data_in=11101101,En=0,Parity_Bit=1
data_in=11111001,En=0,Parity_Bit=1
data_in=11000101,En=0,Parity_Bit=1
data_in=11100101,En=1,Parity_Bit=1
data_in=00010010,En=1,Parity_Bit=0
data_in=11110010,En=0,Parity_Bit=0
```

WAVEFORMS:-



SCHEMATIC:-