DAY-69

#100DAYSOFRTL

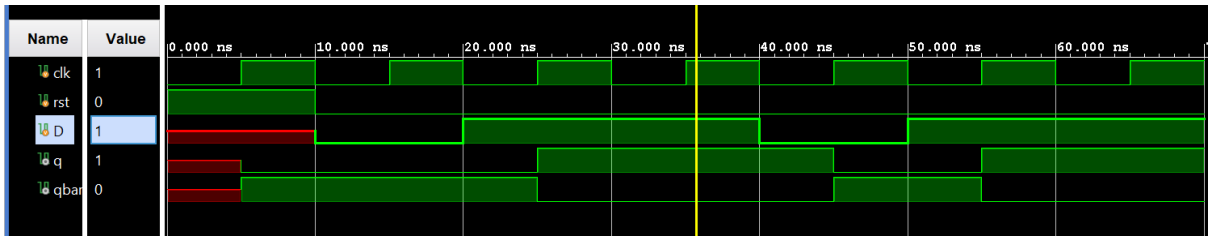
Aim:- Implementation of T F/F TO D F/F using Verilog.

RTL CODE:-

```
///DATE:-09/03/2024
////DAY-69
////Implementation of T f/f to D f/f
module Day_69(input clk,rst,D,
output q,qbar);
wire w1;
xor g1(w1,D,q);
Tff tflipflop(clk,rst,w1,q,qbar);
endmodule


module Tff(input clk,rst,T,
output reg q, output qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(T)
1'b0:{q}={q};
1'b1:{q}={~q};
endcase
end
end
assign qbar=~q;
endmodule
```

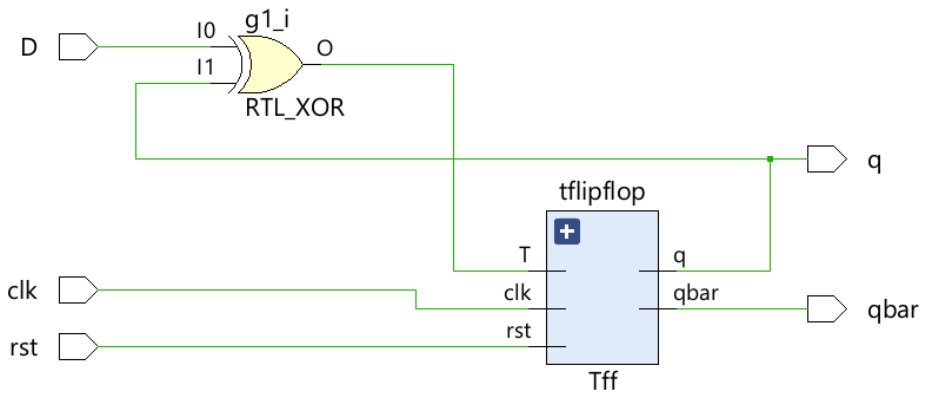
WAVEFORMS:-



TESTBENCH:-

```
module Day_69_tb();
reg clk,rst,D;
wire q,qbar;
Day_69 uut(clk,rst,D,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
D=0; #10;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
D=1; #20;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
D=0; #10;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
D=1; #20;
$display("D=%b,q=%b,qbar=%b",D,q,qbar);
$finish();
end
endmodule
```

SCHEMATIC:-



OUTPUT:-

```
D=0,q=0,qbar=1
D=1,q=1,qbar=0
D=0,q=0,qbar=1
D=1,q=1,qbar=0
```

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