DAY-34

#100DAYSOFRTL

Aim:- Implementation of 2x4 Decoder using Verilog.

RTL CODE:-

```
////DATE:-03/02/2024
///Implementation of 2x4 Decoder.
module Decoder_2x4(input [1:0] A,
  output [3:0] Y);
wire w1,w2,w3,w4;
and g1(Y[0],(~A[1]),(~A[0]));
and g2(Y[1],(~A[1]),(A[0]));
and g3(Y[2],(A[1]),(~A[0]));
and g4(Y[3],(A[1]),(A[0]));
endmodule

```

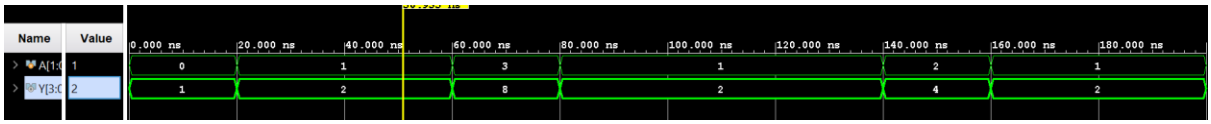
TESTBENCH:-

```
module Decoder_tb();
reg [1:0] A;
//reg E;
wire [3:0] Y;
Decoder_2x4 uut(A,Y);
initial begin
for(int i=0; i<10; i=i+1) begin
A=$random();
#10;
$display("A=%d,Y=%d",A,Y);
#10;
end
end
initial begin
#200;
$finish();
end
endmodule
```

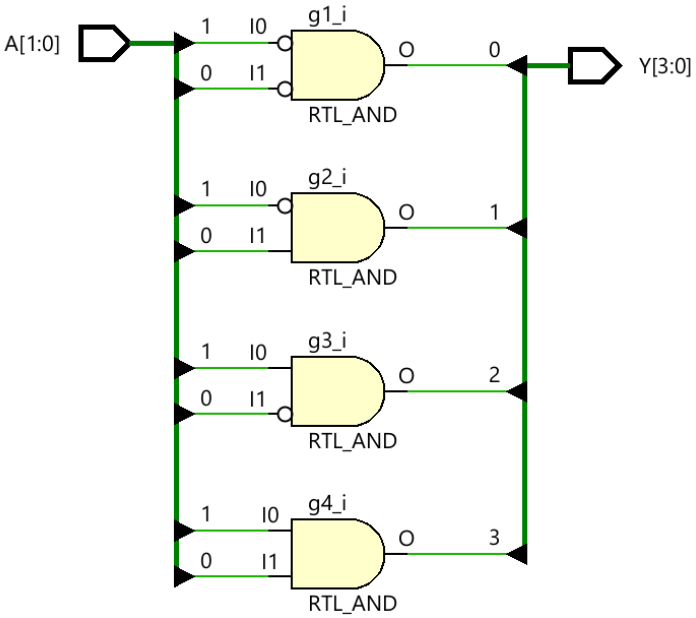
OUTPUT:-

```
A=0,Y= 1
A=1,Y= 2
A=1,Y= 2
A=3,Y= 8
A=1,Y= 2
A=1,Y= 2
A=1,Y= 2
A=2,Y= 4
A=1,Y= 2
A=1,Y= 2
```

WAVEFORMS:-



SCHEMATIC:-



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