DAY-4

#100DAYSOFRTL

Aim:- Implementation of 5-input majority circuit using Verilog.

TRUTH TABLE:-

	A	B	C	D	E	0	1
0	0	0	0	0	0	◉	○
1	0	0	0	0	1	◉	○
2	0	0	0	1	0	◉	○
3	0	0	0	1	1	◉	○
4	0	0	1	0	0	◉	○
5	0	0	1	0	1	◉	○
6	0	0	1	1	0	◉	○
7	0	0	1	1	1	○	◉
8	0	1	0	0	0	◉	○
9	0	1	0	0	1	◉	○
10	0	1	0	1	0	◉	○
11	0	1	0	1	1	○	◉
12	0	1	1	0	0	◉	○
13	0	1	1	0	1	○	◉
14	0	1	1	1	0	○	◉
15	0	1	1	1	1	○	◉
16	1	0	0	0	0	◉	○
17	1	0	0	0	1	◉	○
18	1	0	0	1	0	◉	○
19	1	0	0	1	1	○	◉
20	1	0	1	0	0	◉	○
21	1	0	1	0	1	○	◉
22	1	0	1	1	0	○	◉
23	1	0	1	1	1	○	◉
24	1	1	0	0	0	◉	○
25	1	1	0	0	1	○	◉
26	1	1	0	1	0	○	◉
27	1	1	0	1	1	○	◉
28	1	1	1	0	0	○	◉
29	1	1	1	0	1	○	◉
30	1	1	1	1	0	○	◉
31	1	1	1	1	1	○	◉

OUTPUT:-

Z=Min terms of(7,11,13,14,15,19,21,22,23,25,26, 27,28,29,30,31);

RTL CODE:-

```
////DATE:-04/01/2024
////5-InputMajorityCircuit
module Fiveinput_MajorityCircuit( input A,B,C,D,E,
output Z);
wire [9:0] W;
and g1(W[0],A,C,D);
and g2(W[1],B,D,E);
and g3(W[2],A,B,E);
and g4(W[3],A,B,C);
and g5(W[4],A,D,E);
and g6(W[5],A,C,E);
and g7(W[6],B,C,D);
and g8(W[7],B,C,E);
and g9(W[8],C,D,E);
and g10(W[9],B,D,E);
assign Z=W[0]|W[1]|W[2]|W[3]|W[4]|W[5]|W[6]|W[7]|W[8]|W[9];
endmodule
```

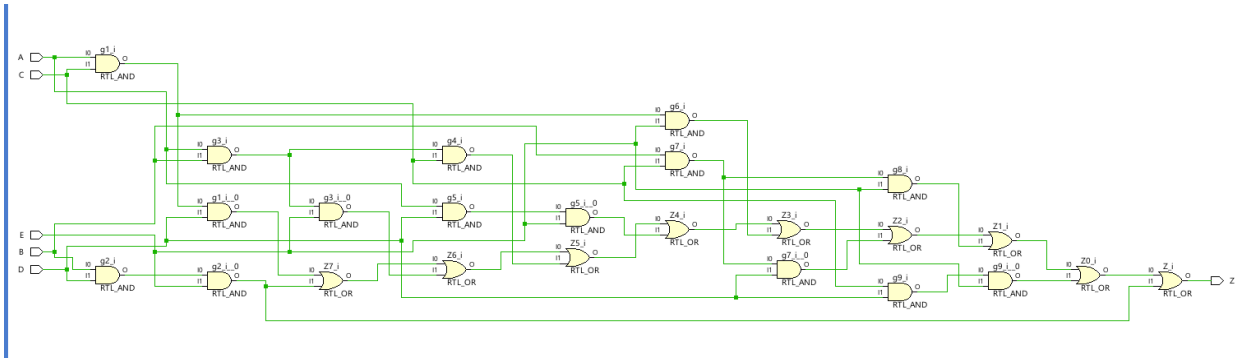
TESTBENCH:-

```
///DATE:-04/01/2024
////5-InputMajorityCircuit
module Fiveinput_MajorityCircuit_tb();
reg A,B,C,D,E;
wire Z;
Fiveinput_MajorityCircuit dut( A,B,C,D,E,
 Z);
initial begin
A=0;B=0;C=0;D=0;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=0;C=1;D=1;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=1;C=1;D=1;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=0;B=0;C=1;D=1;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=1;C=1;D=1;E=1;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=0;C=1;D=1;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=0;C=0;D=1;E=0;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=1;B=0;C=1;D=1;E=1;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
A=0;B=0;C=0;D=0;E=1;
#10;
$display("A=%b,B=%b,C=%b,D=%b,E=%b,Z=%b",A,B,C,D,E,Z);
end
initial begin
#100;
$finish();
end
endmodule
```

OUTPUT:-

```
A=0,B=0,C=0,D=0,E=0,Z=0
A=1,B=0,C=1,D=1,E=0,Z=1
A=1,B=1,C=1,D=1,E=0,Z=1
A=0,B=0,C=1,D=1,E=0,Z=0
A=1,B=1,C=1,D=1,E=1,Z=1
A=1,B=0,C=1,D=1,E=0,Z=1
A=1,B=0,C=0,D=1,E=0,Z=0
A=1,B=0,C=1,D=1,E=1,Z=1
A=0,B=0,C=0,D=0,E=1,Z=0
```

SCHEMATIC:-



WAVEFORMS:-