DAY-67

#100DAYSOFRTL

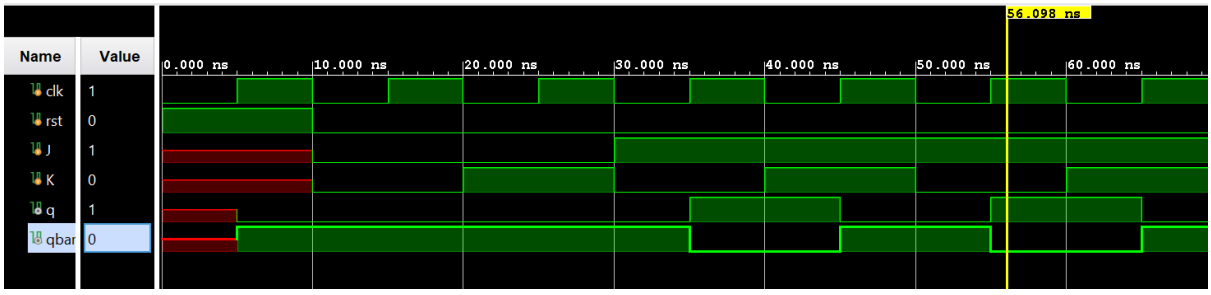
Aim:- Implementation of SR F/F TO JK F/F using Verilog.

RTL CODE:-

```
///DATE:-07/03/2024
////DAY-67
////IMPLEMENTATION OF SR F/F TO JK F/F
module Day_67(input clk,rst,J,K,
output  q,
output qbar);
wire w1,w2;
and g1(w1,J,qbar);
and g2(w2,K,q);
SRff Dut(.clk(clk),.rst(rst),.S(w1),.R(w2),.q(q),.qbar(qbar));
endmodule

module SRff(input clk,rst,S,R,
output reg q,
output qbar);
always@(posedge clk) begin
if(rst) q<=0;
else begin
case({S,R})
2'b00:q<=q; ////No change
2'b01:q<=0; ////reset
2'b10:q<=1; ////set
2'b11:q<=1'bx; ///Invalid inputs
endcase
end
end
assign qbar=~q;
endmodule
```

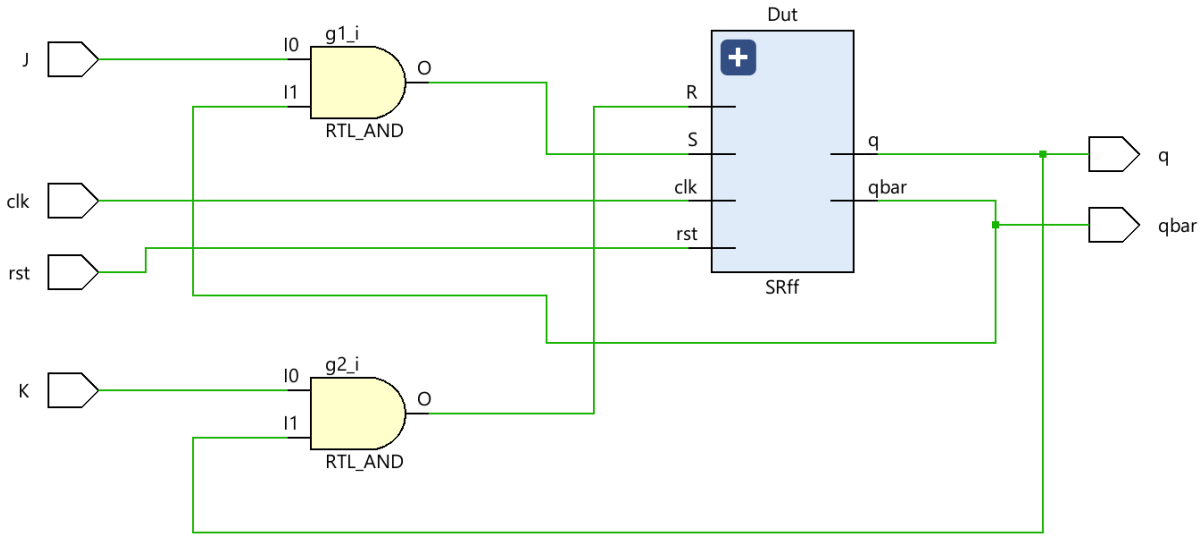
WAVEFORMS:-



TESTBENCH:-

```
module Day_67_tb();
reg clk,rst,J,K;
wire q,qbar;
Day_67 uut(clk,rst,J,K,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
J=0; K=0; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
J=0; K=1; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
J=1; K=0; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
J=1; K=1; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
J=1; K=0; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
J=1; K=1; #10;
$display("J=%d,K=%d,q=%d,qbar=%d",J,K,q,qbar);
$finish();
end
endmodule
```

SCHEMATIC:-



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