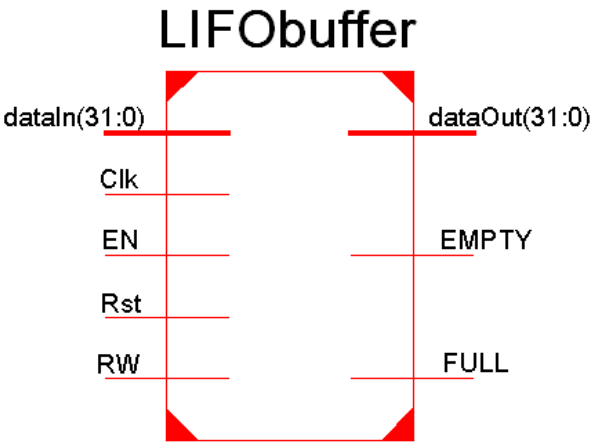
DAY-98

#100DAYSOFRTL

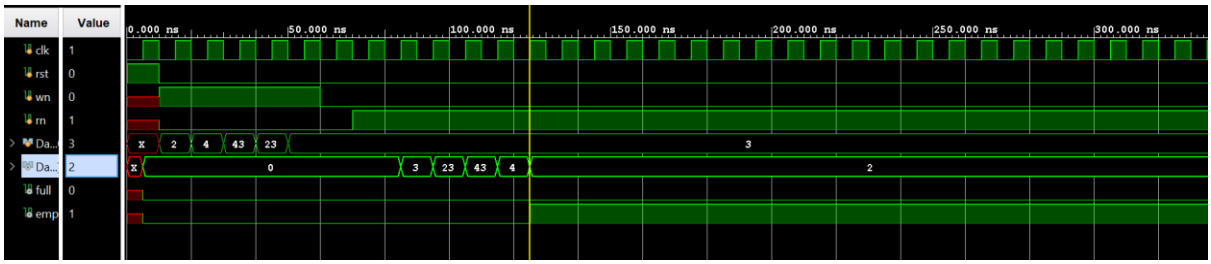
Aim:- Implementation of LIFO (LAST-IN FIRST OUT).



RTL CODE:-

```
////DATE:-07/04/2024
///DAY-98
////Implementation of LIFO using Verilog
module Day_98(input clk,rst,wn,rn, input [7:0] Data_in,
output  reg [7:0] Data_out, output full,empty);
reg [2:0] ptr;  ////One pointer for incrementing and  decrementing
reg [7:0] mem [7:0];
assign full=(ptr==3'b111)?1:0;
assign empty=(ptr==3'b000)?1:0;
always@(posedge clk) begin
if(rst) begin
{mem[0],mem[1],mem[2],mem[3],mem[4],mem[5],mem[6],mem[7]}<=0;
Data_out<=0;
ptr<=1;
end
else if(wn&!full) begin
mem[ptr]<=Data_in;
ptr<=ptr+1;
end
else if(rn&!empty)
begin
ptr<=ptr-1;
Data_out<=mem[ptr];
end
end
endmodule
```

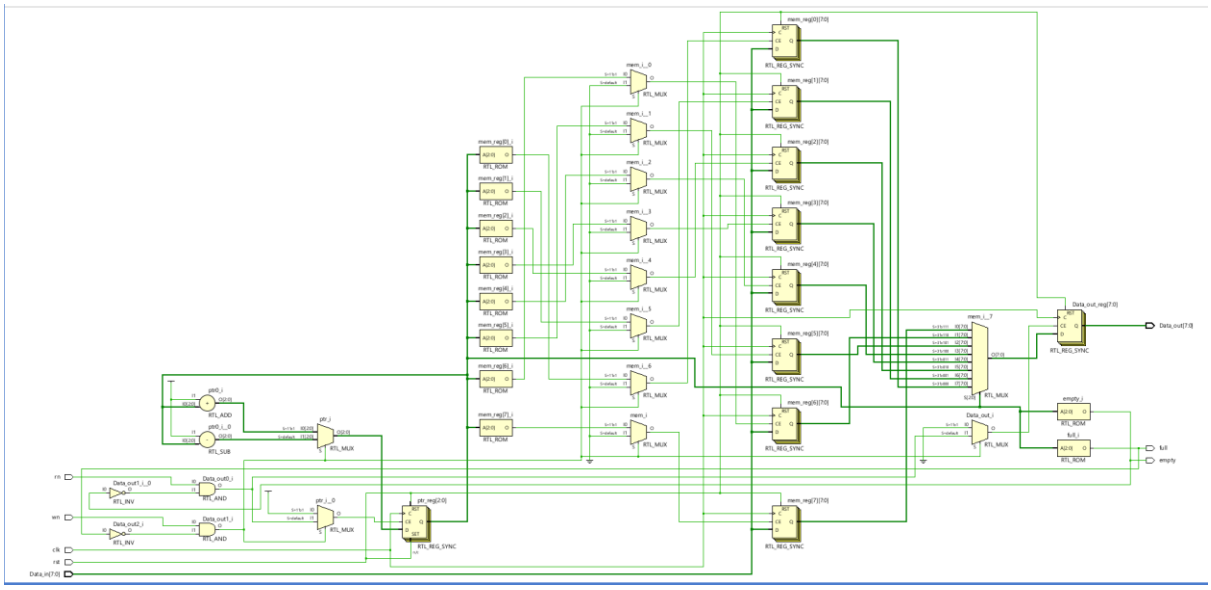
WAVEFORMS:-



TESTBENCH:-

```
module Day_98_tb();
reg clk,rst,wn,rn;
reg [7:0] Data_in;
wire [7:0] Data_out;
wire full,empty;
Day_98 uut(clk,rst,wn,rn,Data_in,Data_out,full,empty);
initial clk=0;
always #5 clk=~clk;
initial begin
rst=1; #10;
rst=0;
wn=1;rn=0;
Data_in=8'd2;
#10;
Data_in=8'd4;
#10;
Data_in=8'd43;
#10;
Data_in=8'd23;
#10;
Data_in=8'd3;
#10;
wn=0; #10; rn=1;
end
endmodule
```

SCHEMATIC:-



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