DAY-78

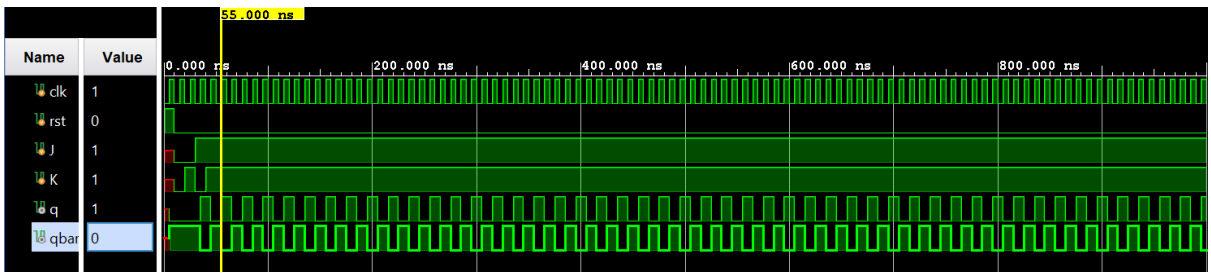
#100DAYSOFRTL

Aim:- Implementation of D FLIPFLOP TO JK FLIPFLOP.

RTL CODE:-

```
1   ////DATE:-18/03/2024
2   ///DAY-78
3   ///Implementation of D FF TO JK FF
4   module Day_78(input clk,rst,J,K,output
5   q,qbar);
6   wire w1,w2,w3;
7   and g1(w1,J,qbar);
8   and g2(w2,(~K),q);
9   or g3(w3,w1,w2);
10  Dff DFF(w3,clk,rst,q,qbar);
11  endmodule
12
13  module Dff(input D,clk,rst,
14  output reg q,qbar);
15  always @(posedge clk) begin
16  if(rst) begin
17  q<=0;
18  qbar<=1;
19  end
20  else begin
21  case(D)
22  1'b0:{q,qbar}<={1'b0,1'b1};
23  1'b1:{q,qbar}<={1'b1,1'b0};
24  endcase
25  end
26  end
27  endmodule
```

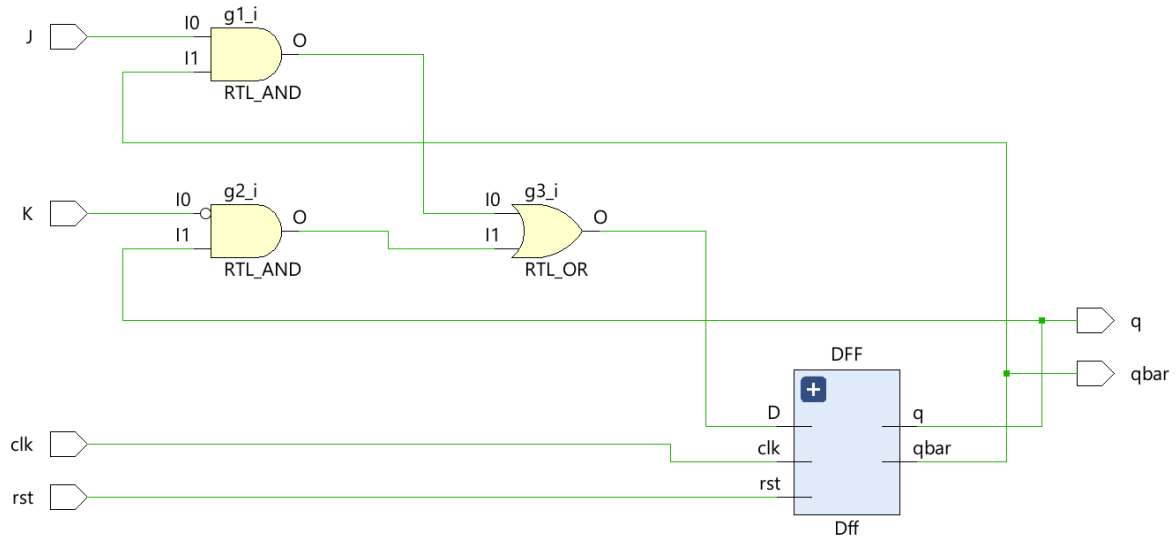
WAVEFORMS:-



TESTBENCH:-

```
module Day_78_tb();
reg clk,rst,J,K;
wire q,qbar;
Day_78 uut(clk,rst,J,K,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
J=0; K=0; #10;
J=0; K=1; #10;
J=1; K=0; #10;
J=1; K=1; #10;
end
endmodule
```

SCHEMATIC:-



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