DAY-64

#100DAYSOFRTL

Aim:- Implementation of Fixed Priority Arbiter using Verilog.

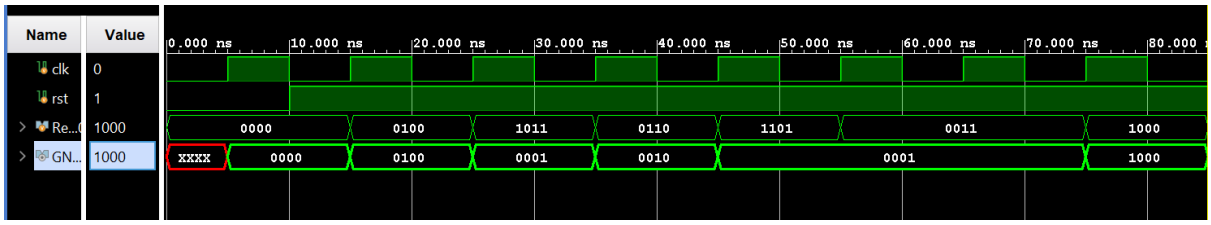
RTL CODE:-

```
////DATE:-04/03/2024
/////DAY-64
/////Implementation of Fixed Proirity Arbiter
module Day_64(input clk,rst,
input [3:0] Req, output  reg [3:0] GNT);
always@(posedge clk) begin
if(!rst)
GNT<=4'b0000;
else if(Req[0])
GNT<=4'b0001;
else if(Req[1])
GNT<=4'b0010;
else if(Req[2])
GNT<=4'b0100;
else if(Req[3])
GNT<=4'b1000;
else
GNT<=4'b0000;
end
endmodule
```

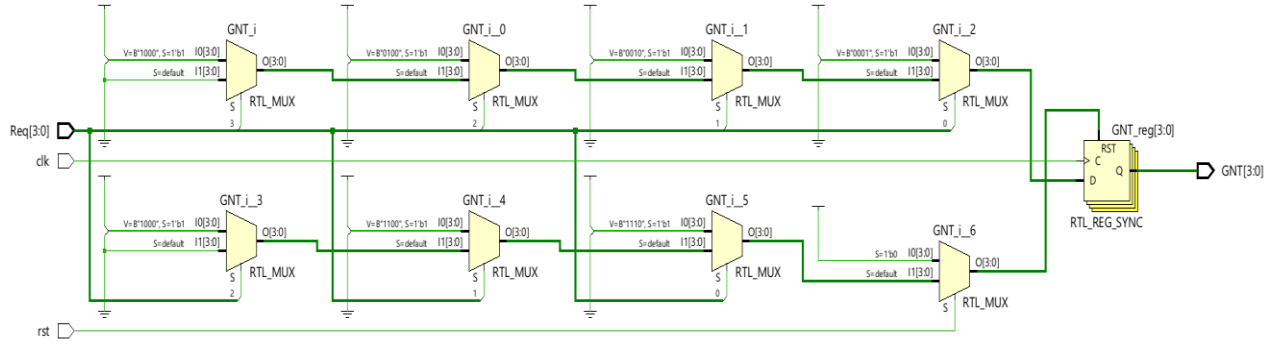
TESTBENCH:-

```
module Day_64_tb();
reg clk,rst;
reg [3:0] Req;
wire [3:0] GNT;
Day_64 uut(clk,rst,Req,GNT);
always #5 clk=~clk;
initial clk=0;
initial begin
clk=0;
rst=0;
Req=4'b0;
#10;
rst=1;
@(posedge clk) Req=4'b0100;
@(posedge clk) Req=4'b1011;
@(posedge clk) Req=4'b0110;
@(posedge clk) Req=4'b1101;
@(posedge clk) Req=4'b0011;
@(posedge clk) Req=4'b0011;
@(posedge clk) Req=4'b1000;
#10;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



==========