DAY-6

#100DAYSOFRTL

Aim:- Implementation of Half Adder using Gate level Modelling.

RTL CODE:-

```
////06/01/2024
////HalfAdder Implementation in Gate level modelling
module HalfAdder(input A,B,
output Sum,Carry);
wire w1,w2;
///GATE LEVEL MODELLING
and g1(Carry,A,B);
and g2(w1,(~A),B);
and g3(w2,A,(~B));
or g4(Sum,w1,w2);
endmodule
```

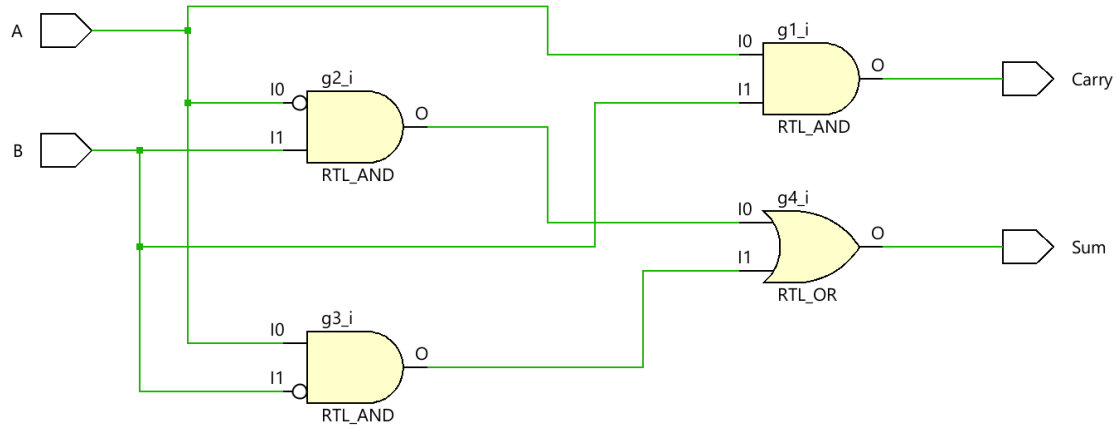
TESTBENCH:-

```
module HalfAdder_tb();
reg A,B;
wire Sum,Carry;
HalfAdder dut( A,B,
Sum,Carry);
initial begin
A=0;
B=0;
#10;
$display("A=%b,B=%b,Sum=%b,Carry=%b",A,B,Sum,Carry);
A=0;
B=1;
#10;
$display("A=%b,B=%b,Sum=%b,Carry=%b",A,B,Sum,Carry);
A=1;
B=0;
#10;
$display("A=%b,B=%b,Sum=%b,Carry=%b",A,B,Sum,Carry);
A=1;
B=1;
#10;
$display("A=%b,B=%b,Sum=%b,Carry=%b",A,B,Sum,Carry);
end
initial begin
#50;
$finish();
end
endmodule
```

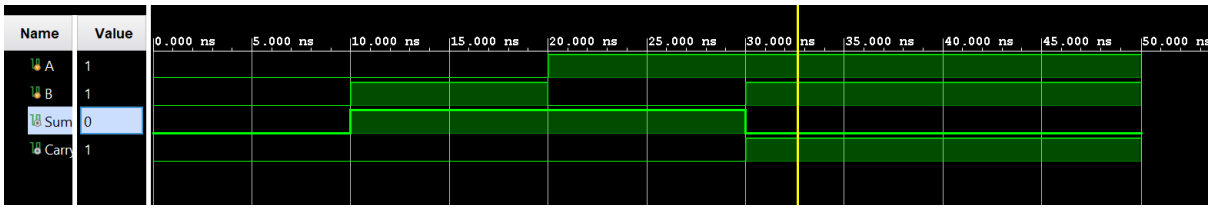
OUTPUT:-

```
A=0,B=0,Sum=0,Carry=0
A=0,B=1,Sum=1,Carry=0
A=1,B=0,Sum=1,Carry=0
A=1,B=1,Sum=0,Carry=1
```

SCHEMATIC:-



WAVEFORMS:-



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