DAY-42

#100DAYSOFRTL

Aim:- Implementation of Gray to Binary Conversion using Verilog.

RTL CODE:-

```
///DAY-42
////Date:-11/02/2024
////Implemenatation of Gray code to Binary Code
module GtoB(input [4:0] G,
output [4:0] B);
assign B[4]=G[4];
assign B[3]=G[4]^G[3];
assign B[2]=G[4]^G[3]^G[2];
assign B[1]=G[4]^G[3]^G[2]^G[1];
assign B[0]=G[4]^G[3]^G[2]^G[1]^G[0];
endmodule
```

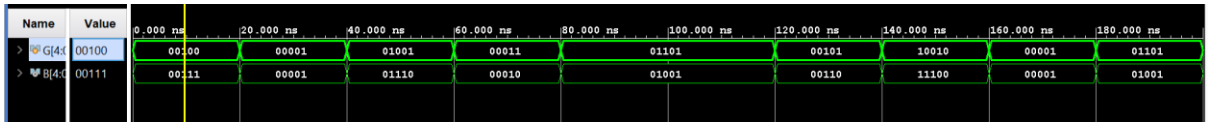
TESTBENCH:-

```
module GtoB_tb();
reg [4:0] G;
wire [4:0] B;
GtoB uut(G,B);
initial begin
for(int i=0; i<10; i=i+1) begin
G=$random();
#10;
$display("G=%b,B=%b",G,B);
#10;
end
end
initial begin
#200;
$finish();
end
endmodule
```

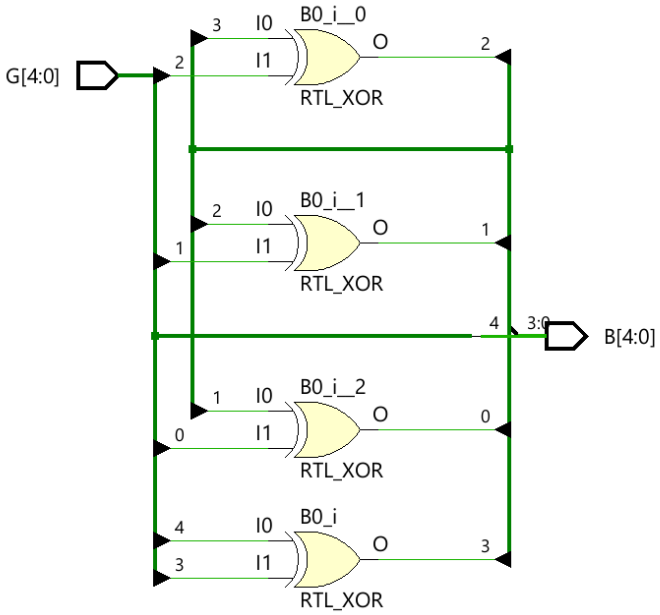
OUTPUT:-

```
G=00100,B=00111
G=00001,B=00001
G=01001,B=01110
G=00011,B=00010
G=01101,B=01001
G=01101,B=01001
G=00101,B=00110
G=10010,B=11100
G=00001,B=00001
G=01101,B=01001
```

WAVEFORMS:-



SCHEMATIC:-



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