DAY-2

#100DAYSOFRTL

Aim:- Basic Logic gates implementation using NOR GATE(Universal gate)

RTL CODE:-

```
1  ///DATE:-02/01/2024
2  ///Gate level Modelling
3  module Nor_Gate(input a,b,output y_not,
4  y_or,y_and,y_nand,y_xor,y_xnor);//Port declaration
5  wire [12:0] W; //wire declaration
6  nor g1(y_not,a,a);//NOT GATE
7  nor g2(W[0],a,b);
8  nor g3(y_or,W[0],W[0]);//OR GATE
9  nor g4(W[1],a,a);
10 nor g5(W[2],b,b);
11 nor g6(y_and,W[1],W[2]);//AND GATE
12 nor g7(W[3],a,a);
13 nor g8(W[4],b,b);
14 nor g9(W[5],W[3],W[4]);
15 nor g10(y_nand,W[5],W[5]);//NAND GATE
16 nor g11(W[6],a,b);
17 nor g12(W[7],a,W[6]);
18 nor g13(W[8],b,W[6]);
19 nor g14(y_xnor,W[7],W[8]);//XNOR GATE
20 nor g15(W[9],a,b);
21 nor g16(W[10],a,W[9]);
22 nor g17(W[11],b,W[9]);
23 nor g18(W[12],W[10],W[11]);
24 nor g19(y_xor,W[12],W[12]); //XOR GATE
25 endmodule
```

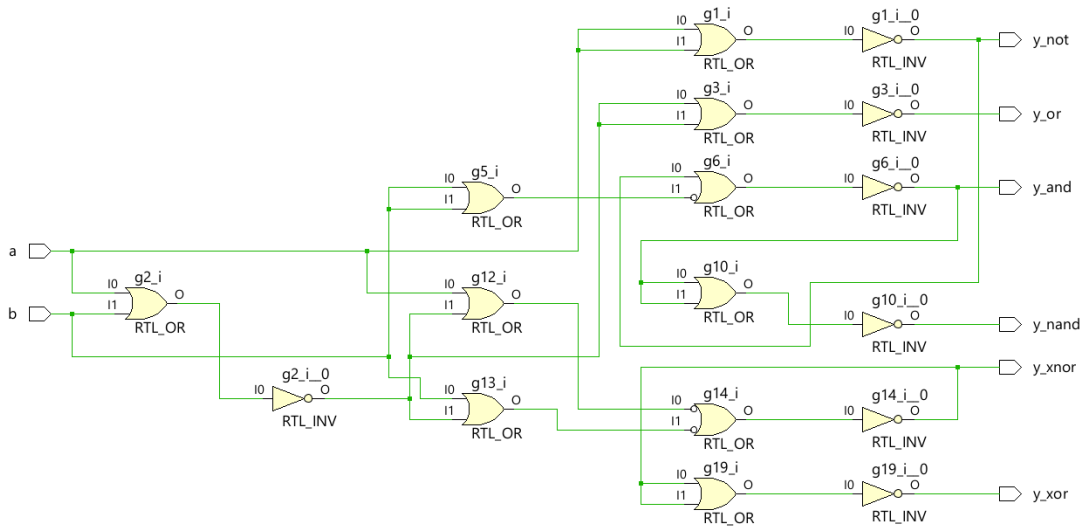
OUTPUT:-

```
a=0,b=0,y_not=1,y_and=0,y_or=0,y_nand=1,y_xor=0,y_xnor=1
a=0,b=1,y_not=1,y_and=0,y_or=1,y_nand=1,y_xor=1,y_xnor=0
a=1,b=0,y_not=0,y_and=0,y_or=1,y_nand=1,y_xor=1,y_xnor=0
a=1,b=1,y_not=0,y_and=1,y_or=1,y_nand=0,y_xor=0,y_xnor=1
```

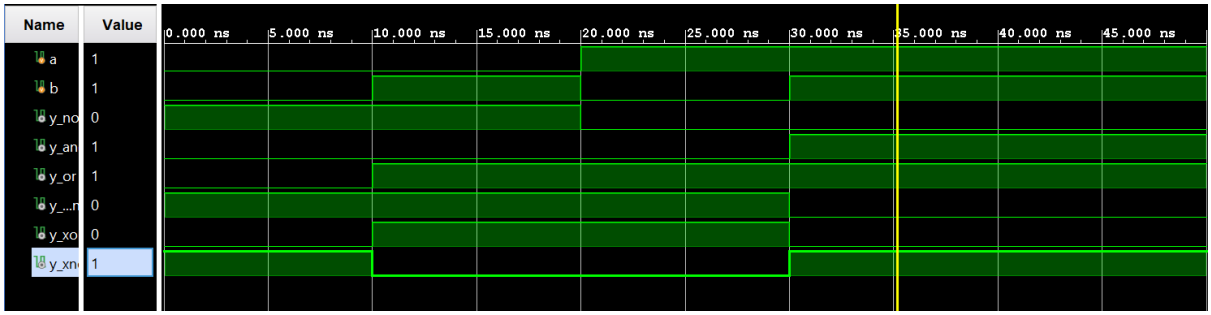
TESTBENCH:-

```
///DATE:-02/01/2024
module Nor_Gate_tb();
reg a,b;
wire y_not,y_and,y_or,y_nand,y_xor,
y_xnor;
Nor_Gate dut(a,b,y_not,
y_or,y_and,y_nand,y_xor,y_xnor);//Module Instantiation
initial begin
a=0;b=0;
#10;
$display("a=%d,b=%d,y_not=%b,y_and=%b,y_or=%b,y_nand=%b,y_xor=%b,y_xnor=%b",
a,b,y_not,y_and,y_or,y_nand,y_xor,y_xnor);
a=0;b=1;
#10;
$display("a=%d,b=%d,y_not=%b,y_and=%b,y_or=%b,y_nand=%b,y_xor=%b,y_xnor=%b",
a,b,y_not,y_and,y_or,y_nand,y_xor,y_xnor);
a=1;b=0;
#10;
$display("a=%d,b=%d,y_not=%b,y_and=%b,y_or=%b,y_nand=%b,y_xor=%b,y_xnor=%b",
a,b,y_not,y_and,y_or,y_nand,y_xor,y_xnor);
a=1;b=1;
#10;
$display("a=%d,b=%d,y_not=%b,y_and=%b,y_or=%b,y_nand=%b,y_xor=%b,y_xnor=%b",
a,b,y_not,y_and,y_or,y_nand,y_xor,y_xnor);
end
initial begin
#50;
$finish();
end
endmodule
```

SCHEMATIC:-



WAVEFORMS:-


Name
Value
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
40.000 ns
45.000 ns
a
1
b
1
y_no
0
y_an
1
y_or
1
y_...
0
y_xo
0
y_xn
1