DAY-58

#100DAYSOFRTL

Aim:- Implementation of Left and Right Shift Registers using Verilog.

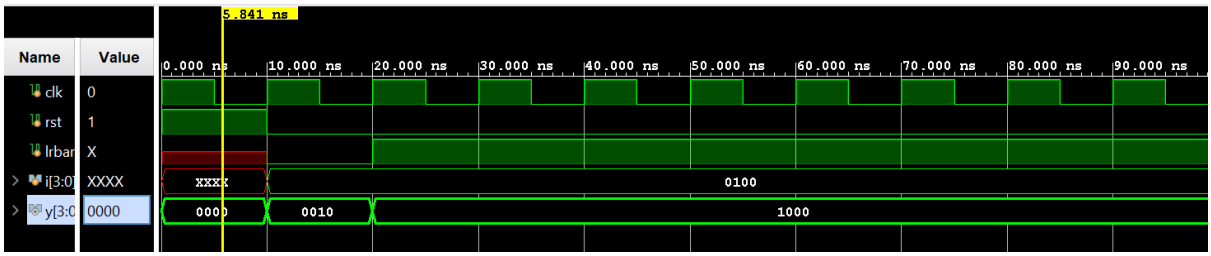
RTL CODE:-

```
////DATE:-27/02/2024
////DAY-58
////Implementation of Left and right shift Registers
module Day_58(input clk,rst,lrbar,
input [3:0] i,output  reg [3:0] y);
always @(posedge clk) begin
if(rst)
y<=4'b0000;
else
begin
if(lrbar)
y<=(i<<1);
else
y<=(i>>1);
end
end
endmodule
```

OUTPUT:-

```
Time resolution is 1 ps
clk=0,rst=0,lrbar=0,i=0100,y=0010
clk=0,rst=0,lrbar=1,i=0100,y=1000
```

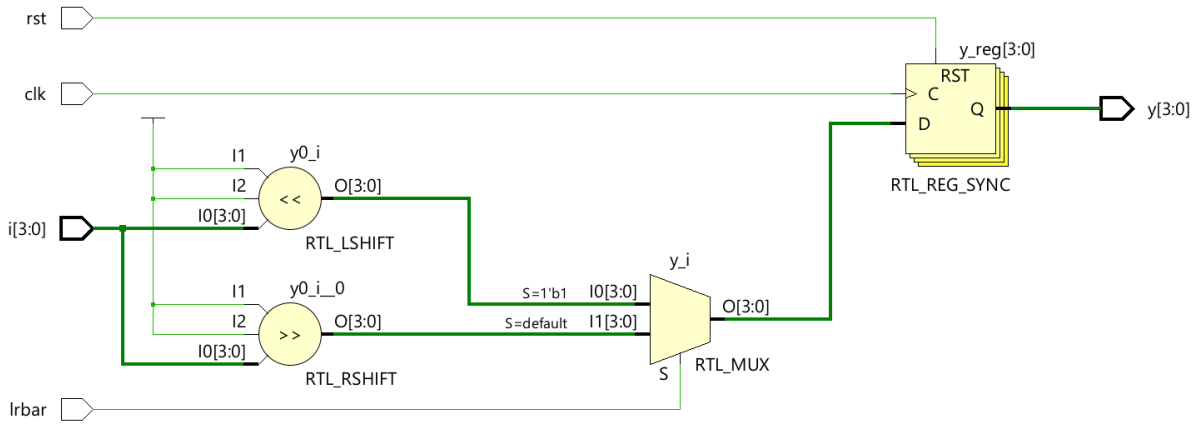
WAVEFORMS:-



TESTBENCH:-

```
module Day_58_tb();
reg clk,rst,lrbar;
reg [3:0] i;
wire [3:0] y;
Day_58 uut(clk,rst,lrbar,i,y);
always #5 clk=~clk;
initial clk=5;
initial begin
rst=1; #10;
rst=0;
lrbar=0;
i=4'b0100;
#10;
$display("clk=%d,rst=%d,lrbar=%d,i=%b,y=%b",clk,rst,lrbar,i,y);
lrbar=1;
i=4'b0100;
#10;
$display("clk=%d,rst=%d,lrbar=%d,i=%b,y=%b",clk,rst,lrbar,i,y);
end
initial begin
#100;
$finish();
end
endmodule
```

SCHEMATIC:-



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