DAY-36

#100DAYSOFRTL

Aim:- Implementation of 5x32 Decoder using Verilog.

RTL CODE:-

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//////DATE:-05/02/2024
////Implementation of 5:32 Decoder using 2:4 Decoder and 3:8 Decoder.
////It requires one 2:4 Decoder and four 3:8 Decoders to construct.
module Dec2_2x4(input [1:0] A,
output reg [3:0] Y);
always@(*) begin
//if(E) begin
case(A)
2'b00:Y=4'd1;
2'b01:Y=4'd2;
2'b10:Y=4'd4;
2'b11:Y=4'd8;
default: begin end
endcase
end
//else Y=0;
//end
endmodule

module Dec3_3x8(input [2:0] A, input E,
output  reg [7:0] Y);
always @(*) begin
if(E) begin
case(A)
3'b000:Y=8'd1;
3'b001:Y=8'd2;
3'b010:Y=8'd4;
3'b011:Y=8'd8;
3'b100:Y=8'd16;
3'b101:Y=8'd32;
3'b110:Y=8'd64;
3'b111:Y=8'd128;

default: begin end
endcase
end
else Y=0;
end
endmodule

module Decoder_5x32(input [4:0] A,
output [31:0] Y);
wire [3:0] w;
Dec2_2x4 A1(A[4:3],w[3:0]);
Dec3_3x8 A2(A[2:0],w[0],Y[7:0]);
Dec3_3x8 A3(A[2:0],w[1],Y[15:8]);
Dec3_3x8 A4(A[2:0],w[2],Y[23:16]);
Dec3_3x8 A5(A[2:0],w[3],Y[31:24]);
endmodule
```

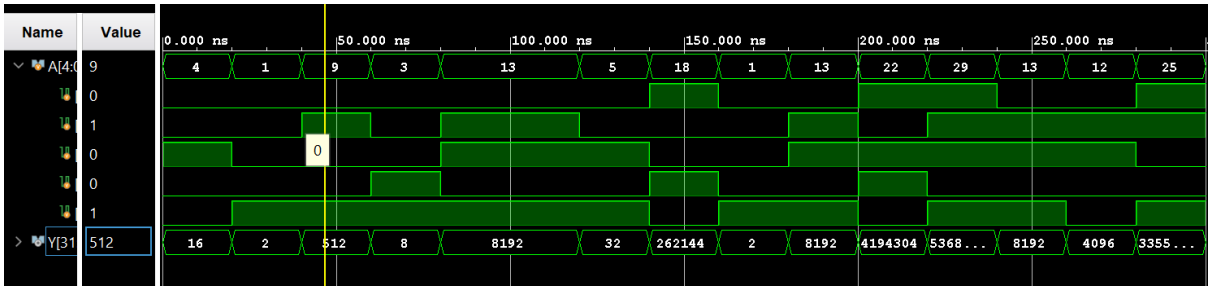
TESTBENCH:-

```
module Decoder_5x32_tb();
reg [4:0] A;
wire [31:0] Y;
Decoder_5x32 uut(A,Y);
initial begin
for(int i=0; i<20; i=i+1) begin
A=$random();
#10;
$display("A=%d,Y=%d",A,Y);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

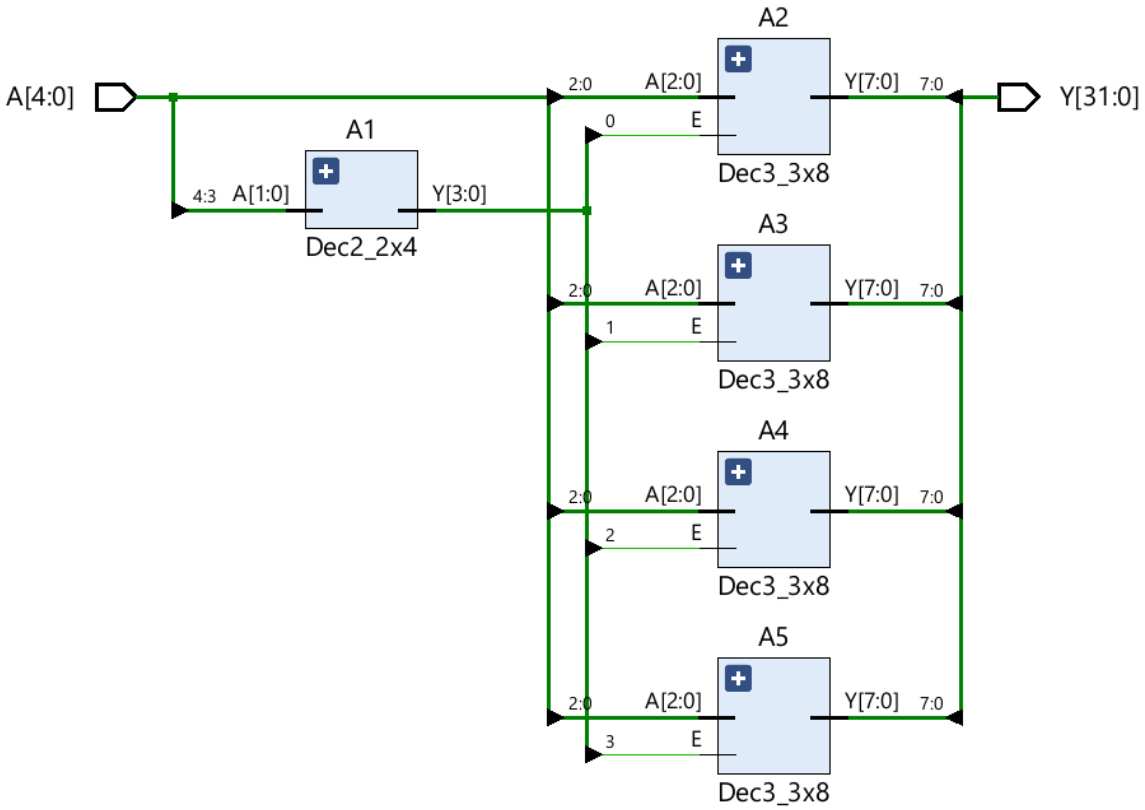
OUTPUT:-

```
A= 4,Y=         16
A= 1,Y=          2
A= 9,Y=        512
A= 3,Y=          8
A=13,Y=       8192
A=13,Y=       8192
A= 5,Y=         32
A=18,Y=     262144
A= 1,Y=          2
A=13,Y=       8192
A=22,Y=    4194304
A=29,Y= 536870912
A=13,Y=       8192
A=12,Y=       4096
A=25,Y=   33554432
```

WAVEFORMS:-



SCHEMATIC:-


A[4:0]
A1
4:3
A[1:0]
Y[3:0]
Dec2_2x4
A2
2:0
A[2:0]
0
E
Y[7:0]
7:0
Y[31:0]
Dec3_3x8
A3
1
Dec3_3x8
A4
2
Dec3_3x8
A5
3
Dec3_3x8

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