DAY-28

#100DAYSOFRTL

Aim:- Implementation of 1:8 Demultiplexer Using Verilog.

RTL CODE:-

```
///DATE:-28/01/2024
////Implementation of 1:8 Demux using Behavioral modelling
module Demux_1x8(input i,
input [2:0] Sel, output reg [7:0]y);
always @(*) begin
case(Sel)
3'b000:y={7'b0,i};
3'b001:y={6'b0,i,1'b0};
3'b010:y={5'b0,i,2'b0};
3'b011:y={4'b0,i,3'b0};
3'b100:y={3'b0,i,4'b0};
3'b101:y={2'b0,i,5'b0};
3'b110:y={1'b0,i,6'b0};
3'b111:y={i,7'b0};
endcase
end
endmodule
```

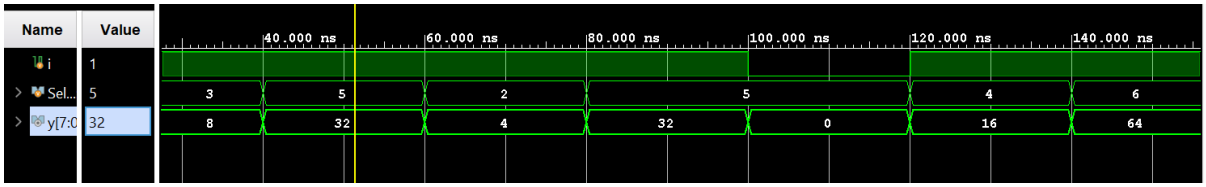
OUTPUT:-

```
i=0,Sel=1,y=  0
i=1,Sel=3,y=  8
i=1,Sel=5,y= 32
i=1,Sel=2,y=  4
i=1,Sel=5,y= 32
i=0,Sel=5,y=  0
i=1,Sel=4,y= 16
i=1,Sel=6,y= 64
i=1,Sel=2,y=  4
i=1,Sel=7,y=128
i=0,Sel=7,y=  0
```

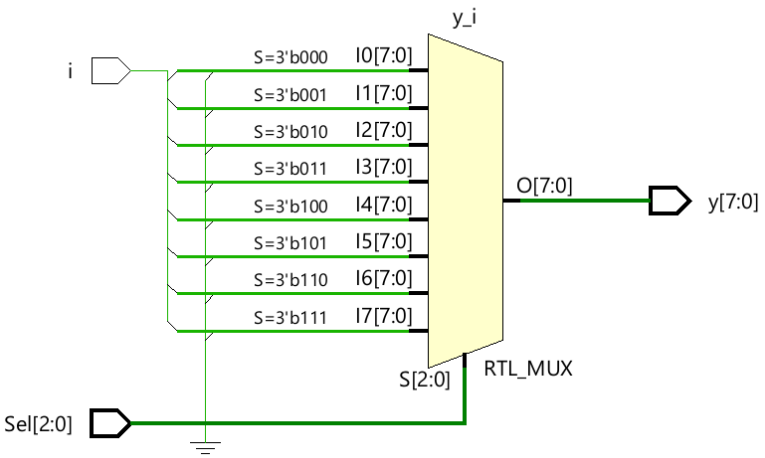
TESTBENCH:-

```
module Demux1x8_tb();
reg i;
reg [2:0] Sel;
wire [7:0] y;
Demux_1x8 uut(i,Sel,y);
initial begin
for(int k=0; k<15; k=k+1) begin
i=$random();
Sel=$random();
#10;
$display("i=%d,Sel=%d,y=%d", i,Sel,y);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



==========