DAY-32

#100DAYSOFRTL

Aim:- Implementation of N-Bit Comparator Using Verilog.

RTL CODE:-

```
////DATE:-01/02/2024
////Implementation of N-Bit Comparator
module Comp_Nbit#(parameter N=32)(input [N-1:0] A,B,
 output reg L,E,G);
always @(*) begin
if(A>B) begin
L=0; E=0; G=1;///GREATER THAN CONDITION
end
else if(A<B) begin////LESS THAN CONDITION
L=1;E=0; G=0;
end
else begin
L=0;E=1; G=0; ////EQUALS TO CONDITION
end
end
endmodule
```

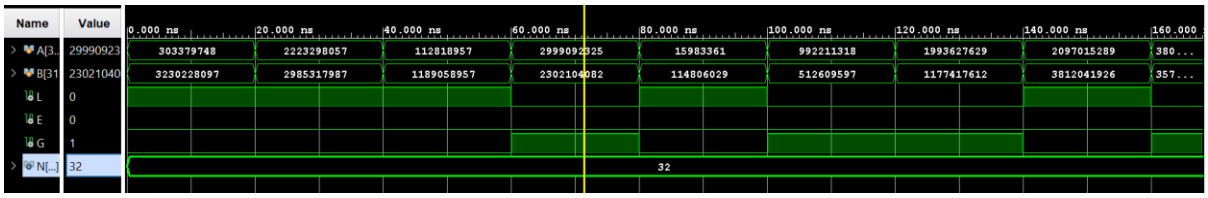
TESTBENCH:-

```
module Comp_Nbit_tb#(parameter N=32)();
reg [N-1:0] A,B;
wire L,E,G;
Comp_Nbit uut(A,B,L,E,G);
initial begin
for (int i=0; i<40; i=i+1) begin
A=$random();
B=$random();
#10;
$display("A=%d,B=%d,L=%d,E=%d,G=%d",A,B,L,E,G);
#10;
end
end
initial begin
#600;
$finish();
end
endmodule
```

OUTPUT:-

```
A= 303379748,B=3230228097,L=1,E=0,G=0
A=2223298057,B=2985317987,L=1,E=0,G=0
A= 112818957,B=1189058957,L=1,E=0,G=0
A=2999092325,B=2302104082,L=0,E=0,G=1
A=  15983361,B= 114806029,L=1,E=0,G=0
A= 992211318,B= 512609597,L=0,E=0,G=1
A=1993627629,B=1177417612,L=0,E=0,G=1
A=2097015289,B=3812041926,L=1,E=0,G=0
A=3807872197,B=3574846122,L=0,E=0,G=1
A=1924134885,B=3151131255,L=1,E=0,G=0
A=2301810194,B=1206705039,L=0,E=0,G=1
A=2033215986,B=3883308750,L=1,E=0,G=0
A=4093672168,B=3804909253,L=0,E=0,G=1
A= 777537884,B=3733858493,L=1,E=0,G=0
A=2527811629,B=2997298789,L=1,E=0,G=0
A=2985255523,B=  91457290,L=0,E=0,G=1
A=3225100928,B= 274997536,L=0,E=0,G=1
```

WAVEFORMS:-



SCHEMATIC:-