DAY-37

#100DAYSOFRTL

Aim:- Implementation of Full Adder using 3:8 Decoder.

RTL CODE:-

```verilog
////Day-37
////DATE:-06/02/2024
////Implementation of Full Adder using 3:8 Decoder
module Dec_3x8(input [2:0] A,
output  reg [7:0] Y);
always @(*) begin
case(A)
3'b000:Y=8'd1;
3'b001:Y=8'd2;
3'b010:Y=8'd4;
3'b011:Y=8'd8;
3'b100:Y=8'd16;
3'b101:Y=8'd32;
3'b110:Y=8'd64;
3'b111:Y=8'd128;
default: begin end
endcase
end
endmodule

module Dec_Fa(input [2:0] A,
output Sum,Carry);
wire [7:0] Y;
Dec_3x8 M1(A,Y);
assign Sum=Y[1]|Y[2]|Y[4]|Y[7];
assign Carry=Y[3]|Y[5]|Y[6]|Y[7];
endmodule
```

TESTBENCH:-

```verilog
module Dec_Fa_tb();
reg [2:0] A;
wire Sum,Carry;
Dec_Fa uut(A,Sum,Carry);
initial begin
for(int i=0; i<10; i=i+1) begin
A=$random();
#10;
$display("A=%b,Sum=%d,Carry=%d",A,Sum,Carry);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

OUTPUT:-

```
A=100,Sum=1,Carry=0
A=001,Sum=1,Carry=0
A=001,Sum=1,Carry=0
A=011,Sum=0,Carry=1
A=101,Sum=0,Carry=1
A=101,Sum=0,Carry=1
A=101,Sum=0,Carry=1
A=010,Sum=1,Carry=0
A=001,Sum=1,Carry=0
A=101,Sum=0,Carry=1
```
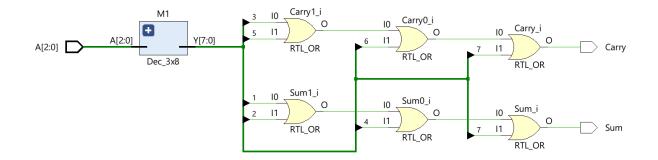
WAVEFORMS:-

Name	Value	0.000 ns	50.000 ns	100.000 ns	150.000 ns	200.000 ns	250.000 ns
A[2:0]	001	100	001	011	101	010	001	101
Sum	1							
Carry	0							

SCHEMATIC:-