DAY-74

#100DAYSOFRTL

Aim:- Implementation of D-LATCH USING 2X1MUX.

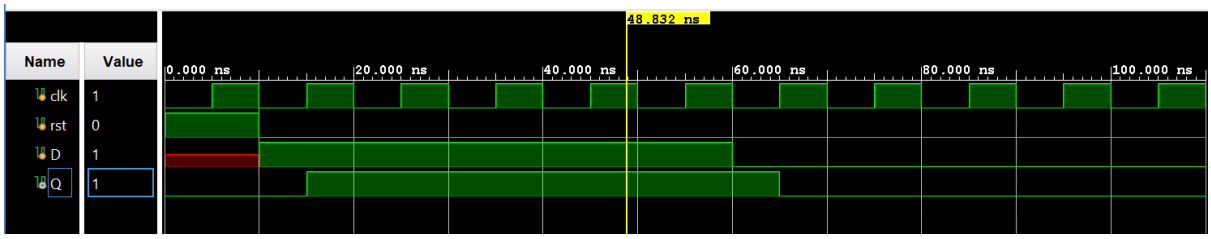
RTL CODE:-

```
////DATE:-14/03/2024
///DAY-74
////Implementation of D-LATCH USING 2X1 MUX
module Day_74_(input clk,rst,D,
output Q  );
assign Q=(~rst)&(((~clk)&Q)|(clk & D));
endmodule
```

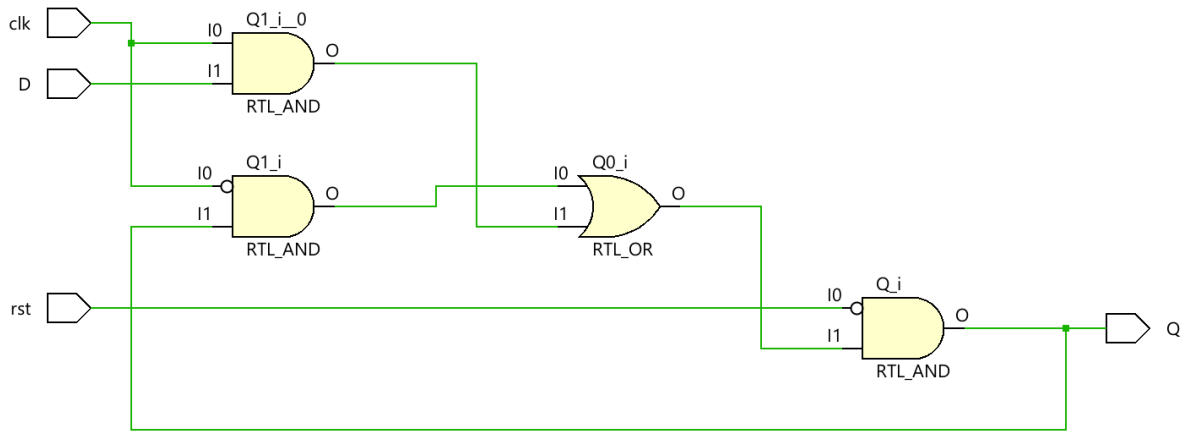
TESTBENCH:-

```
module Day_74_tb();
reg clk,rst,D;
wire Q;
Day_74_ uut(clk,rst,D,Q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
D=1; #50;
D=0; #50;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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