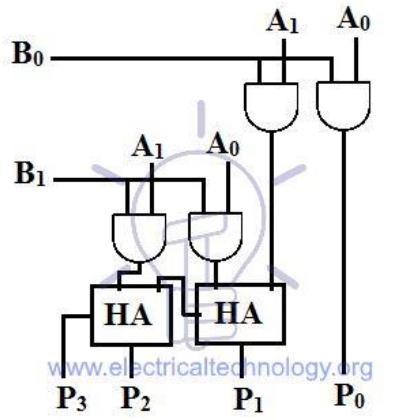
DAY-16

#100DAYSOFRTL

Aim:- Implementation of 2X2 BIT MULTIPLIER Using Verilog.

BLOCK DIAGRAM:-



Schematic of 2x2 Bit Multiplier Using Single Bit Adder

RTL CODE:-

```
////DATE:-16/01/2024
////Implementation of Two Bit Multiplier(2X2)
module HalfAdder(input A,B,
output Sum,Carry);
assign Sum=A^B;
assign Carry=A&B;
endmodule

module Two_BitMul(input [1:0]A,B,
output [3:0] P);
wire [3:0]W;
and g1(P[0],A[0],B[0]);
and g2(W[0],A[0],B[1]);
and g3(W[1],A[1],B[0]);
and g4(W[2],A[1],B[1]);
HalfAdder M0(.A(W[1]),.B(W[0]),.Sum(P[1]),.Carry(W[3]));
HalfAdder M1(.A(W[2]),.B(W[3]),.Sum(P[2]),.Carry(P[3]));
endmodule
```

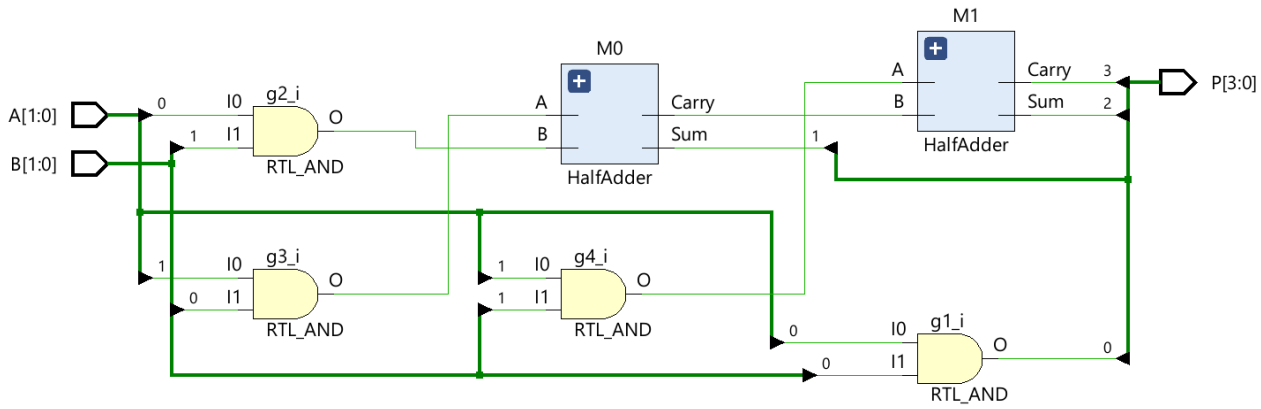
TESTBENCH:-

```
module Two_BitMul_tb();
reg [1:0] A,B;
wire [3:0] P;
Two_BitMul uut(.A(A),.B(B),.P(P));
initial begin
for(integer i=0; i<10; i=i+1) begin
A=$random();
B=$random();
#10;
$display("A=%d,B=%d,P=%d",A,B,P);
#10;
end
end
initial begin
#200;
$finish();
end
endmodule
```

OUTPUT:-

```
A=0,B=1,P= 0
A=1,B=3,P= 3
A=1,B=1,P= 1
A=1,B=2,P= 2
A=1,B=1,P= 1
A=2,B=1,P= 2
A=1,B=0,P= 0
A=1,B=2,P= 2
A=1,B=2,P= 2
A=1,B=3,P= 3
```

SCHEMATIC:-



WAVEFORMS:-