

DAY-41 #100DAYSOFRTL

Aim:- Implementation of Binary to Gray Conversion using Verilog.

RTL CODE:-

```
////DAY-41
////DATE:-10/02/2024
////Implementation of Binary to Gray Converter
module BtoG(input [4:0] A,
output [4:0] B);
//wire w1,w2,w3,w4;

O assign B[4]=A[4];
O assign B[3]=A[4]^A[3];
O assign B[2]=A[3]^A[2];
O assign B[1]=A[2]^A[1];
O assign B[0]=A[1]^A[0];
endmodule
```

TESTBENCH:-

```
module BtoG tb();
   reg [4:0] A;
   wire [4:0] B;
   BtoG uut(A,B);
   initial begin
for(int i=0; i<10; i=i+1) begin</pre>
O A=$random();
O #10;
$\display("A=\b', B=\b'', A, B);
O ¦#10;
   end
   end
   initial begin
O |#200;
⇒$finish();
   end
   endmodule!
```

OUTPUT:-

A=00100,B=00110

A=00001,B=00001

A=01001, B=01101

A=00011, B=00010

A=01101,B=01011

A=01101, B=01011

A=00101,B=00111

A=10010,B=11011

A=00001,B=00001

A=01101,B=01011

WAVEFORMS:-

Name	Value	0.000 ns	20.000 ns	40.000 ns	60.	000 ns	80.000 ns 100.000 ns	120.000 ns	140.000 ns	160.000 ns	180.000 ns
> MA[4:0	00011	00100	00001	01001		00011	01101	00101	10010	00001	01101
> 🐸 B[4:C	00010	00110	00001	01101		00010	01011	00111	11011	00001	01011

SCHEMATIC:-



