# DAY-39

# #100DAYSOFRTL

**Aim:-** Implementation of Tri-state Buffer.

## RTL CODE:-

```
////DAY-39
////DATE:-08/02/2024
////Implemenation of Tristate buffer in verilog
module Tristate_Buf(input A,en,
output reg  Y);
always @(A or en) begin
if(en) begin
Y=A;
end
else begin
Y=1'bz;
end
end
endmodule
```

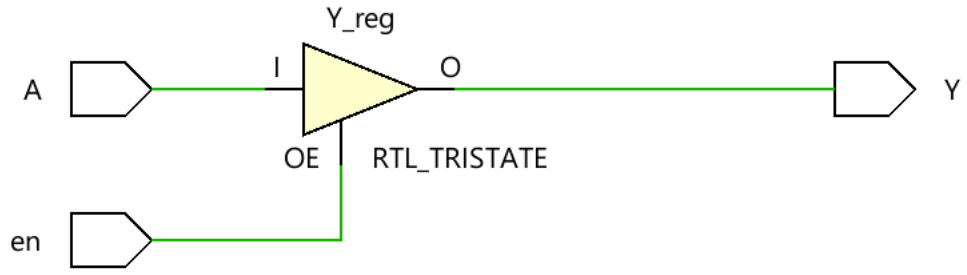
## TESTBENCH:-

```
module Tristate_Buf_tb();
reg A,en;
wire Y;
////Unit Under Test
Tristate_Buf uut(A,en,Y);
initial begin
for(int i=0; i<10; i++) begin
A=$random();
en=$random();
#10;
$display("A=%d,en=%d,Y=%d",A,en,Y);
#10;
end
end
initial begin
#130;
$finish;
end
endmodule
```

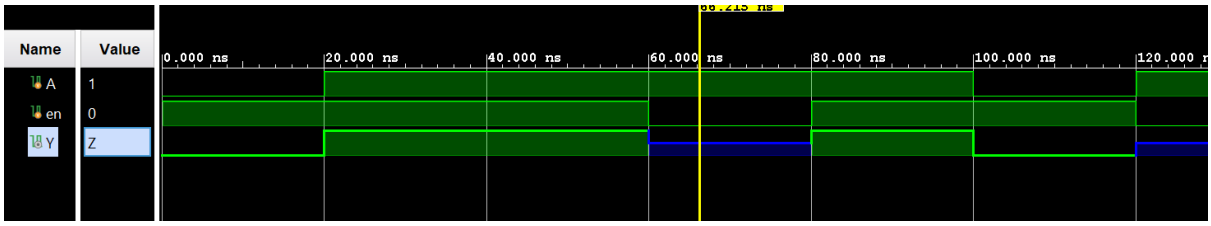
# OUTPUT:-

```
A=0,en=1,Y=0
A=1,en=1,Y=1
A=1,en=1,Y=1
A=1,en=0,Y=z
A=1,en=1,Y=1
A=0,en=1,Y=0
```

# SCHEMATIC:-




# WAVEFORMS:-

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