# DAY-70

# #100DAYSOFRTL

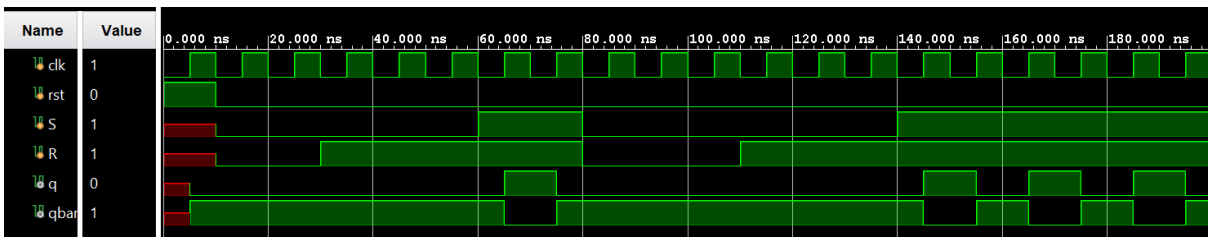
**Aim:-** Implementation of T F/F TO SR F/F using Verilog.

## RTL CODE:-

```
///DATE:-10/03/2024
///DAY-70
////Implementation of T FF TO SR FF
module Day_70(input clk,rst,S,R,
output q,qbar);
wire w1,w2,w3;
and g1(w1,S,qbar);
and g2(w2,R,q);
or g3(w3,w1,w2);
Tff t1(clk,rst,w3,q,qbar);
endmodule


////T-Flipflop
module Tff(input clk,rst,T,
output reg q, output qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(T)
1'b0:{q}={q};
1'b1:{q}={~q};
endcase
end
end
assign qbar=~q;
endmodule
```

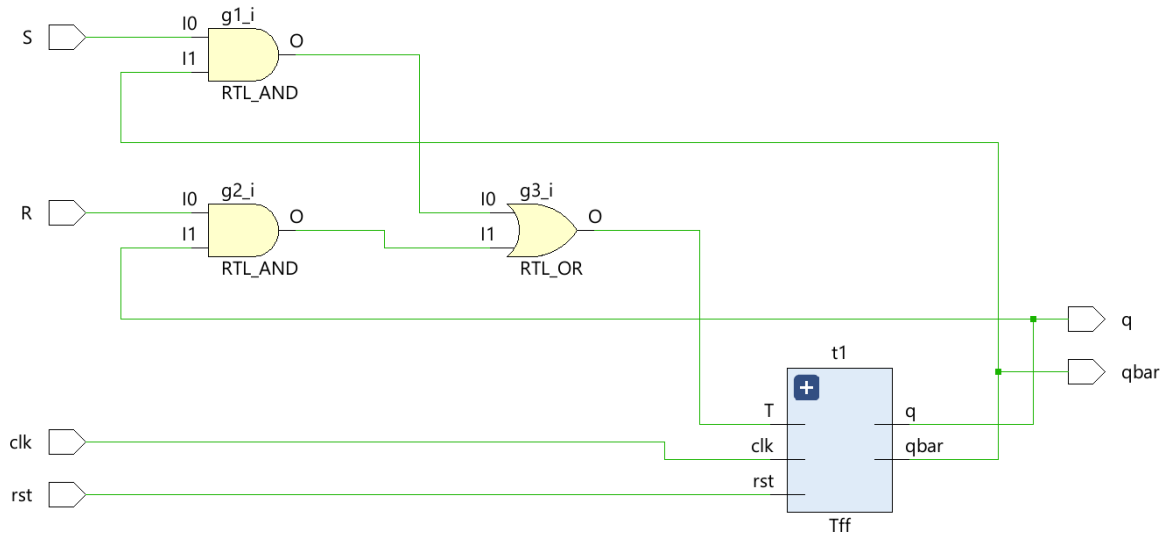
## WAVEFORMS:-



# TESTBENCH:-

```
module Day_70_tb();
reg clk,rst,S,R;
wire q,qbar;
Day_70 uut(clk,rst,S,R,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
S=0; R=0; #20;
S=0; R=1; #30;
S=1; R=1; #20;
S=0; R=0; #30;
S=0; R=1; #30;
S=1; R=1; #20;
end
initial begin
#200;
$finish();
end
endmodule
```

# SCHEMATIC:-




==========