

DAY-42 #100DAYSOFRTL

Aim:- Implementation of Gray to Binary Conversion using Verilog.

RTL CODE:-

```
///DAY-42
///Date:-11/02/2024
///Implemenatation of Gray code to Binary Code
module GtoB(input [4:0] G,
output [4:0] B);

output [4:0] B);

lassign B[4]=G[4];

assign B[3]=G[4]^G[3];

lassign B[2]=G[4]^G[3]^G[2];

assign B[1]=G[4]^G[3]^G[2]^G[1];

lassign B[0]=G[4]^G[3]^G[2]^G[1]^G[0];
lendmodule
```

TESTBENCH:-

```
module GtoB tb();
   reg [4:0] G;
   wire [4:0] B;
   GtoB uut (G, B);
   initial begin
O |for(int i=0; i<10; i=i+1) begin
G=$random();
O #10;
$\int \display("G=\b', B=\b'', G, B);
O |#10;
   end
   end
   initial begin
O \#200;
○⇒$finish();
   end
   endmodule
```

OUTPUT:-

G=00100,B=00111

G=00001,B=00001

G=01001,B=01110

G=00011,B=00010

G=01101,B=01001 G=01101,B=01001

G=00101,B=00110

G=10010,B=11100

G=00001,B=00001

G=01101,B=01001

WAVEFORMS:-

Name	Value	0.000 ns	20.000 ns	40.000 ns	60.000 ns	80.000 ns 100.000 ns	120.000 ns	140.000 ns	160.000 ns	180.000 ns
> 6 G[4:0	00100	00:00	00001	01001	00011	01101	00101	10010	00001	01101
> ₩ B[4:0	00111	00:11	00001	01110	00010	01001	00110	11100	00001	01001

SCHEMATIC:-



