DAY-49

#100DAYSOFRTL

Aim:- Implementation of T Flip-Flop using Verilog.

RTL CODE:-

```
////DAY-49
////DATE:-18/02/2024
////Implementation of T-Flipflop
module Day_49(input clk,rst,T,
output reg q, output qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(T)
1'b0:{q}={q};
1'b1:{q}={~q};
endcase
end
end
assign qbar=~q;
endmodule
```

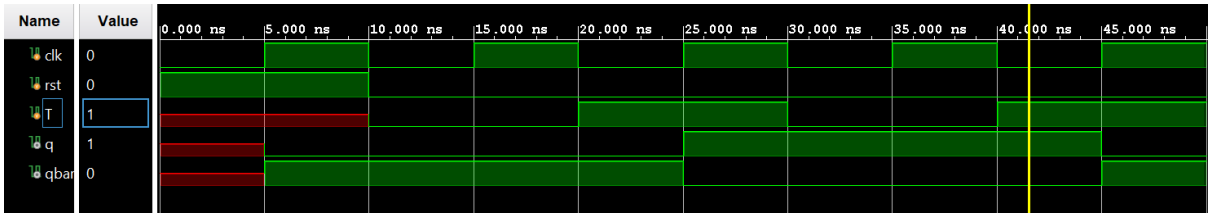
TESTBENCH:-

```
module Day_49_tb();
reg clk,rst,T;
wire q,qbar;
Day_49 uut(clk,rst,T,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
T=1'b0; #10;
$display("T=%b,q=%b,qbar=%b",T,q,qbar);
T=1'b1; #10;
$display("T=%b,q=%b,qbar=%b",T,q,qbar);
T=1'b0; #10;
$display("T=%b,q=%b,qbar=%b",T,q,qbar);
T=1'b1; #10;
$display("T=%b,q=%b,qbar=%b",T,q,qbar);
$finish();
end
endmodule
```

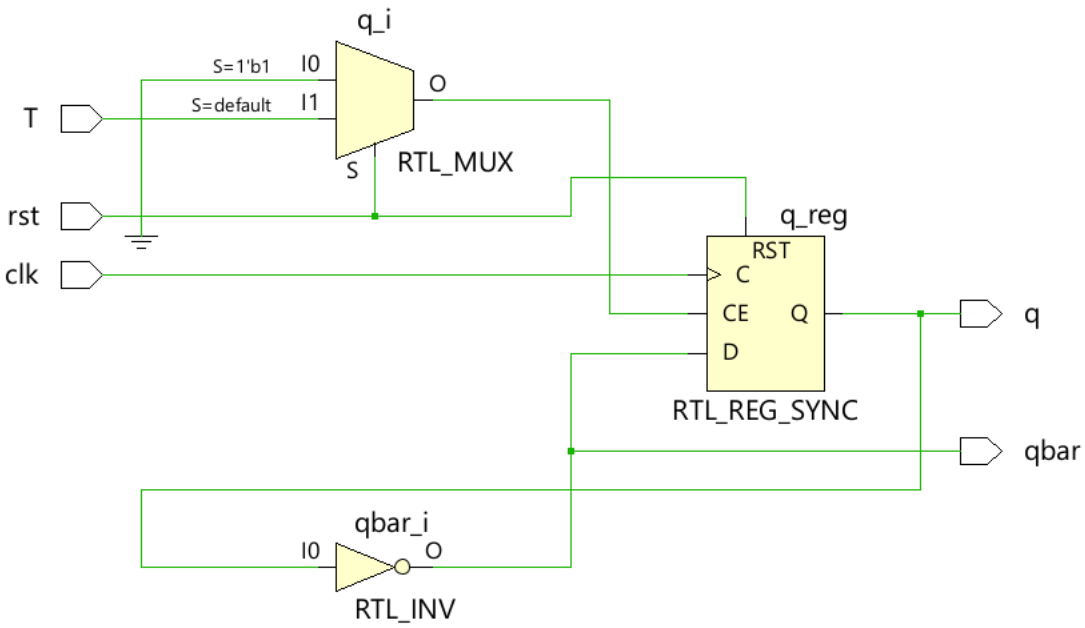
OUTPUT:-

```
T=0,q=0,qbar=1
T=1,q=1,qbar=0
T=0,q=1,qbar=0
T=1,q=0,qbar=1
```

WAVEFORMS:-



SCHEMATIC:-



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