DAY-3

#100DAYSOFRTL

Aim:- Random Boolean expression(**ABC+A'C'+D**) implementation using Verilog.

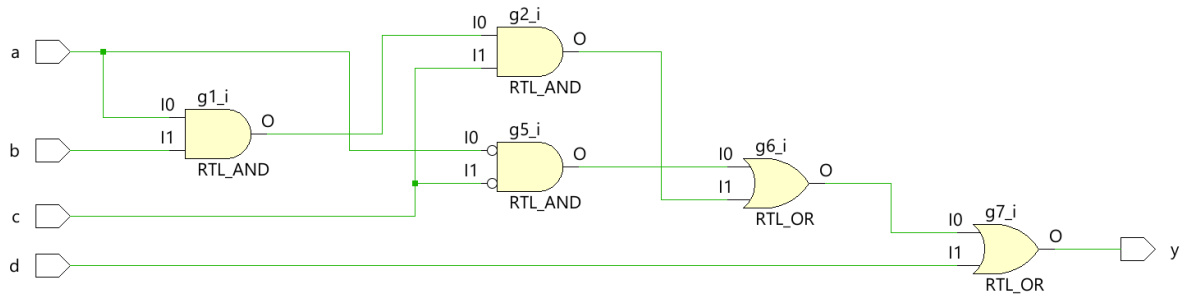
RTL CODE:-

```
///DATE:-03/01/2024
module Boolean_func(input a,b,c,d,
 output y);
////////ABC+A'C'+D USING GATE LEVEL MODELLING
wire w1,w2,w3,w4,w5,w6;
and g1(w1,a,b);
and g2(w2,w1,c);
not g3(w3,a);
not g4(w4,c);
and g5(w5,w3,w4);
or g6(w6,w5,w2);
or g7(y,w6,d);
endmodule
```

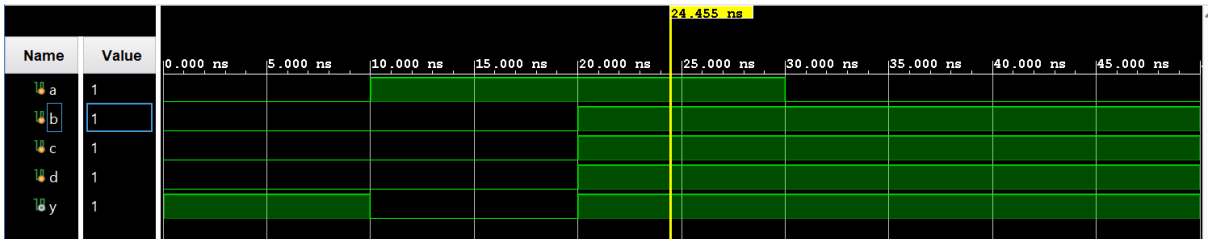
TESTBENCH:-

```
module Boolean_tb();
reg a,b,c,d;
wire y;
Boolean_func dut(a,b,c,d, y);
initial begin
a=0;b=0;c=0;d=0;
#10;
$display("a=%b,b=%b,c=%b,d=%b,y=%b",a,b,c,d,y);
a=1; b=0; c=0; d=0;
#10;
$display("a=%b,b=%b,c=%b,d=%b,y=%b",a,b,c,d,y);
a=1;b=1;c=1;d=1;
#10;
$display("a=%b,b=%b,c=%b,d=%b,y=%b",a,b,c,d,y);
a=0;b=1;c=1;d=1;
#10;
$display("a=%b,b=%b,c=%b,d=%b,y=%b",a,b,c,d,y);
end
initial begin
#50;
$finish();
end
endmodule
```

SCHEMATIC:-



WAVEFORMS:-



OUTPUT:-

a=0,b=0,c=0,d=0,y=1

a=1,b=0,c=0,d=0,y=0

a=1,b=1,c=1,d=1,y=1

a=0,b=1,c=1,d=1,y=1