

DAY-62 #100DAYSOFRTL

Aim:- Implementation of POSITIVE EDGE DETECTOR using Verilog.

RTL CODE:-

```
////DATE:-02/03/2024
////DAY-62
////Implementation of Posedge Detector
module Day_62(input clk,data,
output posedgeDetect);
reg data_d;
always @(posedge clk) begin
data_d<=data;
end

assign posedgeDetect data)&(~data_d);
endmodule</pre>
```

TESTBENCH:-

```
module Day_62_tb();
   reg clk;
   reg data;
   wire posedgeDetect;
   Day_62 uut(clk,data,posedgeDetect);
o always #5 clk=~clk;
   initial begin
O clk=0;
O data=0;
O #15; data=1;
O |#20;data=0;
0 #15;data=1;
O #15; data=1;
|#20;data=0;
O #15;data=1;
O #15; data=1;
O |#20;data=0;
|#15;data=1;
O #15; data=1;
#20;data=0;
() #15; data=1;
O #15; data=1;
|#20;data=0;
0 #15;data=1;
   end
   endmodule
```

WAVEFORMS:-

Name	Value	0.000 ns	50.000 ns	100.000 ns	150.000 ns	200.000 ns	250.000 ns	300.000 ns
¥ clk	1							
[™] data	1							
Ъ ро	0							

SCHEMATIC:-



