DAY-88

#100DAYSOFRTL

Aim:- Implementation of 2-BIT SYNCHRONOUS COUNTER USING JK Flipflop.

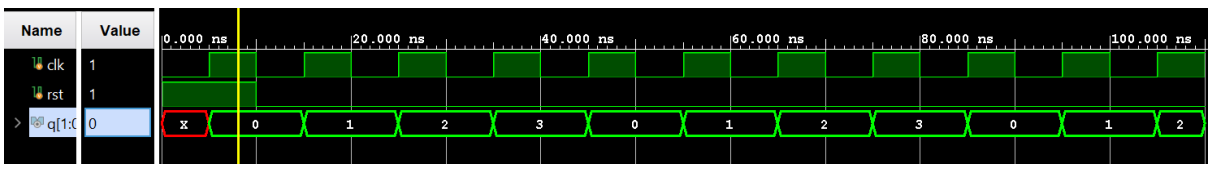
RTL CODE:-

```
////DATE:-28/03/2024
////DAY-88
////Implementation of 2-Bit Synchronous Counter by JK-Flipflop
module Day_88_(input clk,rst, output [1:0] q);
wire [3:0] w;
Jkff M1(clk,rst,1'b1,1'b1,w[0],w[1]);
Jkff M2(clk,rst,w[0],w[0],w[2],w[3]);
assign q[0]=w[0];
assign q[1]=w[2];
endmodule



module Jkff(input clk,rst,J,K,
 output  reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case({J,K})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={2'b10};
2'b11:{q,qbar}<={qbar,q};
default: begin end
endcase
end
 end
 endmodule
```

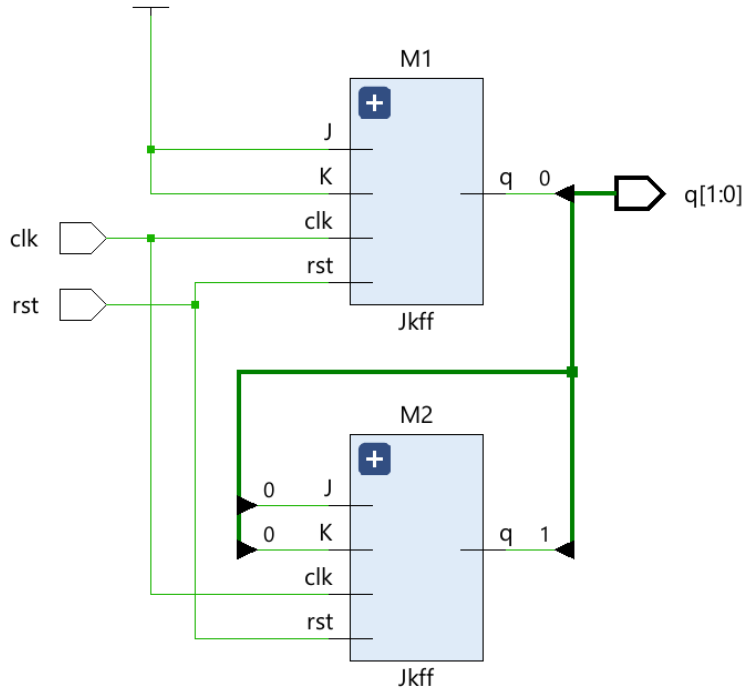
WAVEFORMS:-



TESTBENCH:-

```
module Day_88_tb();
reg clk,rst;
wire [1:0] q;
Day_88_ uut (clk,rst,q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
#100;
$finish();
end
endmodule
```

SCHEMATIC:-



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