



DAY-27

#100DAYSOFRTL

Aim:- Implementation of 7:1 Mux with 1-bit latch.

RTL CODE:-

```
//////DATE:-27/01/2024
//////Implementation of 7x1 Mux with 1 bit latch
module Mux_7x1(input [6:0] A,
input [2:0] Sel, output reg y);
○ always @(*) begin
○ case(Sel)
○ 3'b000:y=A[0];
○ 3'b001:y=A[1];
○ 3'b010:y=A[2];
○ 3'b011:y=A[3];
○ 3'b100:y=A[4];
○ 3'b101:y=A[5];
○ 3'b110:y=A[6];
○ 3'b111:y=A[6];
default:begin
end
endcase
end
endmodule
```

TESTBENCH:-

```
module Mux_7x1_tb();
reg [6:0] A;
reg [2:0] Sel;
wire y;
Mux_7x1 uut(A,Sel,y);
initial begin
○ for(int i=0; i<10; i++) begin
○ A=$random();
○ Sel=$random();
○ #10;
○ $display("A=%b,Sel=%d,y=%d",A,Sel,y);
○ #10;
end
end
initial begin
○ #200;
○ → $finish();
end
endmodule
```

OUTPUT:-

```
A=0100100, Sel=1, y=0
A=0001001, Sel=3, y=1
A=0001101, Sel=5, y=0
A=1100101, Sel=2, y=1
A=0000001, Sel=5, y=0
A=1110110, Sel=5, y=1
A=1101101, Sel=4, y=0
A=1111001, Sel=6, y=1
A=1000101, Sel=2, y=1
A=1100101, Sel=7, y=1
```

WAVEFORMS:-

Name	Value	0.000 ns	20.000 ns	40.000 ns	60.000 ns	80.000 ns	100.000 ns	120.000 ns	140.000 ns	160.000 ns	180.000 ns
> A[6:0]	1100101	0100100	0001001	0001101	1100101	0000001	1110110	1101101	1111001	1000101	1100101
> Sel...	111	001	011	101	010	101	100	110	010	111	
y	1										

SCHEMATIC:-

