

DAY-25 #100DAYSOFRTL

Aim:- Implementation of 16 BIT ALU with 16 Operations.

RTL CODE:-

```
1 \(\Date: -25/01/2024\)
 2 \(\hat{\rho}\) ///Implementation of ALU with 16 operations of 16 bit numbers
 4 input en, input [3:0] opcode, output reg [31:0] result);
 5 🖯 always @(A or B or opcode or en ) begin
 6 \ominus \text{ if (en==1)}
 7 🖯 case (opcode)
   4'b0000: result=A+B;///ADDITION
9 ! 4'b0001: result=A-B;///Subtraction
10 | 4'b0010: result=A*B;///Multiplication
11  4'b0011: result=A+1;///Increment
12 4'b0100: result=A-1;//Decrement
   4'b0101: result=A;///Buffer
14 | 4'b0110: result=~(A);//not gate
15 4'b0111: result=A&B;///AND GATE
16 | 4'b1000: result=A|B;///OR GATE
17 | 4'b1001: result=A^B;///XOR GATE
18 | 4'b1010: result=~(A^B);///XNOR GATE
19 4'b1011: result=~(A&B);///NAND GATE
20 4'b1100: result=~(A|B);///NOR GATE
22 4'b1110: result=A>>1;///RIGHT SHIFT
23 4'b1111: result=A/B;///DIVISION
24 default : result=16'hxxxx;
25 🖨 endcase
26 | else
27 esult=16'hzzzz;
28 🗎 end
29 🖨 endmodule
```

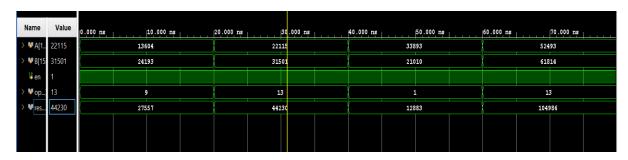
TESTBENCH:-

```
1 module ALU tb();
 2 reg [15:0] A,B;
 3 ¦
    reg en;
 4 | reg [3:0] opcode;
 5 wire [31:0] result;
 6 | ALU uut(A,B,en,opcode,result);
7 🖯 initial begin
8 of for(integer i=0; i<20; i=i+1) begin
9 | A=$random();
10 | B=$random();
11
    en=1;
12 opcode=$random();
13 !
    #10;
14 | $display("A=%d,B=%d,en=%d,opcode=%b,result=%d",A,B,en,opcode,result);
15 | #10;
16 🖨 end
17 🖨 end
18 \begin{tabular}{l} \end{tabular} initial begin
19 | #400;
20 $finish();
21 🖨 end
22 🖨 endmodule
```

OUTPUT:-

A=13604, B=24193, en=1, opcode=1001, result=	27557
A=22115,B=31501,en=1,opcode=1101,result=	14230
A=33893,B=21010,en=1,opcode=0001,result=	12883
A=52493,B=61814,en=1,opcode=1101,result= 10	14986
A=22509, B=63372, en=1, opcode=1001, result=	1057
A= 9414, B=33989, en=1, opcode=1010, result=429492	6332
A=63461,B=29303,en=1,opcode=0010,result=185959	7683
A=56207,B=27122,en=1,opcode=1110,result=	28103
A=31464, B=20165, en=1, opcode=1100, result=429493	34802

WAVEFORMS:-



SCHEMATIC:-

