DAY-18

#100DAYSOFRTL

Aim:- Implementation of 8-BIT Subtractor.

RTL CODE:-

```verilog
////DATE:-18/01/2024
////Implementation of 8-BIT Subtractor
module Subtractor(input [7:0] A,B,
output reg [7:0] sub);
reg [7:0] Temp_sub;
always@(*) begin
Temp_sub=(~B)+1'b1;///2'S COMPLEMENT SUBTRACTION;
sub=Temp_sub+A;
end
endmodule
```
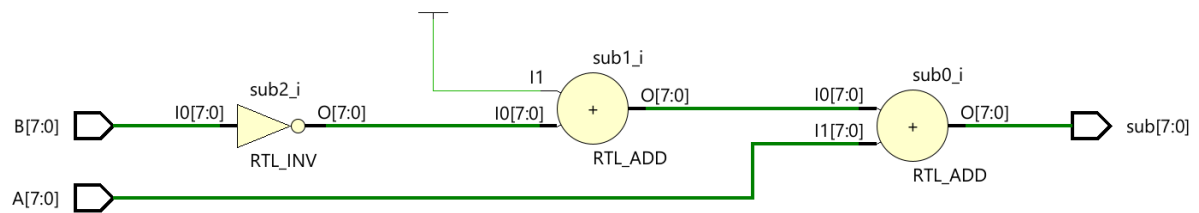
TESTBENCH:-

```verilog
module Sub_tb();
reg [7:0] A,B;
wire [7:0] sub;
Subtractor uut(A,B,sub);
initial begin
for(integer i=0; i<10; i=i+1)
begin
A=$random();
B=$random();
#10;
$display("A=%d,B=%d,sub=%d",A,B,sub);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```
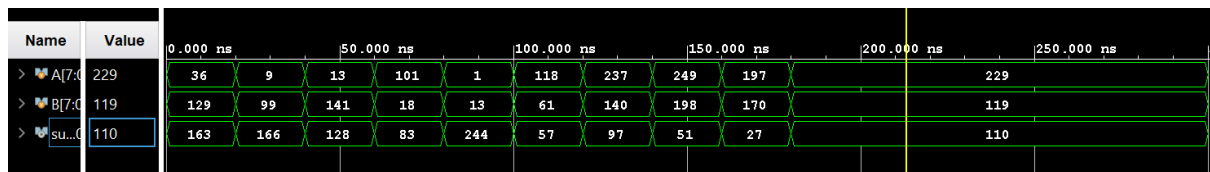
OUTPUT:-

```
A= 36,B=129,sub=163
A=  9,B= 99,sub=166
A= 13,B=141,sub=128
A=101,B= 18,sub= 83
A=  1,B= 13,sub=244
A=118,B= 61,sub= 57
A=237,B=140,sub= 97
A=249,B=198,sub= 51
A=197,B=170,sub= 27
A=229,B=119,sub=110
```

SCHEMATIC:-

WAVEFORMS:-

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