DAY-23

#100DAYSOFRTL

Aim:- Implementation of 16x1 Mux using 2x1 Mux by instantiating in Verilog.

RTL CODE:-

```
////DATE:-23/01/2024
////Implementation of 16X1 Mux using 2X1 Mux
module Mux2_2x1(input [1:0] A,
input Sel, output y);
assign y=Sel ? A[1]:A[0];
endmodule

module Day_23(input [15:0] A,
input [3:0] Sel,
output y);
wire [13:0] w;
Mux2_2x1 B1(A[1:0],Sel[0],w[0]);
Mux2_2x1 B2(A[3:2],Sel[0],w[1]);
Mux2_2x1 B3(A[5:4],Sel[0],w[2]);
Mux2_2x1 B4(A[7:6],Sel[0],w[3]);
Mux2_2x1 B5(A[9:8],Sel[0],w[4]);
Mux2_2x1 B6(A[11:10],Sel[0],w[5]);
Mux2_2x1 B7(A[13:12],Sel[0],w[6]);
Mux2_2x1 B8(A[15:14],Sel[0],w[7]);
Mux2_2x1 B9(w[1:0],Sel[1],w[8]);
Mux2_2x1 B10(w[3:2],Sel[1],w[9]);
Mux2_2x1 B11(w[5:4],Sel[1],w[10]);
Mux2_2x1 B12(w[7:6],Sel[1],w[11]);
Mux2_2x1 B13(w[9:8],Sel[2],w[12]);
Mux2_2x1 B14(w[11:10],Sel[2],w[13]);
Mux2_2x1 B15(w[13:12],Sel[2],y);
endmodule
```

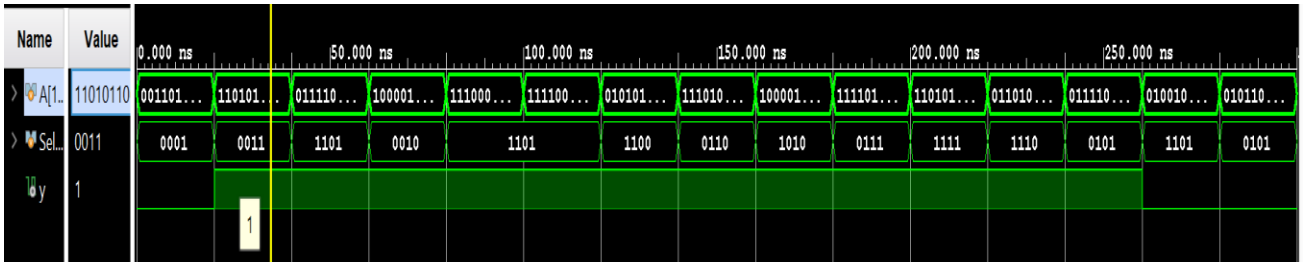
OUTPUT:-

```
A=0011010100100100,Sel= 1,y=0
A=1101011000001001,Sel= 3,y=1
A=0111101100001101,Sel=13,y=1
A=1000010001100101,Sel= 2,y=1
A=1110001100000001,Sel=13,y=1
A=1111000101110110,Sel=13,y=1
A=0101011111101101,Sel=12,y=1
A=1110100111111001,Sel= 6,y=1
A=1000010011000101,Sel=10,y=1
A=1111011111100101,Sel= 7,y=1
A=1101011000010010,Sel=15,y=1
A=0110100111110010,Sel=14,y=1
A=0111101011101000,Sel= 5,y=1
A=0100100101011100,Sel=13,y=0
A=0101100000101101,Sel= 5,y=0
```

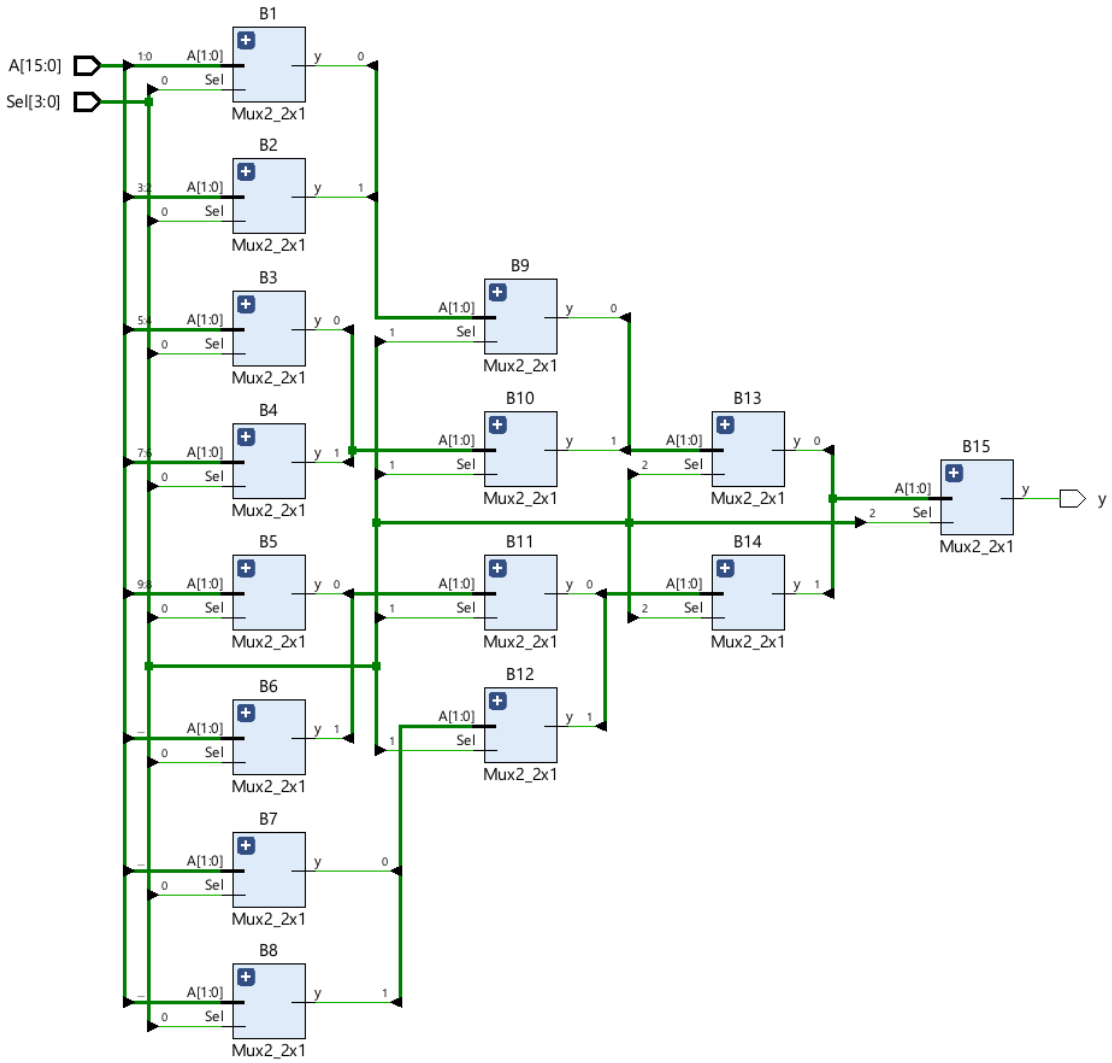
TESTBENCH:-

```
module Day_23_tb();
reg [15:0] A;
reg [3:0] Sel;
wire y;
Day_23  uut(A,Sel,y);
initial begin
for(integer i=0; i<15; i=i+1) begin
A=$random();
Sel=$random();
#10;
$display("A=%b,Sel=%d,y=%d",A,Sel,y);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-


A[15:0]
Sel[3:0]
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
B13
B14
B15
A[1:0]
Sel
y
Mux2_2x1