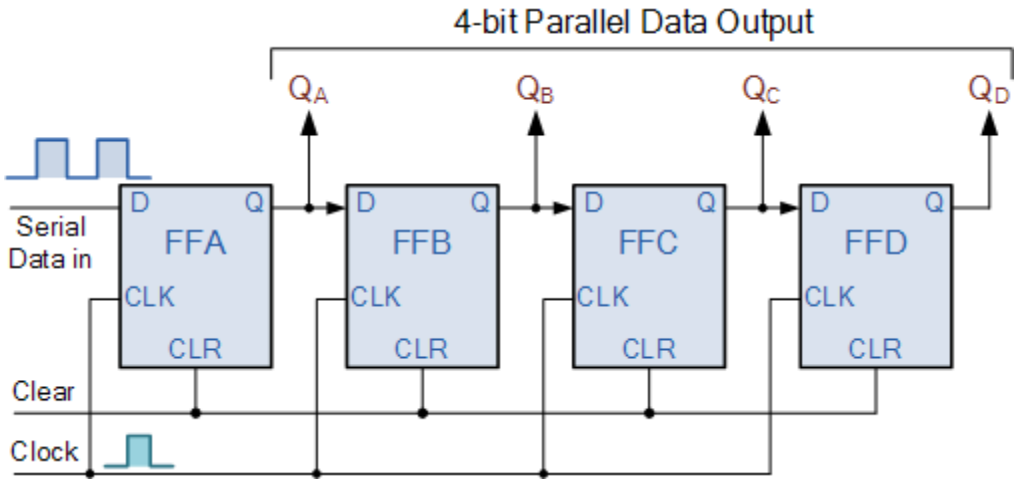
DAY-82

#100DAYSOFRTL

Aim:- Implementation of Serial-in Parallel-Out Shift Register.



RTL CODE:-

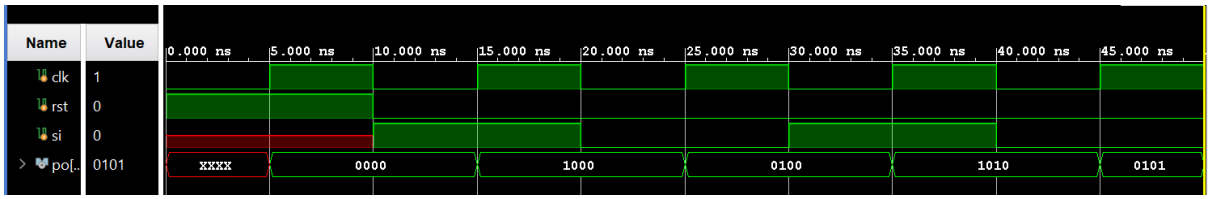
```
////DATE:-22/03/2024
////DAY-82
////Implementation of Serial-in Parallel-Out
module Day_82(input clk,rst,si,output [3:0] po);
wire [2:0] q;
Dff D1(clk,rst,si,q[2]);
Dff D2(clk,rst,q[2],q[1]);
Dff D3(clk,rst,q[1],q[0]);
Dff D4(clk,rst,q[0],po[0]);
assign po[3:1]=q[2:0];
endmodule

module Dff(input clk,rst,D,
output reg q);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(D)
1'b0:q=1'b0;
1'b1:q=1'b1;
endcase
end
end
endmodule
```

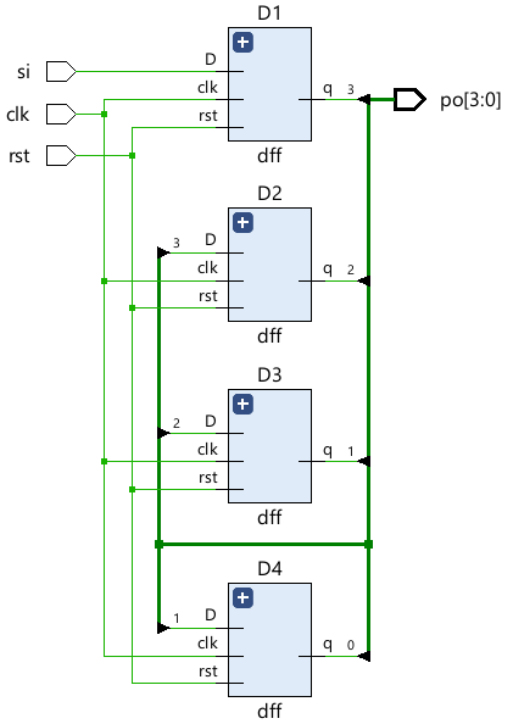
TESTBENCH:-

```
module Day_82_tb();
reg clk,rst,si;
wire [3:0] po;
Day_82 uut(clk,rst,si,po);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
si=1; #10;
si=0; #10;
si=1; #10;
si=0; #10;
//#20;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-


D1
si
clk
rst
D
clk
rst
q 3
dff
po[3:0]
D2
3
D
clk
rst
q 2
dff
D3
2
D
clk
rst
q 1
dff
D4
1
D
clk
rst
q 0
dff

==========