DAY-14

#100DAYSOFRTL

Aim:- Implementation of BCD adder Using Verilog.

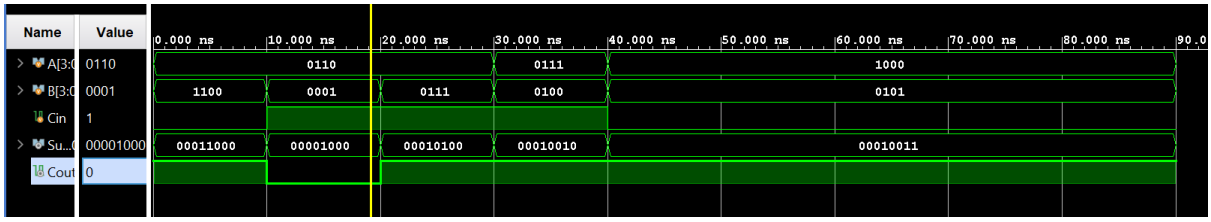
RTL CODE:-

```
////DATE:-14/01/2024
////4-BIT BCD ADDER
module BCD_Adder(
input [3:0] A,B,
input Cin, output  reg [7:0] Sum,
output reg Cout);
reg [7:0] Temp_Sum;
always @(*)
begin
Temp_Sum=A+B+Cin;
if(Temp_Sum>9) begin
Temp_Sum=Temp_Sum+4'b0110;
Cout=1;
Sum=Temp_Sum[7:0];
end
else begin
Cout=0;
Sum=Temp_Sum[7:0];
end
end
endmodule
```

OUTPUT:-

```
A= 6,B=12,Cin=0,Sum=00011000,Cout=1
A= 6,B= 1,Cin=1,Sum=00001000,Cout=0
A= 6,B= 7,Cin=1,Sum=00010100,Cout=1
A= 7,B= 4,Cin=1,Sum=00010010,Cout=1
A= 8,B= 5,Cin=0,Sum=00010011,Cout=1
```

WAVEFORMS:-



TESTBENCH:-

```
module BCDadder_tb();
reg [3:0]A,B;
reg Cin;
wire [7:0] Sum;
wire Cout;
BCD_Adder dut(.A(A),.B(B),.Cin(Cin),.Sum(Sum),.Cout(Cout));
initial begin
$monitor("A=%d,B=%d,Cin=%d,Sum=%b,Cout=%d",A,B,Cin,Sum,Cout);
A=6; B=12;
Cin=0;
#10;
A=6; B=1;
Cin=1;
#10;
A=6; B=7;
Cin=1;
#10;
A=7; B=4;
Cin=1;
#10;
A=8; B=5;
Cin=0;
#10;
end
initial begin
#90;
$finish();
end
endmodule
```

SCHEMATIC:-