DAY-24

#100DAYSOFRTL

Aim:- Implementation of 64x1 Mux using 4x1 Mux by instantiating in Verilog.

RTL CODE:-

```
////DATE:-24/01/2024
////Implementation of 64x1 Mux using 4x1 Mux by instantiating
module Mux2_4x1(input [3:0] A,
input [1:0] Sel, output reg y);
always @(*) begin
case(Sel)
2'b00:y=A[0];
2'b01:y=A[1];
2'b00:y=A[2];
2'b00:y=A[3];
endcase
end
endmodule

module Day_24(input [63:0] A,
input [5:0] Sel, output y);
wire [19:0] w;
Mux2_4x1 P1(A[3:0],Sel[1:0],w[0]);
Mux2_4x1 P2(A[7:4],Sel[1:0],w[1]);
Mux2_4x1 P3(A[11:8],Sel[1:0],w[2]);
Mux2_4x1 P4(A[15:12],Sel[1:0],w[3]);
Mux2_4x1 P5(A[19:16],Sel[1:0],w[4]);
Mux2_4x1 P6(A[23:20],Sel[1:0],w[5]);
Mux2_4x1 P7(A[27:24],Sel[1:0],w[6]);
Mux2_4x1 P8(A[31:28],Sel[1:0],w[7]);
Mux2_4x1 P9(A[35:32],Sel[1:0],w[8]);
Mux2_4x1 P10(A[39:36],Sel[1:0],w[9]);
Mux2_4x1 P11(A[43:40],Sel[1:0],w[10]);
Mux2_4x1 P12(A[47:44],Sel[1:0],w[11]);
Mux2_4x1 P13(A[51:48],Sel[1:0],w[12]);
Mux2_4x1 P14(A[55:52],Sel[1:0],w[13]);
Mux2_4x1 P15(A[59:56],Sel[1:0],w[14]);

Mux2_4x1 P16(A[63:60],Sel[1:0],w[15]);
Mux2_4x1 P17(w[3:0],Sel[3:2],w[16]);
Mux2_4x1 P18(w[7:4],Sel[3:2],w[17]);
Mux2_4x1 P19(w[11:8],Sel[3:2],w[18]);
Mux2_4x1 P20(w[15:12],Sel[3:2],w[19]);
Mux2_4x1 P21(w[19:16],Sel[5:4],y);
endmodule
```

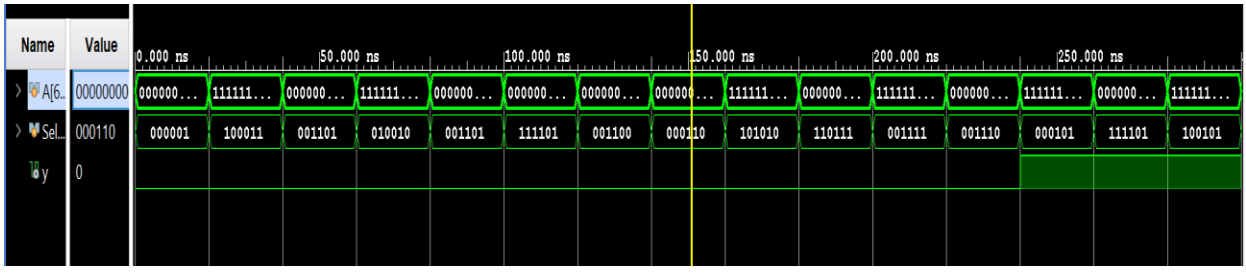
OUTPUT:-

```
A=0000000000000000000000000000000000001001000010101001101010010010,Sel= 1,y=0
A=1111111111111111111111111111111110000100100001001101011000001001,Sel=35,y=0
A=0000000000000000000000000000000000001101011100101111011000011101,Sel=13,y=0
A=1111111111111111111111111111111101100101100001010000100011001101,Sel=18,y=0
A=0000000000000000000000000000000000000011110011111000110000000001,Sel=13,y=0
A=0000000000000000000000000000000000001110110010001111110001011101l0,Sel=61,y=0
A=0000000000000000000000000000000000011101101101010001010111111101101,Sel=12,y=0
A=0000000000000000000000000000000000011111001111110111101001111110001,Sel= 6,y=0
A=1111111111111111111111111111111111110001011110111100001001100010l,Sel=42,y=0
A=0000000000000000000000000000000000011100101010111111110111111001101,Sel=55,y=0
A=1111111111111111111111111111111110001001001100101101011000001001O,Sel=15,y=0
A=0000000000000000000000000000000000011110010011000001101001111100l0,Sel=14,y=0
A=1111111111111111111111111111111111111010000000000011110101110100O,Sel= 5,y=1
A=0000000000000000000000000000000000010111001011000010010010101110O,Sel=61,y=1
A=1111111111111111111111111111111110010110101010110101100000101101,Sel=37,y=1
```

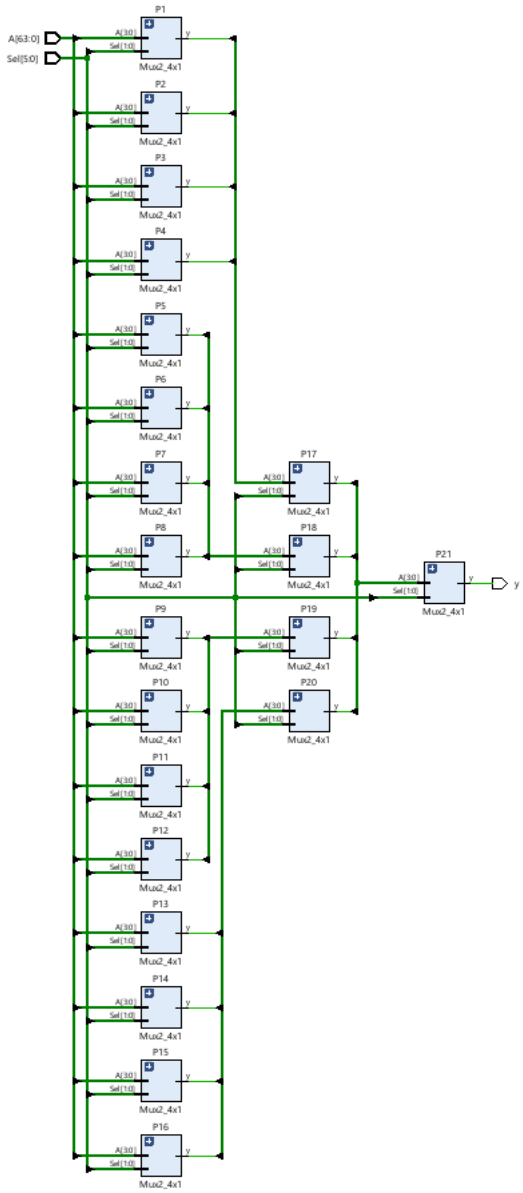
TESTBENCH:-

```
module Day24_tb();
reg [63:0] A;
reg [5:0] Sel;
wire y;
Day_24 uut(A,Sel,y);
initial begin
for(integer i=0; i<15; i=i+1) begin
A=$random();
Sel=$random();
#10;
$display("A=%b,Sel=%d,y=%d",A,Sel,y);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-


A[63:0]
Sel[5:0]
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
A[30]
Sel[1:0]
y
Mux2_4x1