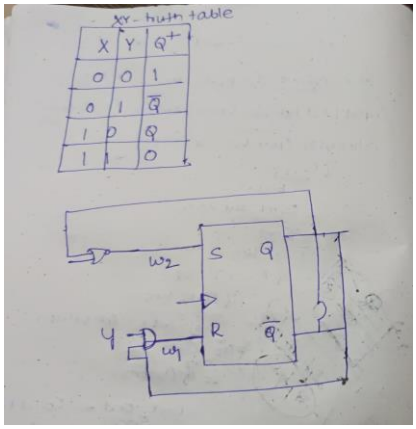
DAY-79

#100DAYSOFRTL

Aim:- Implementation of SR FLIPFLOP TO RANDOM XY FLIPFLOP.

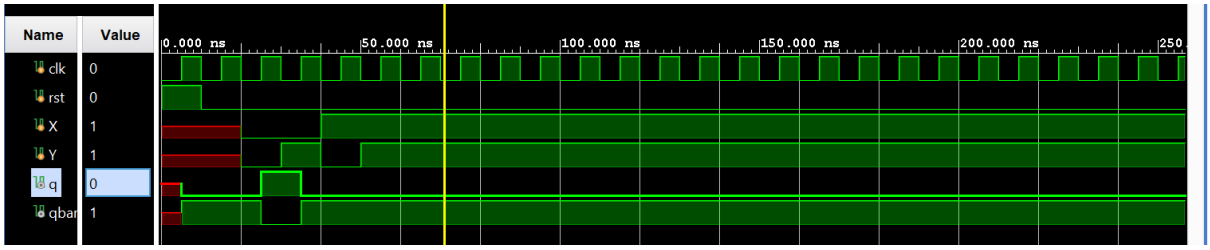


RTL CODE:-

```
////DATE:-19/03/2024
///DAY-79
////Implementation of SR Flipflop TO Random XY Flipflop
module Day_79(input clk,rst,X,Y, output q,qbar);
wire w1,w2;
xor g1(w1,X,qbar);
and g2(w2,Y,q);
SRff Srff(clk,rst,w1,w2,q,qbar);
endmodule


module SRff(input clk,rst,S,R,
output reg q,
output qbar);
always@(posedge clk) begin
if(rst) q<=0;
else begin
case({S,R})
2'b00:q<=q; ////No change
2'b01:q<=0; ////reset
2'b10:q<=1; ////set
endcase
end
end
assign qbar=~q;
endmodule
```

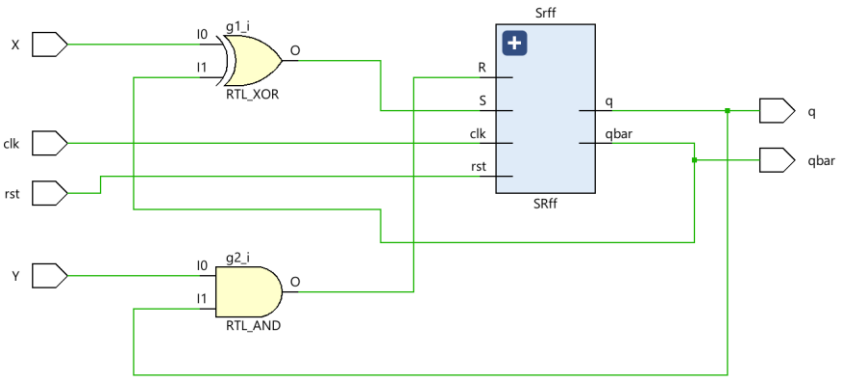
WAVEFORMS:-



TESTBENCH:-

```
module Day_79_tb();
reg clk,rst,X,Y;
wire q,qbar;
Day_79 uut(clk,rst,X,Y,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0; #10;
X=0; Y=0; #10;
X=0; Y=1; #10;
X=1; Y=0; #10;
X=1; Y=1; #10;
end
endmodule
```

SCHEMATIC:-



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