DAY-60

#100DAYSOFRTL

Aim:- Implementation of BCD TO 7 SEVEN SEGMENT DISPLAY using Verilog.

RTL CODE:-

```
////DATE:-29/02/2024
////DAY-60
/////Implementation of BCD TO 7 SEVEN DISPLAY
module Day_60(input [3:0] BCD,
output reg [6:0] S);
always @(BCD) begin
case(BCD)
4'b0000: S=7'b0111111; ///Display 0
4'b0001: S=7'b0000110;  ///Display 1
4'b0010: S=7'b1011011;  ///Display 2
4'b0011: S=7'b1001111;  ///Display 3
4'b0100: S=7'b1100110;  ///Display 4
4'b0101: S=7'b1101101;  ///Display 5
4'b0110: S=7'b1111101;  ///Display 6
4'b0111: S=7'b0000111;  ///Display 7
4'b1000: S=7'b1111111;  ///Display 8
4'b1001: S=7'b1100111;  ///Display 9
default: S=7'b0;
endcase
end
endmodule

```

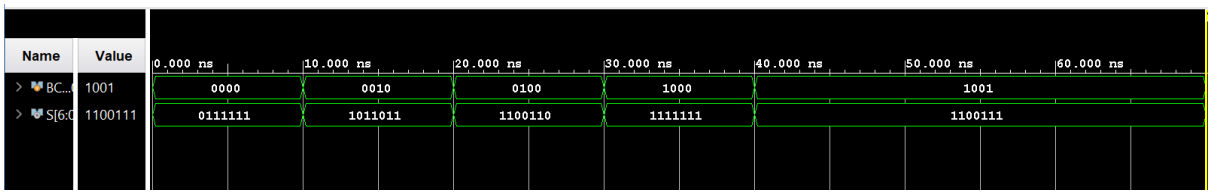
OUTPUT:-

```
Time resolution is 1 ps
BCD=0000,S=0111111
BCD=0010,S=1011011
BCD=0100,S=1100110
BCD=1000,S=1111111
BCD=1001,S=1100111
```

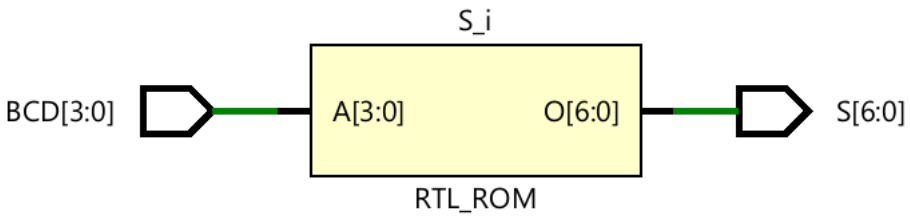
TESTBENCH:-

```
1  module Day_60_tb();
2  reg [3:0] BCD;
3  wire [6:0] S;
4  Day_60 uut(BCD,S);
5  initial begin
6  $monitor("BCD=%b,S=%b",BCD,S);
7  BCD=4'b0000;
8  #10;
9  BCD=4'b0010;
10 #10;
11 BCD=4'b0100;
12 #10;
13 BCD=4'b1000;
14 #10;
15 BCD=4'b1001;
16 #10;
17 end
18 initial begin
19 #70;
20 $finish();
21 end
22 endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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