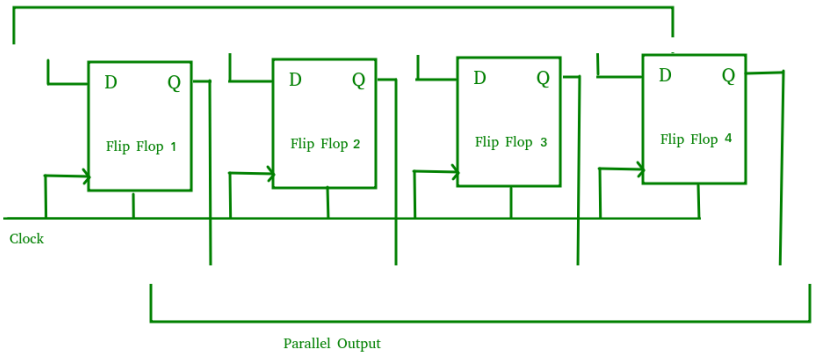
DAY-83

#100DAYSOFRTL

Aim:- Implementation of Parallel-in Parallel-Out Shift Register.



RTL CODE:-

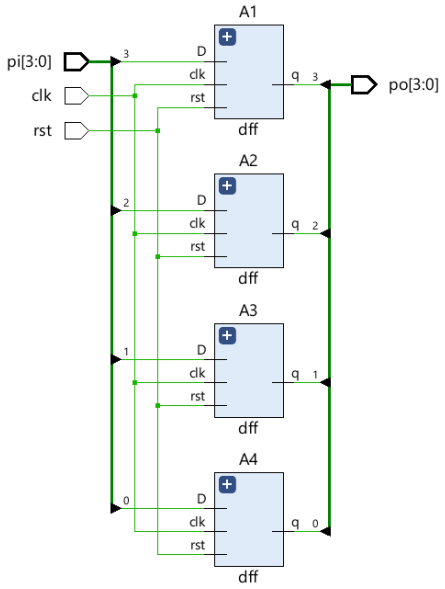
```
////DATE:-23/03/2024
///DAY-83
////Implementation of Parallel-in Parallel-out Shift Register
module Day_83(input clk,rst,[3:0]pi,output [3:0] po);
dff A1(clk,rst,pi[3],po[3]);
dff A2(clk,rst,pi[2],po[2]);
dff A3(clk,rst,pi[1],po[1]);
dff A4(clk,rst,pi[0],po[0]);
endmodule

module dff(input clk,rst,D,
output reg q);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(D)
1'b0:q=1'b0;
1'b1:q=1'b1;
endcase
end
end
endmodule
```

TESTBENCH:-

```
module Day_83_tb();
reg clk,rst;
reg [3:0] pi;
wire [3:0] po;
Day_83 uut(clk,rst,pi,po);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
pi=1010; #10;
pi=1011; #10;
pi=1001; #10;
pi=1110; #10;
$finish();
end
endmodule
```

WAVEFORMS:-

SCHEMATIC:-



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