DAY-21

#100DAYSOFRTL

Aim:- Implementation of 4x1 Mux using Verilog.

RTL CODE:-

```
////DATE:-21/01/2024
////Implementation of 4X1 MUX
module Mux_4x1(input [3:0]A,
input [1:0] Sel,
output reg y);
always @(A or Sel)
begin
case(Sel)
2'b00:y=A[0];
2'b01:y=A[1];
2'b10:y=A[2];
2'b11:y=A[3];
default:begin end
endcase
end
endmodule
```

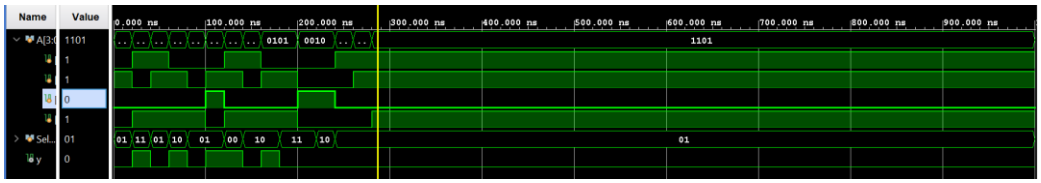
OUTPUT:-

```
A=0100,Sel=1,y=0
A=1001,Sel=3,y=1
A=1101,Sel=1,y=0
A=0101,Sel=2,y=1
A=0001,Sel=1,y=0
A=0110,Sel=1,y=1
A=1101,Sel=0,y=1
A=1001,Sel=2,y=0
A=0101,Sel=2,y=1
A=0101,Sel=3,y=0
A=0010,Sel=3,y=0
A=0010,Sel=2,y=0
A=1000,Sel=1,y=0
A=1100,Sel=1,y=0
A=1101,Sel=1,y=0
```

TESTBENCH:-

```
module Mux_tb();
reg [3:0] A;
reg [1:0] Sel;
wire y;
Mux_4x1 uut(A,Sel,y);
initial begin
for(integer i=0; i<15; i=i+1)
begin
A=$random();
Sel=$random();
#10;
$display("A=%b,Sel=%d,y=%d",A,Sel,y);
#10;
end
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-