DAY-66

#100DAYSOFRTL

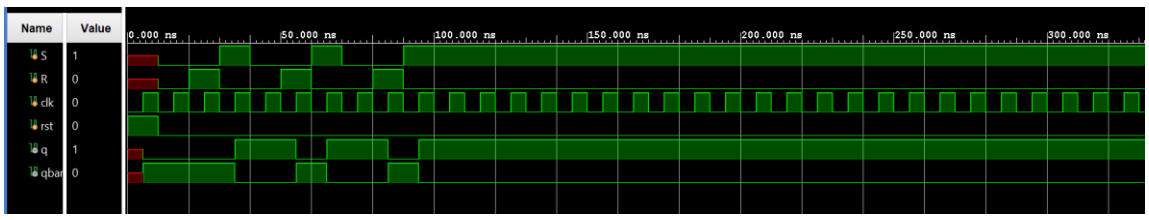
Aim:- Implementation of D F/F TO SR F/F using Verilog.

RTL CODE:-

```
////DATE:-06/03/2024
////DAY-66
////Implementation of D flipflop to SR flipflop
module Day_66(input clk,rst,S,R,
output q,qbar);
wire w1,w2,w3;
not g1(w1,R);
and g2(w2,w1,q);
or g3(w3,w2,S);
Dff dff1(.D(w3),.clk(clk),.rst(rst),.q(q),.qbar(qbar));
endmodule

module Dff(input D,clk,rst,
output reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case(D)
1'b0:{q,qbar}<={1'b0,1'b1};
1'b1:{q,qbar}<={1'b1,1'b0};
endcase
end
end
endmodule
```

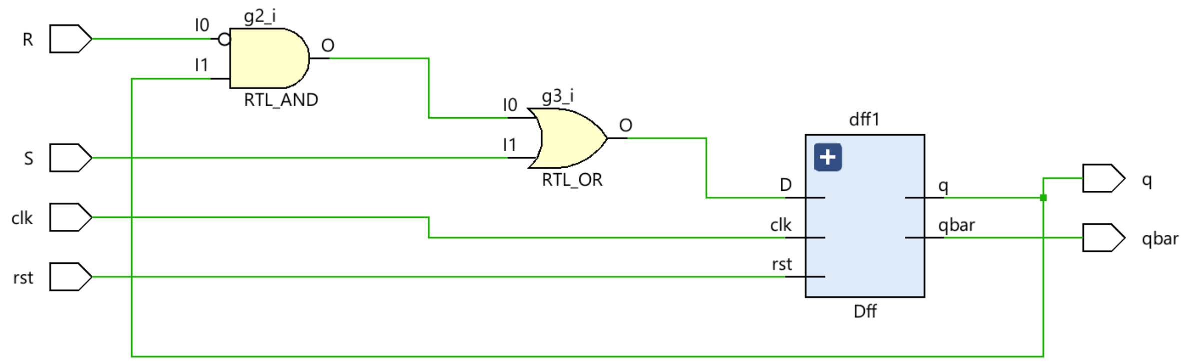
WAVEFORMS:-



TESTBENCH:-

```
module Day_66_tb();
reg S,R,clk,rst;
wire q,qbar;
Day_66 uut(clk,rst,S,R,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
{S,R}=2'b00; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b01; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b10; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b00; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b01; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b10; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b00; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b01; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b10; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
end
endmodule
```

SCHEMATIC:-



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