DAY-61

#100DAYSOFRTL

Aim:- Implementation of BINARY TO ONE-HOT ENCODER using Verilog.

RTL CODE:-

```
////DATE:-01/03/2024
////DAY-61
////Implementation of BINARY TO ONE-HOT ENCODER of
//both MSB TYPE AND LSB TYPE USING ENABLE INPUT.
module Day_61(input [4:0] bin,
input en,
output reg [31:0] One_hot_cold);
always@(*) begin
if(en) begin
One_hot_cold=1'b1<<bin;
end
else
One_hot_cold=1'b1>>bin;
end
endmodule
```

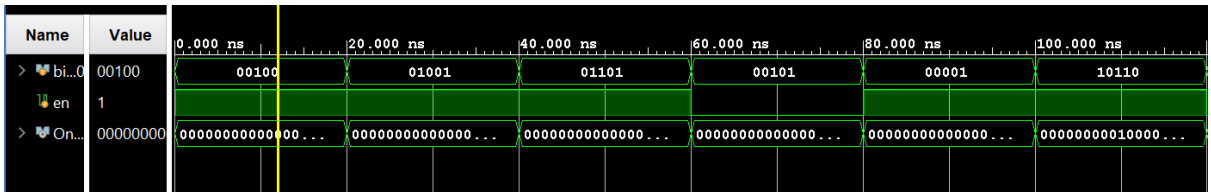
TESTBENCH:-

```
module Day_61_tb();
reg [4:0] bin;
reg en;
wire [31:0] One_hot_cold;
Day_61 uut(bin,en,One_hot_cold);
initial begin
for(integer i=0; i<32; i=i+1) begin
bin=$random();
en=$random();
#10;
$display("bin=%b,en=%d,One_hot_cold=%b",bin,en,One_hot_cold);
#10;
end
end
initial begin
#400;
$finish();
end
endmodule
```

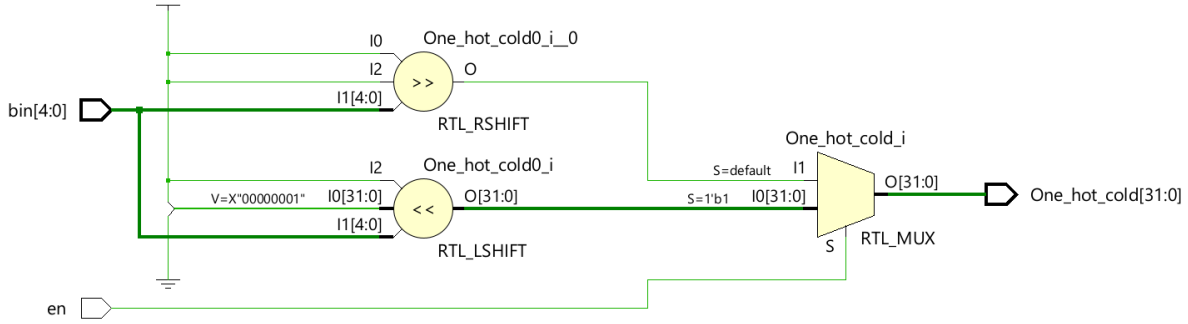
OUTPUT:-

```
bin=00100,en=1,One_hot_cold=00000000000000000000000000010000
bin=01001,en=1,One_hot_cold=00000000000000000000001000000000
bin=01101,en=1,One_hot_cold=00000000000000000010000000000000
bin=00101,en=0,One_hot_cold=00000000000000000000000000000000
bin=00001,en=1,One_hot_cold=00000000000000000000000000000010
bin=10110,en=1,One_hot_cold=00000000100000000000000000000000
bin=01101,en=0,One_hot_cold=00000000000000000000000000000000
bin=11001,en=0,One_hot_cold=00000000000000000000000000000000
bin=00101,en=0,One_hot_cold=00000000000000000000000000000000
bin=00101,en=1,One_hot_cold=00000000000000000000000000100000
bin=10010,en=1,One_hot_cold=00000000000001000000000000000000
bin=10010,en=0,One_hot_cold=00000000000000000000000000000000
bin=01000,en=1,One_hot_cold=00000000000000000000000100000000
bin=11100,en=1,One_hot_cold=00010000000000000000000000000000
bin=01101,en=1,One_hot_cold=00000000000000000010000000000000
bin=00011,en=0,One_hot_cold=00000000000000000000000000000000
bin=00000,en=0,One_hot_cold=00000000000000000000000000000001
```

WAVEFORMS:-



SCHEMATIC:-



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