DAY-63

#100DAYSOFRTL

Aim:- Implementation of NEGATIVE EDGE DETECTOR using Verilog.

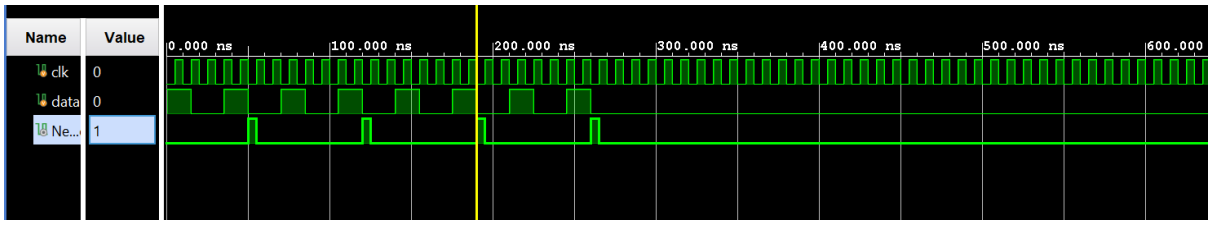
RTL CODE:-

```
////DATE:-03/03/2024
////DAY-63
////Implementation of NEGATIVE EDGE DETECTOR
module Day_63(input clk,data,
output NegativeDetector);
reg data_d;
always @(posedge clk) begin
data_d<=data;
end
assign NegativeDetector=(~data)&(data_d);
endmodule
```

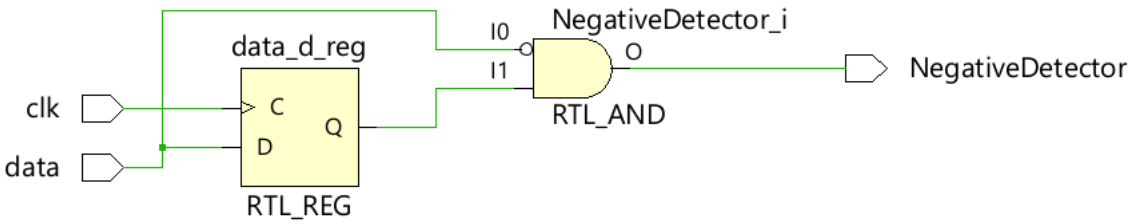
TESTBENCH:-

```
module Day_63_tb();
reg clk;
reg data;
wire NegativeDetector;
Day_63 uut(clk,data,NegativeDetector);
always #5 clk=~clk;
initial clk=0;
initial begin
data=1;
#15; data=0;
#20;data=1;
#15;data=0;
#20; data=1;
#15;data=0;
#20;data=1;
#15; data=0;
#20;data=1;
#15;data=0;
#20; data=1;
#15;data=0;
#20;data=1;
#15; data=0;
#20;data=1;
#15;data=0;
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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