DAY-71

#100DAYSOFRTL

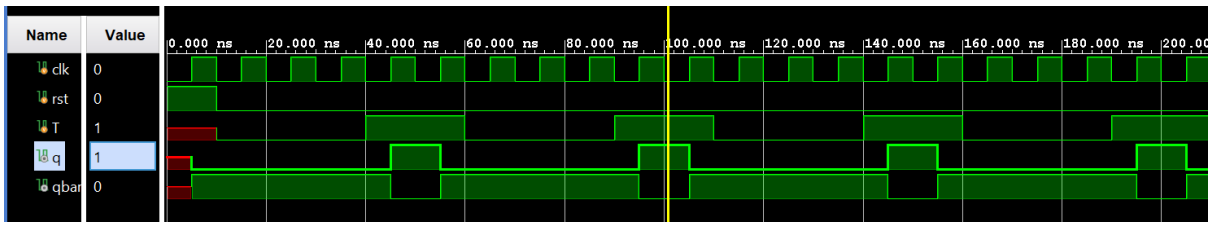
Aim:- Implementation of SR F/F TO T F/F using Verilog.

RTL CODE:-

```
////DATE:-11/03/2024
///DAY-71
///Implementation of SR FF TO T FF
module Day_71(input clk,rst,T,
output q,qbar );
wire w1,w2;
and g1(w1,T,qbar);
and g2(w2,T,q);
SRff SRFF(clk,rst,w1,w2,q,qbar);
endmodule

////SR Flipflop
module SRff(input clk,rst,S,R,
output reg q,
output qbar);
always@(posedge clk) begin
if(rst) q<=0;
else begin
case({S,R})
2'b00:q<=q; ////No change
2'b01:q<=0; ////reset
2'b10:q<=1; ////set
2'b11:q<=1'bx; ///Invalid inputs
endcase
end
end
assign qbar=~q;
endmodule
```

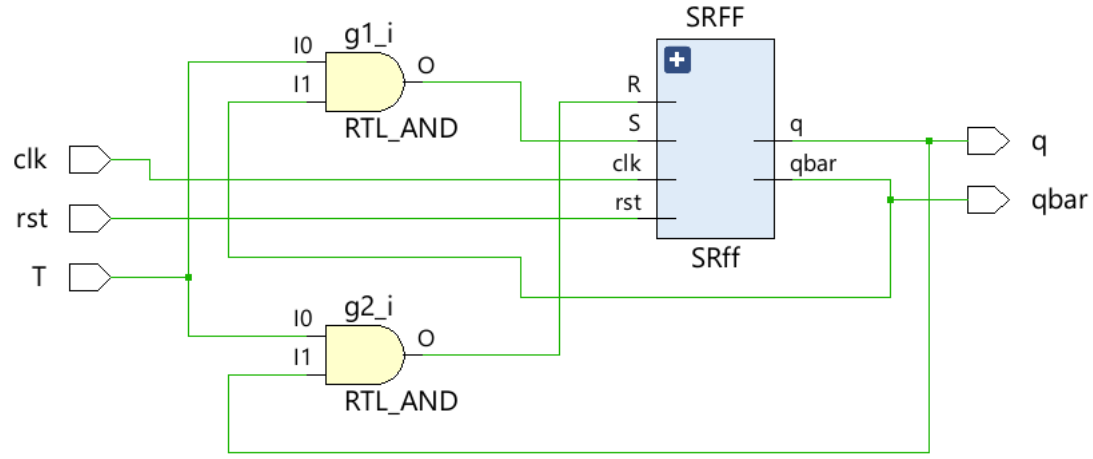
WAVEFORMS:-



TESTBENCH:-

```
module Day_71_tb();
reg clk,rst,T;
wire q,qbar;
Day_71 uut(clk,rst,T,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1;  #10;
rst=0;
T=0; #30;
T=1; #20;
T=0; #30;
T=1; #20;
T=0; #30;
T=1; #20;
T=0; #30;
T=1; #20;
$finish();
end
endmodule
```

SCHEMATIC:-



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