DAY-40

#100DAYSOFRTL

Aim:- Implementation of Clock Buffer.

Clock buffers have equal rise and falltime. This prevents the duty cycle of the clock signal from changing when it passes through a chain of clock buffers. Normal buffers are designed with a W/L ratio such that the sum of rise time and fall time is minimum. They too are having High Drive Strength.

RTL CODE:-

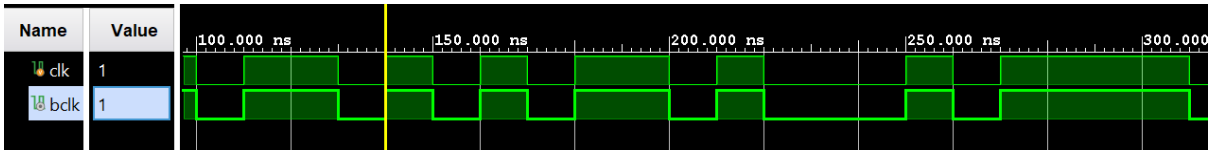
```
////Day-40
////Date:-09/02/2024
////Implementation of Clock Buffer in Verilog
////Clock buffers have equal rise and falltime.
//This prevents duty cycle of clock signal from
//changing when it passes through a chain of clock buffers.
module Clk_buffer(input clk,
output bclk);
buf b1(bclk,clk);
endmodule

```

TESTBENCH:-

```
module Clk_buffer_tb();
reg clk;
wire bclk;
Clk_buffer uut(clk,bclk);
initial begin
for(int i=0; i<20; i=i+1) begin
clk=$random();
#10;
end
end
initial begin
#1000;
$finish();
end
endmodule
```

SCHEMATIC:-

WAVEFORMS:-



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