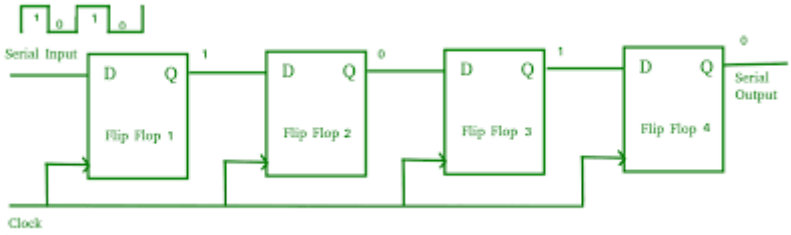
DAY-80

#100DAYSOFRTL

Aim:- Implementation of Serial-in Serial-Out Shift Register.



RTL CODE:-

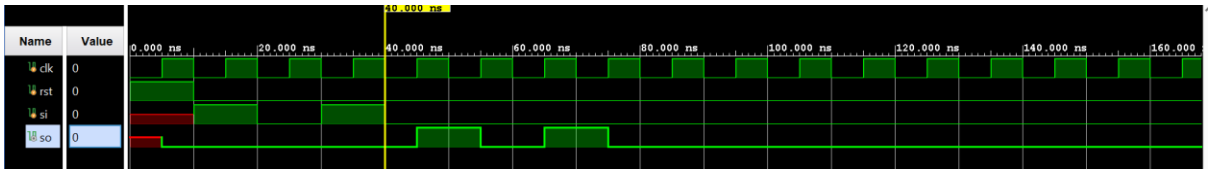
```
////DATE:-20/03/2024
///DAY-80
////Implementation of Serial-in Serial-Out
module Day_80(input clk,rst,si, output so);
wire [3:0] w;
dff DFF1(clk,rst,si,w[3]);
dff DFF2(clk,rst,w[3],w[2]);
dff DFF3(clk,rst,w[2],w[1]);
dff DFF4(clk,rst,w[1],w[0]);
assign so=w[0];
endmodule


module dff(input clk,rst,D,
output reg q);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(D)
1'b0:q=1'b0;
1'b1:q=1'b1;
endcase
end
end
endmodule
```

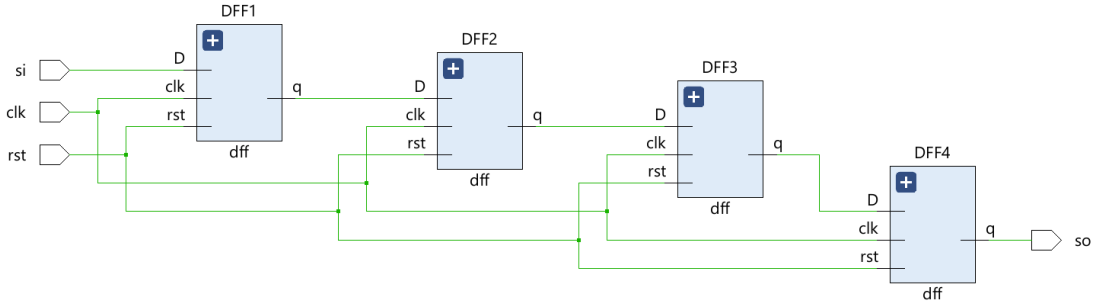
TESTBENCH:-

```
module Day_80_tb();
reg clk,rst,si;
wire so;
Day_80 uut(clk,rst,si,so);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
si=1; #10;
si=0; #10;
si=1; #10;
si=0; #10;
#200;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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