DAY-20

#100DAYSOFRTL

Aim:- Implementation of 2x1 Mux using Verilog.

RTL CODE:-

```
////DATE:-20/01/2024
////Implementation of 2X1 MUX
////Gate level Modelling
/*module Mux_2x1(input [1:0]A,
input Sel,output y);
wire [1:0] w;
and g1(w[0],A[0],(~Sel));
and g2(w[1],A[1],Sel);
or g3(y,w[0],w[1]);
endmodule*/
module Mux_2x1(input [1:0] A,
input Sel, output y);
assign y=Sel?A[1]:A[0];
endmodule
```

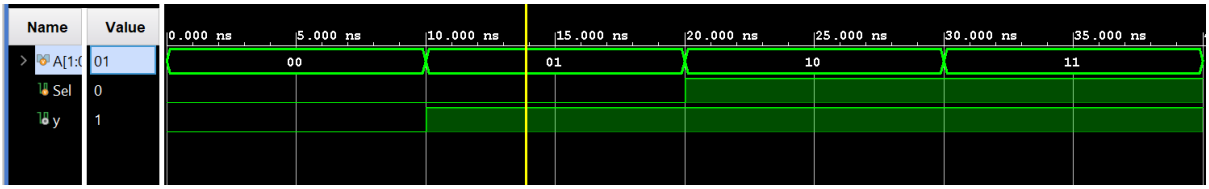
TESTBENCH:-

```
module Mux_2x1_tb();
reg [1:0] A;
reg Sel;
wire y;
Mux_2x1 uut(A,Sel,y);
initial begin
A=2'b00; Sel=0;
#10;
$display("A=%b,Sel=%b,y=%b",A,Sel,y);
A=2'b01; Sel=0;
#10;
$display("A=%b,Sel=%b,y=%b",A,Sel,y);
A=2'b10; Sel=1;
#10;
$display("A=%b,Sel=%b,y=%b",A,Sel,y);
A=2'b11; Sel=1;
#10;
$display("A=%b,Sel=%b,y=%b",A,Sel,y);
$finish();
end
endmodule
```

OUTPUT:-

```
A=00,Sel=0,y=0
A=01,Sel=0,y=1
A=10,Sel=1,y=1
A=11,Sel=1,y=1
```

WAVEFORMS:-



SCHEMATIC:-