DAY-41

#100DAYSOFRTL

Aim:- Implementation of Binary to Gray Conversion using Verilog.

RTL CODE:-

```
////DAY-41
////DATE:-10/02/2024
////Implementation of Binary to Gray Converter
module BtoG(input [4:0] A,
output [4:0] B);
//wire w1,w2,w3,w4;
assign B[4]=A[4];
assign B[3]=A[4]^A[3];
assign B[2]=A[3]^A[2];
assign B[1]=A[2]^A[1];
assign B[0]=A[1]^A[0];
endmodule
```

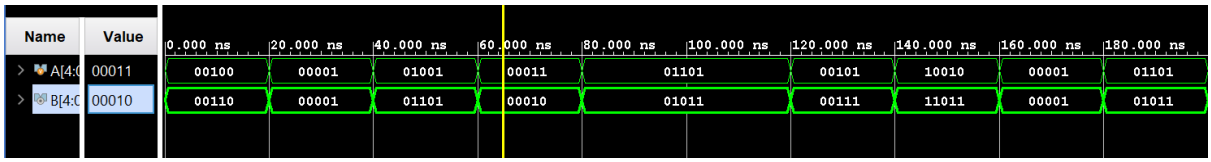
TESTBENCH:-

```
module BtoG_tb();
reg [4:0] A;
wire [4:0] B;
BtoG uut(A,B);
initial begin
for(int i=0; i<10; i=i+1) begin
A=$random();
#10;
$display("A=%b,B=%b",A,B);
#10;
end
end
initial begin
#200;
$finish();
end
endmodule
```

OUTPUT:-

```
A=00100,B=00110
A=00001,B=00001
A=01001,B=01101
A=00011,B=00010
A=01101,B=01011
A=01101,B=01011
A=00101,B=00111
A=10010,B=11011
A=00001,B=00001
A=01101,B=01011
```

WAVEFORMS:-



SCHEMATIC:-