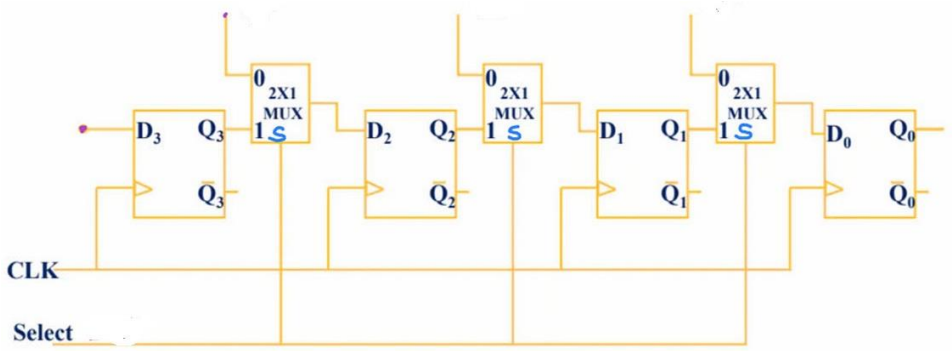
DAY-84

#100DAYSOFRTL

Aim:- Implementation of Parallel-in Serial-Out Shift Register.



RTL CODE:-

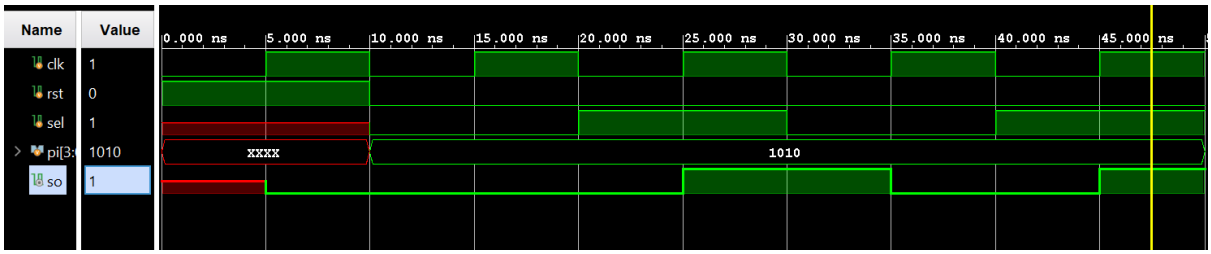
```
////DATE:-24/03/2024
////DAY-84
////Implementation of Parallel-in Serial-Out
module Day_84(input clk,rst,sel,
input [3:0] pi, output so);
wire [5:0] w;
dFF D1(clk,rst,pi[3],w[5]);
dFF D2(clk,rst,w[4],w[3]);
dFF D3(clk,rst,w[2],w[1]);
dFF D4(clk,rst,w[0],so);
mux_2x1 D5(w[5],pi[2],sel,w[4]);
mux_2x1 D6(w[3],pi[1],sel,w[2]);
mux_2x1 D7(w[1],pi[0],sel,w[0]);
endmodule

module dFF(input clk,rst,D,
output reg q);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(D)
1'b0:q<=0;
1'b1:q<=1;
endcase
end
end
endmodule

module mux_2x1(input i0,i1,sel,
output  reg y);
```

```
always @(*) begin
if(sel) begin
y=i0;
end
else begin
y=i1;
end
end
endmodule
```

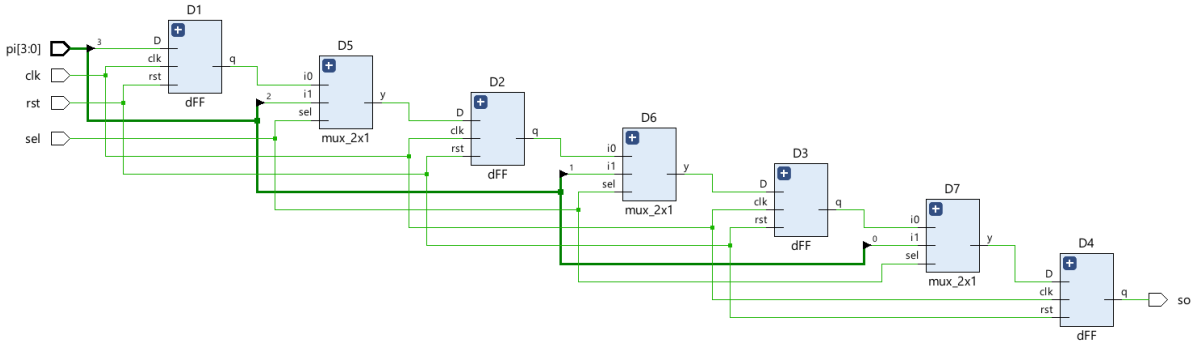
WAVEFORMS:-



TESTBENCH:-

```
module Day_84_tb();
reg clk,rst,sel;
reg [3:0] pi;
wire so;
Day_84 uut(clk,rst,sel,pi,so);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
sel=0;
pi=4'b1010;
#10;
sel=1;
pi=4'b1010;
#10;
sel=0;
pi=4'b1010;
#10;
sel=1;
pi=4'b1010;
#10;
$finish;
end
endmodule
```

SCHEMATIC:-


pi[3:0]
clk
rst
sel
D1
dFF
D5
mux_2x1
D2
dFF
D6
mux_2x1
D3
dFF
D7
mux_2x1
D4
dFF
so

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