DAY-75

#100DAYSOFRTL

Aim:- Implementation of 16-BIT DEPTH SYNCHRONOUS FIFO(First-in First-out).

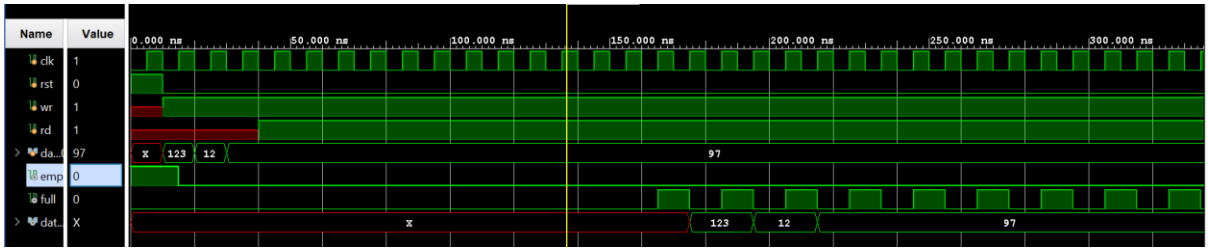
RTL CODE:-

```
////DATE:-15/03/2024
/////DAY-75
/////Implementation of 16 BIT FIFO
module Day_75(input clk,rst,wr,rd,
input [7:0] data_in, output empty,full,
output reg [7:0] data_out);
reg [3:0] wptr,rptr=0;
reg [4:0] cnt=0;
reg [7:0] mem[15:0] ;
always @(posedge clk) begin
if(rst==1'b1)
begin
wptr<=0;
rptr<=0;
cnt<=0;
end
else if(wr && (!full))
begin
mem[wptr]<=data_in;
wptr<=wptr+1;
cnt<=cnt+1;
end
else if(rd && (!empty))
begin
data_out<=mem[rptr];
rptr<=rptr+1;
cnt<=cnt-1;
end
end
assign empty=(cnt==0)?1'b1:1'b0;
assign full=(cnt==16)?1'b1:1'b0;
endmodule
```

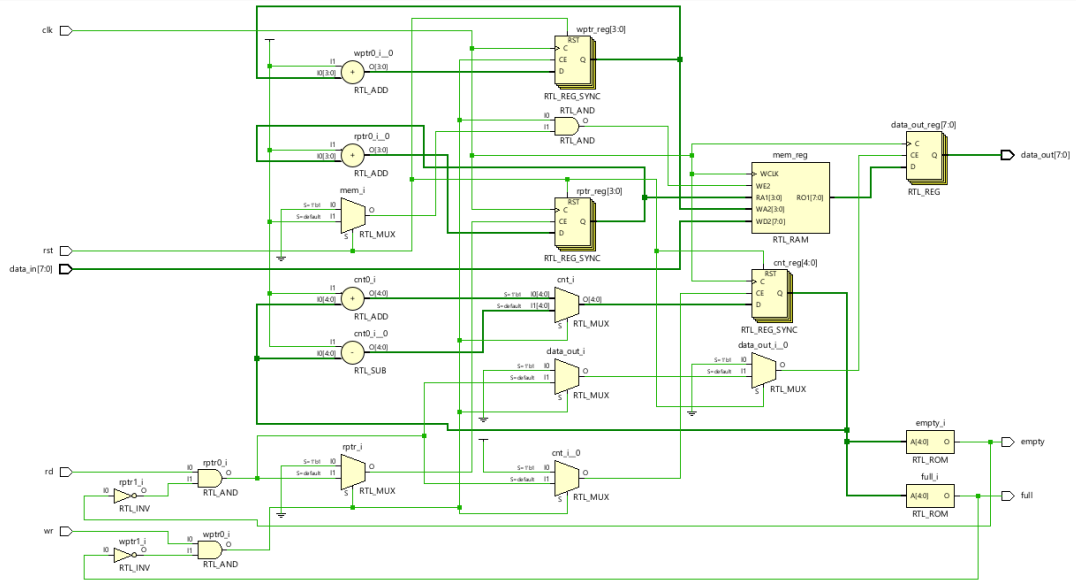
TESTBENCH:-

```
module Day_75_tb();
reg clk,rst,wr,rd;
reg [7:0] data_in;
wire empty,full;
wire [7:0] data_out;
Day_75 uut(clk,rst,wr,rd,data_in,empty,full,data_out);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1;
#10;
rst=0;
wr=1; /////Testing for write data
data_in=8'd123;
#10;
wr=1; /////Testing for write data
data_in=8'd12;
#10;
wr=1; /////Testing for write data
data_in=8'd97;
#10;
rd=1;
//rd=1;
#300;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-


clk
rst
data_in[7:0]
rd
wr
wptr_reg[3:0]
wptr0_i__0
RTL_ADD
RTL_REG_SYNC
RTL_AND
rptr0_i__0
RTL_ADD
mem_i
RTL_MUX
rptr_reg[3:0]
RTL_REG_SYNC
mem_reg
WCLK
WE2
RA1[3:0]
WA2[3:0]
WD2[7:0]
RO1[7:0]
RTL_RAM
data_out_reg[7:0]
RTL_REG
data_out[7:0]
cnt0_i
RTL_ADD
cnt_i
RTL_MUX
cnt_reg[4:0]
RTL_REG_SYNC
cnt0_i__0
RTL_SUB
data_out_i
RTL_MUX
data_out_i__0
RTL_MUX
empty_i
RTL_ROM
empty
full_i
RTL_ROM
full
rptr0_i
RTL_AND
rptr1_i
RTL_INV
rptr_i
RTL_MUX
cnt_i__0
RTL_MUX
wptr1_i
RTL_INV
wptr0_i
RTL_AND

==========