DAY-38

#100DAYSOFRTL

Aim:- Implementation of 8:3 Priority Encoder.

RTL CODE:-

```verilog
///Day-38
////DATE:-07/02/2024
////Implementation of Priority Encoder
module Encoder1_8x3(input [7:0] A,
output reg [2:0] Y);
always @(*) begin
casex(A)
8'b00000001:Y=3'b000;
8'b0000001x:Y=3'b001;
8'b000001xx:Y=3'b010;
8'b00001xxx:Y=3'b011;
8'b0001xxxx:Y=3'b100;
8'b001xxxxx:Y=3'b101;
8'b01xxxxxx:Y=3'b110;
8'b1xxxxxxx:Y=3'b111;
default: begin end
endcase
end
endmodule
```

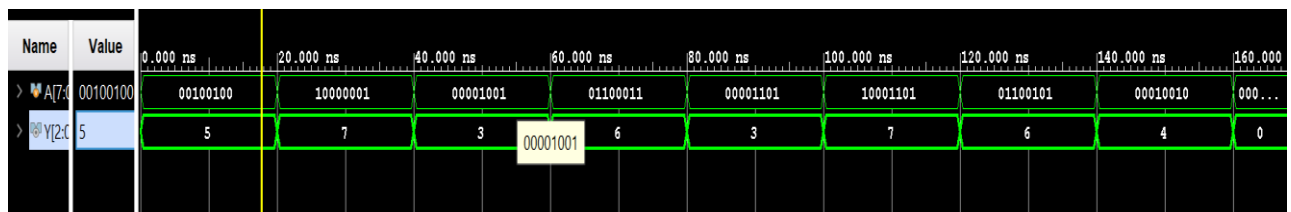## TESTBENCH:-

```verilog
module Enc_tb();
reg [7:0] A;
wire [2:0] Y;
Encoder1_8x3 uut(A,Y);
initial begin
for(int i=0; i<20; i=i+1) begin
A=$random();
#10;
$display("A=%b,Y=%d",A,Y);
#10;
end
end
initial begin
#250;
$finish();
end
endmodule
```
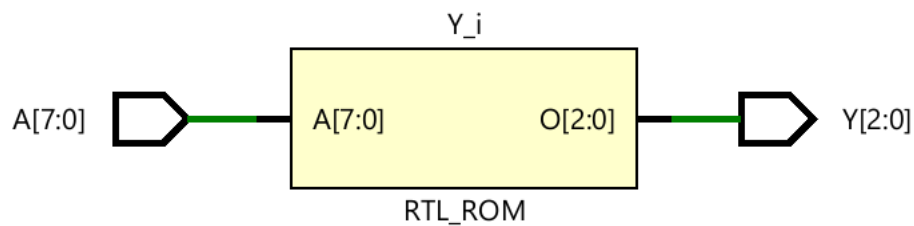
OUTPUT:-

```
A=00100100,Y=5
A=10000001,Y=7
A=00001001,Y=3
A=01100011,Y=6
A=00001101,Y=3
A=10001101,Y=7
A=01100101,Y=6
A=00010010,Y=4
A=00000001,Y=0
A=00001101,Y=3
A=01110110,Y=6
A=00111101,Y=5
```

WAVEFORMS:-

Name	Value	0.000 ns	20.000 ns	40.000 ns	60.000 ns	80.000 ns	100.000 ns	120.000 ns	140.000 ns	160.000
A[7:0	00100100	00100100	10000001	00001001	01100011	00001101	10001101	01100101	00010010	000...
Y[2:0	5	5	7	3	00001001 6	3	7	6	4	0

SCHEMATIC:-

Y_i

A[7:0] → A[7:0] O[2:0] → Y[2:0]

RTL_ROM

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