DAY-68

#100DAYSOFRTL

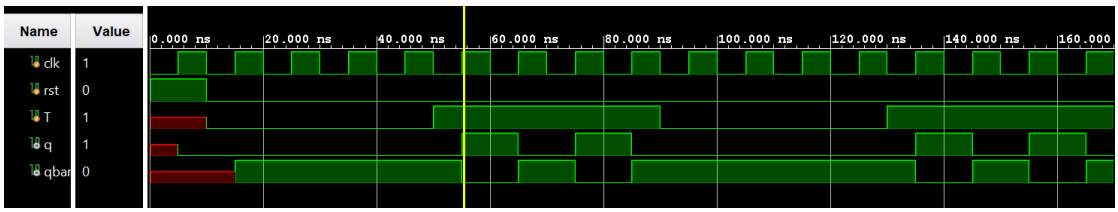
Aim:- Implementation of D F/F TO T F/F using Verilog.

RTL CODE:-

```
////DATE:-08/03/2024
///DAY-68
////Implementation of D f/f to T f/f
module Day_68(input clk,rst,T,
output  q,output qbar);
wire [3:0] w;
not g1(w[0],T);
and g2(w[1],T,qbar);
and g3(w[2],w[0],q);
or g4(w[3],w[1],w[2]);
////instantiation d flipflop
dff Dff(.clk(clk),.rst(rst),.D(w[3]),.q(q),.qbar(qbar));
endmodule


module dff(input clk,rst,D,
output reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0;
end
else begin
case(D)
1'b0:{q,qbar}={1'b0,1'b1};
1'b1:{q,qbar}={1'b1,1'b0};
endcase
end
end
endmodule
```

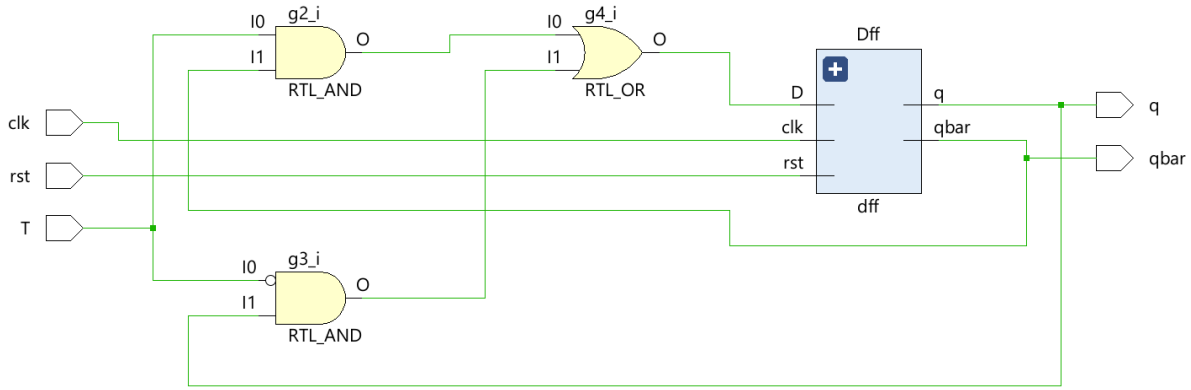
WAVEFORMS:-



TESTBENCH:-

```
module Day_68_tb();
reg clk,rst,T;
wire q,qbar;
Day_68 uut(clk,rst,T,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
T=1'b0; #40;
T=1'b1; #40;
T=1'b0; #40;
T=1'b1; #40;
$finish();
end
endmodule
```

SCHEMATIC:-



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