

DAY-46 #100DAYSOFRTL

Aim:- Implementation of SR Flipflop using Verilog.

RTL CODE:-

```
1 🖯 ///DAY-46
    ///Date:-15/02/2024
3 	☐ ///Implementation of SR FlipFlop
4 Dmodule Day_46(input S,R, rst,clk,
5 output reg q,qbar);
6 always @(posedge clk) begin
7 ⊕ if(rst) begin
8 | q<=0; qbar<=1;
9 🖨 end
12 2'b00:{q,qbar}<={q,qbar};
13
    2'b01:{q,qbar}<={1'b0,1'b1};
   2'b10:{q,qbar}<={1'b1,1'b0};
14
15 | 2'b11:{q,qbar}<={1'bx,1'bx};
16 default: begin end
17 \bigcirc endcase
18 A end
19 🖒 end
20 🖨 endmodule
21
```

TESTBENCH:-

```
1 module Day 46 tb();
2 reg S,R,rst,clk;
 3 | wire q,qbar;
 4 Day 46 uut(S,R,rst,clk,q,qbar);
 5 | always #5 clk=~clk;
 6 | initial clk=0;
7 🖯 initial begin
8 rst=1; #10;
9 | rst=0;
10 ¦
    {S,R}=2'b00; #10;
11
   $display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
    {S,R}=2'b01; #10;
    $display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
    {S,R}=2'b10; #10;
15 | $display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
    {S,R}=2'b11; #10;
17 | $\display("S=\b,R=\b,q=\b,qbar=\b",S,R,q,qbar);
18 | $finish();
19 🖒 end
20 endmodule
```

OUTPUT:-

S=0,R=0,q=0,qbar=1 S=0,R=1,q=0,qbar=1 S=1,R=0,q=1,qbar=0 S=1,R=1,q=x,qbar=x

WAVEFORMS:-

Name	Value	0.000 ns	5.000 ns	10.000 ns	15.000 ns	20.000 ns	25.000 ns	30.000 ns	35.000 ns	40.000 ns	45,000 ns 5
ሤ clk	0										
¼ rst	0										
₩s	0										
₩R	1										
1⊌ q	0										
¹⊌ qbar	1										

SCHEMATIC:-



