DAY-59

#100DAYSOFRTL

Aim:- Implementation of BCD TO EXCESS-3 CODE using Verilog.

RTL CODE:-

```
////DATE:-28/02/2024
////DAY-59
////Implementation of BCD TO EXCESS-3 CODE
module Day_59(input [3:0]b,
output [3:0] y);
assign y[3]=b[3]|b[2]&b[1]|b[2]&b[0];
assign y[2]=(~b[2])&b[1]|(~b[2])&b[0]|b[2]&(~b[1])&(~b[0]);
assign y[1]=b[1]&b[0]|(~b[1])&(~b[0]);
assign y[0]=(~b[0]);
endmodule
```

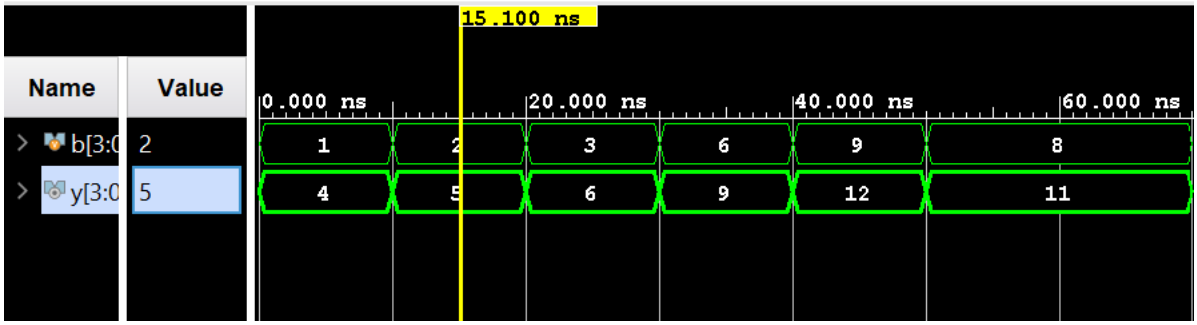
TESTBENCH:-

```
module Day_59_Tb();
reg [3:0] b;
wire [3:0] y;
Day_59 uut(b,y);
initial begin
b=1;
#10;
$display("b=%d,y=%d",b,y);
b=2;
#10;
$display("b=%d,y=%d",b,y);
b=3;
#10;
$display("b=%d,y=%d",b,y);
b=6;
#10;
$display("b=%d,y=%d",b,y);
b=9;
#10;
$display("b=%d,y=%d",b,y);
b=8;
#10;
$display("b=%d,y=%d",b,y);
#10;
end
initial begin
#70;
$finish();
end
endmodule
```

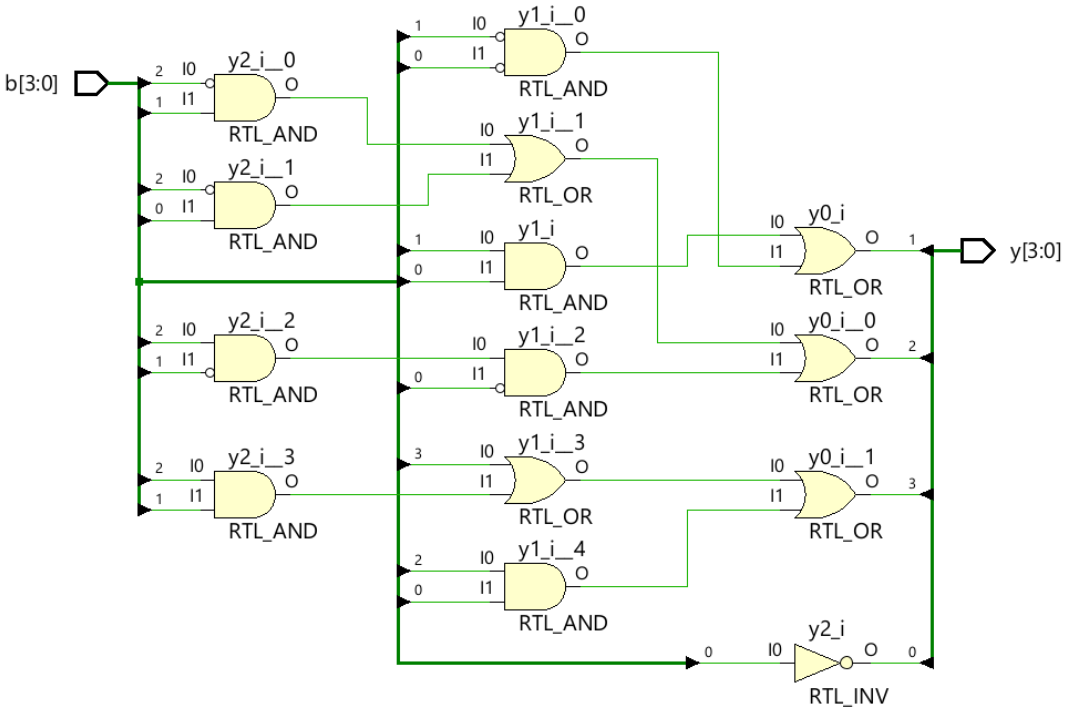
OUTPUT:-

```
b= 1,y= 4
b= 2,y= 5
b= 3,y= 6
b= 6,y= 9
b= 9,y=12
b= 8,y=11
```

WAVEFORMS:-



SCHEMATIC:-



==========