DAY-46

#100DAYSOFRTL

Aim:- Implementation of SR Flipflop using Verilog.

RTL CODE:-

```
///DAY-46
///Date:-15/02/2024
///Implementation of SR FlipFlop
module Day_46(input S,R, rst,clk,
output reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0; qbar<=1;
end
else begin
case({S,R})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={1'b1,1'b0};
2'b11:{q,qbar}<={1'bx,1'bx};
default: begin end
endcase
end
end
endmodule

```

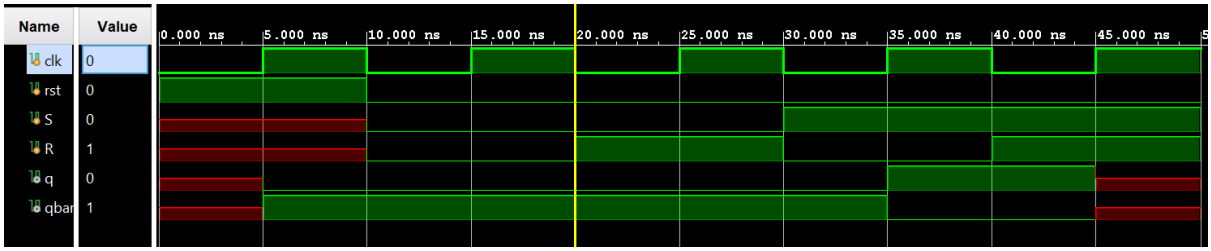
TESTBENCH:-

```
module Day_46_tb();
reg S,R,rst,clk;
wire q,qbar;
Day_46 uut(S,R,rst,clk,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
{S,R}=2'b00; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b01; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b10; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
{S,R}=2'b11; #10;
$display("S=%b,R=%b,q=%b,qbar=%b",S,R,q,qbar);
$finish();
end
endmodule
```

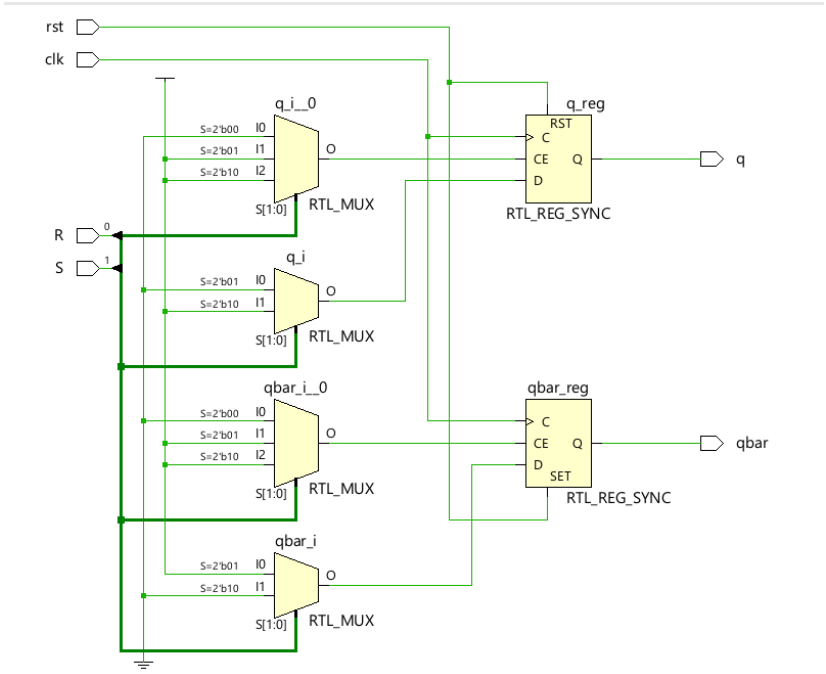
OUTPUT:-

```
S=0,R=0,q=0,qbar=1
S=0,R=1,q=0,qbar=1
S=1,R=0,q=1,qbar=0
S=1,R=1,q=x,qbar=x
```

WAVEFORMS:-



SCHEMATIC:-



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