DAY-94

#100DAYSOFRTL

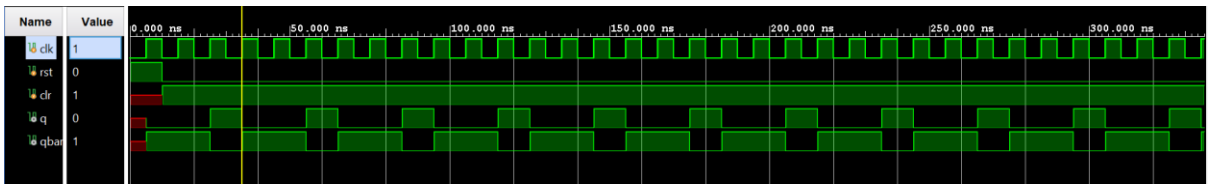
Aim:- Implementation of Implementation of Clock Divider by 3.

RTL CODE:-

```
////DATE:-03/04/2024
////DAY-94
////Implementation of Clock divider by 3  (F/3).
module Day_94(input clk,rst,clr, output  q,qbar);
wire w2,w3;
assign clr=w2&&q;
dFF D1(clk,rst,clr,w2,w3);
dFF D2((~w2),rst,clr,q,qbar);
endmodule

module dFF(input clk,rst,clr, output reg q,
output qbar);
always @(clr) q<=0;
always@(posedge clk) begin
if(rst)
q<=0;
else begin
q<=qbar;
end
end
assign qbar=~q;
endmodule
```

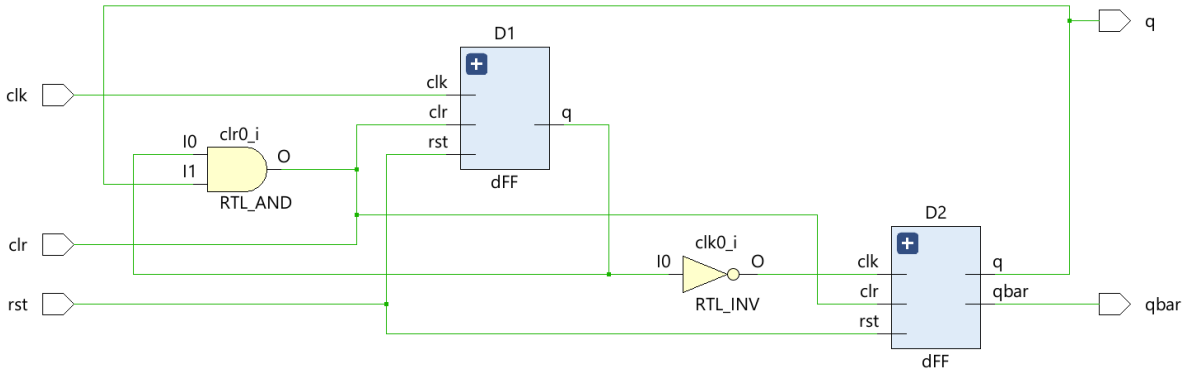
WAVEFORMS:-



TESTBENCH:-

```
module Day_94_tb();
reg clk,rst,clr;
wire q,qbar;
Day_94 uut(clk,rst,clr,q,qbar);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
clr=1; #10;
end
endmodule
```

SCHEMATIC:-



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