

# DAY-91 #100DAYSOFRTL

**Aim:-** Implementation of 4-BIT Ring Counter using Verilog HDL.

### **RTL CODE:-**

```
////DATE:-31/03/2024
///DAY-91

///Implementation of 4-BIT Ring Counter

module Day_91(input clk,rst, output [3:0] q);
reg [3:0] A;

always@(posedge clk) begin

if(rst)
A<=4'b0001;

else begin
A<=A<<1;
A[0]<=A[3];
end
end
assign q=A;
endmodule</pre>
```

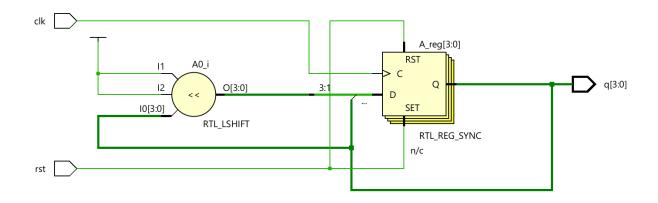
# **WAVEFORMS:-**

Name	Value	0.000 ns	P	0.000 ns		20.000 ns		30.000 ns		40.000 ns		50.000 ns		60.000 ns		70.000 ns		80.000 1
<sup>1</sup> dk	0																	
₩ rst	0																	
> ® q[3:0	0001	XXXX	000		0010		0100		1000		0001		0010		0100		1000	

#### **TESTBENCH:-**

```
module Day_91_tb();
reg clk,rst;
wire [3:0] q;
Day_91 uut(clk,rst,q);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
end
endmodule
```

## **SCHEMATIC:-**





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