DAY-65

#100DAYSOFRTL

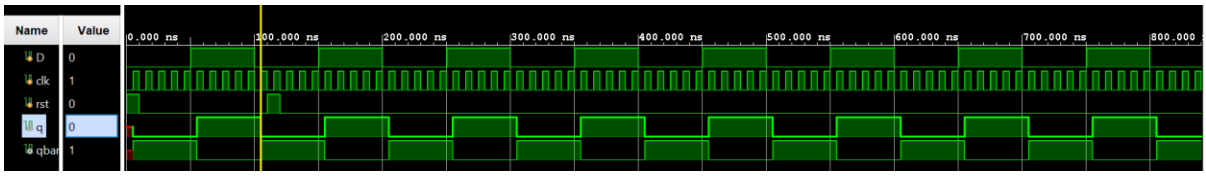
Aim:- Implementation of SR F/F TO D F/F using Verilog.

RTL CODE:-

```
////DATE:-05/03/2024
////DAY:-65
/////Implementation of SR flipflop to D flipflop
module srff_Dff(input D,clk,rst,output  q,qbar);
Day_46 srff(D,(~D),rst,clk,q,qbar);
endmodule

module Day_46(input S,R, rst,clk,
output reg q,qbar);
always @(posedge clk) begin
if(rst) begin
q<=0; qbar<=1;
end
else begin
case({S,R})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={1'b1,1'b0};
2'b11:{q,qbar}<={1'bx,1'bx};
default: begin end
endcase
end
end
endmodule
```

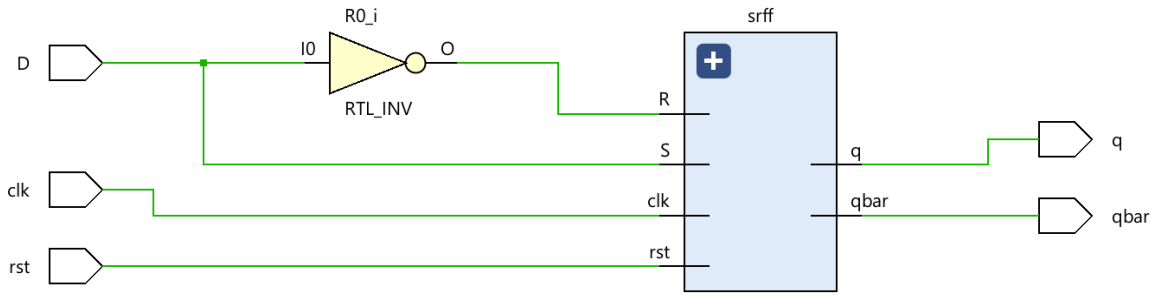
WAVEFORMS:-



TESTBENCH:-

```
module srff_Dff_tb();
reg D,clk,rst;
wire q,qbar;
srff_Dff uut(D,clk,rst,q,qbar);
always #5 clk=~clk;
always #50 D=~D;
initial clk=0;
initial begin
D=0;
rst=1;
#10;
rst=0; #100;
rst=1; #10;
rst=0;
end
endmodule
```

SCHEMATIC:-



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