DAY-62

#100DAYSOFRTL

Aim:- Implementation of POSITIVE EDGE DETECTOR using Verilog.

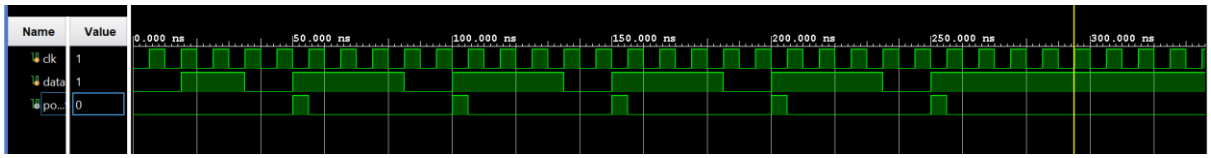
RTL CODE:-

```
////DATE:-02/03/2024
////DAY-62
/////Implementation of Posedge Detector
module Day_62(input clk,data,
output posedgeDetect);
reg data_d;
always @(posedge clk) begin
data_d<=data;
end
assign posedgeDetect = (data)&(~data_d);
endmodule
```

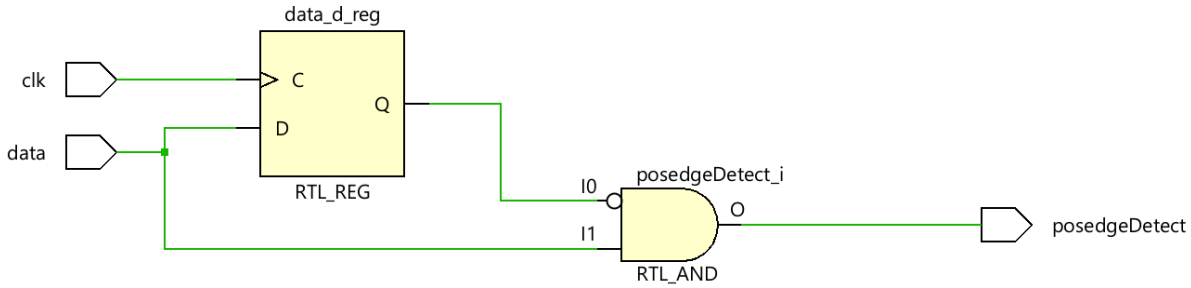
TESTBENCH:-

```
module Day_62_tb();
reg clk;
reg data;
wire posedgeDetect;
Day_62 uut(clk,data,posedgeDetect);
always #5 clk=~clk;
initial begin
clk=0;
data=0;
#15; data=1;
#20;data=0;
#15;data=1;
#15; data=1;
#20;data=0;
#15;data=1;
#15; data=1;
#20;data=0;
#15;data=1;
#15; data=1;
#20;data=0;
#15;data=1;
#15; data=1;
#20;data=0;
#15;data=1;
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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