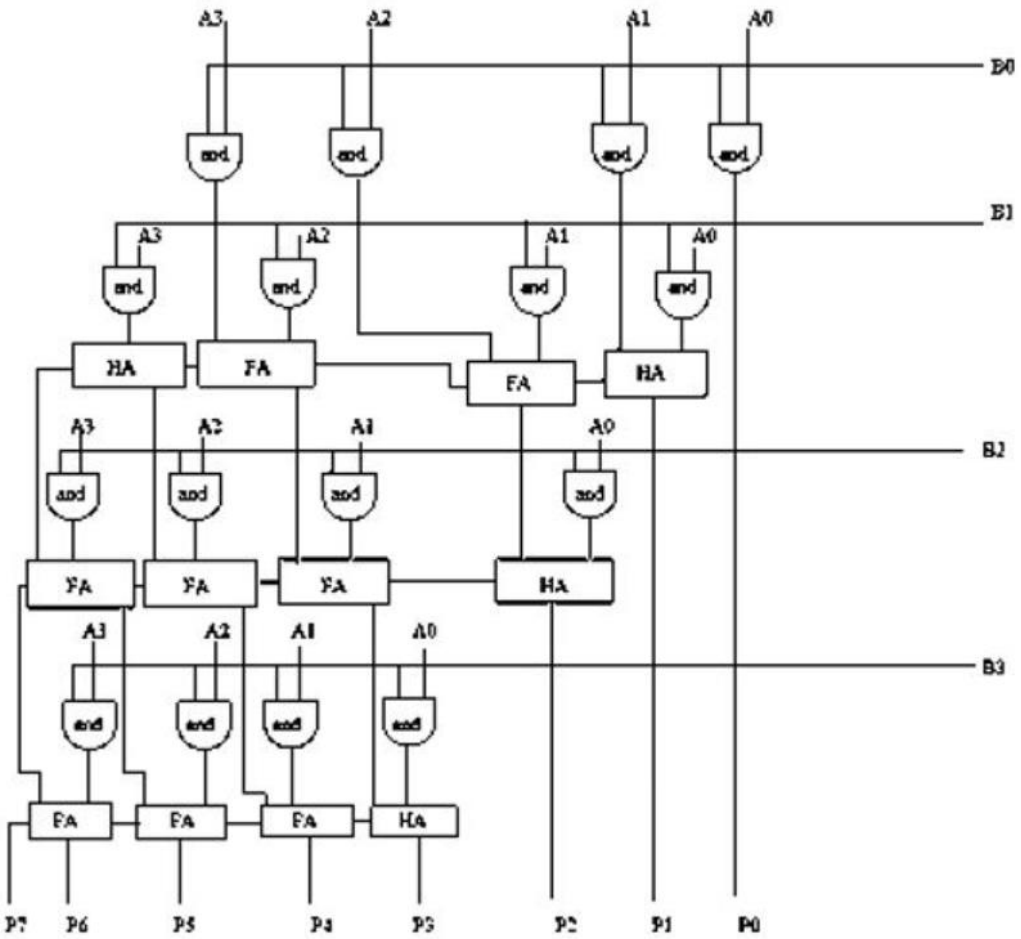
DAY-17

#100DAYSOFRTL

Aim:- Implementation of 4X4 BIT ARRAY MULTIPLIER IN GATE LEVEL MODELLING

BLOCK DIAGRAM:-



RTL CODE:-

```
////DATE:-17/01/2024
////Implementation of 4X4 BIT Multiplier
module HalfADDER(input A,B,
output S,C);
assign S=A^B;
assign C=A&B;
endmodule

module Fa(input A,B,Cin,
output Sum,Cout);
assign Sum=A^B^Cin;
assign Cout=A&B|B&Cin|Cin&A;
endmodule

module Mul(input [3:0] A,B,
output [7:0] P);
wire [15:0]W;
wire [11:0]I;
wire [5:0] F;
and g1(P[0],A[0],B[0]);
and g2(W[0],A[1],B[0]);
and g3(W[1],A[2],B[0]);
and g4(W[2],A[3],B[0]);

and g5(W[3],A[0],B[1]);
and g6(W[4],A[1],B[1]);
and g7(W[5],A[2],B[1]);
and g8(W[6],A[3],B[1]);

and g9(W[7],A[0],B[2]);
and g10(W[8],A[1],B[2]);
and g11(W[9],A[2],B[2]);

and g12(W[10],A[3],B[2]);

and g13(W[11],A[0],B[3]);
and g14(W[12],A[1],B[3]);
and g15(W[13],A[2],B[3]);
and g16(W[14],A[3],B[3]);

HalfADDER K1(W[0],W[3],P[1],I[0]);
Fa K2(W[1],W[4],I[0],F[0],I[1]);
Fa K3(W[2],W[5],I[1],F[1],I[2]);
HalfADDER K4(W[6],I[2],F[2],I[3]);

HalfADDER K5(W[7],F[0],P[2],I[4]);
Fa K6(W[8],F[1],I[4],F[3],I[5]);
Fa K7(W[9],F[2],I[5],F[4],I[6]);
Fa K8(W[10],I[3],I[6],F[5],I[7]);

HalfADDER K9(W[11],F[3],P[3],I[8]);
Fa K10(W[12],F[4],I[8],P[4],I[9]);
Fa K11(W[13],F[5],I[9],P[5],I[10]);
Fa K12(W[14],I[7],I[10],P[6],P[7]);

endmodule
```

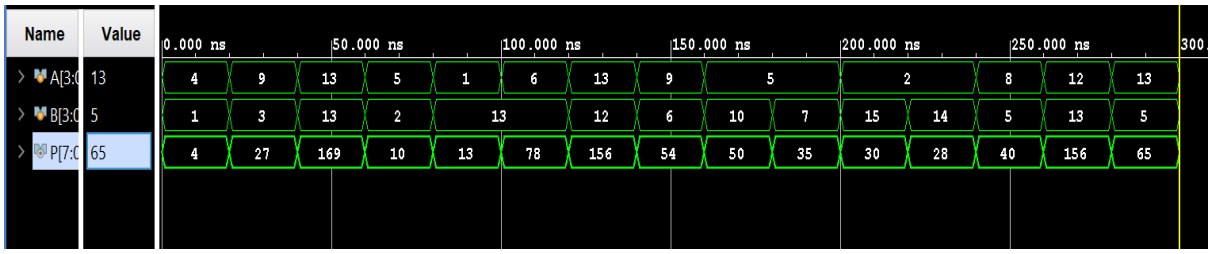
TESTBENCH:-

```
module Mul_tb();
reg [3:0] A,B;
wire [7:0] P;
Mul uut(A,B,P);
initial begin
for(integer i=0; i<16; i=i+1) begin
A=$random();
B=$random();
#10;
$display("A=%d,B=%d,P=%d",A,B,P);
#10;
end
end
initial begin
#300;
$finish();
end
endmodule
```

OUTPUT:-

```
A= 4,B= 1,P=  4
A= 9,B= 3,P= 27
A=13,B=13,P=169
A= 5,B= 2,P= 10
A= 1,B=13,P= 13
A= 6,B=13,P= 78
A=13,B=12,P=156
A= 9,B= 6,P= 54
A= 5,B=10,P= 50
A= 5,B= 7,P= 35
A= 2,B=15,P= 30
A= 2,B=14,P= 28
A= 8,B= 5,P= 40
A=12,B=13,P=156
A=13,B= 5,P= 65
```

WAVEFORMS:-



SCHEMATIC:-