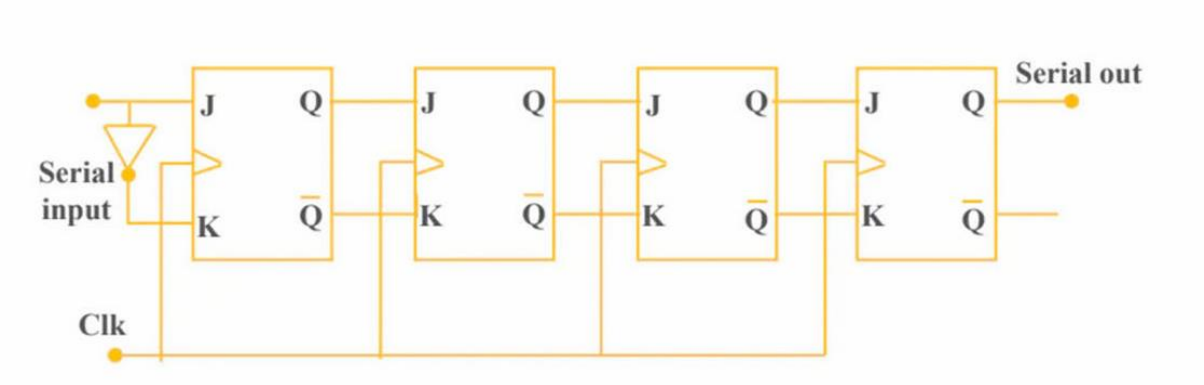
DAY-81

#100DAYSOFRTL

Aim:- Implementation of Serial-in Serial-Out Shift Register Using JK Flip-Flop



RTL CODE:-

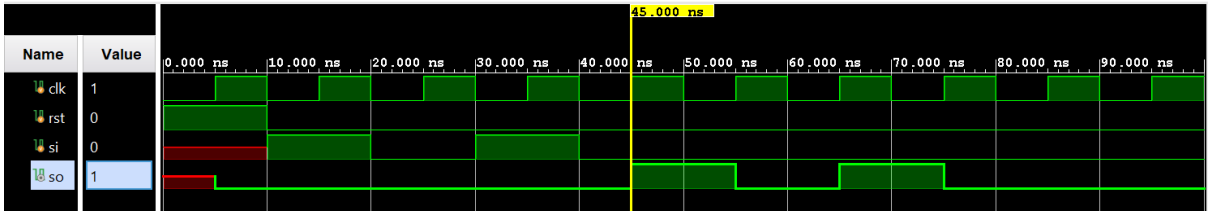
```
////DATE:-21/03/2024
////DAY-81
/////////Implementation of Serial-in Serial Out using JK FF
module Day_81(input clk,rst,si, output so);
wire [2:0] q;
wire [3:0] qb;
wire w1;
not g1(w1,si);
JKFf M1(clk,rst,si,w1,q[2],qb[3]);
JKFf M2(clk,rst,q[2],qb[3],q[1],qb[2]);
JKFf M3(clk,rst,q[1],qb[2],q[0],qb[1]);
JKFf M4(clk,rst,q[0],qb[1],so,qb[0]);
endmodule

module JKFf(input clk,rst,J,K,
output reg q, qbar);
always@(posedge clk) begin
if(rst) begin
q<=0;
qbar<=1;
end
else begin
case({J,K})
2'b00:{q,qbar}<={q,qbar};
2'b01:{q,qbar}<={1'b0,1'b1};
2'b10:{q,qbar}<={1'b1,1'b0};
2'b11:{q,qbar}<={qbar,q};
default: begin end
endcase
end
end
endmodule
```

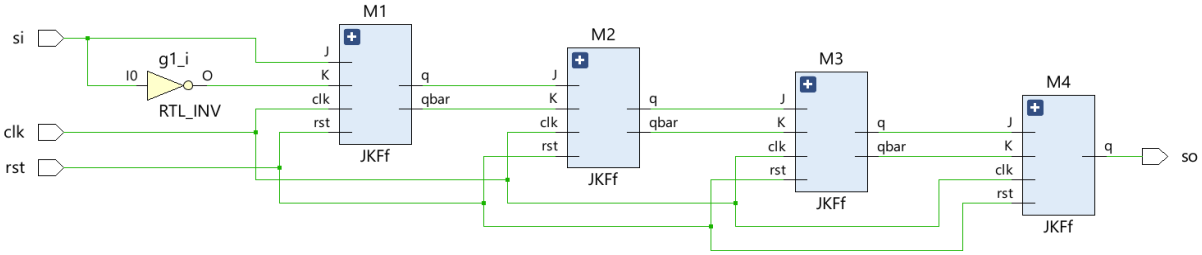
TESTBENCH:-

```
module Day_81_tb();
reg clk,rst,si;
wire so;
Day_81 uut(clk,rst,si,so);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
si=1; #10;
si=0; #10;
si=1; #10;
si=0; #10;
#50;
$finish();
end
endmodule
```

WAVEFORMS:-



SCHEMATIC:-



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