DAY-96

#100DAYSOFRTL

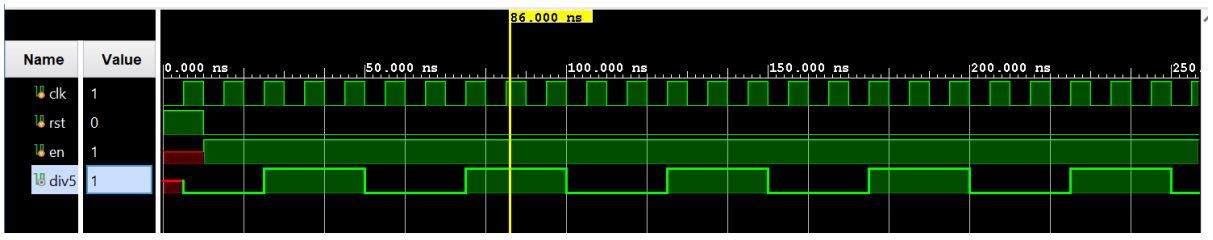
Aim:- Implementation of Clock Divider by 5(F/5).

RTL CODE:-

```
////DATE:-05/04/2024
///DAY-96
///Implementation of Frequency Divider by 5
module Day_96(input clk,rst,en, output div5);
wire w1;
reg [2:0] cnt;
always@(posedge clk) begin
if(rst)
cnt<=3'd0;
else if(en) begin
if(cnt==3'd4)
cnt<=0;
else
cnt<=cnt+1;
end
end
DFF dflipflop(clk,rst,cnt[1],w1);
or g1(div5,w1,cnt[1]);
endmodule

module DFF(input clk,rst, D, output reg q);
always @(negedge clk) begin
if(rst)
q<=0;
else begin
case(D)
1'b0:q<=0;
1'b1:q<=1;
endcase
end
end
endmodule
```

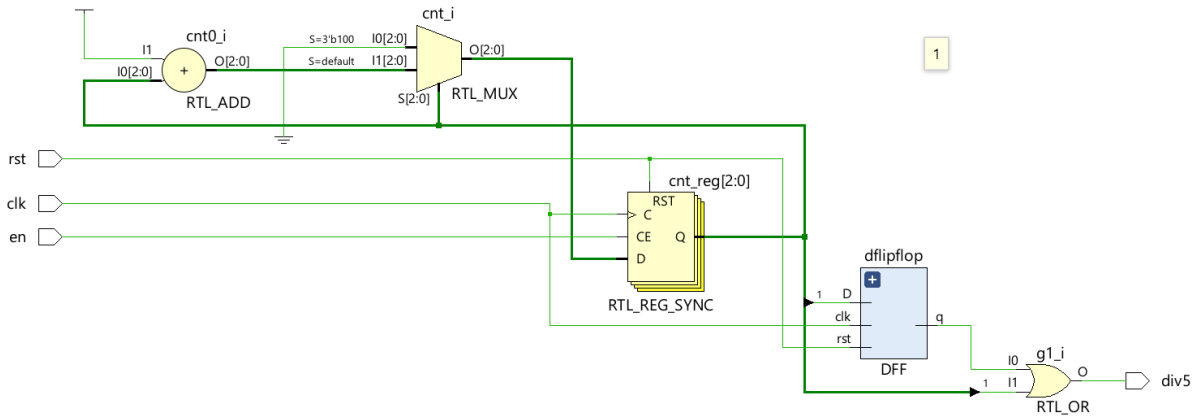
WAVEFORMS:-



TESTBENCH:-

```
module Day_96_tb();
reg clk,rst,en;
wire div5;
Day_96 uut(clk,rst,en,div5);
always #5 clk=~clk;
initial clk=0;
initial begin
rst=1; #10;
rst=0;
en=1;
end
endmodule
```

SCHEMATIC:-



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