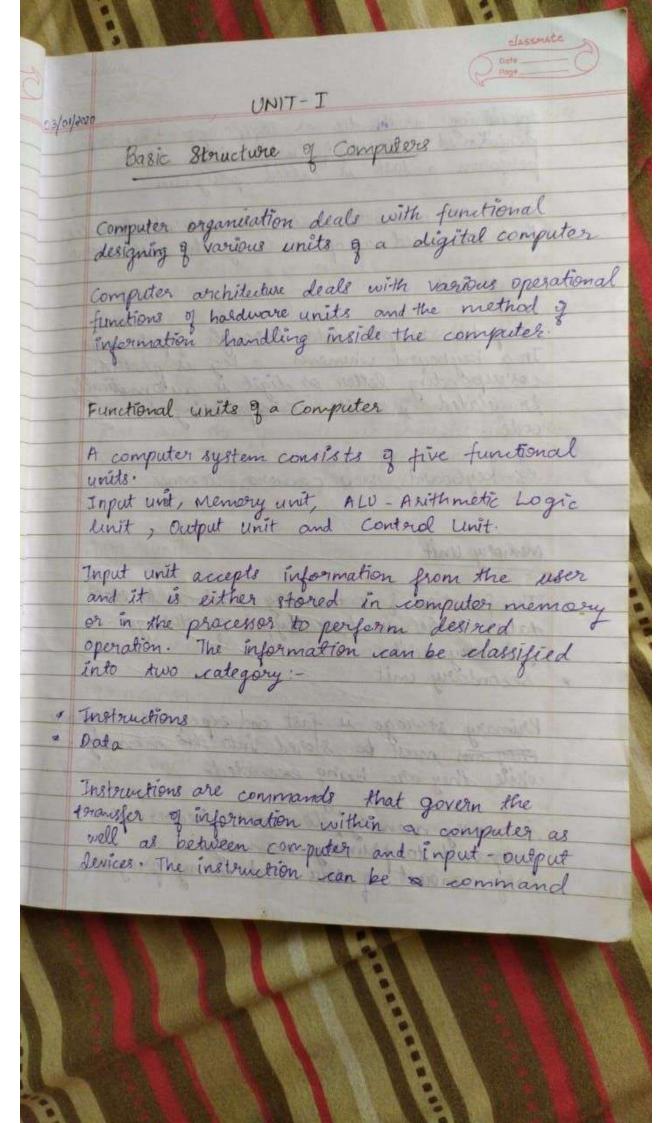


CLASSMATE Pipelining and Vector Processing

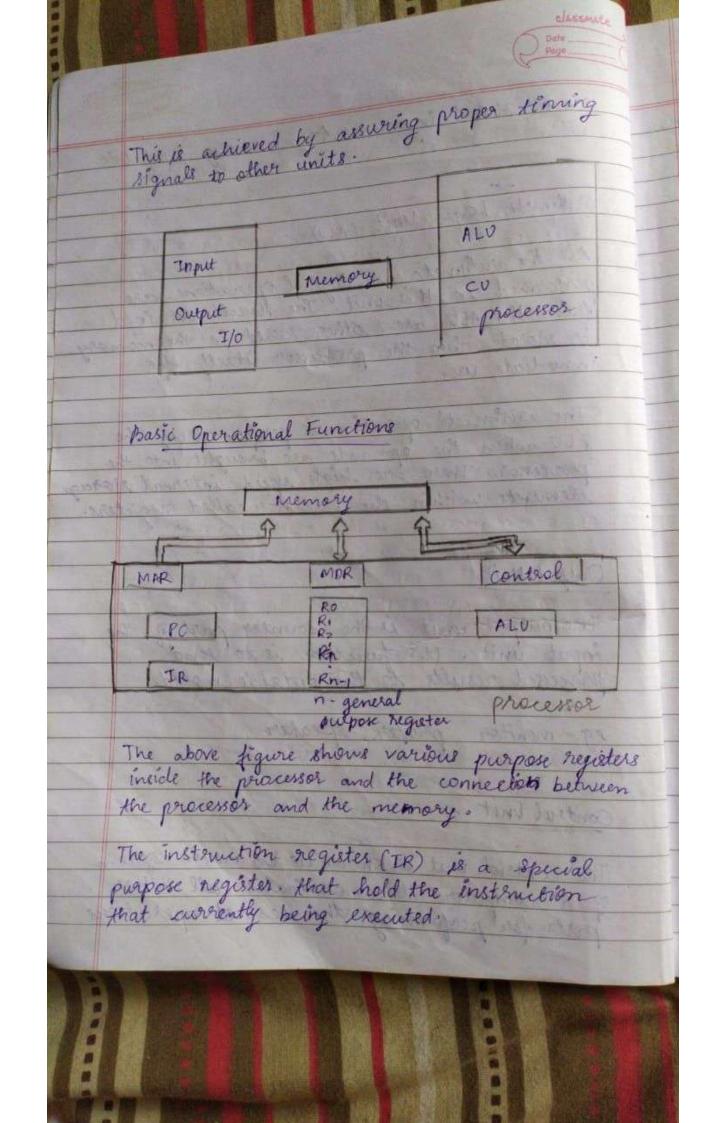
Introduction to pipelining, instruction and arithmetic pipelines, vector processing, array processors. Numer of Organization - Tropics wants was standard started - Sept. STATE TOWN

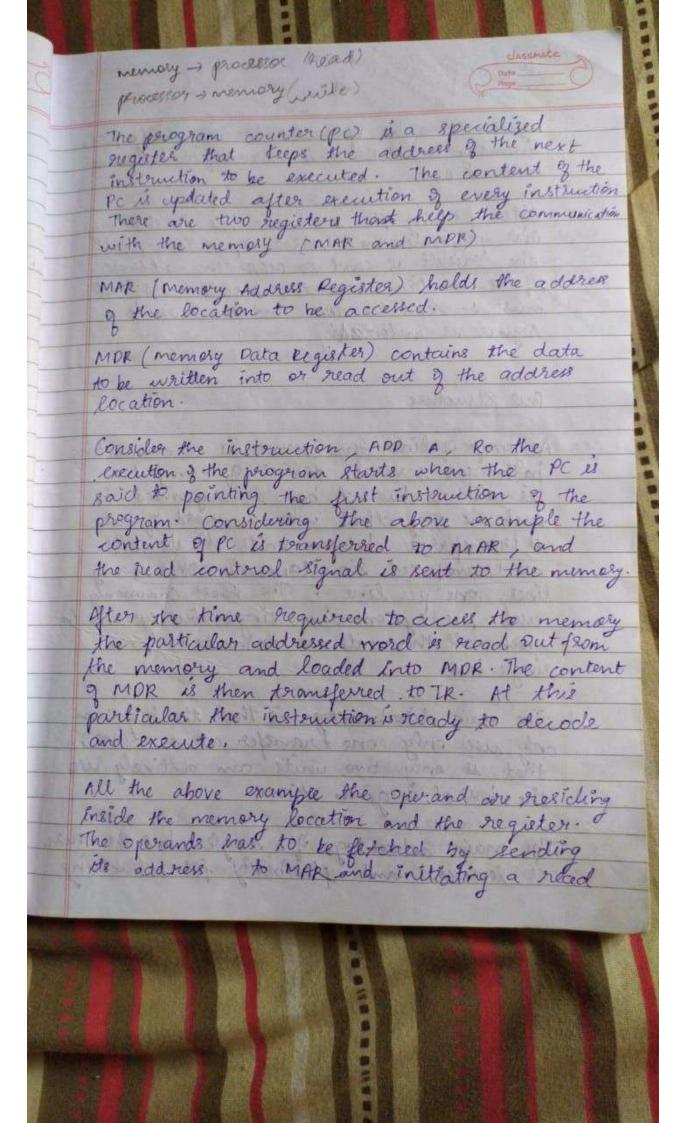


specifying arithmetic or logic operations to be performed. A set of instructions that perform a task is called program Pata are numbers and encountered character that are used as operands by the instructions. Input unit Compider accepts data through in act units.

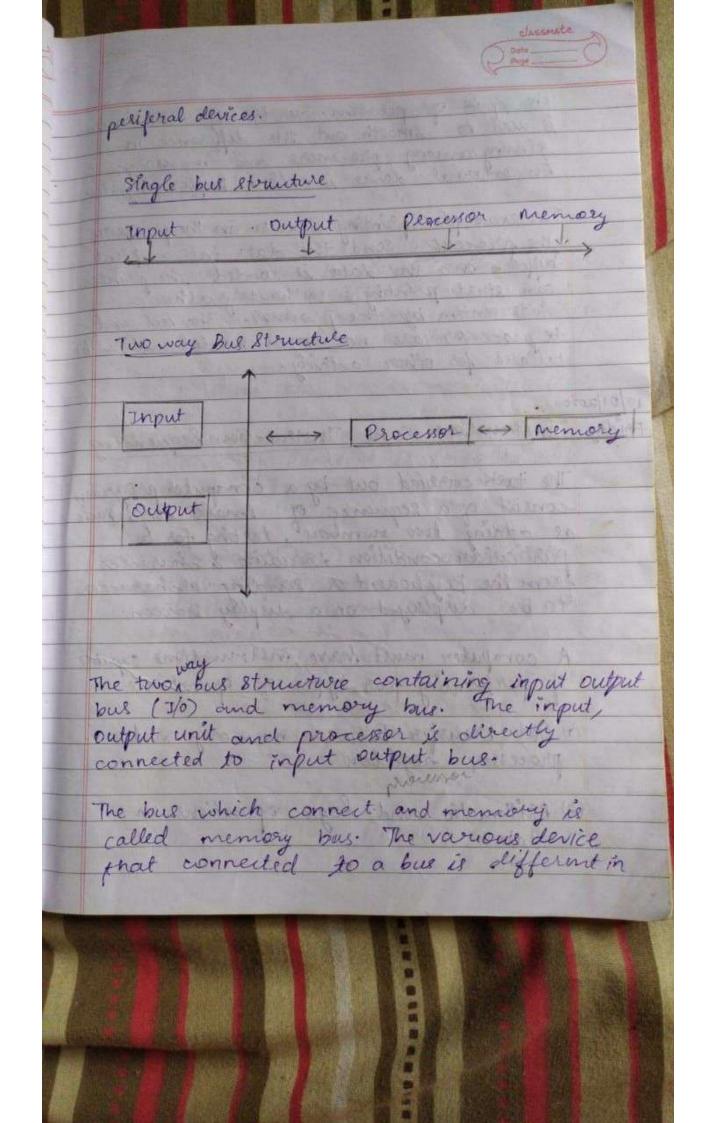
In a Keyboard whenever a key is pressed,
coverponding letter or digit is automatically
transladed into its corresponding binary
code. code eg:- keyboard, web carnera, scanner Memory unit The function of a memory unit is to store data. There are two stypes of storage: · primary unit Secondary unit Primary storage is fast and expensive. Programe white they are being executed. Secondary memory slow and cheaper as compared to primary memory. Large amount of data and many program

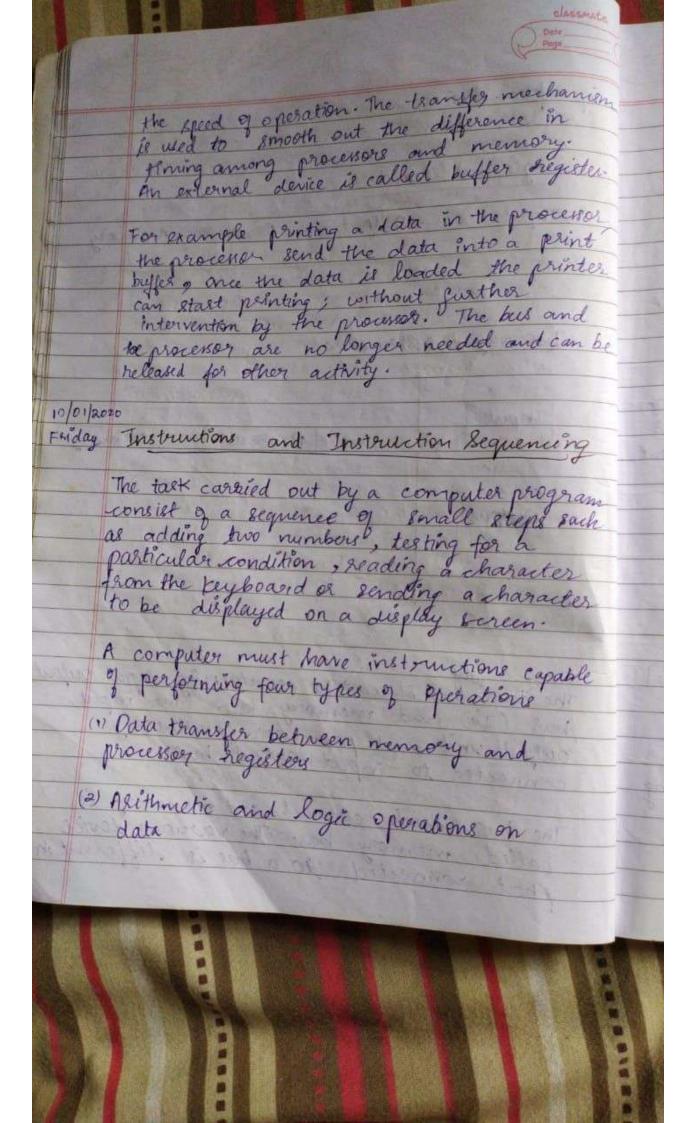
can be stored in secondary memory for future Mithmetic Logic Unit (ALV) All the arithmetic and logical operations are performed in this unit. The hesult obtained from the ALV are either Glored in the memory or stored within the processor itself for immediate use. The arithmetic operation is performed by the processor. There are high speed internal storage elements within the processor called registers. Output unit The output unit is the counter part of the input unit. It's function is to send processed results to the outside world. eg-monitor, printer, speaker who was specied and his following of Control unit The control unit is known as the nerve system of a computer. It co-ordinates all other parts for performing the desired operations

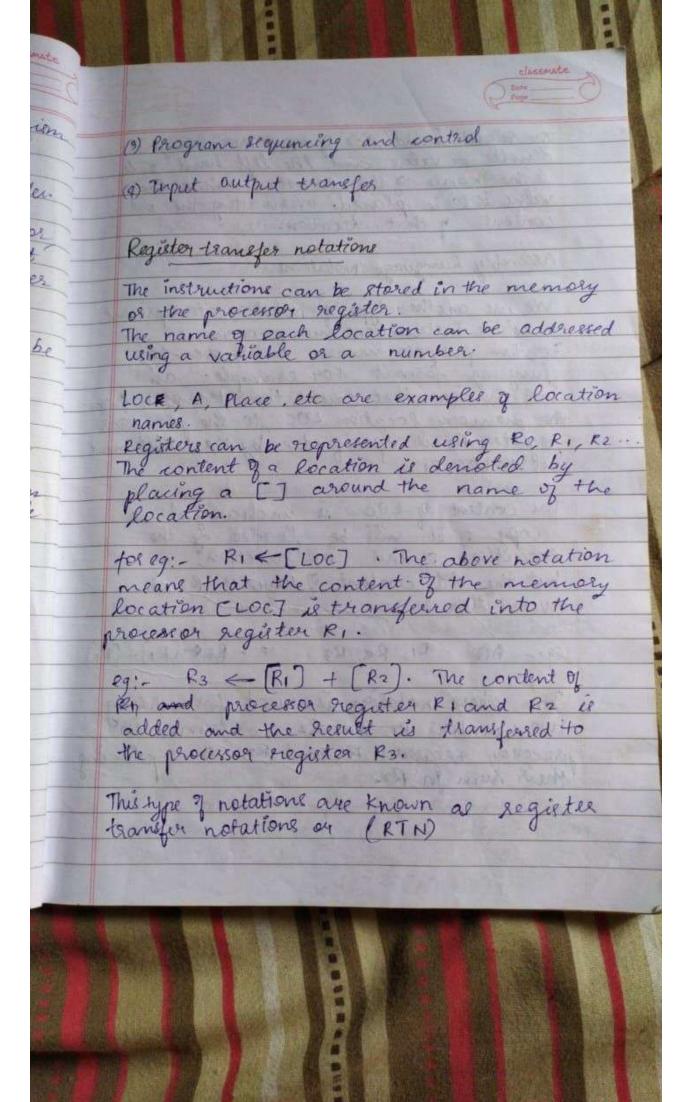




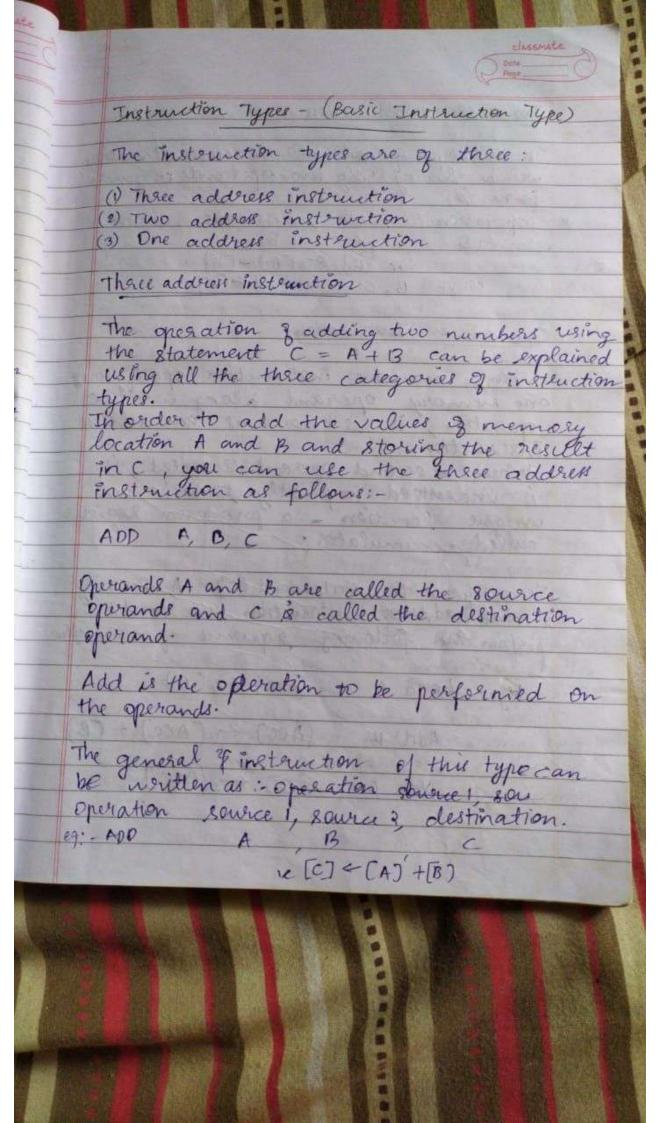
CLASSMAL et and memory to MOR it is transferred to memory to MPR it is transferred from After letching the two operands in this way of ALV performs the desired operation and the result is send to MDR. The address of the result is send to MDR. The address of the peation where the result is stored of stead to MAR and the write signal is initiated Bus Structure A group of lines that scrives as a connecting path for several devices of computer is called a bus. A bus is organised in such as way that when a word of data is to conspersed between units all its bits are transferred simultaneously over many lines, one per line. The most commonly used pus eystem is a single bus system in which all the units are connected to a single but The main disadvantage is that the bus can only use only one transfer at a time; that is only two units can actively use the bus at a given time. The main advantage of a single bus structure is low cost and plexibility for attaching

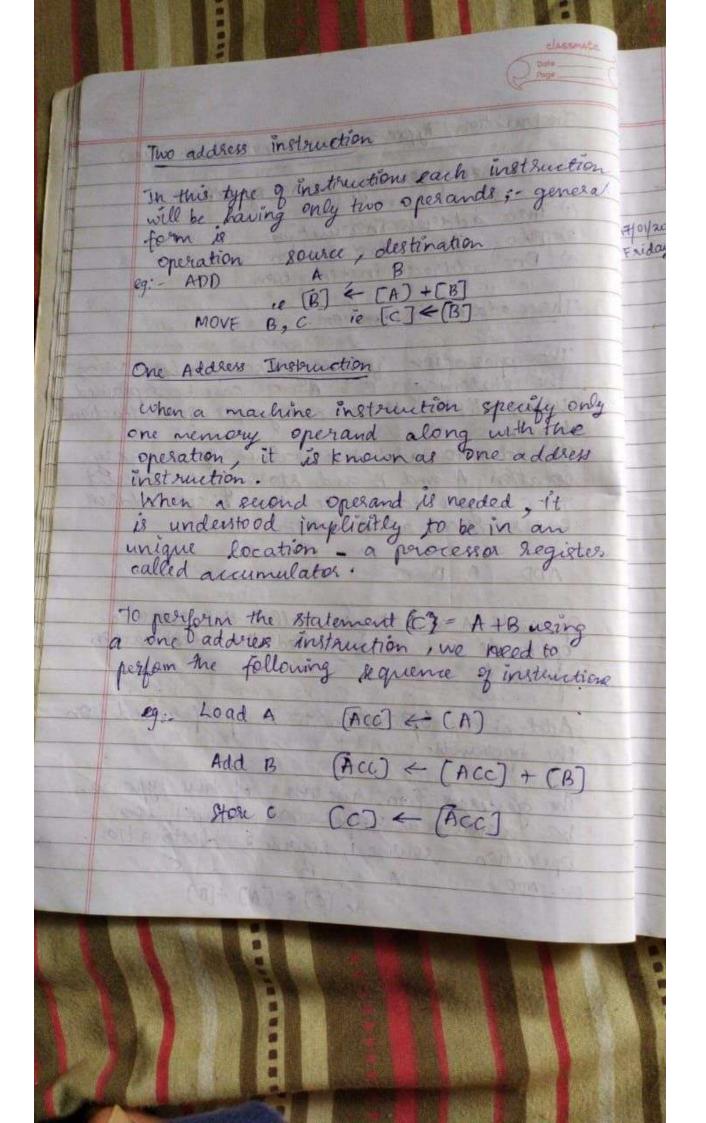


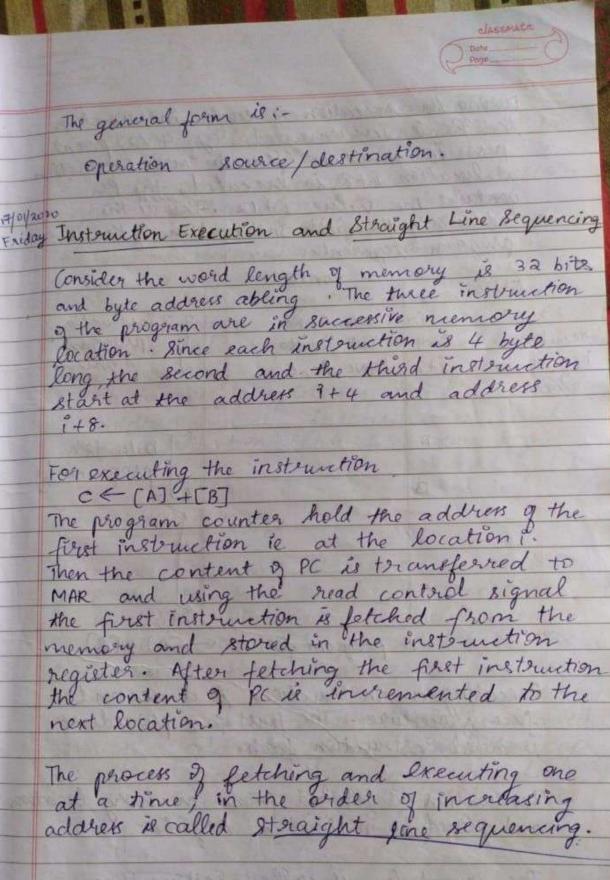




The hight hand side of an RTN always denotes a value and the left hand side is the name of the location where the value is to be placed, overwriting the old contents of that location. Assembly Language Notations We use another type of notation to represent machine instructions and programs.
For this purpose we use an assembly fanguage format For example: an instruction that causes the transfer from the memory location LOC to the processor pregister RI is specified by the statement MOVE LOC P. MOVE LOC, RI The content of LOC is unchanged a copy of it will be loaded by the execution of this instruction but the old content of Register RI es overwritten eg:- ADD R1, R2, R3 18 = R3 (R1)+ [R2] The above notation is used for adding two numbers Rr and Rz contained ind precessor, algisters Ri and Rz and placing Contract of a ferral







The process of fetching and executing one at a time; in the order of increasing address is called straight time sequencing.

The general form is i-

For executing the instruction

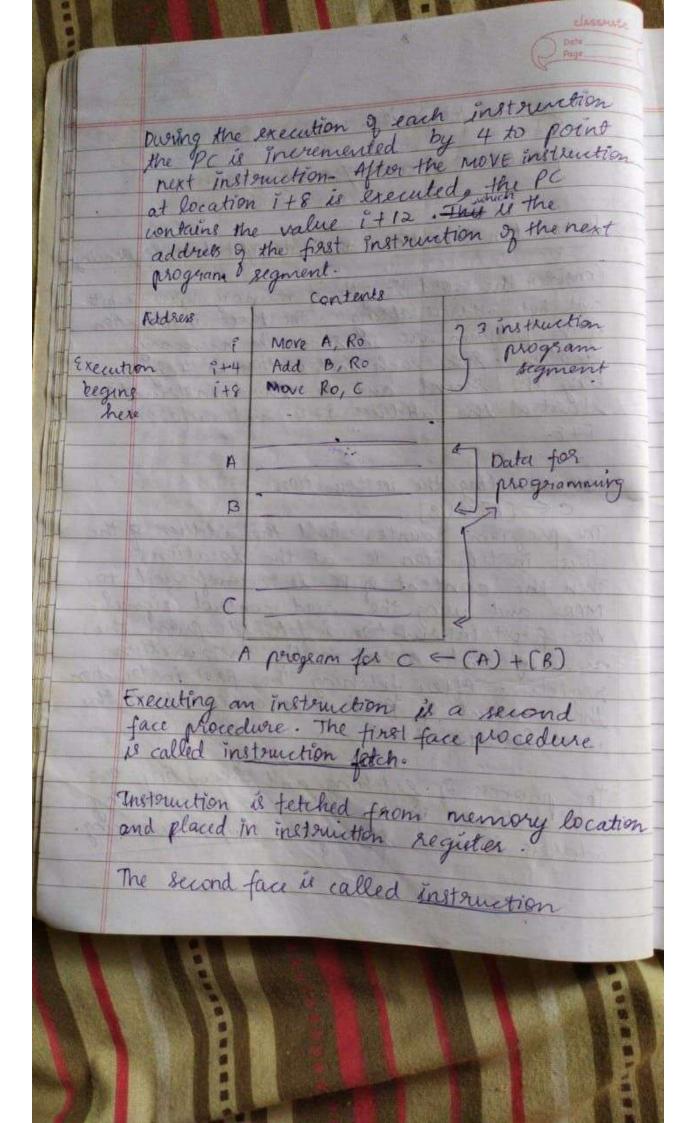
C (A) +[B]

next location.

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1+8.





execution. The instruction in the IR is examined to determine the operation to be performed . This involves fetching operand from the memory or from the processor. registers, performing arithmetic and logical operations and stored the result the in the destination location. At some point during the second face are advanced to point to the next instruction then when they excute face of an instruction is conspleted; the PC contains a new instruction fetch face can begin. Generating Memory Addresses The memory operands addressess cannot be given directly in a single instruction in the loop otherwise it would need to be modified on each pass through the loop. Suppose that a processor fregister, Ri are used to hold the memory addresses of an operand. If it is initially loaded is entered; and is then incremented by 4 on each pass through the loop, it can be provided with the needed capability. To sperify an address of an operand we use

CLASSMATE Date_ addressing modes. The different ways in which the location of an open and is referred specified in an instruction are referred to as addressing modes. 280 husd Total concerned with the way the hardware components are connected together to form a computer system. . It is defined by a its internal registors the timing and control structure and of the set of instructions that it uses A Selection of