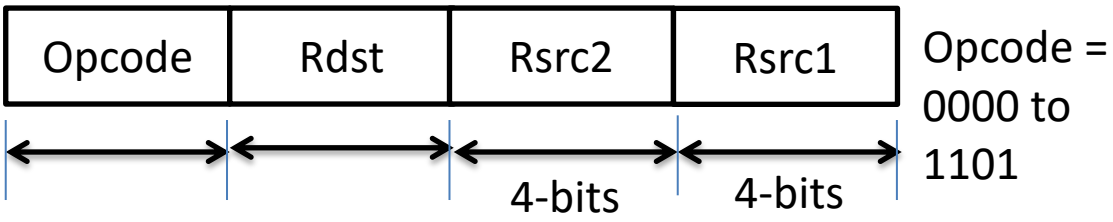
Computer Architecture Practice

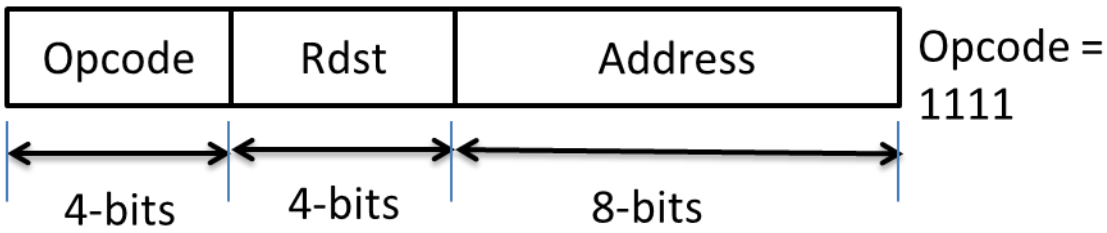
11 Feb 2018

Instruction Set Architecture for 16-bit Processor

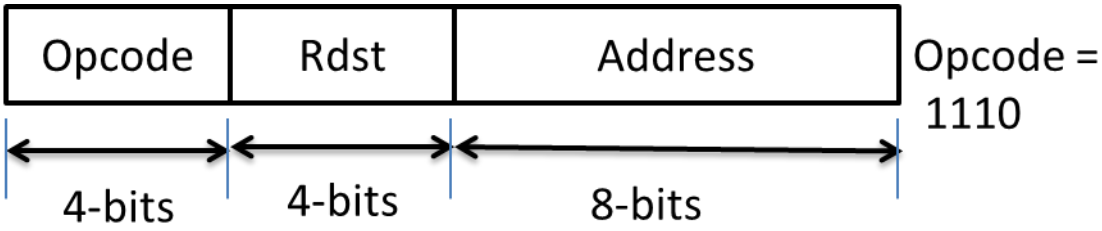
1. Instruction Format and Size:
   This design considers the Instruction size as 16-bits.
   The processor has 16 registers ranging from 0000 to 1111 i.e., r0, r1, …r15.
2. Register based Instructions:



3. Load Instruction:



4. Store Instruction:



5. Opcode (Operation code) Encoding:

Operation Code	**Description**	**Usage**	**Explanation**
0000	Addition	ADD Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 + Rsrc1
0001	Addition with Carry	ADC Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 + Rsrc1 + CF
0010	Subtraction	SUB Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 - Rsrc1
0011	Subtraction With Barrow	SBB Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 - Rsrc1 -1
0100	Multiplication	MUL Rdst, Rsrc2, Rsrc1	{R15, Rdst} = Rsrc2 * Rsrc1
0101	Floating Point Addition	FADD Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 + Rsrc1
0110	Floating Point Subtraction	FSUB Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 - Rsrc1
0111	Floating Point Multiplication	FMUL Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 * Rsrc1
1000	Halt	HLT	Halt
1001	Register Complement	CMP Rdst, Rsrc1	Rdst = ~Rsrc1
1010	Logical Bit Wise XOR	AND Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 ^ Rsrc1
1011	Logical Bit wise NAND	AND Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 ~& Rsrc1
1100	Shift Right	SHR Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 >> Rsrc1 If Rsrc1 = 2 then shift the Rsrc2 in 2bit towards right
1101	Shift Left	LHR Rdst, Rsrc2, Rsrc1	Rdst = Rsrc2 << Rsrc1 If Rsrc1 = 2 then shift the Rsrc2 in 2bit towards Left
1110	Store	STR Rdst, 8-bit Address	[8-bit Address] = Rdst
1111	Load	LDR Rdst, 8-bit Address	Rdst = [8-bit Address]