INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY

HYDERABAD

ANALOG IC DESIGN

COURSE PROJECT

Adithya Sunil Edakkadan

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Contents

1 Design Specification **1**
- 1.1 Design specifications . . . 1
- 1.2 Specification description . . . 1

2 Architecture and hand calculations **2**
- 2.1 Architecture comparison and selection . . . 2
- 2.2 Schematic . . . 2
- 2.3 Design procedure and calculations . . . 2
- 2.4 Tabulating calculated value of design parameters . . . 6
- 2.5 Tabulating calculated specifications . . . 6

3 Simulations **7**
- 3.1 Netlist . . . 7
- 3.2 Tabulating design parameters . . . 8
- 3.3 Operating point . . . 9
- 3.4 STB analysis . . . 10
- 3.5 Slew rate . . . 11
- 3.6 Settling time . . . 12
- 3.7 Systematic offset . . . 13
- 3.8 Noise . . . 14
- 3.9 CMRR . . . 15
- 3.10 PSRR . . . 16
- 3.11 Input common mode range . . . 17
- 3.12 Closed loop gain . . . 18
- 3.13 Closed loop transient analysis . . . 19
- 3.14 Power consumption . . . 19

4 Layout **20**
- 4.1 Layout . . . 20
- 4.2 Post-layout simulations . . . 20
  - 4.2.1 Operating point . . . 22
  - 4.2.2 STB analysis . . . 23
  - 4.2.3 Slew rate . . . 24
  - 4.2.4 Settling time . . . 25
  - 4.2.5 Systematic offset . . . 26
  - 4.2.6 Noise . . . 27
  - 4.2.7 CMRR . . . 28
  - 4.2.8 PSRR . . . 29
  - 4.2.9 Input common mode range . . . 30
  - 4.2.10 Closed loop gain . . . 31

4.2.11 Closed loop transient analysis 32
4.2.12 Power consumption 32

5 Design example **33**
5.1 Multiply-by-two circuit 33
5.2 Transimpedance amplifier (TIA) 35

6 Results **37**
6.1 Tabulation and Comparison 37
6.2 Results 38

CHAPTER 1

DESIGN SPECIFICATION

1.1 DESIGN SPECIFICATIONS

The given design specifications are as follows:

- DC gain $\geq$ 80 dB
- Unity gain frequency $\geq$ 10 MHz
- Output voltage swing $\geq$ 1Vpp
- Slew rate $\geq$ 100 V/µs
- Phase Margin $\geq 65^{\circ}$
- Input referred noise (Thermal only) = 10nv/$\sqrt{Hz}$
- Input Common mode voltage = 0.9 V
- Output load capacitance = 1 pF
- $V_{DD} \leq$ 1.8 V
- Minimum power consumption

1.2 SPECIFICATION DESCRIPTION

The given specifications require the amplifier to have a large gain of 80 dB or greater, a unity gain frequency greater than or equal to 10 MHz and an output voltage swing of 1 V. The slew rate of the amplifier must be greater than or equal to 100 V/μs and phase margin greater than 65°. The input referred noise due to thermal noise must 10 nV/$\sqrt{Hz}$. The input common mode voltage is 0.9 V, output load capacitance is 1 pF and the source voltage is 1.8 V. The specifications also require the power consumption to be minimized while meeting the other requirements.

CHAPTER 2

ARCHITECTURE AND HAND CALCULATIONS

2.1 ARCHITECTURE COMPARISON AND SELECTION

To meet the specifications for high gain, high output swing, minimal power dissipation and low noise performance, a 2 stage op-amp topology is used. The first stage must produce very high gain while the second stage produces high output swing. The telescopic cascode op-amp architecture offers high gain due to the increased output resistance and improved noise performance for lower power consumption. However,the output swing is diminished. The folded-cascode architecture in comparison offers higher swing at the cost of higher power consumption. Hence, the chosen structure for the first stage is the telescopic op-amp as it offers high gain while consuming less power. The second stage is a common source amplifier stage which improves the output swing.

2.2 SCHEMATIC

The schematic of the selected architecture is as shown in Fig. 2.1.

2.3 DESIGN PROCEDURE AND CALCULATIONS

The transistor parameters are as summarized in Table 2.1. These values are taken from the TSMC 180nm wafer tests sheet found here.

TABLE 2.1
Table showing design parameters

Parameter	N-Channel	P-Channel
V_{th} (V)	0.51	-0.51
$\frac{\mu C_{ox}}{2}$ ($\mu A/V^2$)	175.4	-35.6

The design process followed is as follows.

$$V_{DD} = 1.8V$$

The phase margin is given by Eq. (2.1).

$$\phi_M = \pm 180^\circ - Arg[A(j\omega)F(j\omega)] = \pm 180^\circ - tan^{-1}\left(\frac{\omega}{|p_1|}\right) - tan^{-1}\left(\frac{\omega}{|p_2|}\right) - tan^{-1}\left(\frac{\omega}{|z_1|}\right) \quad (2.1)$$

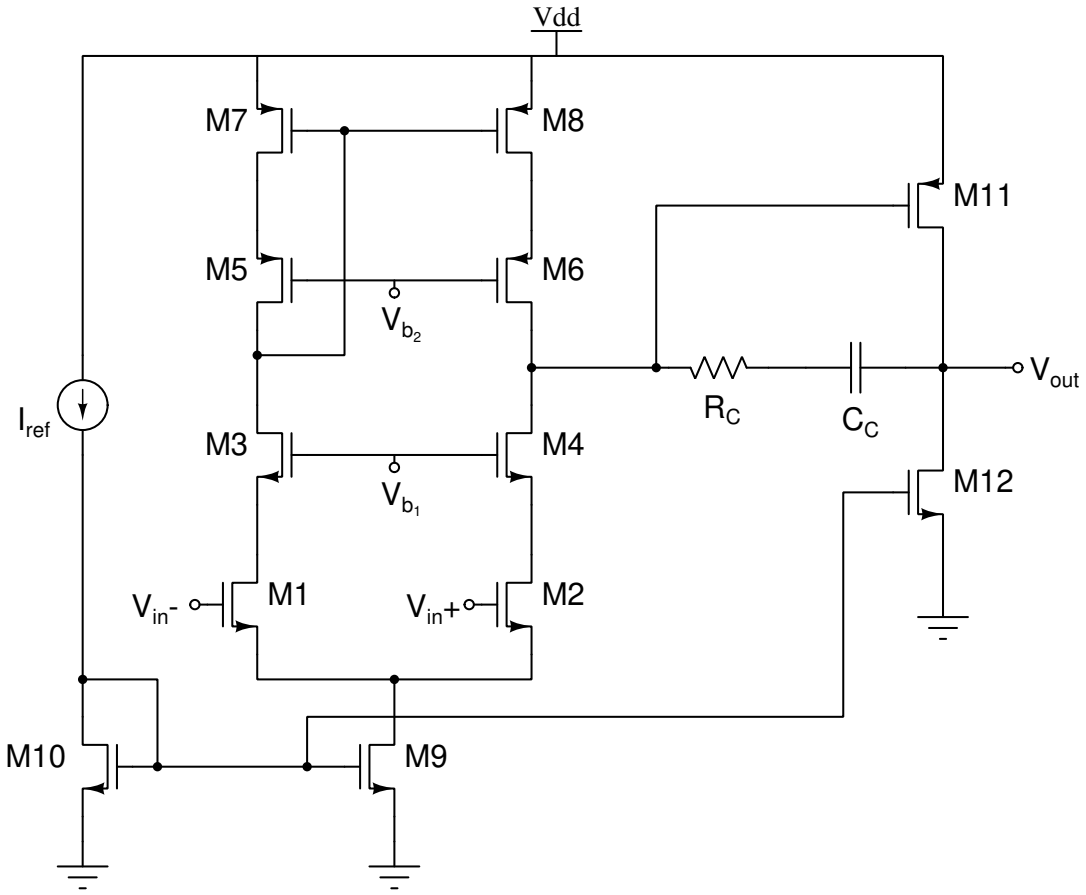


FIGURE 2.1
Schematic of the selected 2-stage op-amp structure

Considering the zero is 10 times higher than gain bandwidth and phase margin of 80°

$$80° = 180° - tan^{-1}[A_V(0)] - tan^{-1}\left(\frac{GB}{|p_2|}\right) - tan^{-1}(0.1)$$

For large $A_V(0)$ the equation can be simplified to

$$4.2894° = tan^{-1}\left(\frac{GB}{|p_2|}\right)$$

Solving for $|p_2|$ as follows

$$|p_2| = \frac{GB}{tan(4.2894°)} = 13.3 \cdot GB$$

The requirement for Miller capacitance (C_C) value for such pole placement is given by Eq. (2.2)

$$C_C > \frac{13.3}{10} C_L \tag{2.2}$$

So the capacitance must be chosen such that

$$C_C > 1.33 \text{ pF}$$

C_C is selected to be 2pF. The slew rate required is $> 100\ V/\mu s$. A slew rate of 200 $V/\mu s$ is selected for the OTA. The tail current I_9 is given by Eq. (2.3).

$$I_9 = SR \cdot C_C \tag{2.3}$$

$$I_9 = 200 \times 10^6 \times 2 \times 10^{-12}$$

$$I_9 = 400\ \mu A$$

Assuming the output of the telescopic stage is biased at $\frac{V_{DD}}{2}$ which is 0.9 V the equations for the saturation drain source voltage are as follows.

$$V_{SD_{sat_6}} + V_{SD_{sat_8}} = 0.375$$

$$V_{DS_{sat_4}} + V_{DS_{sat_2}} + V_{DS_{sat_9}} = 0.375$$

Considering M1, M2, M3 and M4 to be identical and M5, M6, M7 and M8 to be identical

$$V_{SD_{sat_{5-8}}} = 0.1875$$

$$V_{DS_{sat_{1-4}}} = 0.1275$$

The transconductance of a transistor is given by Eq. (2.4).

$$g_m = \frac{2I_D}{V_{DS_{sat}}} \tag{2.4}$$

We have

$$g_{m_{1-4}} = \frac{400\times10^{-6}}{0.1275} = 3.137 \text{ mS}$$

$$g_{m_{5-8}} = \frac{400\times10^{-6}}{0.1875} = 2.133 \text{ mS}$$

The relation between g_m and I_D as given in Eq. (2.5) can be used to find the $\frac{W}{L}$ of the transistors.

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_D} \tag{2.5}$$

We have

$$\left(\frac{W}{L}\right)_{1-4} = 70.1309 \approx 71$$

$$\left(\frac{W}{L}\right)_{5-8} = 159.75 \approx 160$$

For M9 the $\frac{W}{L}$ ratio can be taken as double that of M1 as the current is double.

$$\left(\frac{W}{L}\right)_9 = 142$$

For the 2nd stage of the OTA, the design parameters are derives as follows.

$$g_{m_{11}} = 1.33\left(\frac{C_L}{C_L}\right) g_{m_{1-4}} = 2.086\ mS$$

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{5-8}\left(\frac{g_{m_{11}}}{g_{m_{5-8}}}\right) = 160\left(\frac{2.086}{2.133}\right) = 156.47 \approx 157$$

$$I_{11} = \frac{g_{m_{11}}^2}{2\mu_p C_{ox}\left(\frac{W}{L}\right)_{11}} = 194.63 \approx 195\ \mu A$$

$$\left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_9\left(\frac{I_{11}}{I_9}\right) \approx 70$$

For cancelling the non-dominant pole using a nulling resistor R_C,

$$R_C = \frac{C_C+C_L}{g_{m_{11}}C_C} = \frac{1\times10^{-12}+2\times10^{-12}}{2.086\times10^{-3}\times2\times10^{-12}} = 719.08\Omega$$

Now, the specifications of the designed amplifier can be calculated. The gain of the 2 stage structure will the product of the individual stages.

$$A_v = A_{v_1} A_{v_2}$$

For finding the gain of the telescopic cascode stage, g_{ds} of a transistor is given by Eq. (2.6).

$$g_{ds} = \lambda I_D \tag{2.6}$$

The λ_N and λ_P can be experimentally found to be 0.018 V^{-1} and 0.015 V^{-1}. The g_{ds} and respective r_{ds} values are as follows.

$$g_{ds_{1-4}} = \lambda_N I_{D_{1-4}} = 0.018 \times 200 \times 10^{-6} = 3.6\ \mu S$$
$$r_{ds_{1-4}} = \frac{1}{g_{ds_{1-4}}} = 277.78\ k\Omega$$
$$g_{ds_{5-8}} = \lambda_N I_{D_{5-8}} = 0.015 \times 200 \times 10^{-6} = 3\ \mu S$$
$$r_{ds_{5-8}} = \frac{1}{g_{ds_{5-8}}} = 333.33\ k\Omega$$

The output resistance of the stage r_{out} is given by

$$r_{out} = r_u || r_d$$
$$r_d = g_{m_{1-4}} r_{ds_{1-4}}^2 = 236.9\ M\Omega$$
$$r_u = g_{m_{5-8}} r_{ds_{5-8}}^2 = 242.1\ M\Omega$$
$$r_{out} = 119.7\ M\Omega$$

The DC gain of the telescopic stage is as follows.

$$A_{v_1} = g_{m_1} r_{out} = 375499$$

Similarly, the gain of the common source stage is given by

$$A_{v_2} = \frac{g_{m_{11}}}{I_{D_{11}}(\lambda_N + \lambda_P)}$$
$$g_{m_{11}} = 13.3 \cdot g_{m_{1-4}} \left(\frac{C_L}{C_C}\right)$$
$$A_{v_2} = \frac{g_{m_{11}}}{I_{D_{11}}(\lambda_N + \lambda_P)} \approx 324$$

Hence, the overall gain ($A_v = A_{v_1} A_{v_2}$) is well over 100dB.

The gain bandwidth can be calculated as follows

$$UGB = \frac{g_{m_1}}{C_c} = 1.57\ GHz$$

The power consumption of the OTA is given by

$$P = I_{tot} V_{DD}$$

where I_{tot} will be given by

$$I_{tot} = I_9 + I_{11}$$
$$P = (I_9 + I_{11}) \cdot V_{DD} = (400\mu + 195\mu) \cdot 1.8 = 1.071\ \text{mA}$$

2.4 TABULATING CALCULATED VALUE OF DESIGN PARAMETERS

Table 2.2 shows the design parameters derived in the previous section.

TABLE 2.2
Table showing design parameters

Parameter	Calculated value
$\left(\frac{W}{L}\right)_{1-4}$	71
$\left(\frac{W}{L}\right)_{5-8}$	160
$\left(\frac{W}{L}\right)_{9}$	142
$\left(\frac{W}{L}\right)_{10}$	142
$\left(\frac{W}{L}\right)_{11}$	157
$\left(\frac{W}{L}\right)_{12}$	70
C_C (pF)	2
R_C ($k\Omega$)	0.719

2.5 TABULATING CALCULATED SPECIFICATIONS

Table 2.2 shows the calculated specifications as per the design parameters derived in the previous sections.

TABLE 2.3
Table showing calculated specifications

Specification	Calculated Value
DC gain (dB)	$>$100
Unity gain bandwidth (GHz)	1.57
Phase margin	80°
Slew rate ($V/\mu s$)	200
Power (mW)	1.071

CHAPTER 3

SIMULATIONS

3.1 NETLIST

The netlist for the designed 2 stage OTA is as follows.

```
* Telescopic
.include TSMC_180nm.txt

* Defining supply voltage and transistor sizing parameters
.param SUPPLY=1.8
.param LAMBDA=0.09u
.param length=0.36u

.param width_1234={0.36*71u}
.param width_5678={0.36*160u}
.param width_910={0.36*142u}
.param width_11={0.36*157u}
.param width_12={0.36*70u}

.global gnd vdd

* Defining voltage sources in the circuit
Vdd vdd gnd 'SUPPLY'
Iref gnd ref 400u
Vb1 b1 gnd 1.4
Vb2 b2 gnd 0.75

* Transient and AC
vinp inp gnd dc 0.9 ac 0.01m sin(0.9 0.01m 10k 0 0 0)
vinn inn gnd dc 0.9 ac -0.01m sin(0.9 -0.01m 10k 0 0 0)

* Slew Rate
* vinp inp gnd pulse(1.8 0 -1n 100p 100p 500n 1u)

* Offset
* vinp inp gnd 0.9

* Load and miller compensation
CL out gnd 1p
Cc d4 k 2p
Rs k out 1k

* 1st stage telescopic structure (Transistors are named as per the schematic diagram shown in report)
M1 d1 inn d9 gnd CMOSN W={width_1234} L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M2 d2 inp d9 gnd CMOSN W={width_1234} L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M3 d3 b1 d1 gnd CMOSN W={width_1234} L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M4 d4 b1 d2 gnd CMOSN W={width_1234} L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M5 d3 b2 d5 vdd CMOSP W={width_5678} L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M6 d4 b2 d6 vdd CMOSP W={width_5678} L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M7 d5 d3 vdd vdd CMOSP W={width_5678} L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M8 d6 d3 vdd vdd CMOSP W={width_5678} L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}

* 2nd stage common source structure
M9 d9 ref gnd gnd CMOSN W={width_910} L={length}
+ AS={5*width_910*LAMBDA} PS={10*LAMBDA+2*width_910} AD={5*width_910*LAMBDA} PD={10*LAMBDA+2*width_910}
M10 ref ref gnd gnd CMOSN W={width_910} L={length}
+ AS={5*width_910*LAMBDA} PS={10*LAMBDA+2*width_910} AD={5*width_910*LAMBDA} PD={10*LAMBDA+2*width_910}
```

```
M11      out     d4        vdd     vdd  CMOSP   W={width_11}    L={length}
+ AS={5*width_11*LAMBDA} PS={10*LAMBDA+2*width_11} AD={5*width_11*LAMBDA} PD={10*LAMBDA+2*width_11}
M12      out     ref       gnd     gnd  CMOSN   W={width_12}    L={length}
+ AS={5*width_12*LAMBDA} PS={10*LAMBDA+2*width_12} AD={5*width_12*LAMBDA} PD={10*LAMBDA+2*width_12}


* Analysis
*.tran 1u 1m
*.ac dec 10 1 500Meg
.noise v(out) vinp dec 100 1 500MEG

.control
run

set hcopypscolor = 1
set color0=white
set color1=black

* Plots

* Noise plots
setplot noise1
plot inoise_spectrum
plot onoise_spectrum
setplot noise2
plot inoise_total

* Input/output plots
*plot v(out)
*plot v(inp)
*plot v(inn)
*plot v(inp)-v(inn)

* Fourier analysis
*fourier 10k v(inp)-v(inn)
*fourier 10k v(out)

* Gain magnitude and phase
*plot (v(out))/(v(inp)-v(inn))
*plot 180/PI*phase(v(out)/(v(inp)-v(inn)))
*plot (db(v(out))-db(v(inp)-v(inn))) 180/PI*phase(v(out)/(v(inp)-v(inn)))

.endc
```

3.2 TABULATING DESIGN PARAMETERS

Table 6.2 shows the calculated value of design parameters alongside the values used in simulation.

TABLE 3.1
Table showing design parameters

Parameter	Calculated Value	Simulated Value
$\left(\frac{W}{L}\right)_{1-4}$	71	71
$\left(\frac{W}{L}\right)_{5-8}$	160	160
$\left(\frac{W}{L}\right)_{9}$	142	142
$\left(\frac{W}{L}\right)_{10}$	142	142
$\left(\frac{W}{L}\right)_{11}$	157	157
$\left(\frac{W}{L}\right)_{12}$	70	70
C_C (pF)	2	2
R_C ($k\Omega$)	0.719	1
I_{ref} (μA)	400	400

3.3 OPERATING POINT

The DC operating point analysis is run with the OTA in unity gain feedback mode. Fig. 3.1 shows the results obtained and Fig. 3.2 shows the schematic for the OTA in unity gain feedback mode with labelled nodes.

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
ref                                    0.633179
b1                                         1.4
b2                                        0.75
inp                                        0.9
k                                      1.15266
inn                                    0.899997
d4                                     1.15266
d1                                     0.623397
d9                                     0.216802
d2                                     0.623336
d3                                     1.15768
d5                                     1.48529
d6                                     1.48519
vinp#branch                                0
vb2#branch                                 0
vb1#branch                                 0
vdd#branch                          -0.000574874
```

FIGURE 3.1
DC operating points

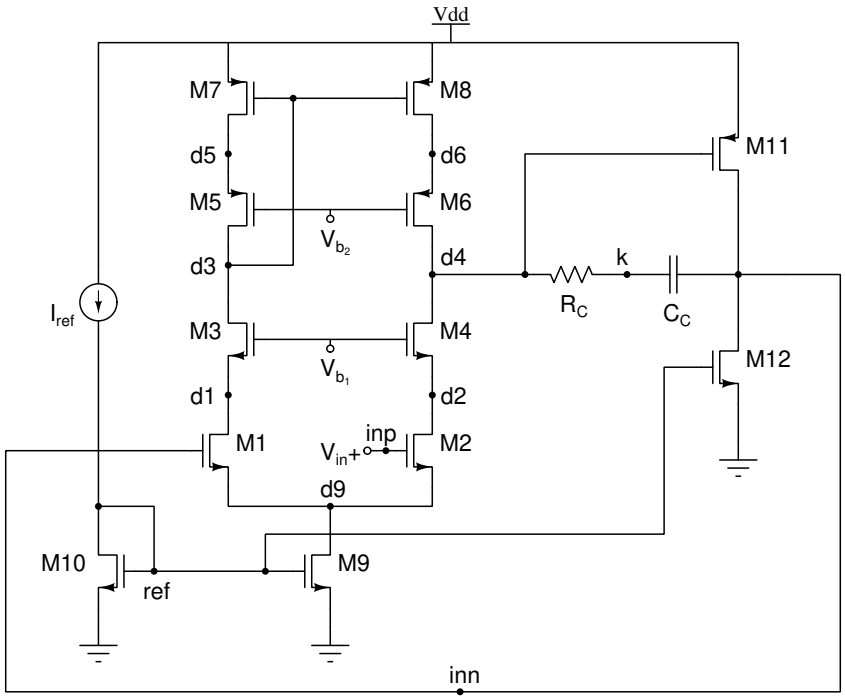


FIGURE 3.2
Schematic for unity gain configuration with labelled nodes

3.4 STB ANALYSIS

The STB analysis is performed on the OTA and the results are as shown in Fig. 3.3.

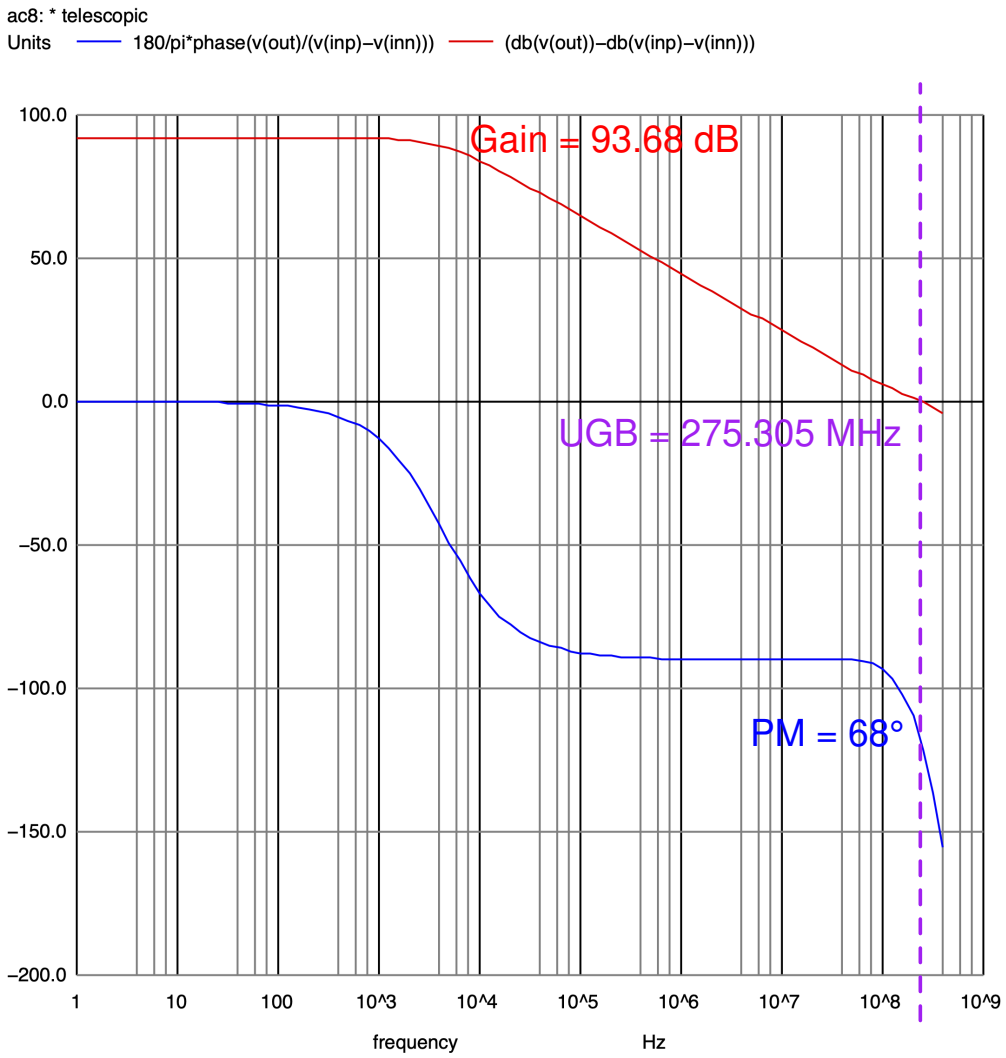


FIGURE 3.3
Magnitude and phase plot

The DC gain obtained is 48327 V/V which is 93.68 dB. The unity gain frequency is 275.305 MHz with a phase margin of 68°.

TABLE 3.2
Table showing design parameters

Parameter	Obtained Value
DC gain (dB)	93.68
Unity gain frequency (MHz)	275.305
Phase margin	68°

3.5 SLEW RATE

With the OTA in unity gain feedback mode, a positive step from 0 to 1.8V with a rise time of 100ps is applied. Fig. 3.4 shows the slewing region.

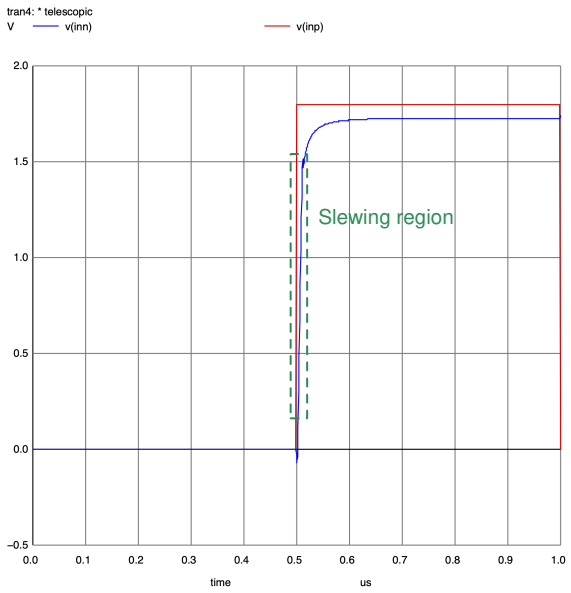


FIGURE 3.4
Plot showing slewing

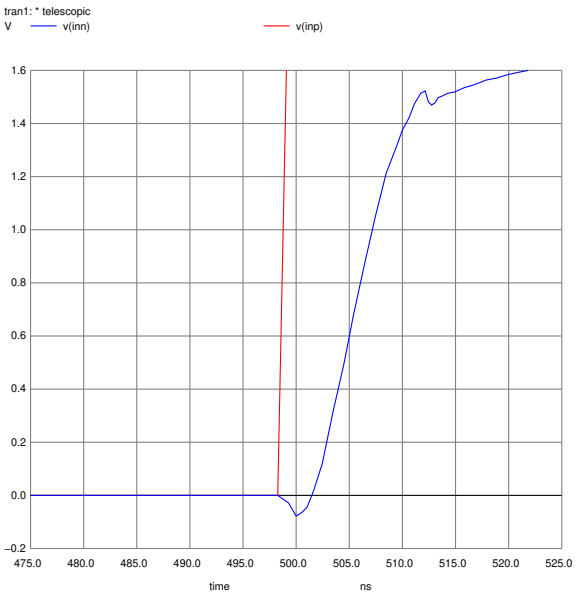


FIGURE 3.5
Plot showing slewing

From zoomed in version of plot shown in Fig. 3.5, the following values of points are obtained of the highest slope region.

```
x0 = 5.08435e-07, y0 = 1.2
```

```
x0 = 5.04e-07, y0 = 0.403922
```

From the above values the slew rate is calculated to be 179.50 V/μs.

3.6 SETTLING TIME

With the OTA in unity gain feedback mode, a positive step from 0 to 1.8V with a rise time of 100ps is applied. For an accuracy of 2% with 1 V input step, the overshoots should fall within 0.02 V from 1 V. Fig. 3.6 shows the settling behavior of the OTA with a settling time of 12.748 ns.

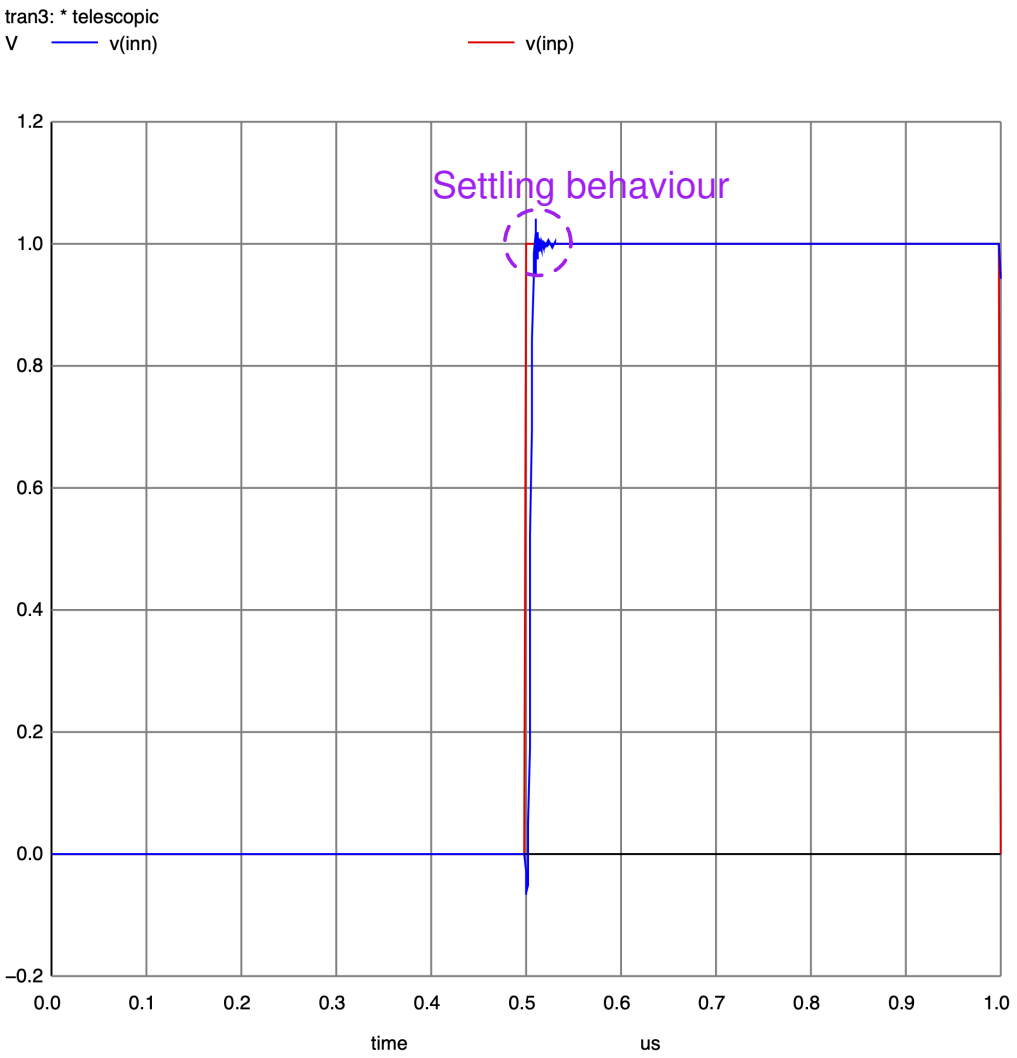


FIGURE 3.6
Plot showing settling behavior

3.7 SYSTEMATIC OFFSET

With the OTA in unity gain feedback mode, the systematic offset value is measured and reported using dc analysis. Fig. 3.7 shows the node voltage on the schematic and the offset of 3.45 μV.

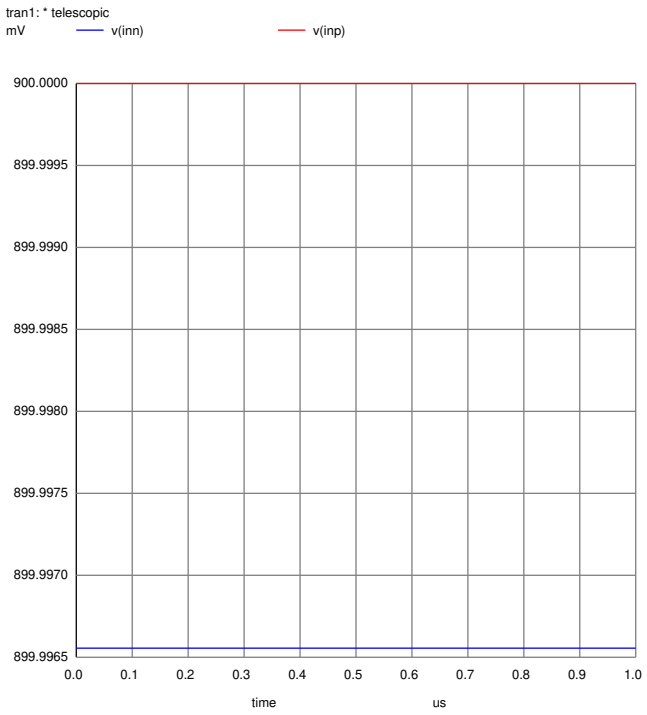


FIGURE 3.7
Plot showing systemic offset

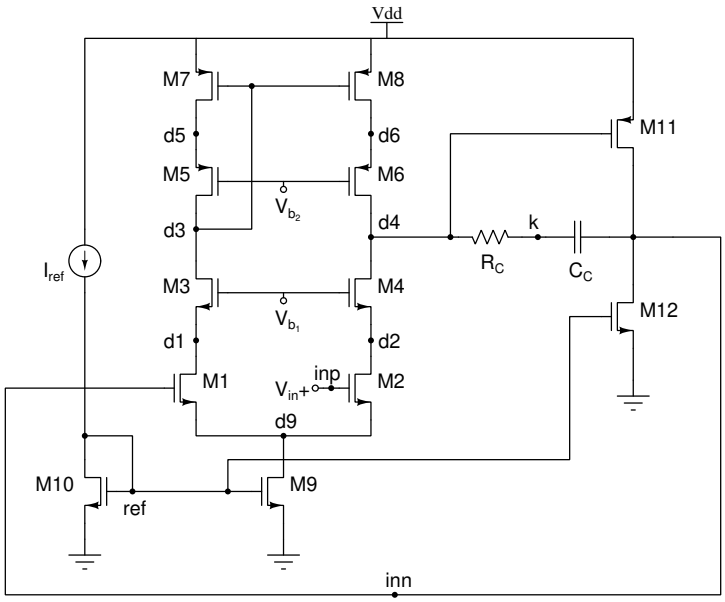


FIGURE 3.8
Schematic for unity gain configuration with labelled nodes

3.8 NOISE

Fig. 3.9 shows the output noise PSD from 1Hz to 1GHz band. Fig. 3.10 shows the input referred noise PSD from 1Hz to 1GHz band.

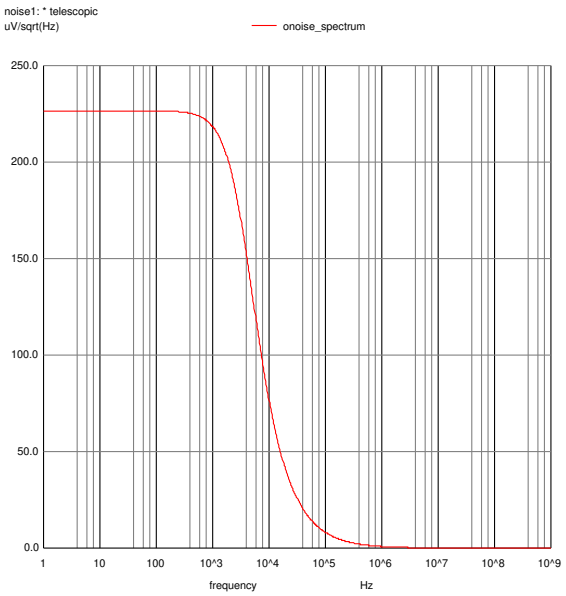


FIGURE 3.9
Plot showing the output noise PSD

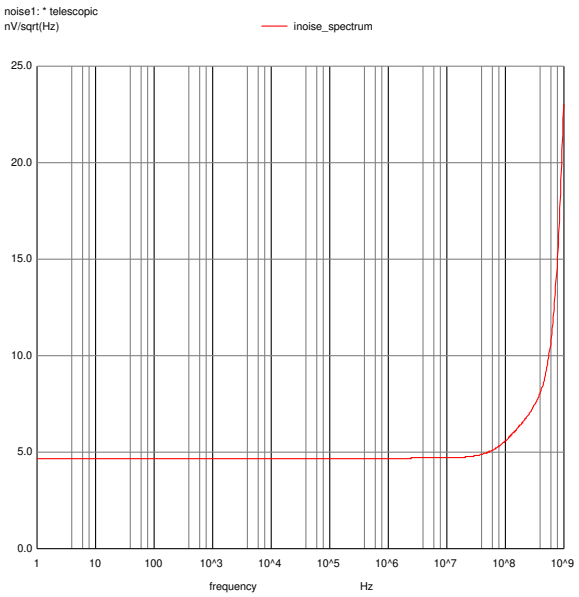
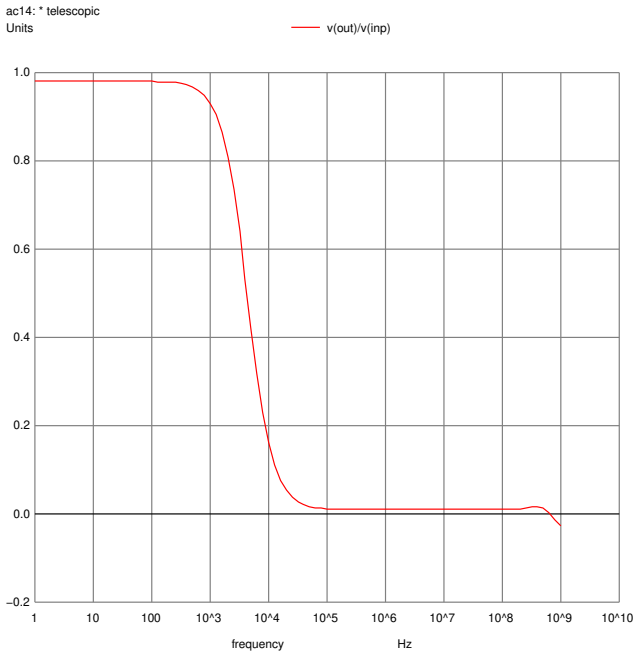


FIGURE 3.10
Plot showing the input referred noise PSD

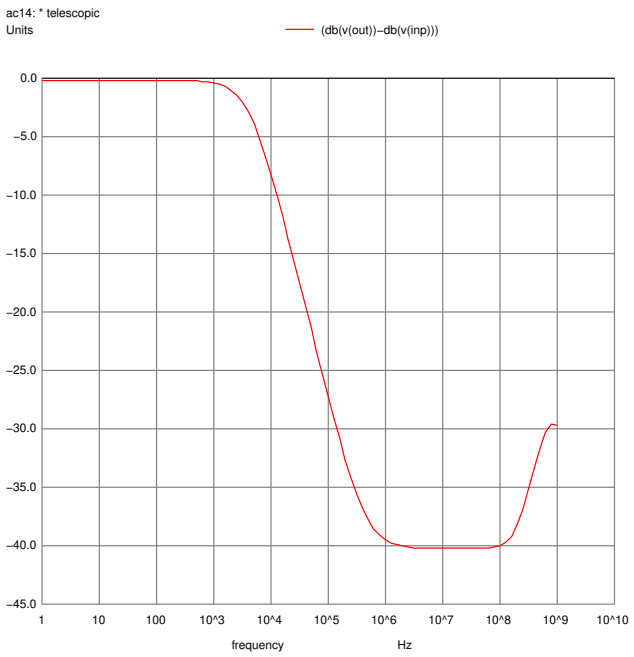
The integrated noise voltage over the unity gain bandwidth is 392.6 μv.

3.9 CMRR

Common mode rejection ratio (CMRR) quantifies the ability of the device to reject common-mode signals. Fig. 3.11 shows the open loop CM gain of the OTA.



((A))



((B))

FIGURE 3.11
Common mode gain: (a) V/V and (b) dB

The CM gain (A_{CM}) of the OTA is found to be 0.98 V/V. The differential gain (A_d) of the device is 40017

V/V. Hence, the CMRR of the OTA is given by $\frac{A_d}{A_{CM}}$ which is equal to 40833.7 which is equivalent to 92.22 dB.

3.10 PSRR

The power supply rejection ratio (PSRR) is used to quantify the ability of the device to reject variations in power supply. The PSRR simulation is performed by adding a small signal component only on the voltage supply of the OTA. Fig. 3.12 shows the results obtained.

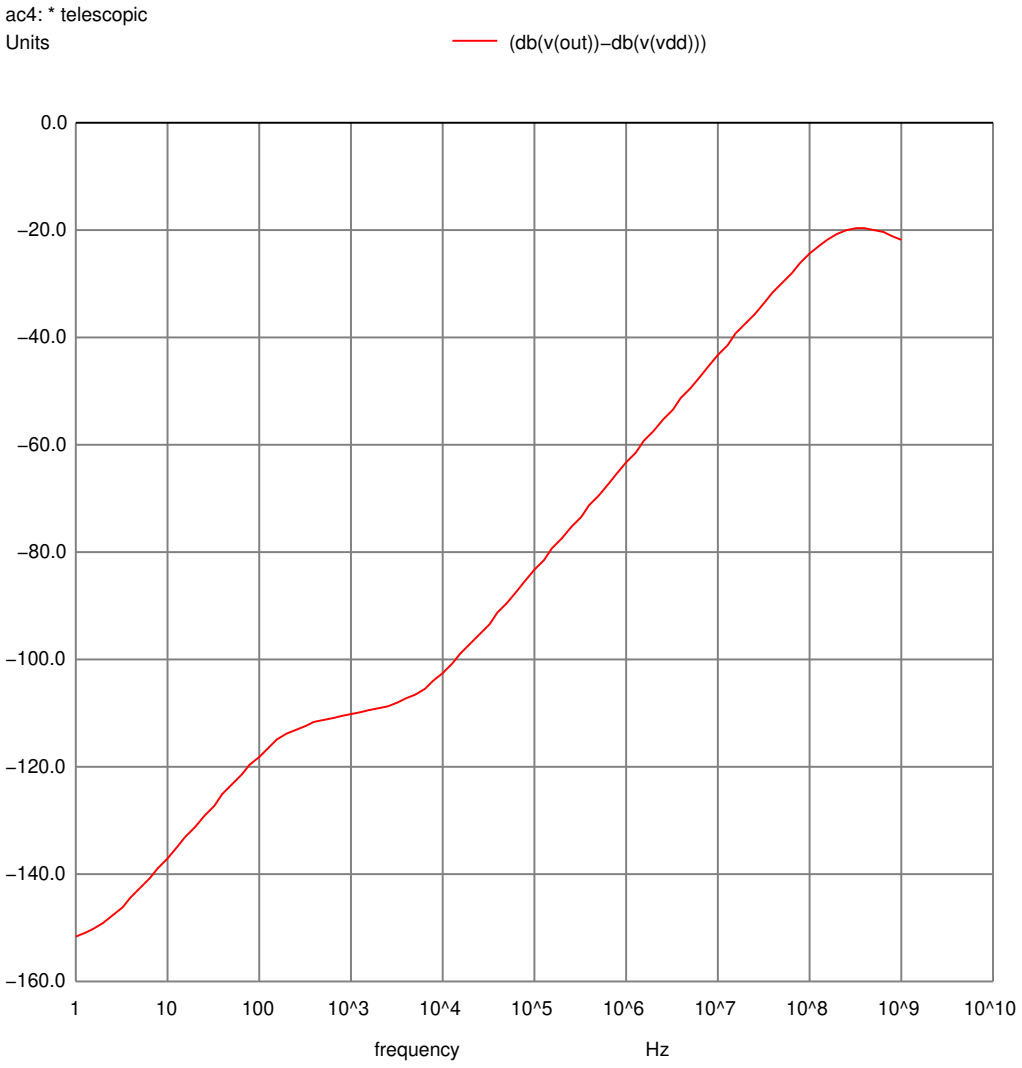


FIGURE 3.12
Gain due to power supply

The PSRR of the OTA is -151.8 dB which means the OTA highly diminishes changes in supply voltage and hence, is resilient to variations in power supply.

3.11 INPUT COMMON MODE RANGE

The input common mode voltage is sweeped in the unity gain configuration. Fig. 3.13 shows the results obtained.

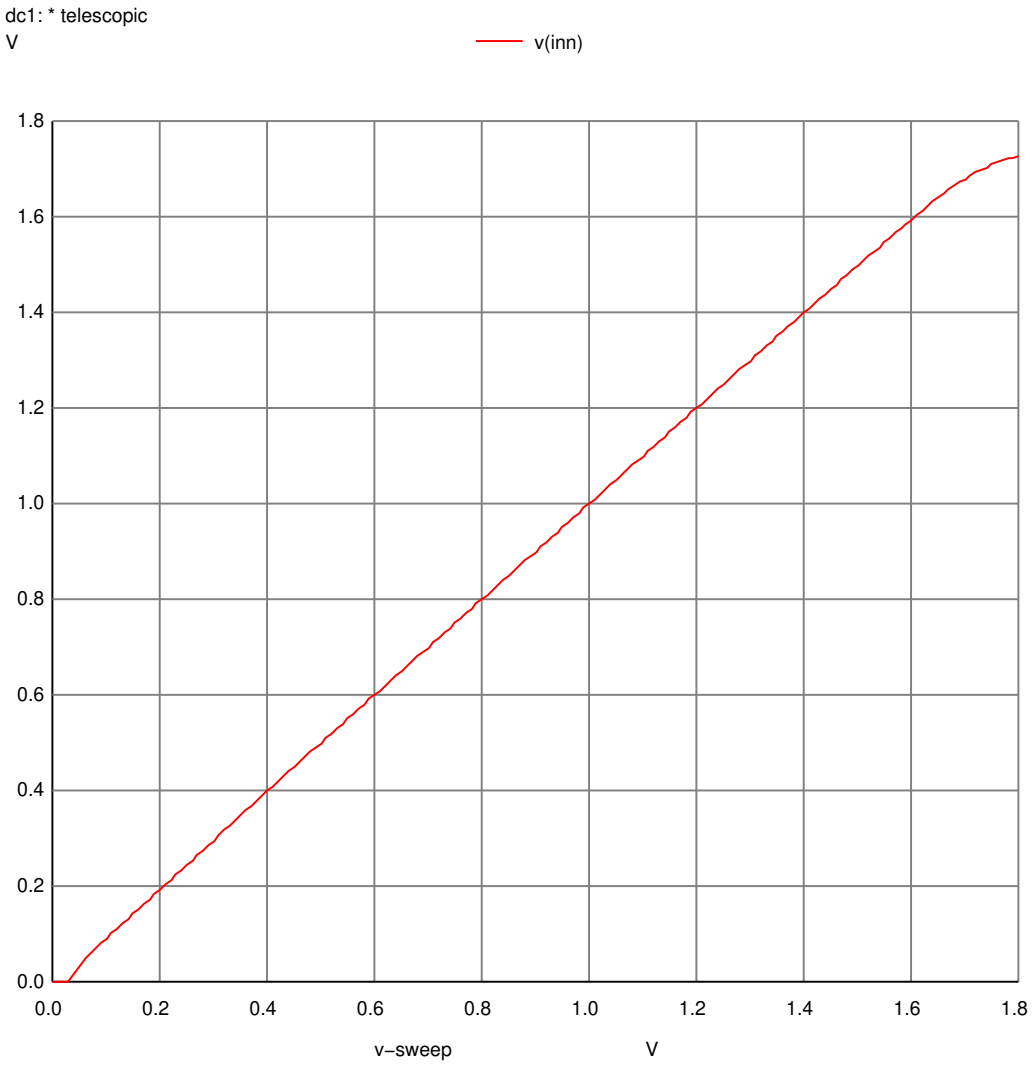


FIGURE 3.13
Variation of output voltage with input common mode voltage

The maximum input common mode range is 0.4 V - 1.45 V.

3.12 CLOSED LOOP GAIN

With the OTA in unity gain feedback mode, ac analysis is performed. Fig. 3.14 shows the results obtained.

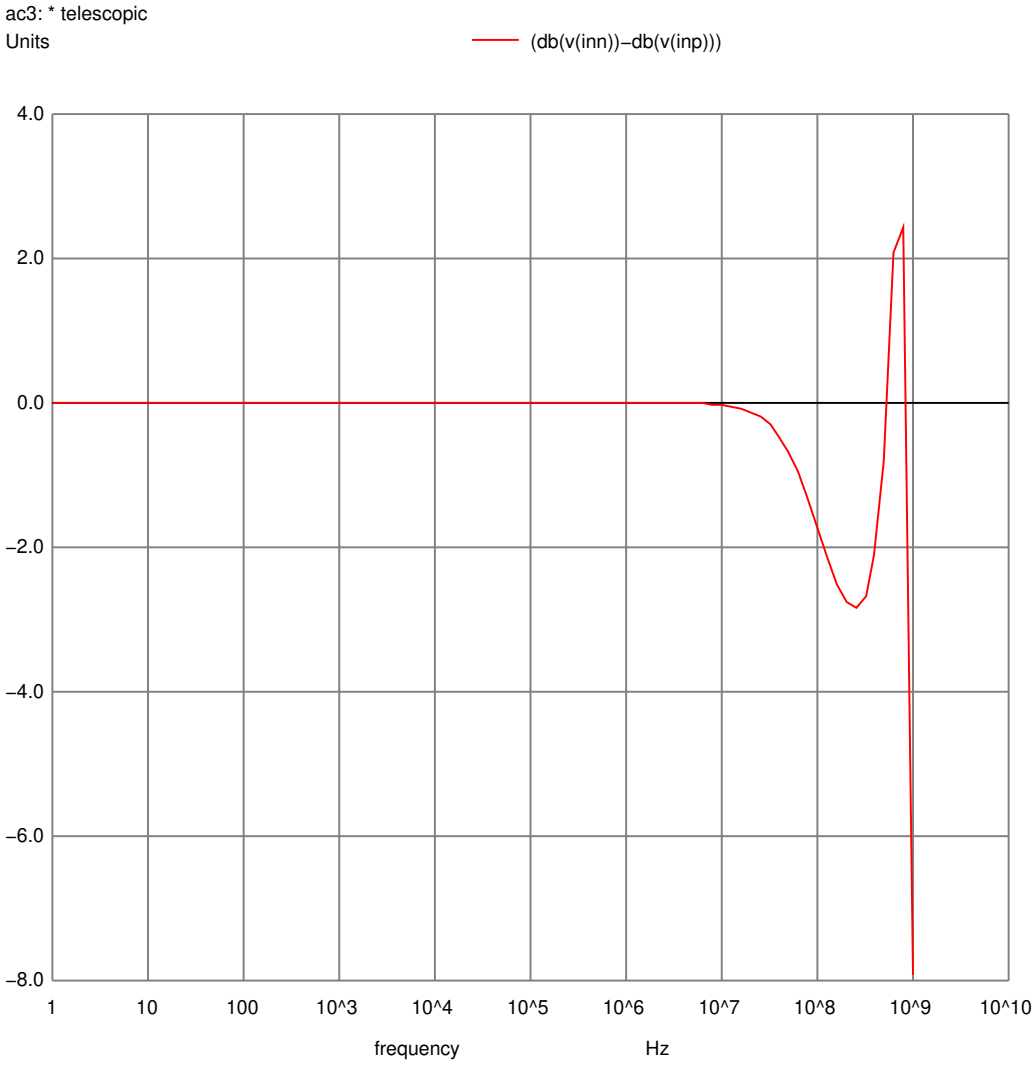


FIGURE 3.14
Closed loop gain

The closed loop gain is 0dB or 1 V/V with a -3dB frequency of 0.899 GHz.

3.13 CLOSED LOOP TRANSIENT ANALYSIS

With the OTA in unity gain feedback mode, a sinusoidal signal of 10KHz frequency is applied for maximum signal swing at the output without distortion Fig. 3.15 shows the results obtained.

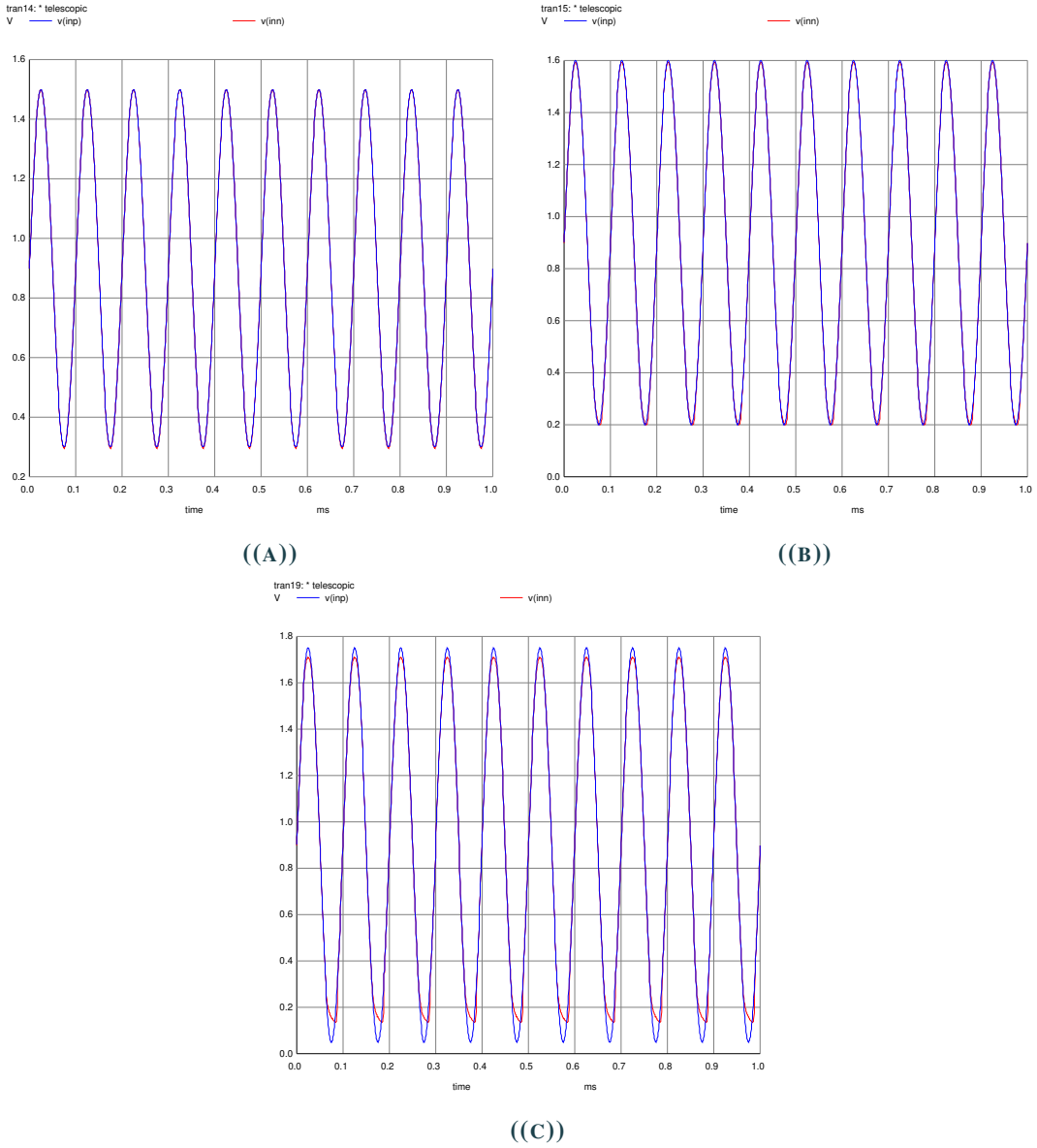


FIGURE 3.15
Closed loop transient analysis plots: (a) Output swing of 1.2 V, (b) Output swing of 1.4 V and (c) Output swing of 1.7 V

Output swing of 1.2 V can be obtained with THD less than 0.3% while a swing of 1.4 V increases the THD to 1.2%. Output swing of upto 1.7 V can be obtained with a THD of 5.5%.

3.14 POWER CONSUMPTION

The average value of current drawn by the OTA from supply in simulation is 569.129 μA and the total power consumption is 1.024 mW.

CHAPTER 4

LAYOUT

4.1 LAYOUT

The proposed OTA has been implemented in 180nm CMOS technology and occupies an area of 65.16 μm $\times$ 23.58 μm. Fig. 4.1 shows the layout of the OTA.

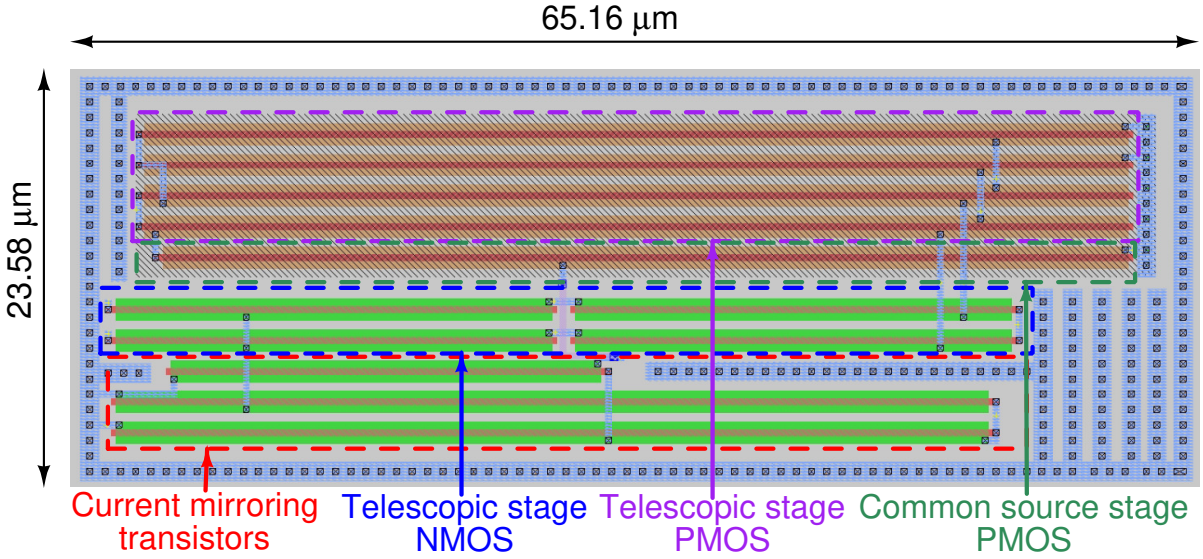


FIGURE 4.1
Layout of implemented OTA

4.2 POST-LAYOUT SIMULATIONS

The extracted netlist for the layout is as follows.

```
* SPICE3 file created from telescopic.ext - technology: scmos

.option scale=0.09u

M1000 d4 b1 d2 gnd CMOSN w=284 l=4
+  ad=1420 pd=578 as=2840 ps=1156
M1001 d4 b2 d6 vdd CMOSP w=640 l=4
+  ad=3200 pd=1290 as=6400 ps=2580
M1002 d6 d3 vdd vdd CMOSP w=640 l=4
+  ad=0 pd=0 as=9540 ps=3846
M1003 d3 b1 d1 gnd CMOSN w=284 l=4
+  ad=1420 pd=578 as=2840 ps=1156
M1004 d9 inp d2 gnd CMOSN w=284 l=4
```

```
+  ad=5680 pd=2302 as=0 ps=0
M1005 ref ref gnd gnd CMOSN w=568 l=4
+  ad=2840 pd=1146 as=7080 ps=2862
M1006 d3 b2 d5 vdd CMOSP w=640 l=4
+  ad=3200 pd=1290 as=6400 ps=2580
M1007 d9 inn d1 gnd CMOSN w=284 l=4
+  ad=0 pd=0 as=0 ps=0
M1008 d5 d3 vdd vdd CMOSP w=640 l=4
+  ad=0 pd=0 as=0 ps=0
M1009 out d4 vdd vdd CMOSP w=628 l=4
+  ad=3140 pd=1266 as=0 ps=0
M1010 gnd ref out gnd CMOSN w=280 l=4
+  ad=0 pd=0 as=1400 ps=570
M1011 d9 ref gnd gnd CMOSN w=568 l=4
+  ad=0 pd=0 as=0 ps=0
C0 d1 d3 0.02fF
C1 out d4 0.02fF
C2 d6 d5 0.13fF
C3 d9 out 0.02fF
C4 b1 d3 0.10fF
C5 out d3 0.02fF
C6 d6 b2 0.10fF
C7 d6 d3 0.15fF
C8 ref out 0.03fF
C9 d5 d3 0.12fF
C10 d2 out 0.09fF
C11 vdd out 0.02fF
C12 d9 inp 0.10fF
C13 d4 d3 0.14fF
C14 d1 out 0.11fF
C15 vdd d6 0.04fF
C16 b2 d3 0.21fF
C17 gnd d4 0.02fF
C18 vdd d5 0.06fF
C19 d9 ref 0.23fF
C20 gnd d9 0.04fF
C21 d2 d4 0.02fF
C22 vdd d4 0.21fF
C23 gnd b2 0.16fF
C24 d9 d2 0.02fF
C25 gnd inp 0.08fF
C26 d1 d4 0.02fF
C27 vdd b2 0.23fF
C28 gnd d3 0.16fF
C29 gnd inn 0.08fF
C30 b1 d4 0.21fF
C31 vdd d3 0.35fF
C32 gnd ref 0.04fF
C33 d9 gnd 0.06fF
C34 inp gnd 0.13fF
C35 inn gnd 0.13fF
C36 ref gnd 0.49fF
C37 d2 gnd 0.06fF
C38 d1 gnd 0.06fF
C39 b1 gnd 0.04fF
C40 out gnd 0.91fF
C41 d6 gnd 0.00fF
C42 d5 gnd 0.00fF
C43 d4 gnd 0.07fF
C44 b2 gnd 0.04fF
C45 d3 gnd 0.09fF
C46 gnd gnd 15.36fF
C47 vdd gnd 70.82fF
```

Simulations run in Chapter 3 are repeated on the post-layout extracted netlist as presented in this section.

4.2.1 OPERATING POINT

The DC operating point analysis is run with the OTA in unity gain feedback mode. Fig. 4.2 shows the results obtained and Fig. 4.3 shows the schematic for the OTA in unity gain feedback mode with labelled nodes.

```
Initial Transient Solution
--------------------------

Node                                   Voltage
----                                   -------
vdd                                        1.8
ref                                    0.63301
b1                                         1.4
b2                                         0.7
inp                                        0.9
k                                      1.15287
inn                                    0.899996
d4                                     1.15287
d2                                     0.623462
d6                                     1.44691
d3                                     1.15894
d1                                     0.623536
d9                                     0.216927
d5                                     1.44705
vinp#branch                                  0
vb2#branch                                   0
vb1#branch                                   0
vdd#branch                          -0.000573722
```

FIGURE 4.2
DC operating points

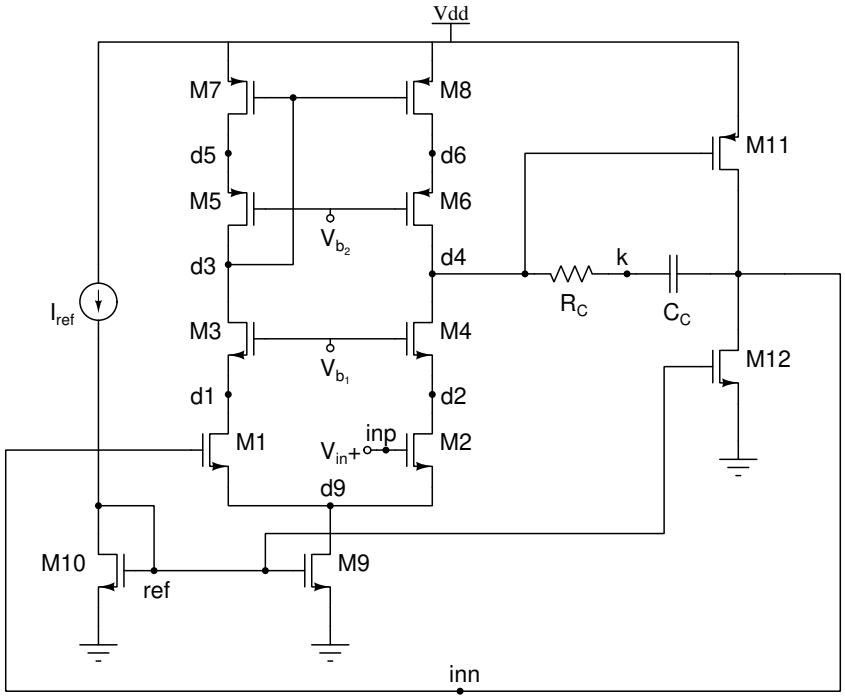


FIGURE 4.3
Schematic for unity gain configuration with labelled nodes

4.2.2 STB ANALYSIS

The STB analysis is performed on the OTA and the results are as shown in Fig. 4.4.

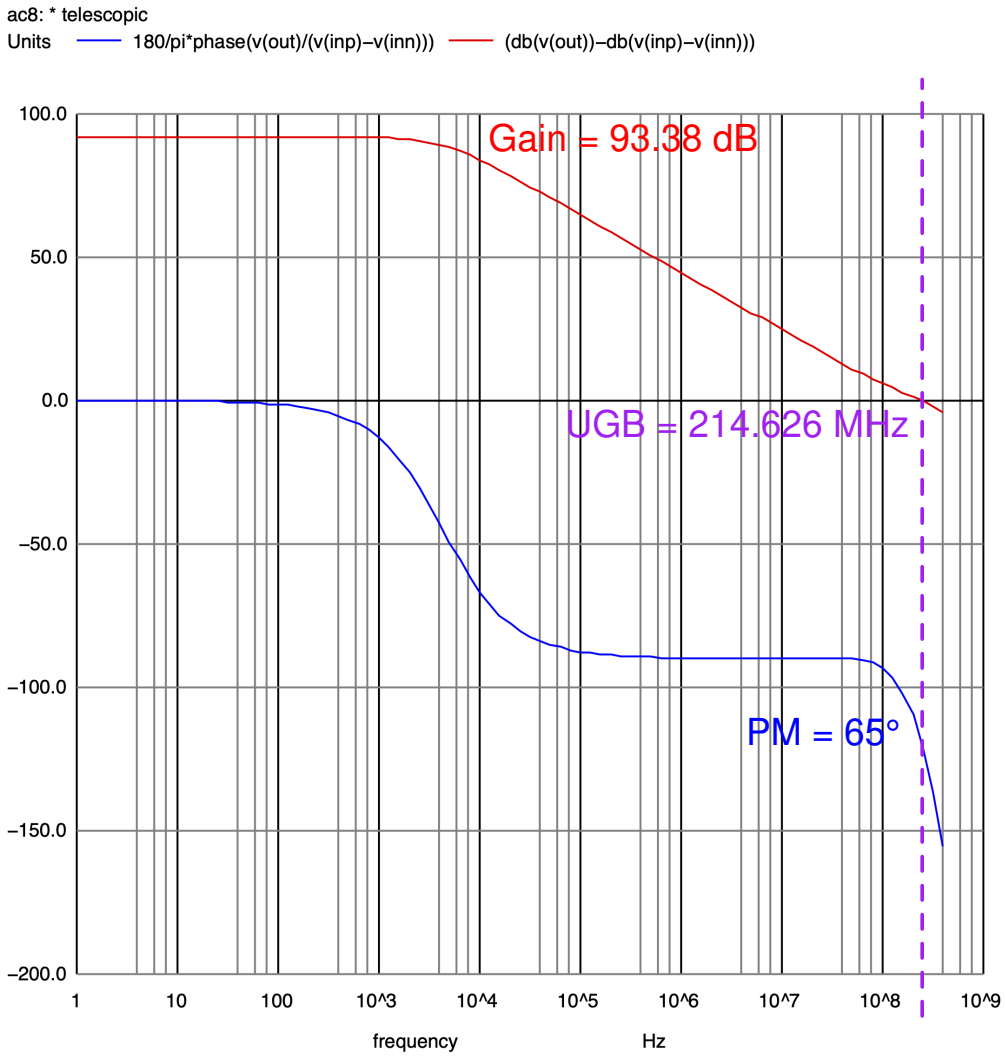


FIGURE 4.4
Magnitude and phase plot

The DC gain obtained is 46669 V/V which is 93.38 dB. The unity gain frequency is 214.626 MHz Hz with a phase margin of 65°.

TABLE 4.1
Table showing design parameters

Parameter	Obtained Value
DC gain (dB)	93.38
Unity gain frequency (MHz)	214.626
Phase margin	65°

4.2.3 SLEW RATE

With the OTA in unity gain feedback mode, a positive step from 0 to 1.8V with a rise time of 100ps is applied. Fig. 4.5 shows the slewing region.

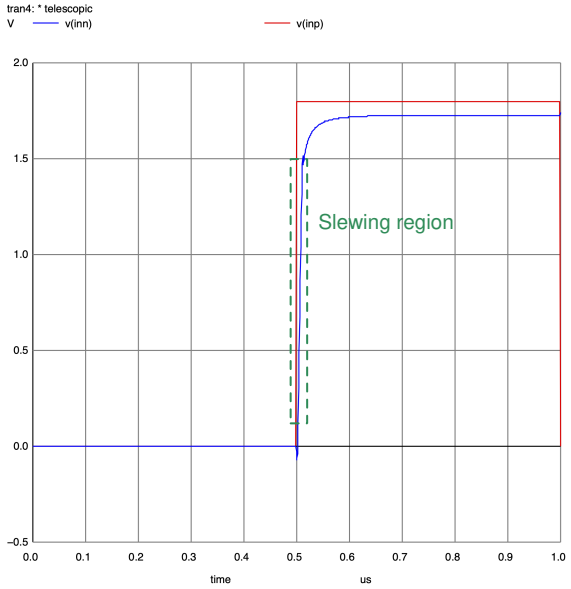


FIGURE 4.5
Plot showing slewing

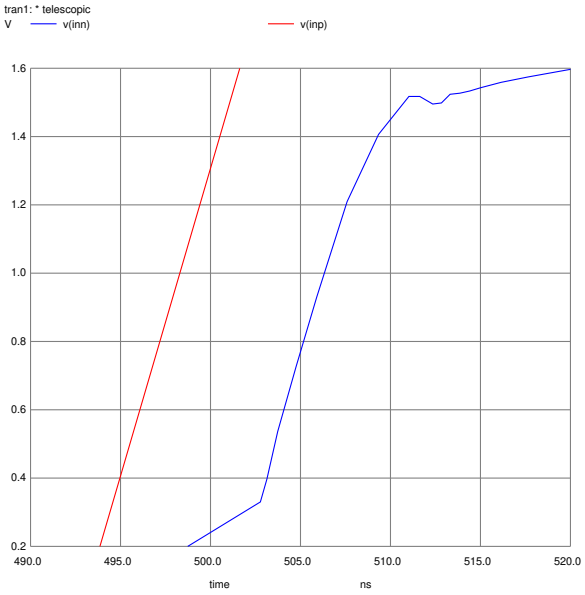


FIGURE 4.6
Plot showing slewing

From zoomed in version of plot shown in Fig. 4.6, the following values of points are obtained of the highest slope region.

```
x0 = 5.02839e-07, y0 = 0.329032
```

```
x0 = 5.07597e-07, y0 = 1.20484
```

From the above values the slew rate is calculated to be 184.07 V/μs.

4.2.4 SETTLING TIME

With the OTA in unity gain feedback mode, a positive step from 0 to 1.8V with a rise time of 100ps is applied. For an accuracy of 2% with 1 V input step, the overshoots should fall within 0.02 V from 1 V. Fig. 4.7 shows the settling behavior of the OTA with a settling time of 12.777 ns.

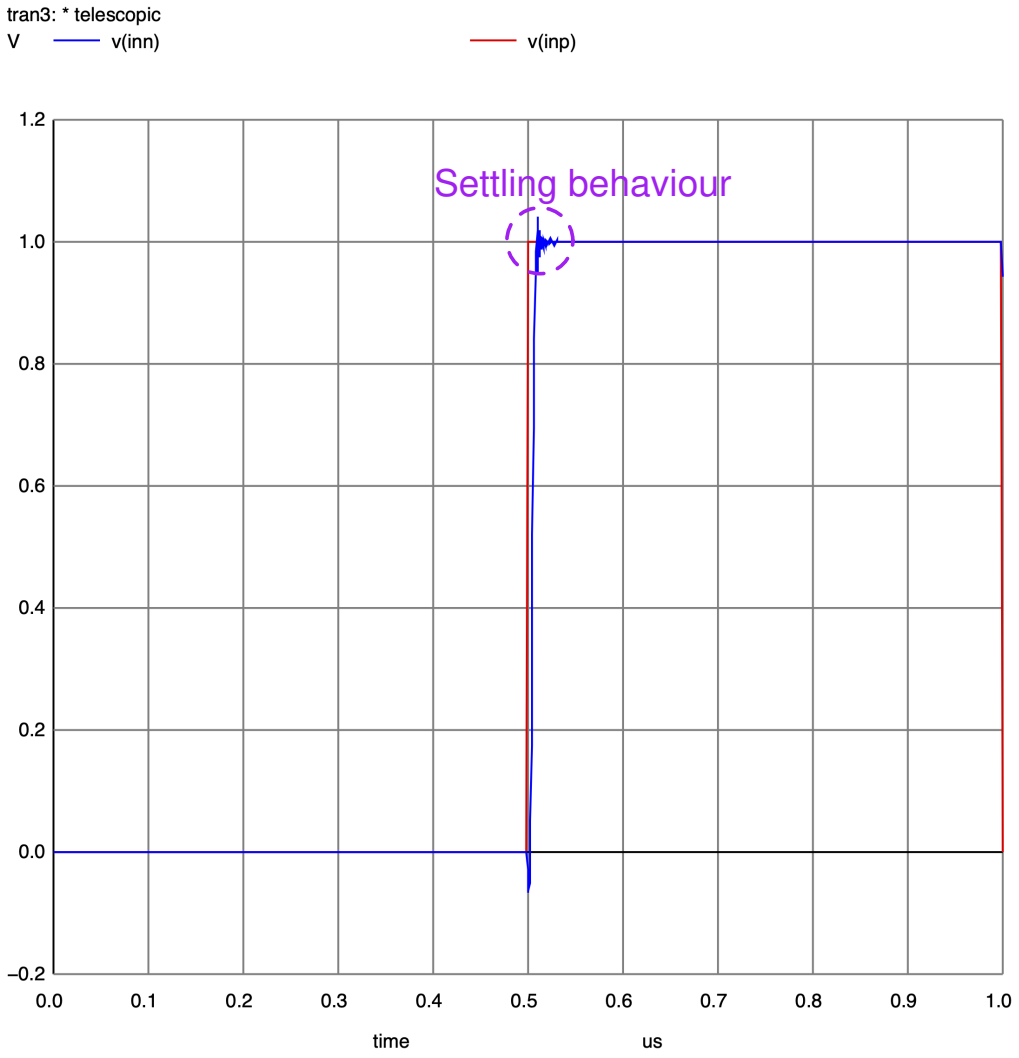


FIGURE 4.7
Plot showing settling behavior

4.2.5 SYSTEMATIC OFFSET

With the OTA in unity gain feedback mode, the systematic offset value is measured and reported using dc analysis. Fig. 4.8 shows the node voltage on the schematic and the offset of 4.3 μV.

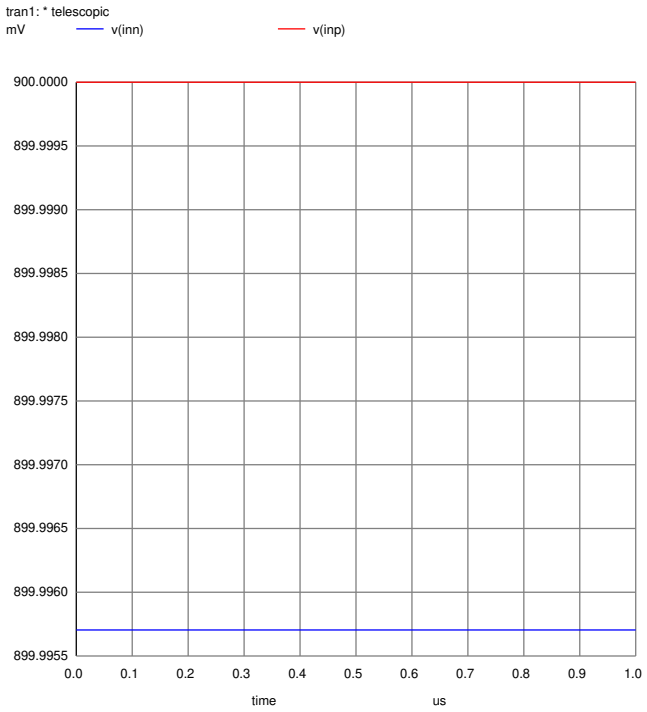


FIGURE 4.8
Plot showing systemic offset

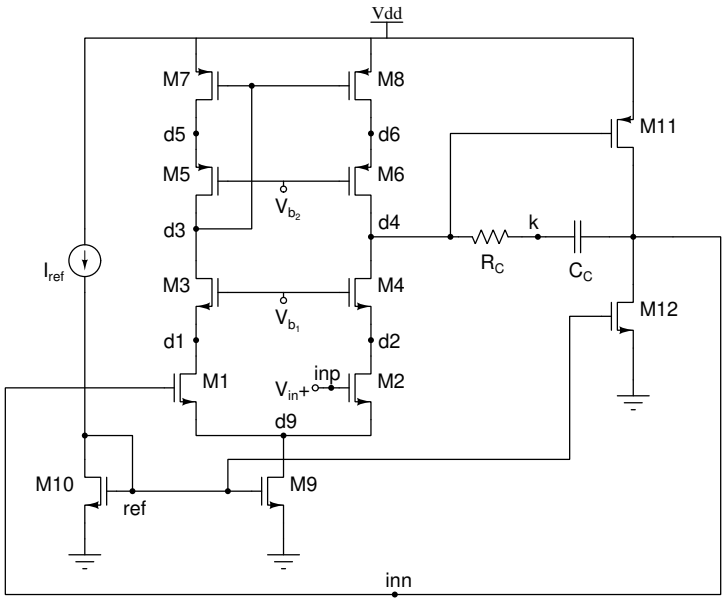


FIGURE 4.9
Schematic for unity gain configuration with labelled nodes

4.2.6 NOISE

Fig. 4.10 shows the output noise PSD from 1Hz to 1GHz band. Fig. Fig. 4.11 shows the input referred noise PSD from 1Hz to 1GHz band.

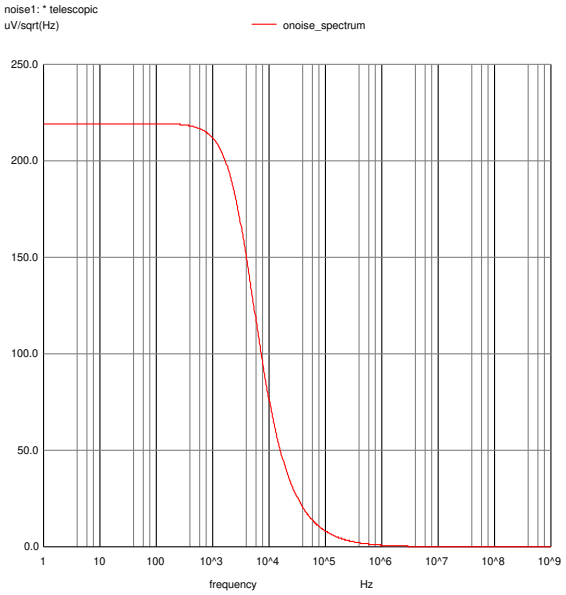


FIGURE 4.10
Plot showing the output noise PSD

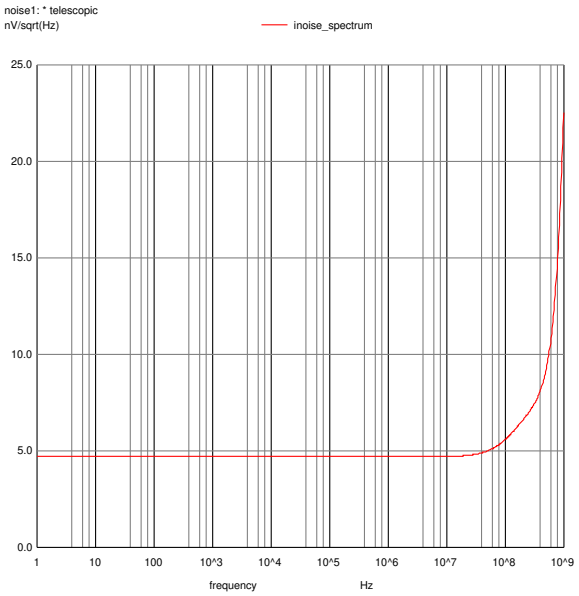
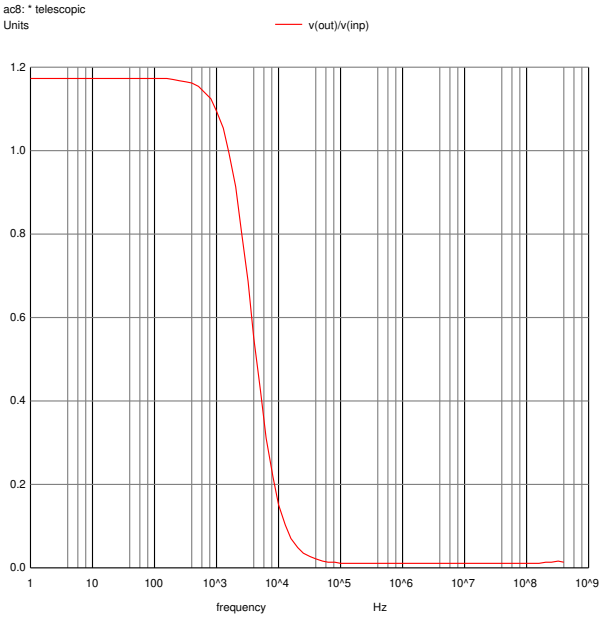


FIGURE 4.11
Plot showing the input referred noise PSD

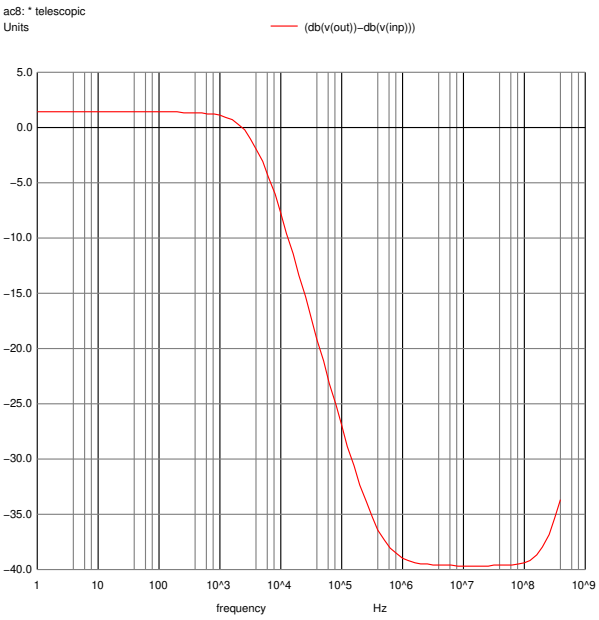
The integrated noise voltage over the unity gain bandwidth is 387.645 μv.

4.2.7 CMRR

Common mode rejection ratio (CMRR) quantifies the ability of the device to reject common-mode signals. Fig. 4.12 shows the open loop CM gain of the OTA.



((A))



((B))

FIGURE 4.12
Common mode gains

The CM gain (A_{CM}) of the OTA is found to be 0.98 V/V. The differential gain (A_d) of the device is 40017 V/V. Hence, the CMRR of the OTA is given by $\frac{A_d}{A_{CM}}$ which is equal to 39752.1 which is equivalent to 91.98 dB.

4.2.8 PSRR

The power supply rejection ratio (PSRR) is used to quantify the ability of the device to reject variations in power supply. The PSRR simulation is performed by adding a small signal component only on the voltage supply of the OTA. Fig. 4.13 shows the results obtained.

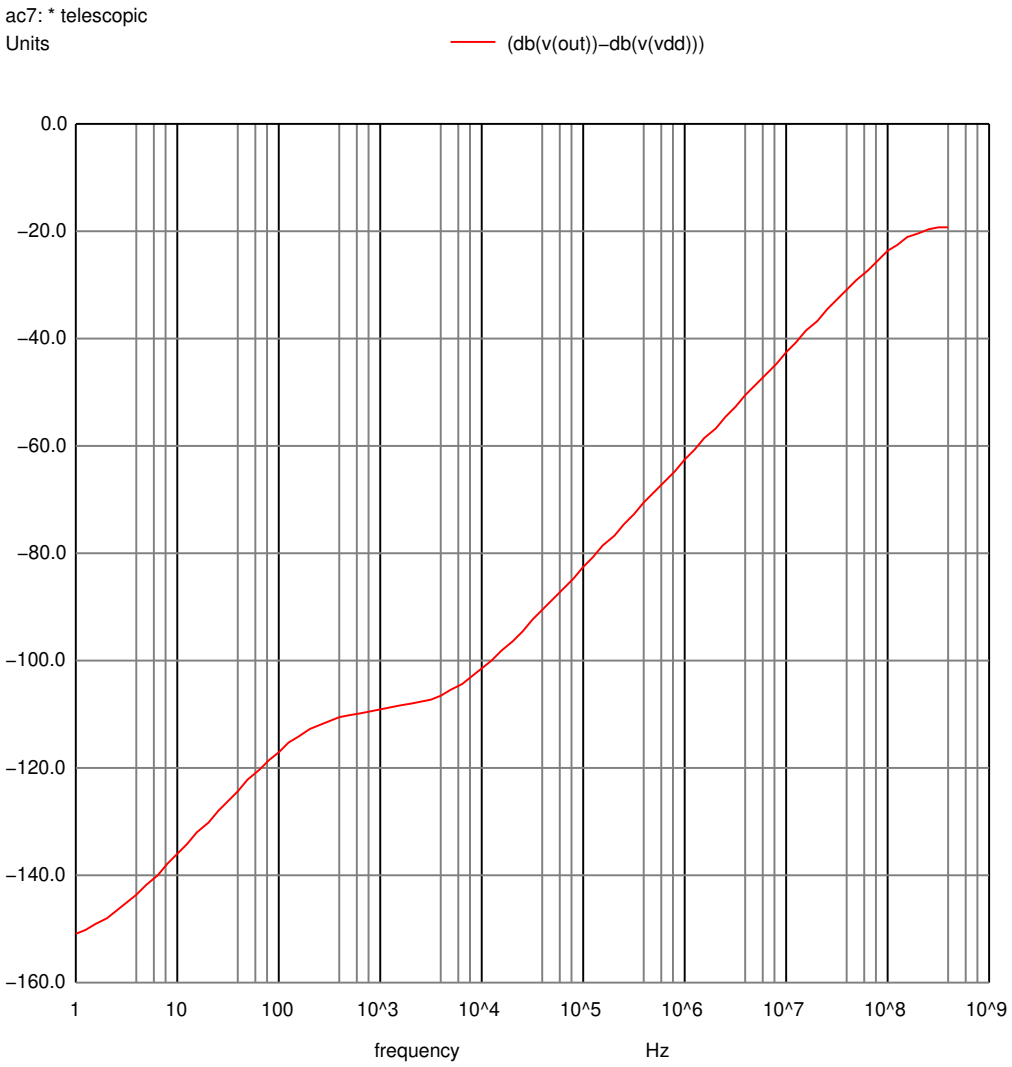


FIGURE 4.13
Gain due to power supply

The PSRR of the OTA is -150.75 dB which means the OTA highly diminishes changes in supply voltage and hence, is resilient to variations in power supply.

4.2.9 INPUT COMMON MODE RANGE

The input common mode voltage is sweeped in the unity gain configuration. Fig. 4.14 shows the results obtained.

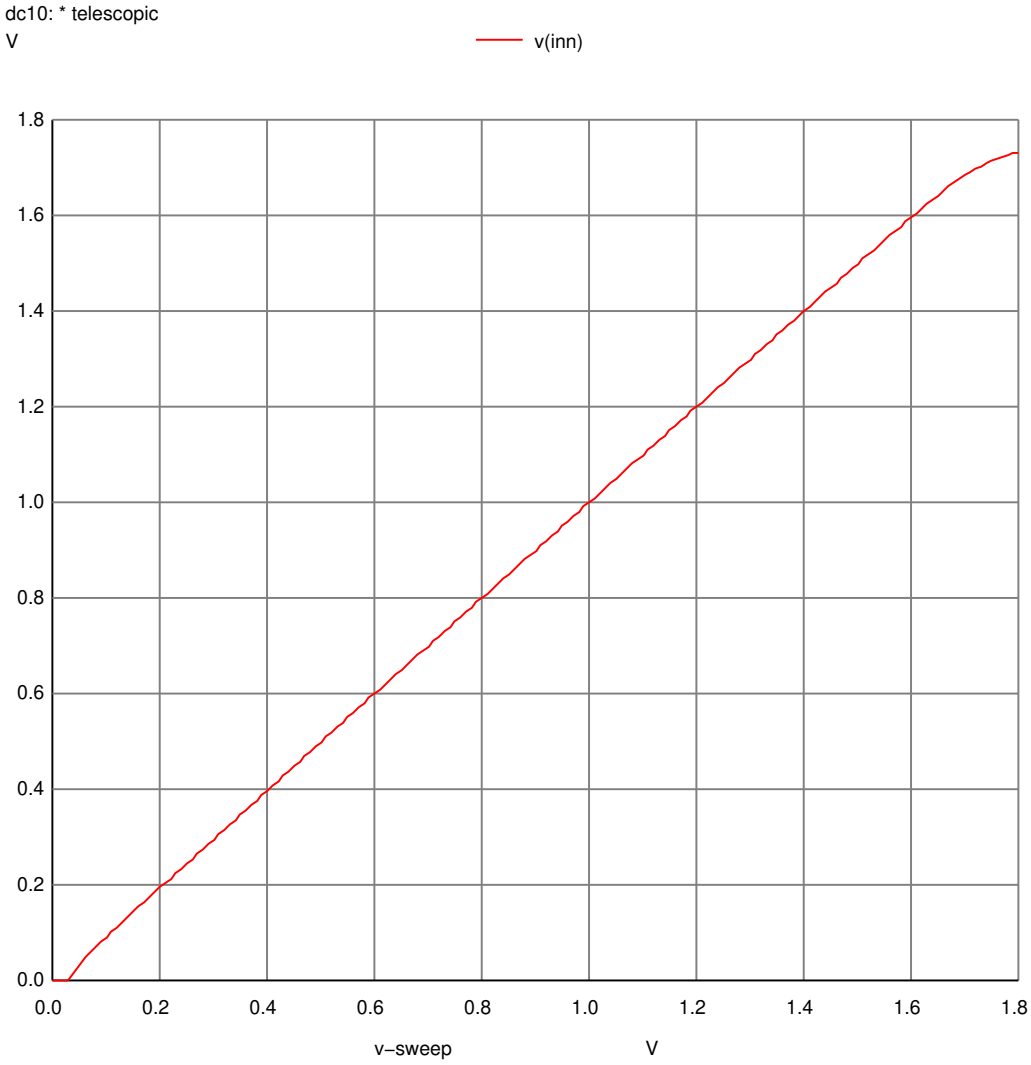


FIGURE 4.14
Variation of output voltage with input common mode voltage

The maximum input common mode range is 0.4 V - 1.45 V.

4.2.10 CLOSED LOOP GAIN

With the OTA in unity gain feedback mode, ac analysis is performed. Fig. 4.15 shows the results obtained.

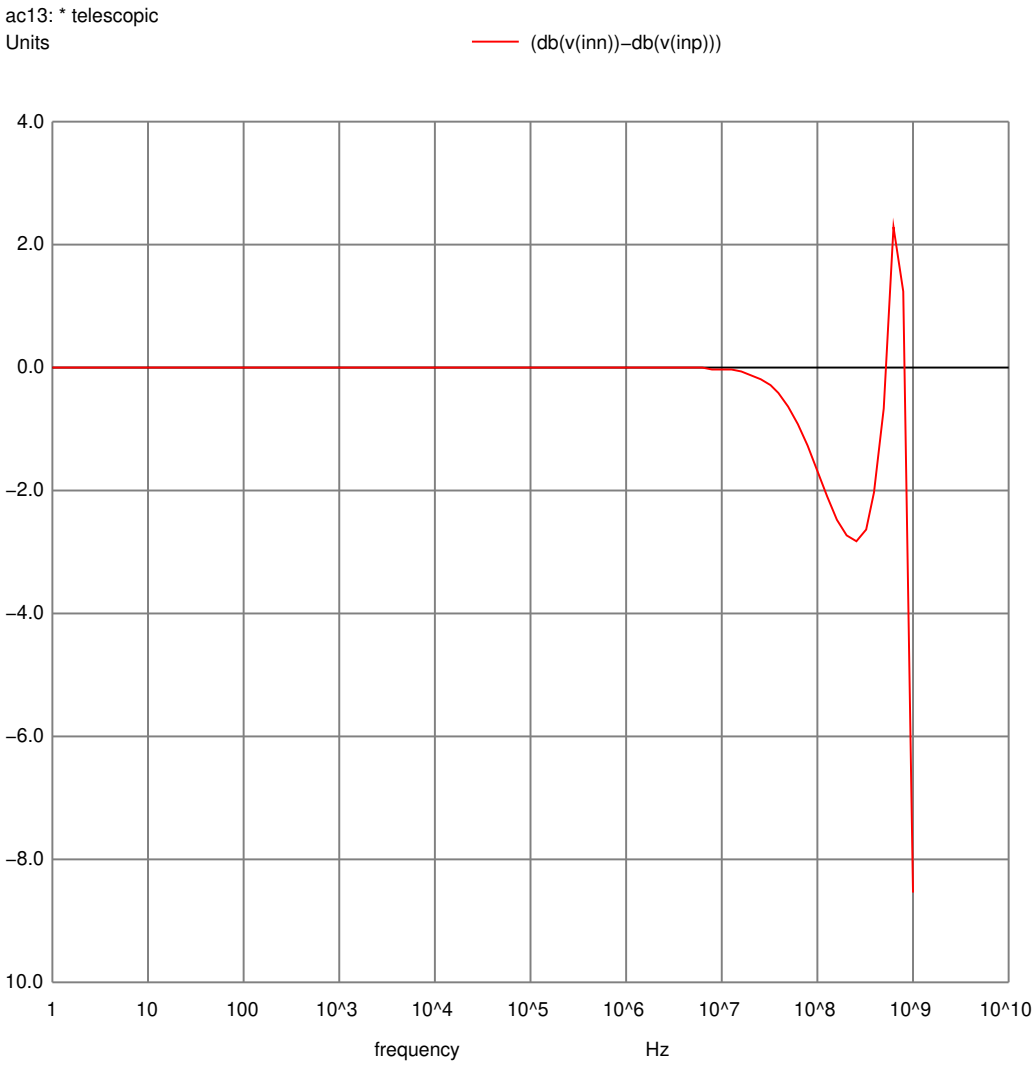


FIGURE 4.15
Closed loop gain

The closed loop gain is 0 dB or 1 V/V with a -3dB frequency of 0.861 GHz.

4.2.11 CLOSED LOOP TRANSIENT ANALYSIS

With the OTA in unity gain feedback mode, a sinusoidal signal of 10KHz frequency is applied for maximum signal swing at the output without distortion Fig. 4.16 shows the results obtained.

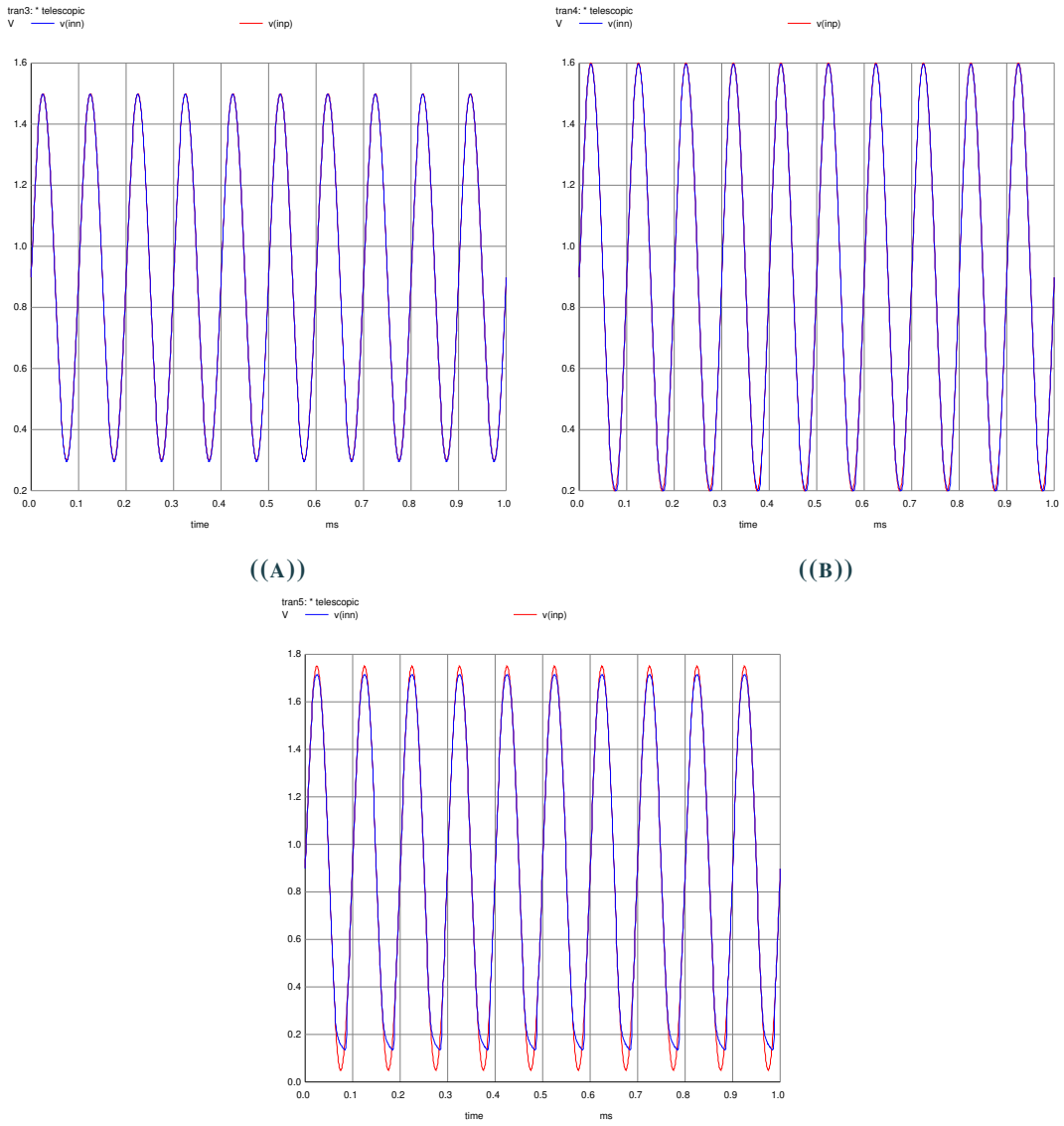


FIGURE 4.16
Closed loop transient analysis plots: (a) Output swing of 1.22 V, (b) Output swing of 1.4 V and (c) Output swing of 1.7 V

Output swing of 1.2 V can be obtained with THD less than 0.3% while a swing of 1.4 V increases the THD to 1.2%. Output swing of upto 1.7 V can be obtained with a THD of 5.5%.

4.2.12 POWER CONSUMPTION

The average value of current drawn by the OTA from supply in simulation is 580.116 μA and the total power consumption is 1.044 mW.

CHAPTER 5

DESIGN EXAMPLE

5.1 MULTIPLY-BY-TWO CIRCUIT

A multiply by 2 circuit can be constructed as shown in Fig. 5.1.

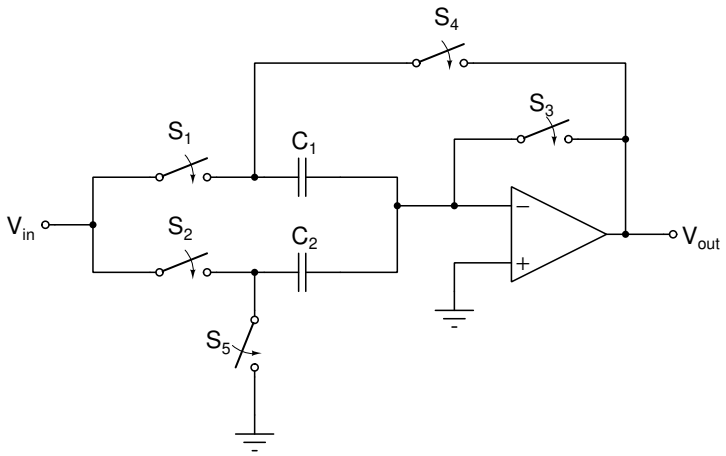


FIGURE 5.1
Multiply-by-2 structure

The switches are implemented using MOSFETs. The switching transistors and capacitors are selected such that sufficient precision and speed are ensured.

Table 5.1 shows the components and their respective sizing used in the circuit.

TABLE 5.1
Table showing design parameters of components used

Parameter	Used value
$\left(\frac{W}{L}\right)_s$ $(\frac{\mu m}{\mu m})$	10
C_1, C_2 (pF)	1

The ngspice netlist is as follows

```
* Multiply by 2
.include ../TSMC_180nm.txt

.param SUPPLY=1.8
.param LAMBDA=0.09u
.param length=0.36u

.param width_1234={0.36*71u}
.param width_5678={0.36*160u}
.param width_910={0.36*142u}
.param width_11={0.36*157u}
.param width_12={0.36*79u}

.param width_s={10u}
.param length_s={1u}

.global gnd vdd

Vdd     vdd     gnd     'SUPPLY'
Iref gnd ref 400u
Vb1 b1 gnd 1.4
Vb2 b2 gnd 0.7


vin in gnd 0.8

vs1 s1 gnd pwl(0 1.8 2.2u 1.8 2.201u 0 10u 0)
vs2 s2 gnd pwl(0 1.8 4u 1.8 4.501u 0 10u 0)
vs3 s3 gnd pwl(0 1.8 2.2u 1.8 2.201u 0 10u 0)
vs4 s4 gnd pwl(0 0 2.2u 0 2.201u 1.8 10u 1.8)
vs5 s5 gnd pwl(0 0 2.8u 0 2.801u 1.8 10u 1.8)

Cc d4 k 2p
Rs k out 1k

M1      d1      inn     d9      gnd  CMOSN  W={width_1234}   L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M2      d2      gnd     d9      gnd  CMOSN  W={width_1234}   L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M3      d3      b1      d1      gnd  CMOSN  W={width_1234}   L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M4      d4      b1      d2      gnd  CMOSN  W={width_1234}   L={length}
+ AS={5*width_1234*LAMBDA} PS={10*LAMBDA+2*width_1234} AD={5*width_1234*LAMBDA} PD={10*LAMBDA+2*width_1234}
M5      d3      b2      d5      vdd  CMOSP  W={width_5678}   L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M6      d4      b2      d6      vdd  CMOSP  W={width_5678}   L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M7      d5      d3      vdd     vdd  CMOSP  W={width_5678}   L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}
M8      d6      d3      vdd     vdd  CMOSP  W={width_5678}   L={length}
+ AS={5*width_5678*LAMBDA} PS={10*LAMBDA+2*width_5678} AD={5*width_5678*LAMBDA} PD={10*LAMBDA+2*width_5678}


M9      d9     ref      gnd     gnd  CMOSN  W={width_910}   L={length}
+ AS={5*width_910*LAMBDA} PS={10*LAMBDA+2*width_910} AD={5*width_910*LAMBDA} PD={10*LAMBDA+2*width_910}
M10      ref      ref      gnd      gnd  CMOSN  W={width_910}   L={length}
+ AS={5*width_910*LAMBDA} PS={10*LAMBDA+2*width_910} AD={5*width_910*LAMBDA} PD={10*LAMBDA+2*width_910}

M11      out     d4      vdd     vdd  CMOSP  W={width_11}   L={length}
+ AS={5*width_11*LAMBDA} PS={10*LAMBDA+2*width_11} AD={5*width_11*LAMBDA} PD={10*LAMBDA+2*width_11}
M12      out     ref      gnd      gnd  CMOSN  W={width_12}   L={length}
+ AS={5*width_12*LAMBDA} PS={10*LAMBDA+2*width_12} AD={5*width_12*LAMBDA} PD={10*LAMBDA+2*width_12}



.subckt switch i o s
M1      i       s       o       gnd  CMOSN  W={width_s}   L={length_s}
+ AS={5*width_s*LAMBDA} PS={10*LAMBDA+2*width_s} AD={5*width_s*LAMBDA} PD={10*LAMBDA+2*width_s}
.ends


C1 inn s1s 1p
C2 inn s2s 1p
xsw1 in s1s s1 switch
xsw2 in s2s s2 switch
xsw3 inn out s3 switch
xsw4 s1s out s4 switch
xsw5 s2s gnd s5 switch


.tran 0.1u 10u


.control
run

plot v(in) v(s1s) v(s1)
plot v(in) v(s2s) v(s2)
plot v(inn) v(out) v(s3)
plot v(s1s) v(out) v(s4)
plot v(s2s) v(gnd) v(s5)
```

```
plot v(out)
* plot v(s1s) v(s2s) v(inn)

* plot v(out)/(v(inp)-v(inn))

.endc
```

5.2 TRANSIMPEDANCE AMPLIFIER (TIA)

A transimpedance amplifier takes current input and converts current into voltage. For a gain of 500K ohm, we connect a feedback resistor of value 500k ohm as shown in Fig. 5.2.

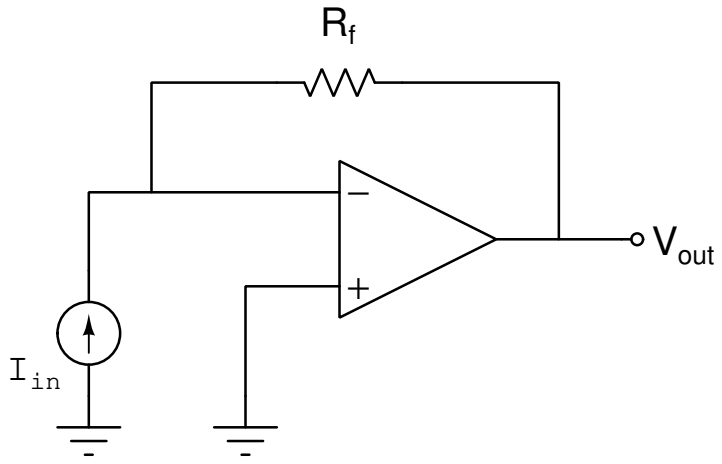


FIGURE 5.2
Transimpedance amplifier using OTA

The transimpedance gain of the circuit is given by Eq. (5.1).

$$\text{Transimpedance gain} = \frac{\Delta V_{out}}{\Delta I_{in}} \tag{5.1}$$

where ΔV_{out} is the peak to peak output voltage value and ΔI_{in} is the peak to peak input current value.

The following lines are added to the netlist to add the feedback resistor and the input current.

```
Rf out inn 500k

Iin gnd inn dc 1u ac 2u sin(1u 2u 10k 0 0 0)
```

An input current with AC amplitude equal to 0.5 μA is given to the TIA circuit. Fig. 5.3 shows the voltage output obtained.

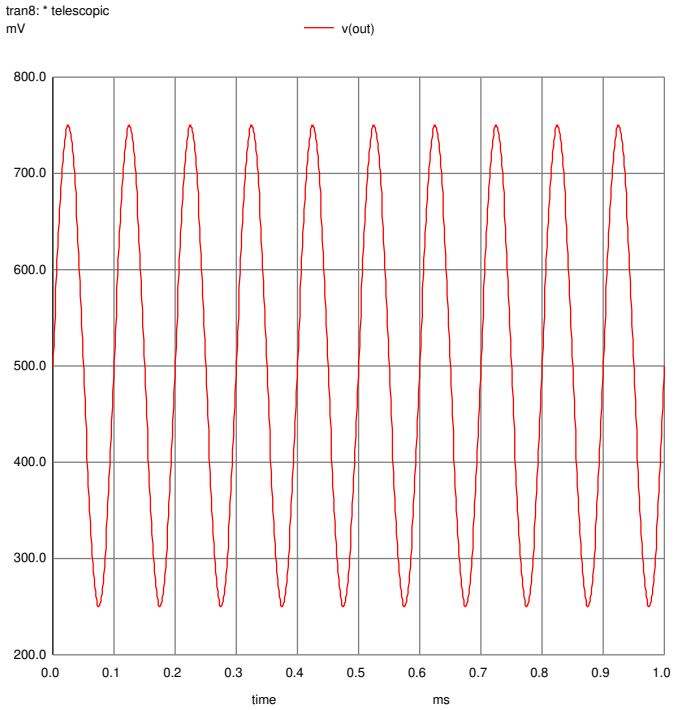


FIGURE 5.3
TIA transient analysis output

The gain can be verified from this transient analysis plot as follows

$$\text{Transimpedance gain} = \frac{\Delta V_{out}}{\Delta I_{in}} = \frac{0.750-0.250}{2\times 0.5\mu} = 500\ k\Omega$$

CHAPTER 6

RESULTS

6.1 TABULATION AND COMPARISON

Table 6.2 summarizes the schematic and post-layout simulation results compared to given requirements.

TABLE 6.1
Table summarizing opamp performance

Specification	Requirement	Schematic	Layout
DC gain (dB)	$\geq$80	93.68	93.38
Unity gain frequency (MHz)	$\geq$10	275.305	214.26
Phase margin (°)	$\geq$65	68	65
ICMR (V)	-	0.4 - 1.45	0.4 - 1.45
CMRR (dB)	-	92.22	91.98
PSRR (dB)	-	151.8	150.75
Slew rate (V/μs)	$\geq$100	179.50	184.07
Settling time (ns)	-	12.748	12.777
Systematic offset (μV)	-	3.45	4.3
Output swing (Vpp)	$\geq$1	1.6	1.6
RMS thermal noise (nV/$\sqrt{Hz}$)	10	4.69	4.70
Power (mW)	-	1.024	1.044

Table 6.2 presents the comparison of proposed OTA specifications with related works.

TABLE 6.2
Table showing comparison of proposed opamp with related works

Specification	[1]	[2]	[3]	[4]	[5]	Schematic	Layout
Technology (nm)	45	350	-	40	180	180	180
V_{DD} (V)	1	3.3	5	1.1	1.8	1.8	1.8
DC gain (dB)	100	78.21	80	49	74	93.68	93.38
Unity gain frequency (MHz)	25	5.81	3.8	3600	160	275.305	214.26
Phase margin (°)	50	64	70	65	75	68	65
ICMR (V)	-	2.15 - (-1.98)	4 - (-2.5)	-	-	0.4 - 1.45	0.4 - 1.45
CMRR (dB)	-	89.05	74	-	-	92.22	91.98
PSRR (dB)	-	117.73	84.5	-	-	151.8	150.75
Slew rate (V/μs)	-	5.58	-	1250	26.7	179.50	184.07
Power (mW)	0.012	0.284	-	3.3	0.477	1.024	1.044

6.2 RESULTS

The proposed OTA design implemented in 180nm CMOS technology achieves high gain 93.38 dB. It consumes 1.044 mW of power on a 1.8 V supply. The amplifier has a phase margin of 65° at a unity gain bandwidth 214.26 MHz. The proposed structure is also able to achieve high slew rates of >179 V/μs. The OTA is also resilient to variations in common mode voltage and supply voltage due to its high CMRR and PSRR. It is seen that the proposed design offers high gain and sufficiently high slew rate without compromising much on phase margin and the gain bandwidth as compared to related works.

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