C2i Semiconductors Pvt. Ltd

Total points 10/50

Written Test - 15 Nov 2024

Has 4 sections namely, i) Digital ii) Analog iii) Programming iv) Aptitude

The respondent's email (**aditiraj20032@gmail.com**) was recorded on submission of this form.

0 of 0 points

Phone *

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Name *

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Preferred Job role *

- ○ Analog Engineer
- ◉ Digital Engineer

College Name *

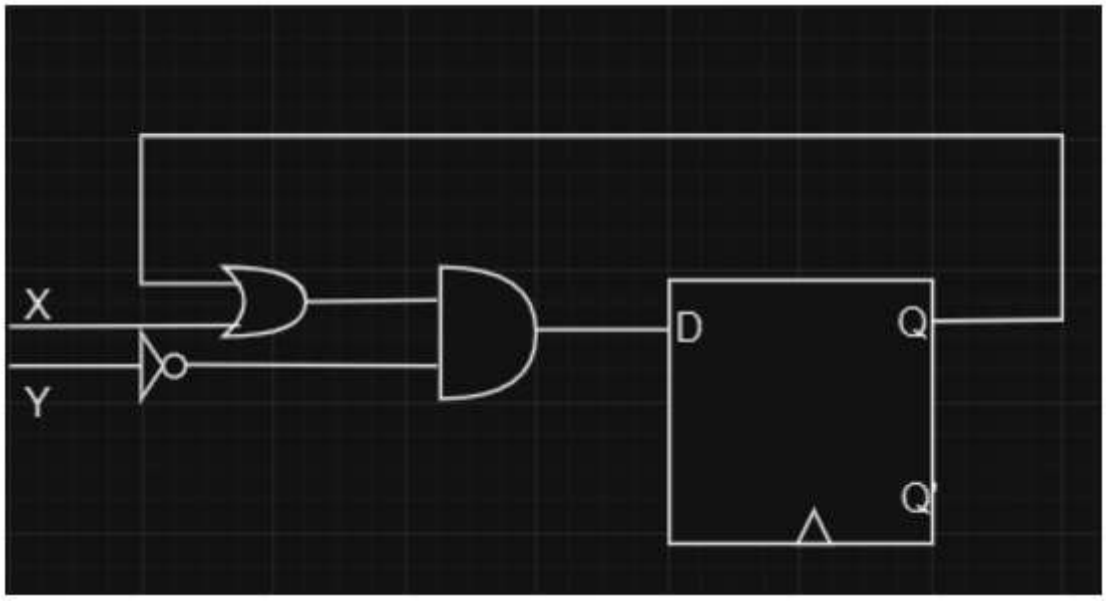
National Institute of Technology Andhra Pradesh

Digital Electronics

7 of 20 points

20 Marks

✓ Determine the characteristic equation of X-Y FF shown 1/1

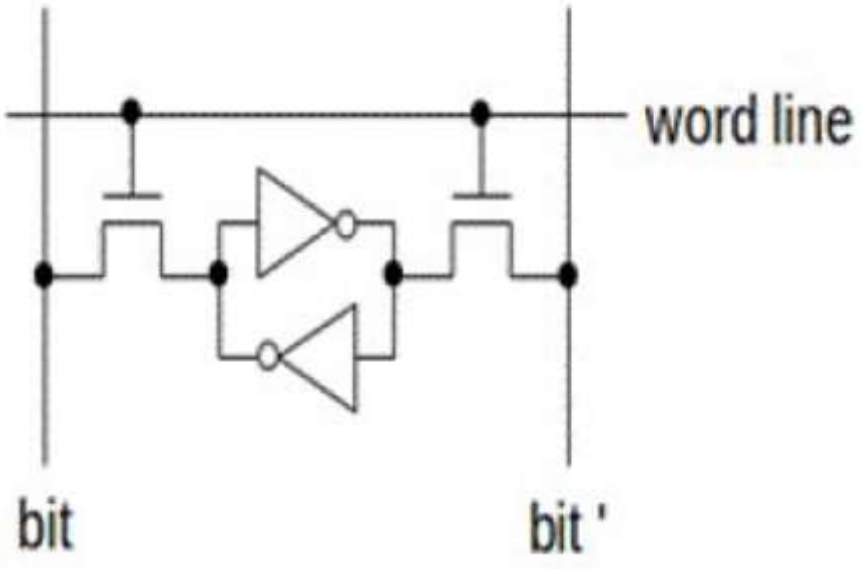


- ○ XY' +QY
- ◉ (Y+X'Q')' ✓
- ○ XY + Y'Q
- ○ None of the above

✕ The SRAM cell is given below. 0/2

Write operation: bit and bit' are forced and word line is made high.

Read operation: bit and bit' are precharged to VDD and word line is made high



- ○ Write will become tougher
- ◉ There is a high potential for read failure ✕
- ○ No difference at all
- ○ Write will become easier

Correct answer

- ◉ Write will become tougher

✗ What is the minimum size of FIFO required for an asynchronous FIFO whose writing clock frequency is 20MHz and reading clock frequency is 30MHz having 2 idle clocks for each read and burst write size is 10? 0/2

- ○ 2
- ◉ 3 ✗
- ○ 4
- ○ 5

Correct answer

- ◉ 5

✗ Optimize the logic using kmap.Input is assumed to 5 digit binary number (EDCBA , E=MSB) 0/1

input	output	input	output	input	output	input	output
0	1	8	1	16	1	24	1
1	1	9	0	17	1	25	0
2	X	10	1	18	1	26	x
3	0	11	0	19	0	27	0
4	1	12	0	20	x	28	x
5	1	13	0	21	1	29	0
6	0	14	0	22	0	30	0
7	0	15	0	23	0	31	0

- ○ kmap can not be used if there are more than 4 variables
- ◉ A'D' + B'D' ✗
- ○ A'C' + B'D'
- ○ None of the above

Correct answer

- ◉ A'C' + B'D'

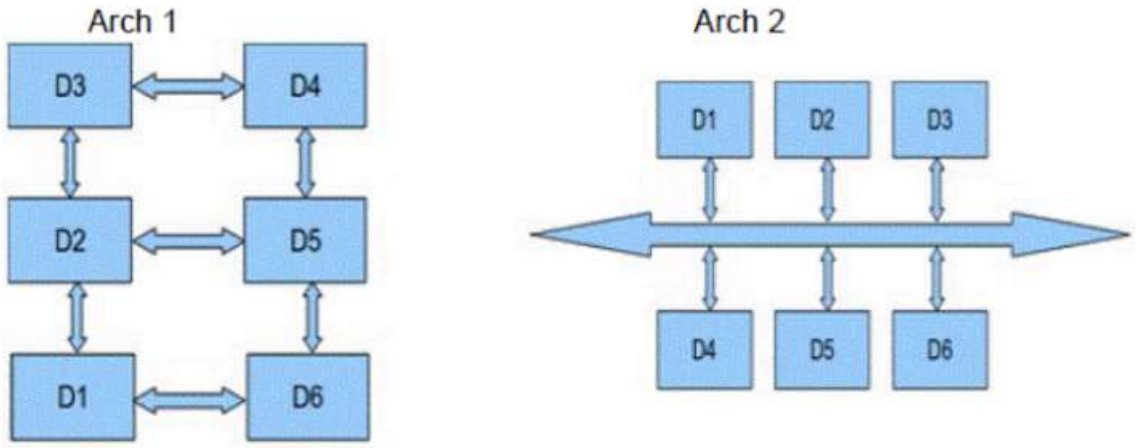
✗ In Verilog , for which of the following data values will the result of arithmetic shift right and logical shift right produce different results? 0/1

- ○ When the register contains the value 1
- ○ When the register contains the value 0
- ○ When the register contains the value -1
- ◉ For all of the above ✗

Correct answer

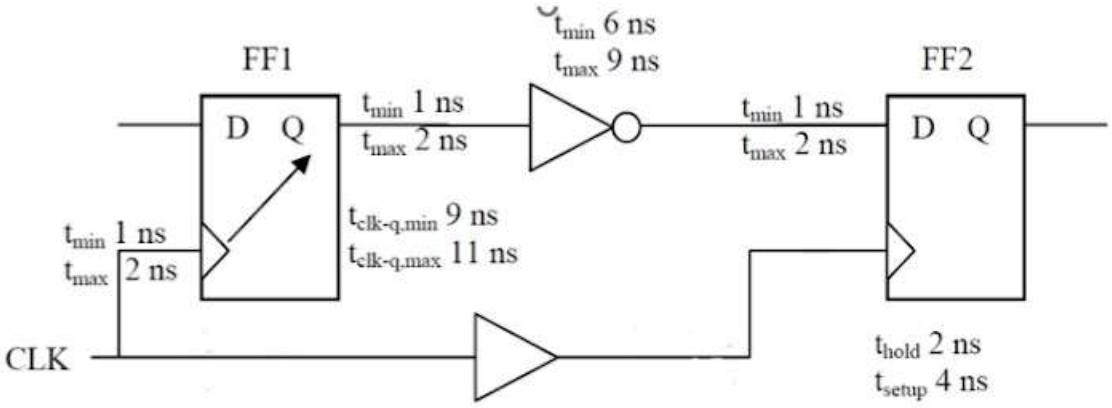
- ◉ When the register contains the value -1

✓ D1 to D6 are devices which communicate with each other via bus 1/1



- ○ Arch 1 is better in every aspect w.r.t Arch 2
- ◉ Arch 1 is better if data transfers is happening only between D1 & D6 ✓
- ○ Arch 1 is better if data transfers is happening only between D2 & D6
- ○ Arch 1 is better if data transfers is happening only between D3 & D6

✗ Calculate the max frequency of operation for the circuit shown below (in MHz) 0/2

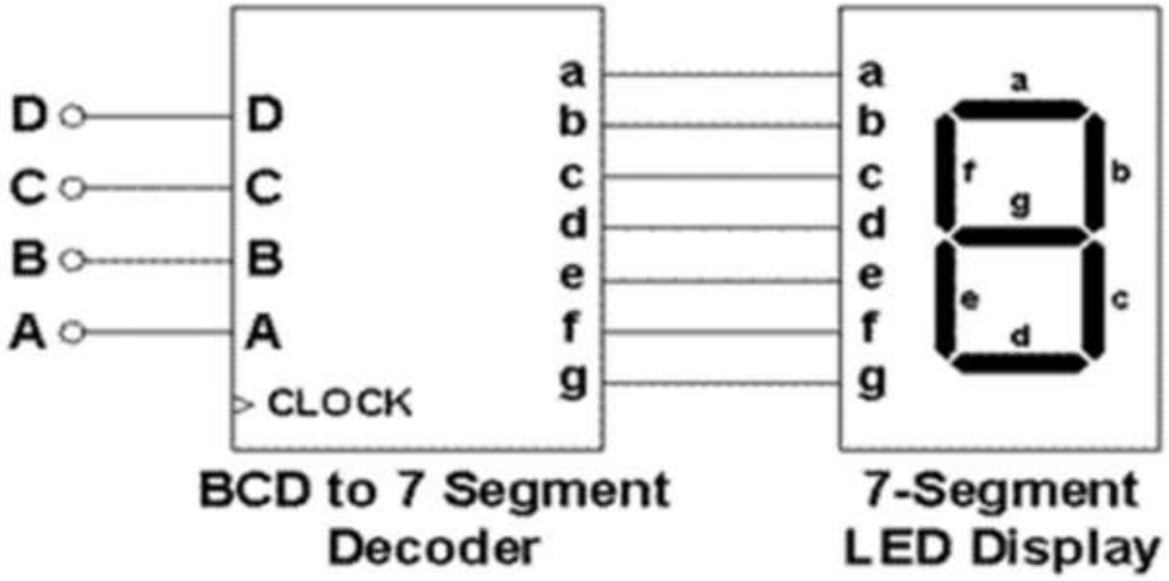


1 ✗

Correct answer

33.33

✕ In the BCD to 7-segment decoder circuit shown below, which of the following correctly describes the signal "b"? 0/2



- ○ b = B' + C'D'
- ◉ b = B + CD ✕
- ○ b = B(C+D)
- ○ None of the above

Correct answer

- ◉ None of the above

✓ The output of a CMOS inverter appears to be stuck at logic 1. Which of the following is NOT a possible reason for this faulty behavior? 1/1

- ○ The input is shorted to ground
- ◉ The NMOS transistor's gate is permanently closed ✓
- ○ The NMOS transistor's gate is permanently open
- ○ The PMOS transistor's gate is permanently closed

✓ In a binary fixed point system with 2's complement representation, a number format is specified
fix(WL,FL) WL is the total number of bits (word length).
FL is the number of bits user for fraction length.
For binary fixed point, if absolute value of smallest positive number is x and absolute value of smallest
negative number is y then 1/1

- ○ x and y are always different
- ◉ x and y are always same ✓
- ○ x and y are same if signed and (WL1)==2*FL
- ○ x and y are same if signed and (WLFL)<(FL+1)

✗ Months in the year are numbered from 1 to 12. January 1, December is 12. If ABCD represents the binary encoding of the month number, which of the following implements a logic that detects all months that have 31 days? 0/1

The function F must be 1 when the month represented by ABCD has 31 days

- ad+a'bd+ac
- a'd+bd+ac ✗
- None of the above
- abd+a'c+cd'

Correct answer

- None of the above

✓ The duty cycle of the most significant bit from a 4-bit (0–9) BCD counter is 1/1

- 10%
- 20% ✓
- 50%
- 80%

✗ Minimum number of 2:1 muxes needed to implement (Only X, Y, Z, VDD, GND are available at your disposal) 0/2

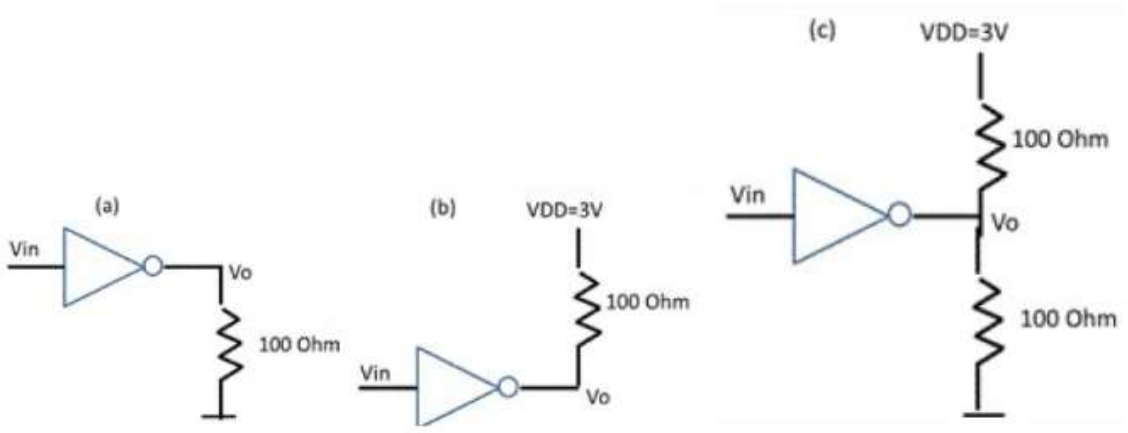
M(X,Y,Z) = X'Y'Z + X'YZ + XY'Z'+ XY'Z

3 ✗

Correct answer

2

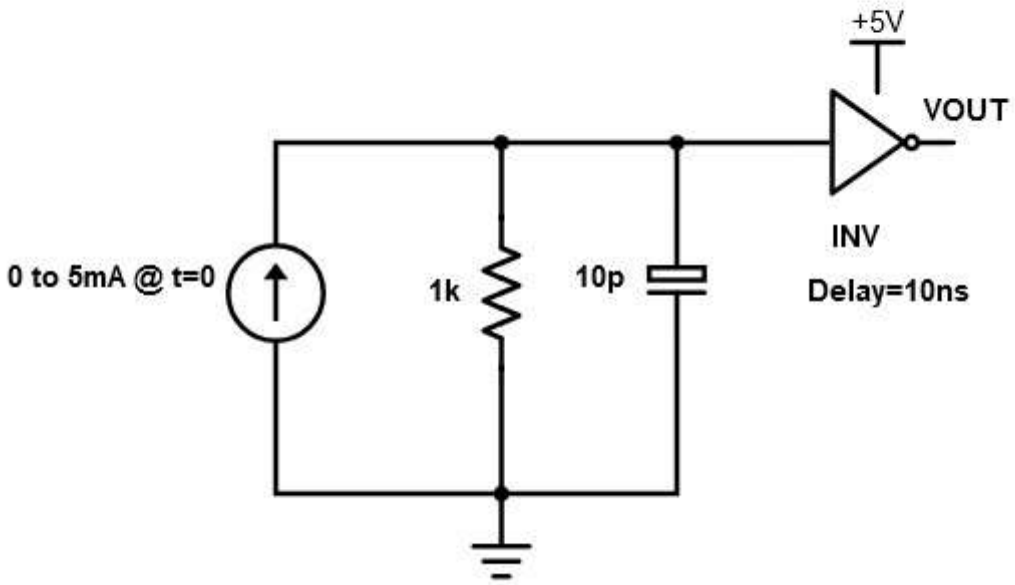
✓ CMOS inverter runs off a 3V supply (with ground at 0V) and is loaded in 3 different ways as shown in (a), (b), (c) below. In (a), it is seen that the logic high level is 2.5V. In (b), it is seen the logic low level is 0.5V. What is the expected logic high level in (c)? 2/2



- 1.5 V
- 2.5 V ✓
- 2.75 V
- 3 V

20 Marks

✗ In the below circuit inverter has switching threshold of ~2.52V and delay of 10ns, Calculate the time at which changes its output state from High to Low 0/2

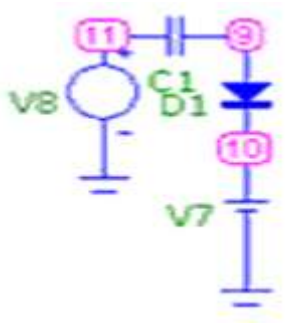


- ○ 15ns
- ◉ 20ns ✗
- ○ 17ns
- ○ 14ns

Correct answer

- ◉ 17ns

✗ If the output is between node 9 and ground, the circuit is known as 0/1

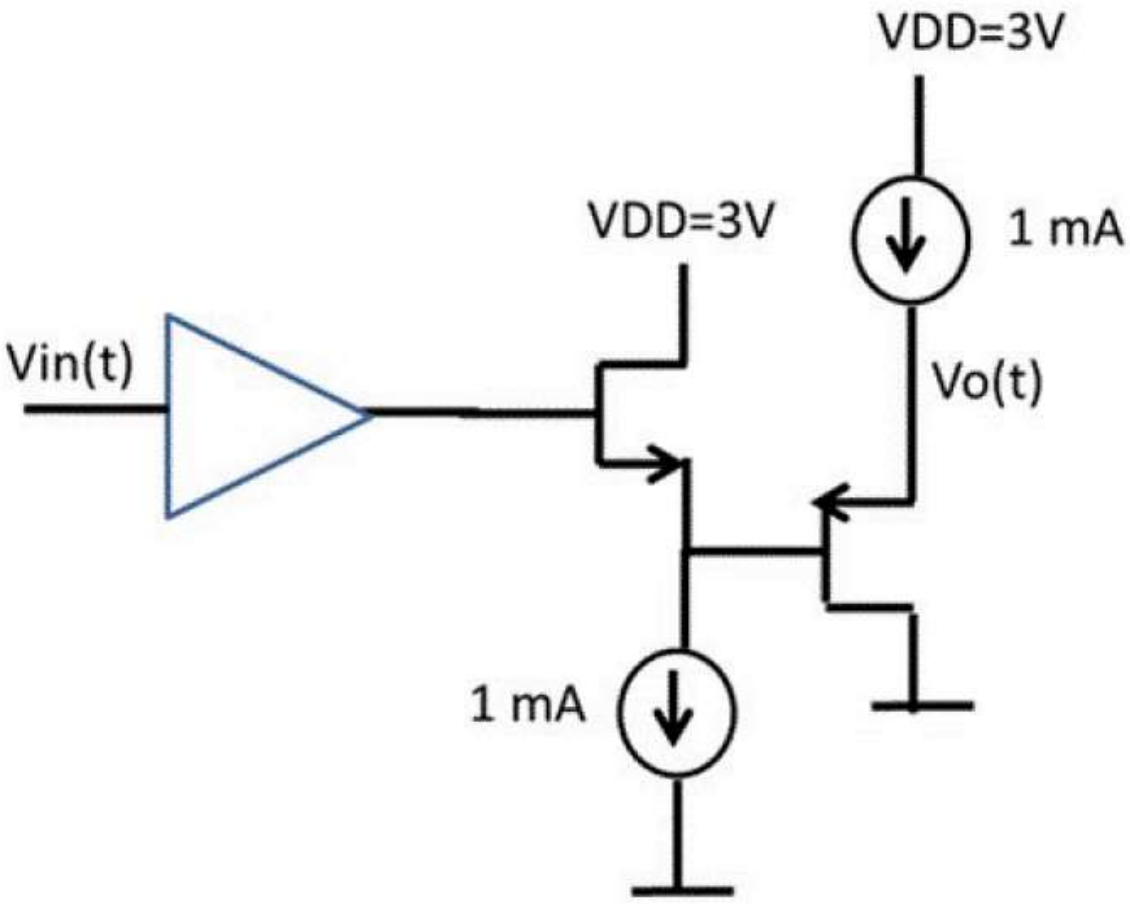


- ○ Clamping Circuit
- ◉ Clipping circuit ✗
- ○ Voltage Doubler
- ○ Resonant circuit

Correct answer

- ◉ Clamping Circuit

✗ The buffer has a DC gain of G and an output impedance of 1 kOhm. Both transistors (NMOS and PMOS) operate in saturation and have gm=0.8 mS, gds=0.2 mS. What is the value of G if Vo(t)/Vin(t) is equal to 100 ? 0/1

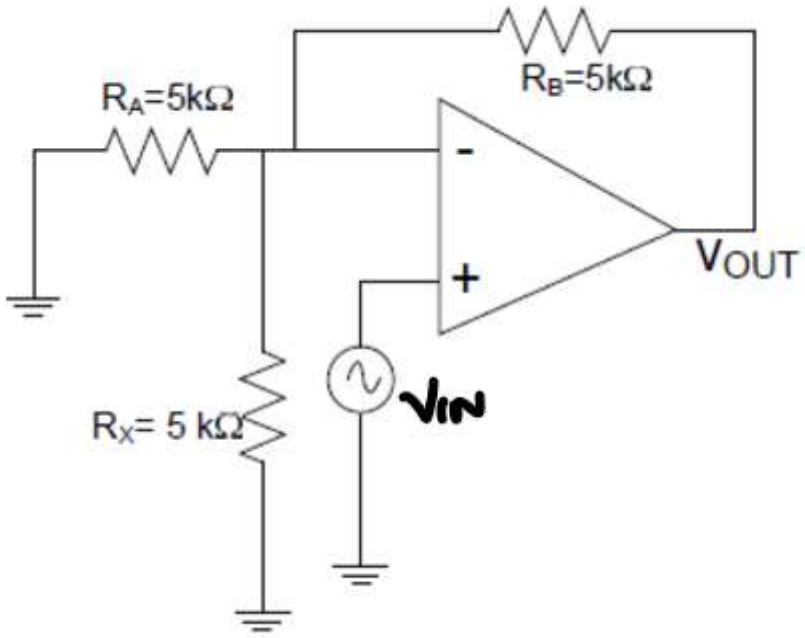


- ○ 156.25
- ◉ 100 ✗
- ○ 125
- ○ 6.25

Correct answer

- ◉ 156.25

✕ Assuming the Open loop amplifier is a single pole system with High gain; What is bandwidth of the closed loop amplifier given below (given Unity Gain Frequency =1MHz) : 0/1



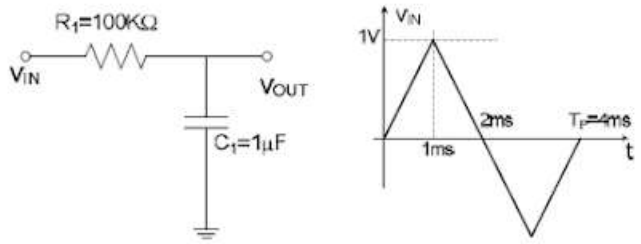
- 1 MHz
- 0.5 MHz ✕
- 0.33 MHz
- 2 MHz

Correct answer

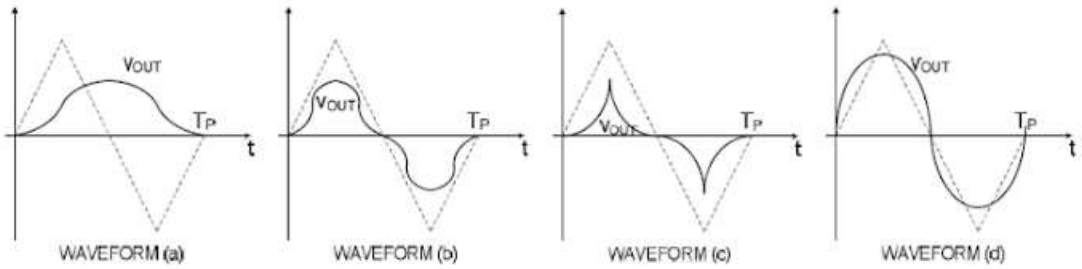
- 0.33 MHz

✕ For the simple RC network shown below, an input vin is applied which varies 0/2

linearly with time. For the waveform, TP << R1C1



Which of the following waveforms best describes the shape of waveform Vout ?



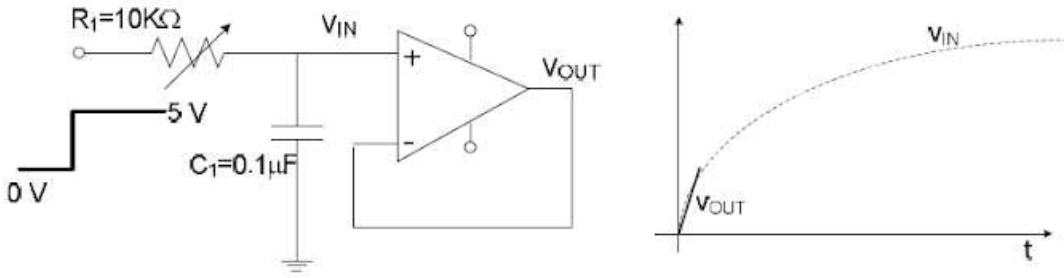
- ○ Waveform (a)
- ○ Waveform (b)
- ○ Waveform (c)
- ◉ Waveform (d) ✕

Correct answer

- ◉ Waveform (a)

✗ Having studied the behavior of RC circuits, a student wants to observe the step response (for a 5V step) of a simple RC circuit for different values of R and C. He builds a unity gain buffer amplifier with a purpose of connecting the response of the RC Circuit Vin to an Analog to Digital converter. Using a variable resistance for R1 he starts with R1=10KOhms and keeps decreasing R1 (keeping C1=0.1uF constant) and suddenly finds that at one particular value of R1, the waveform at VOUT no longer looks like an exponential but the initial part is a straight line. The student looks up the data sheet of the opamp and finds the slew rate = 0.5V/ms. 0/2

What value of R1 would be the one where this limitation begins to appear ?

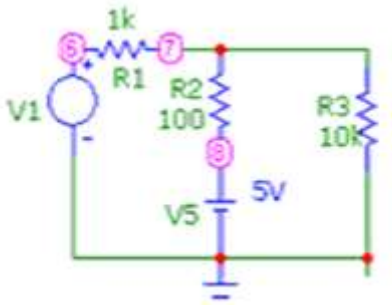


- ○ 200 Ohms
- ◉ 50 Ohms ✗
- ○ 1K Ohms
- ○ 100 Ohms

Correct answer

- ◉ 100 Ohms

✕ A Zener diode regulator is represented by a dc voltage source of 5V in series with 100 ohm as shown in the figure. If the input varies between 6 and 9V, the line regulation (ratio of change in output voltage to the change in the input voltage, where voltage at node 7 is the output voltage and V1 is the input voltage) of the circuit is: 0/1



- ○ 2%
- ◉ 3% ✕
- ○ 6%
- ○ 8%

Correct answer

- ◉ 6%

✗ The first and last critical frequencies of a driving point impedance function of a passive network having two kinds of elements are a pole and zero respectively. This property will be satisfied by - 0/1

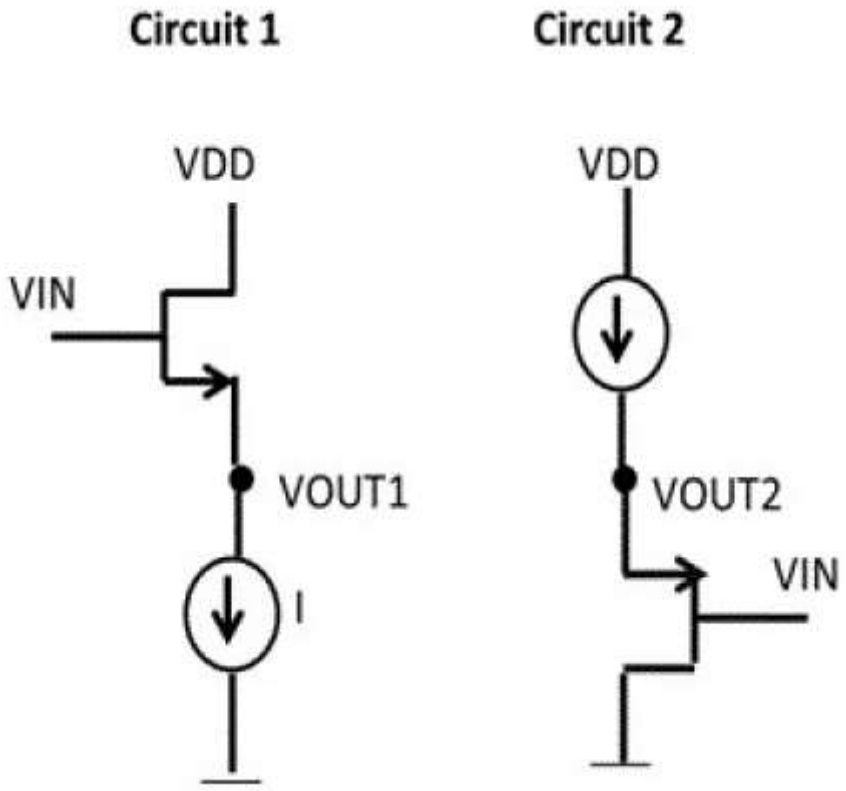
- ○ RL network
- ◉ RC network ✗
- ○ LC network
- ○ None of the above

Correct answer

- ◉ None of the above

✗ Two circuits are shown below. The same input VIN is given to both circuits. In each circuit, the current source is ideal and the transistor operates in saturation. The NMOS has a Vgs=1V and the PMOS has a Vsg=1V. The small signal gain of Circuit 1 (from VIN to VOUT1) is G1 whereas the small signal gain of Circuit 2 (from VIN to VOUT2) is G2. Next, the 2 circuits are connected in parallel, with VOUT1 andVOUT2 shorted. 0/2

What is the approximate small signal gain of the parallel circuit if: G1 = 0.9, G2 = 0.8



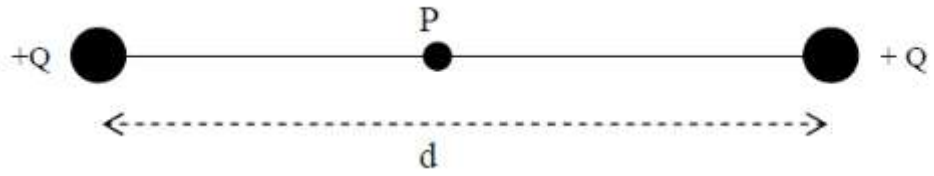
1 ✗

Correct answers

0

0.0

✕ Two charges both equal to +Q are placed at a distance “d” from each other. Consider the mid point “P” of the line joining them. Which of the following statements is applicable to this point “P” 0/1

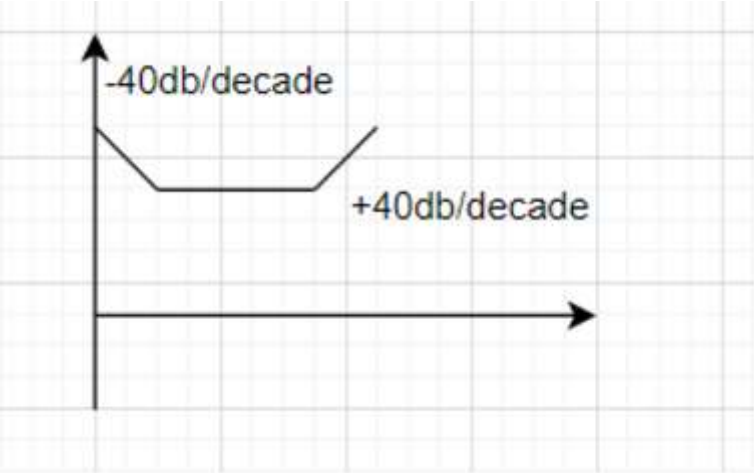


- ○ Electric Field is zero but Electric Potential is non-zero
- ○ Electric Potential is zero Electric Field is non-zero
- ○ Both Field and Potential are zero
- ◉ Both Field and Potential are non-zero ✕

Correct answer

- ◉ Electric Field is zero but Electric Potential is non-zero

✗ The Bode plot shown below corresponds to which of the transfer functions below - 0/1

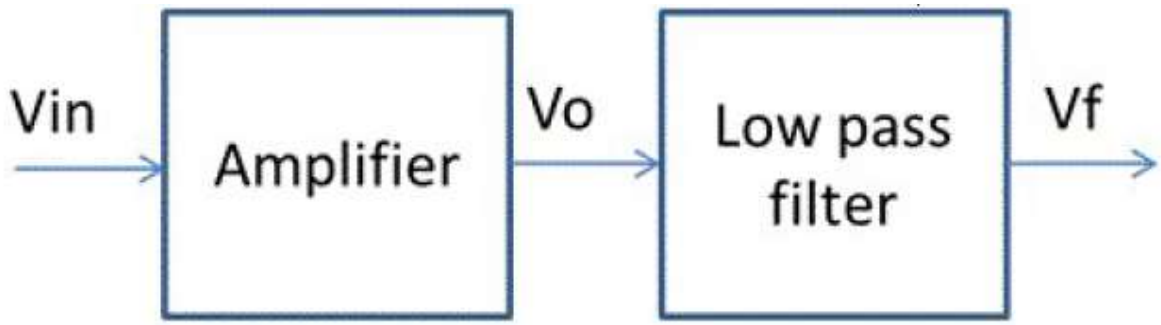


- ○ (k(s+2)(s+2)) / (s(s+1)(s+1))
- ◉ (k(s+2)(s+2)) / (s(s+4)(s+4)) ✗
- ○ k/(s(s+2)(s+2))
- ○ None of above

Correct answer

- ◉ None of above

✕ An amplifier has a nonlinear response given by (Vo = Vin + Vin^3) at all frequencies. When a sine wave of amplitude 1V is input to the amplifier, the output of the amplifier contains a harmonic at 80 dBm. The amplifier output goes to a low pass filter with a 3 dB bandwidth of 1 MHz. What is the approximate amplitude of the harmonic at the output of the low pass filter if the input to the amplifier is a 3.33 MHz sine wave with an amplitude that is equal to 0.5 Volts? 0/2



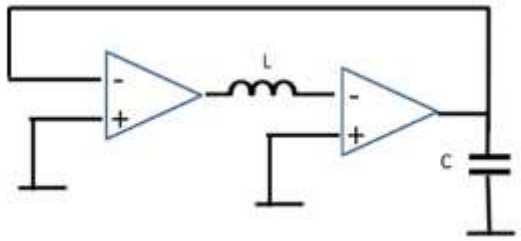
- ○ -106 dB
- ◉ -98 dB ✕
- ○ -78 dB
- ○ -118 dB

Correct answer

- ◉ -118 dB

✗ Assuming both the op amps are ideal, what is the frequency of oscillation? 0/1

L = 100 micro Henries, C = 1 micro Farad

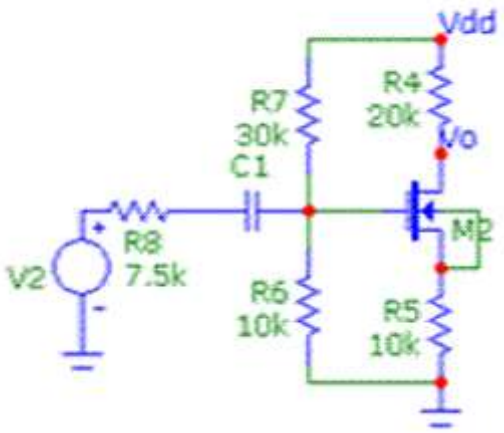


- ○ 1M rad/s
- ◉ 0.071M rad/s ✗
- ○ 0.01M rad/s
- ○ None of the above

Correct answer

- ◉ None of the above

✕ If we assume the gm of the MOSFET to be very high, the voltage gain, V0 / V2 of this amplifier is: 0/1

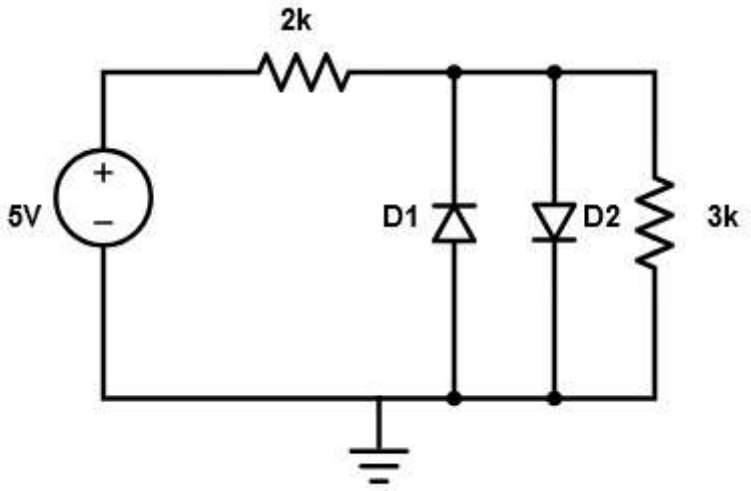


- ○ 1
- ◉ 2 ✕
- ○ -1
- ○ -2

Correct answer

- ◉ -1

✓ If the cut in Voltage of the diodes are 1V; Find the voltage across the 3K resistance 1/1



- ○ 2V
- ◉ 1V ✓
- ○ 3V
- ○ None of the Above

Programming Basics 1 of 5 points

5 Marks

✗ If ‘a’ is an integer array, which of the following is the odd one out? 0/1

- a[-3] = 1;
- *(a+3) = 1; ✗
- (*a+3) = 1;
- a[3] = 1;

Correct answer

- (*a+3) = 1;

✗ What is the output of below code 0/1

```
initial begin
 a = 2'd5;
 b = 3'd7;
 out = (b >> 1)**a;
 $display("out = %0d", out);
end
```

- 1
- 35 ✗
- 3
- 243

Correct answer

- 3

✗ What will be the result of the following program? 0/1

```
int i,j,k,s;

i = 5;
j = 50;
k = 500;
s = i+++j+++k;
printf("%d,%d,%d,%d",s,i,j,k);
```

- ○ 555,6,51,500
- ◉ 557,6,51,501 ✗
- ○ 557,5,51,501
- ○ Compilation Error

Correct answer

- ◉ 555,6,51,500

✗ What is the output of the following program? 0/1

```
main () {
 int a[] = {1,2,3,4,5,6,7};
 char c[] = {'a','x','h','o','k'};
 print {"%d\t, %d ", (&a[4]-&a[0], (&c[4]-&c[0]))};
}
```

- ○ 16, 4
- ◉ 4, 1 ✗
- ○ 4, 4
- ○ 8, 4

Correct answer

- ◉ 4, 4

✓ Which of the following is true? 1/1

- ○ Methods in derived classes can always access base class members
- ○ Methods in base classes can always access derived class members
- ◉ Methods in derived classes can overload virtual methods in base class ✓
- ○ Methods in base classes can overload virtual methods in derived class

Aptitude 1 of 5 points

5 Marks

✗ A simple linear pipeline has three stages. The execution times in the stages are 10, 15, and 12 units respectively. If the pipeline is used to process 100 inputs, then the execution time is

0/1

- ○ 1522 units
- ◉ 3700 units ✗
- ○ 3200 units
- ○ 2730 units

Correct answer

- ◉ 1522 units

✗ It is dark in my bedroom and I want to get two socks of the same color from my drawer, which contains 24 red and 24 blue socks. How many socks do I have to take from the drawer to get at least two socks of the same color?

0/1

- ○ 3
- ◉ 2 ✗
- ○ 4
- ○ 6

Correct answer

- ◉ 3

✗ A lotus lies in the middle of a round pool. The lotus doubles in size every day. After exactly 100 days the pool is fully covered by lotus. So, after how many days will half of the pool be covered by lotus _____? 0/1

98 ✗

Correct answer

99

✓ The area under the curve 1/x from x = 0.5 to x=1.0 is 1/1

- 1
- (●) Greater than 1 ✓
- Less than 1
- Infinity

✗ A speaks truth in 80% of the cases and B in 60% of the cases. Find the percentage of the cases of which they are likely to contradict each other in stating the same fact 0/1

- (●) 40 % ✗
- ( ) 44 %
- ( ) 24 %
- ( ) 43 %

Correct answer

- (●) 44 %