Computer system overview: Basic element, evolution of microprocessor, Instruction execution, Interrupt, Memory Hierarchy, Cache Memory, DMA, Multiprocessor and Multicore Organization

WS 1.1-1.2 (pg.29-32), WS 1.3-1.4 (pg.32-45), WS 1.5-1.8 (pg. 46-57)

BASIC ELEMENTS

1. Processor
2. Main memory
3. I/O modules
4. System bus

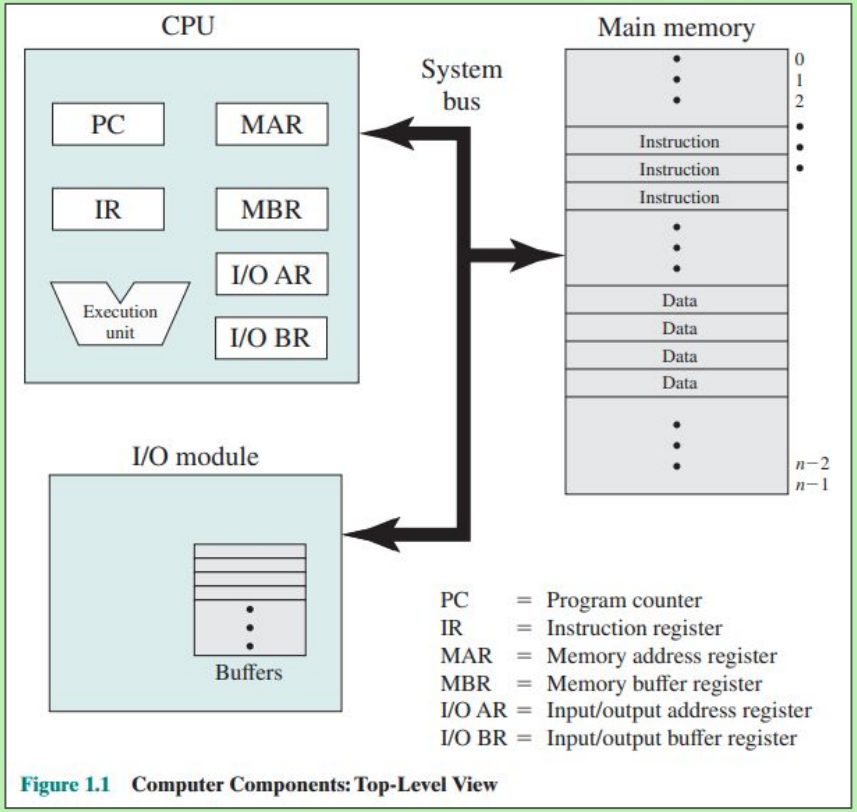


Figure 1.1 Computer Components: Top-Level View

EVOLUTION OF THE MICROPROCESSOR

1. Microprocessor: sub-nanosecond timeframes
2. Multiprocessors: multiple levels of large memory caches,
    a. multiple logical processors sharing the execution units of each core
3. Graphical Processing Units (GPUs) - SIMD
4. Digital Signal Processors (DSPs), other specialized computational devices (fixed function units) co-exist with the CPU to support other standard computations,
    a. such as encoding/decoding speech and video (codecs), or providing support for encryption and security.

INSTRUCTION EXECUTION

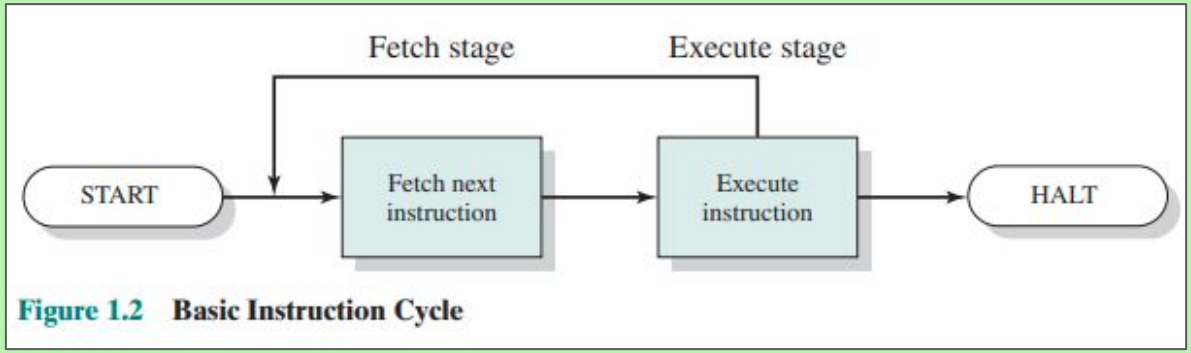


Figure 1.2 **Basic Instruction Cycle**

INSTRUCTION EXECUTION

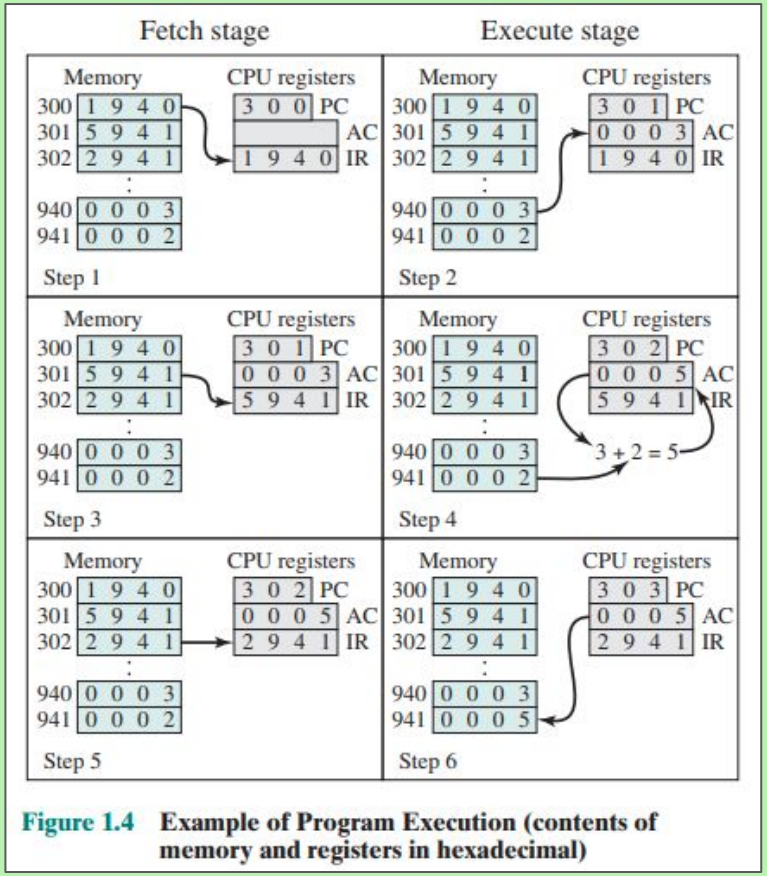
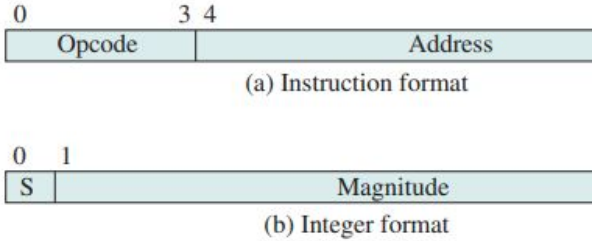


Figure 1.4 Example of Program Execution (contents of memory and registers in hexadecimal)



Program counter (PC) = Address of instruction
Instruction register (IR) = Instruction being executed
Accumulator (AC) = Temporary storage

(c) Internal CPU registers

0001 = Load AC from memory
0010 = Store AC to memory
0101 = Add to AC from memory

(d) Partial list of opcodes

Figure 1.3 Characteristics of a Hypothetical Machine

INTERRUPTS

Table 1.1 Classes of Interrupts

Program	Generated by some condition that occurs as a result of an instruction execution, such as arithmetic overflow, division by zero, attempt to execute an illegal machine instruction, or reference outside a user's allowed memory space.
Timer	Generated by a timer within the processor. This allows the operating system to perform certain functions on a regular basis.
I/O	Generated by an I/O controller, to signal normal completion of an operation or to signal a variety of error conditions.
Hardware failure	Generated by a failure, such as power failure or memory parity error.

INTERRUPTS

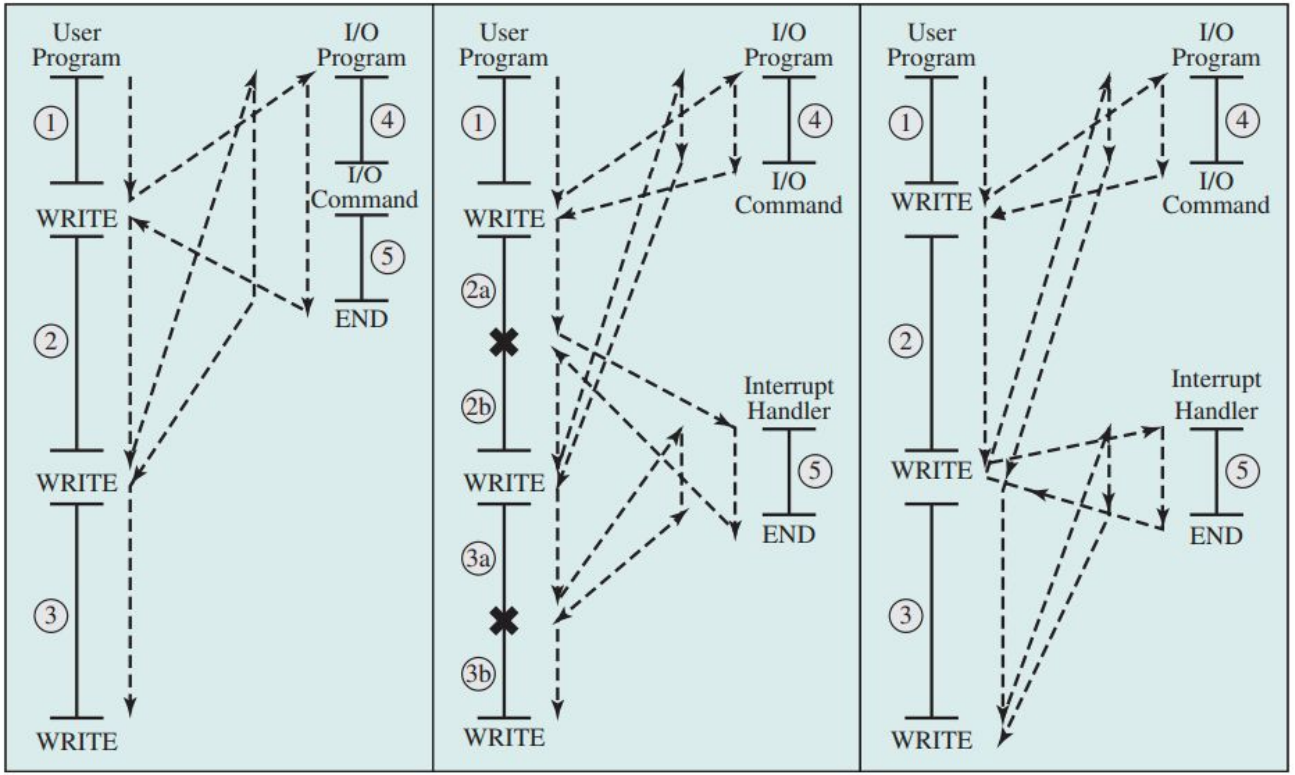


Figure 1.5 **Program Flow of Control Without and With Interrupts**

INTERRUPTS

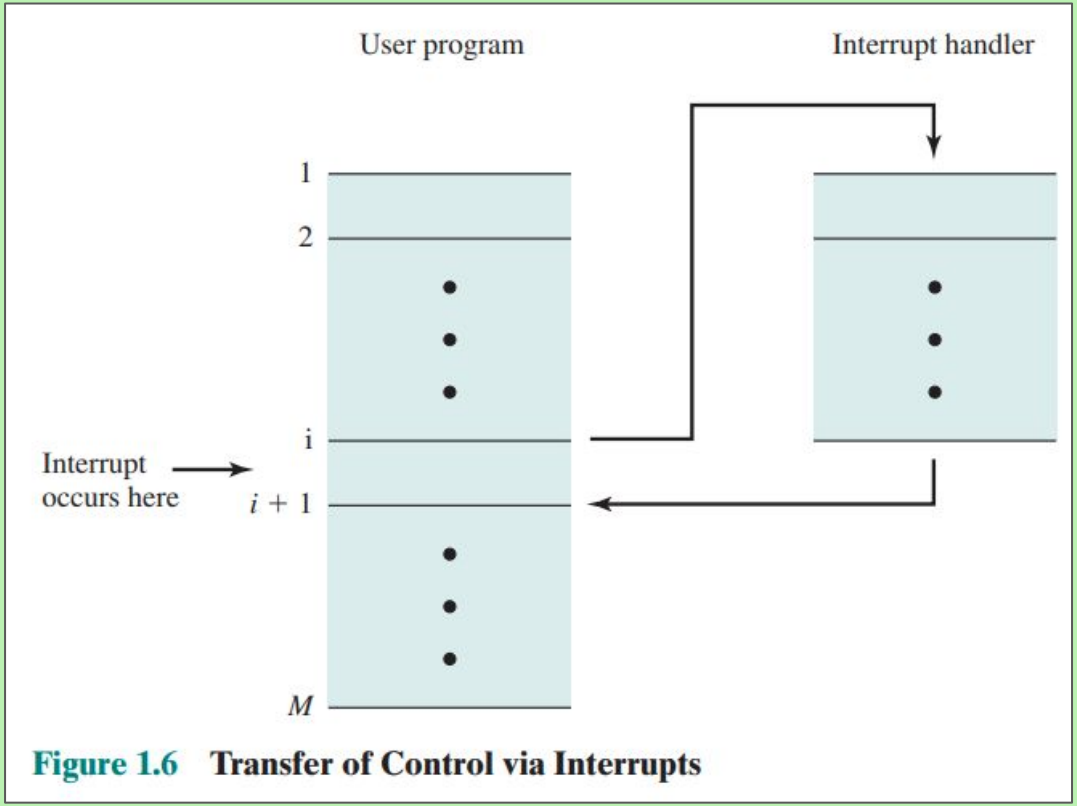


Figure 1.6 **Transfer of Control via Interrupts**

INTERRUPTS

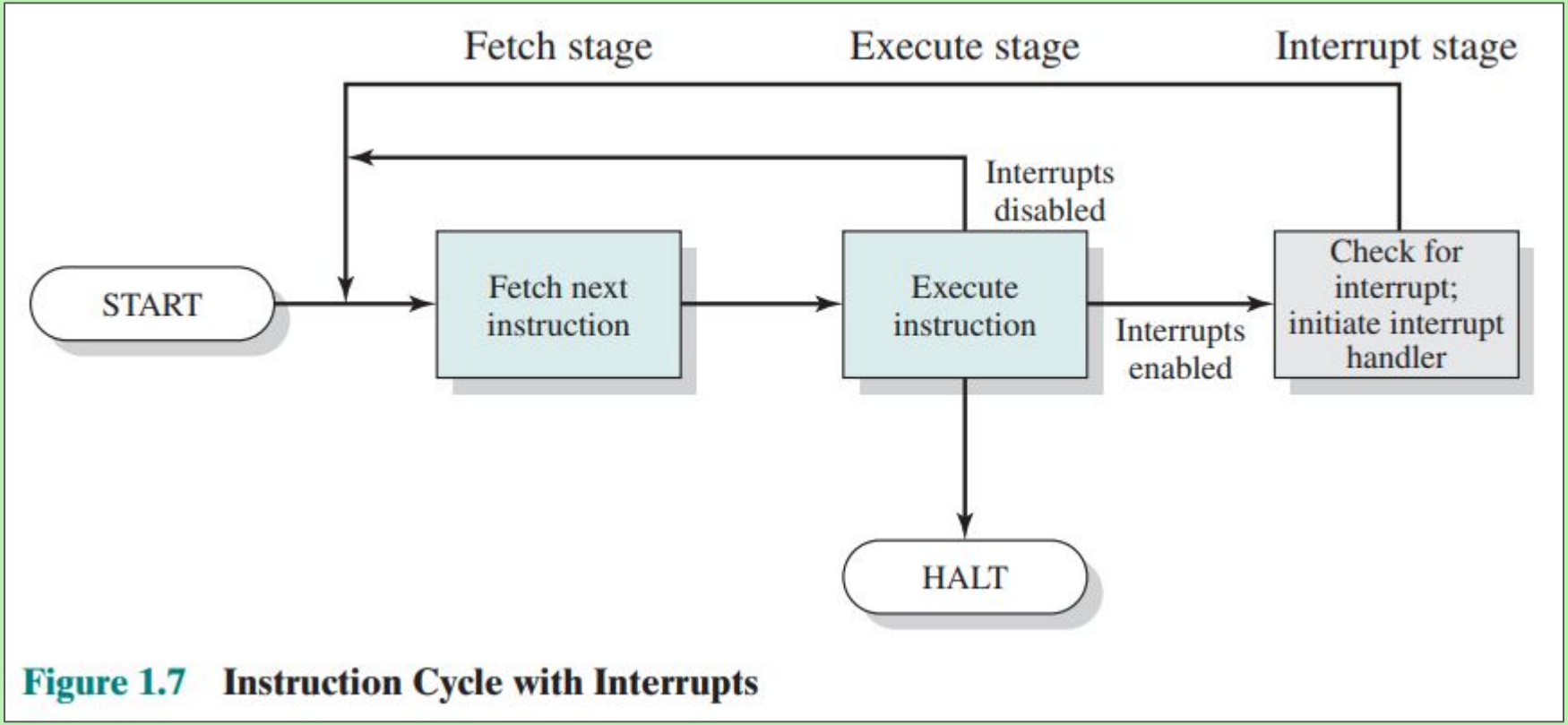


Figure 1.7 **Instruction Cycle with Interrupts**

INTERRUPTS

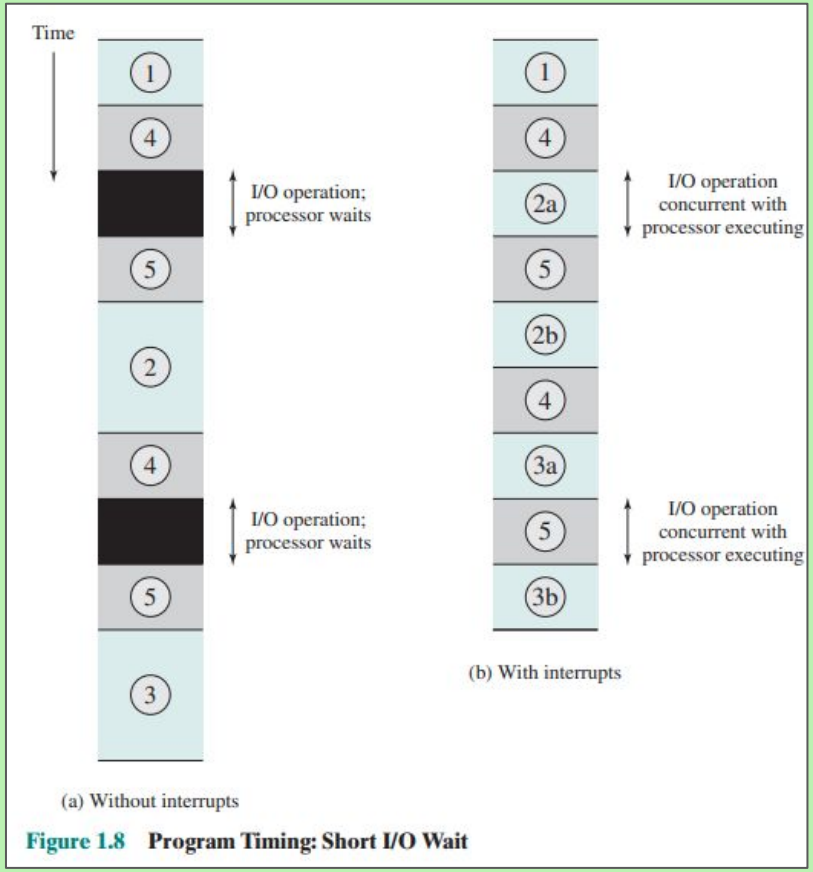


Figure 1.8 **Program Timing: Short I/O Wait**

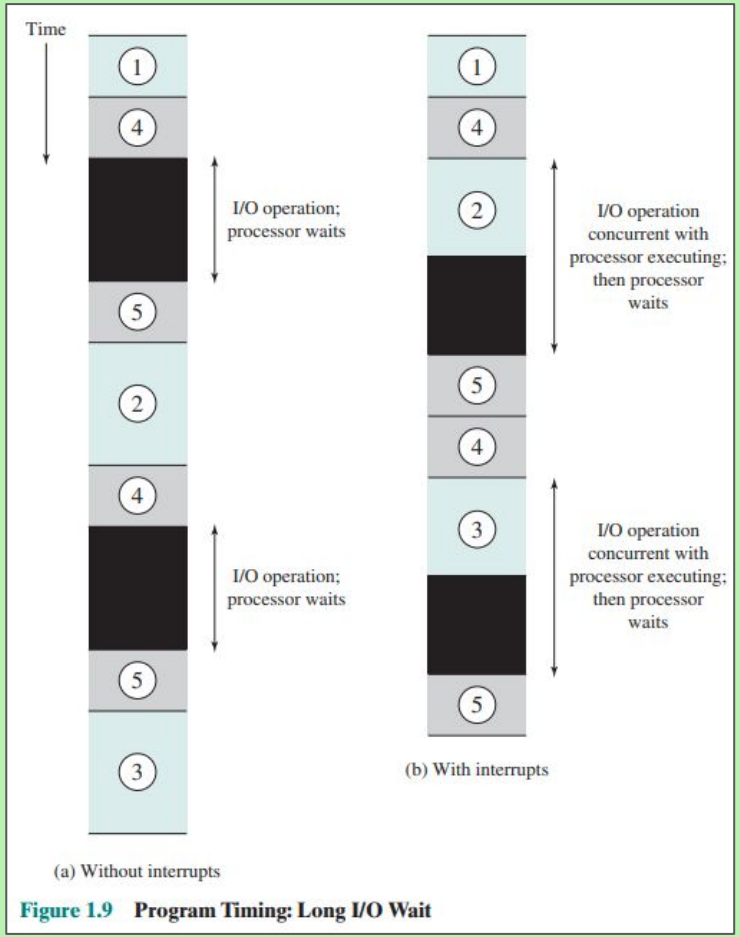


Figure 1.9 **Program Timing: Long I/O Wait**

INTERRUPTS

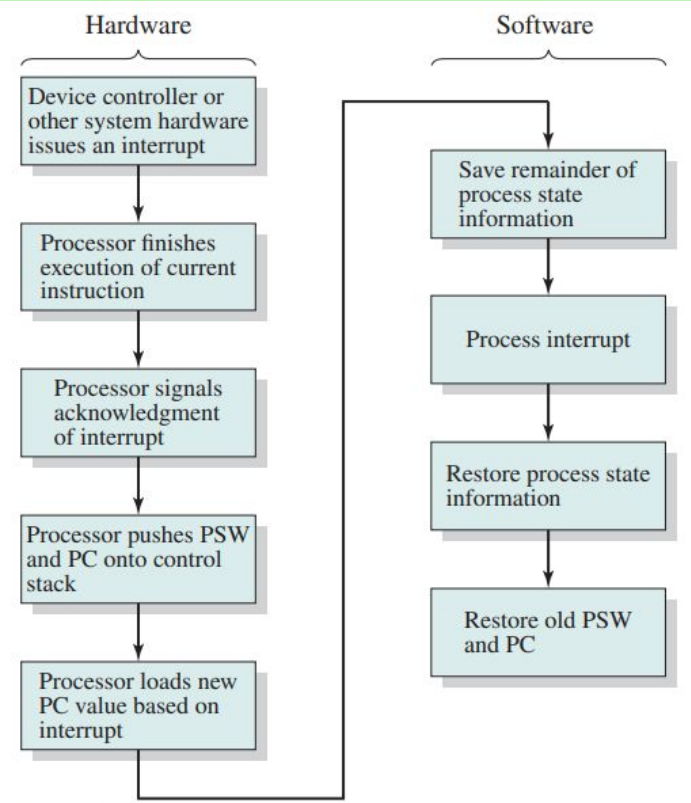


Figure 1.10 Simple Interrupt Processing

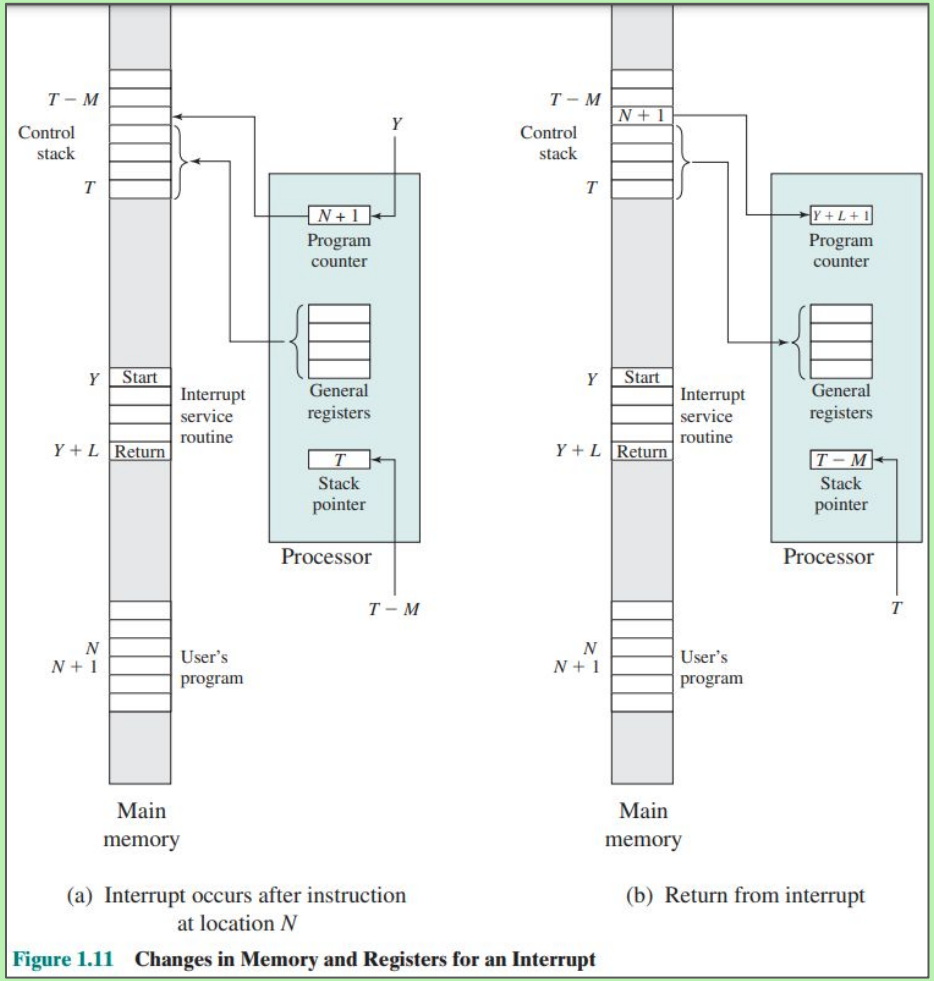


Figure 1.11 Changes in Memory and Registers for an Interrupt

THE MEMORY HIERARCHY

- Faster access time, greater cost per bit
- Greater capacity, smaller cost per bit
- Greater capacity, slower access speed
- As one goes down the hierarchy, the following occur:

  a. Decreasing cost per bit

  b. Increasing capacity

  c. Increasing access time

  d. Decreasing frequency of access to the memory by the processor

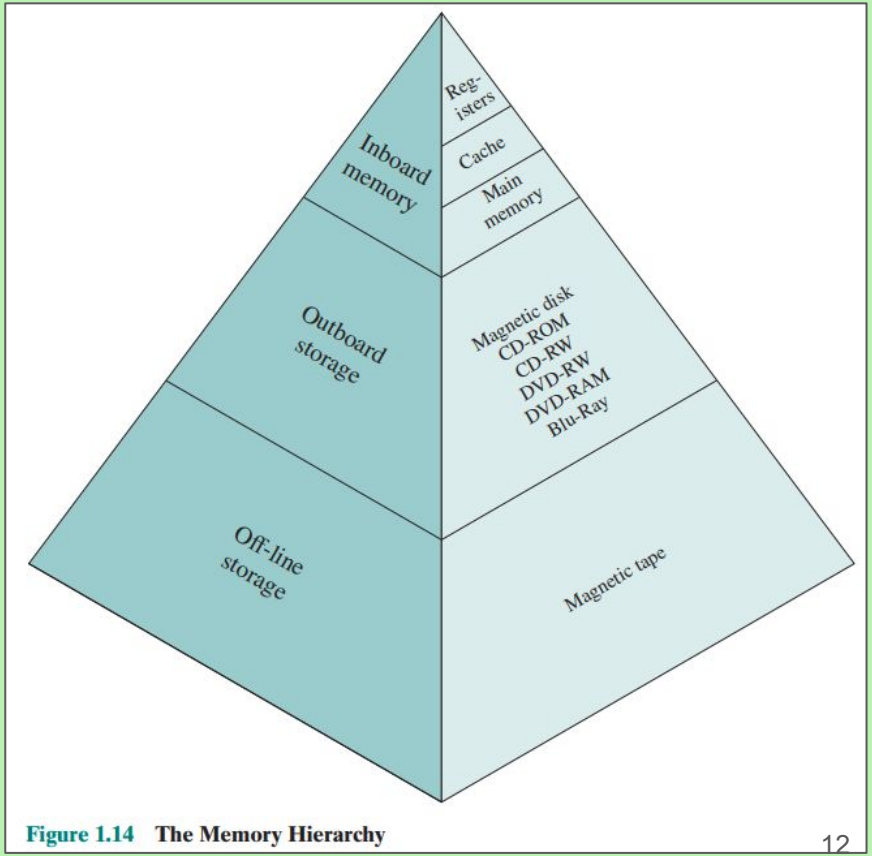


Figure 1.14 The Memory Hierarchy

CACHE MEMORY

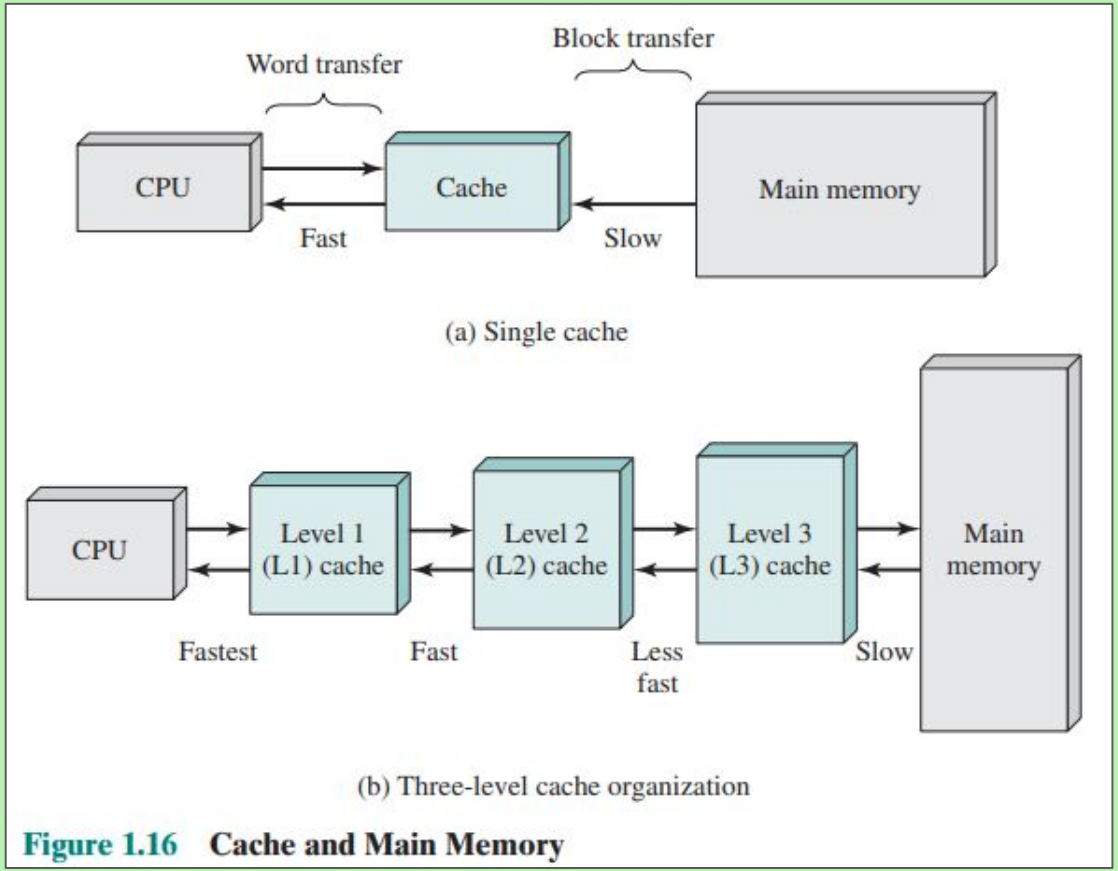


Figure 1.16 **Cache and Main Memory**

CACHE MEMORY

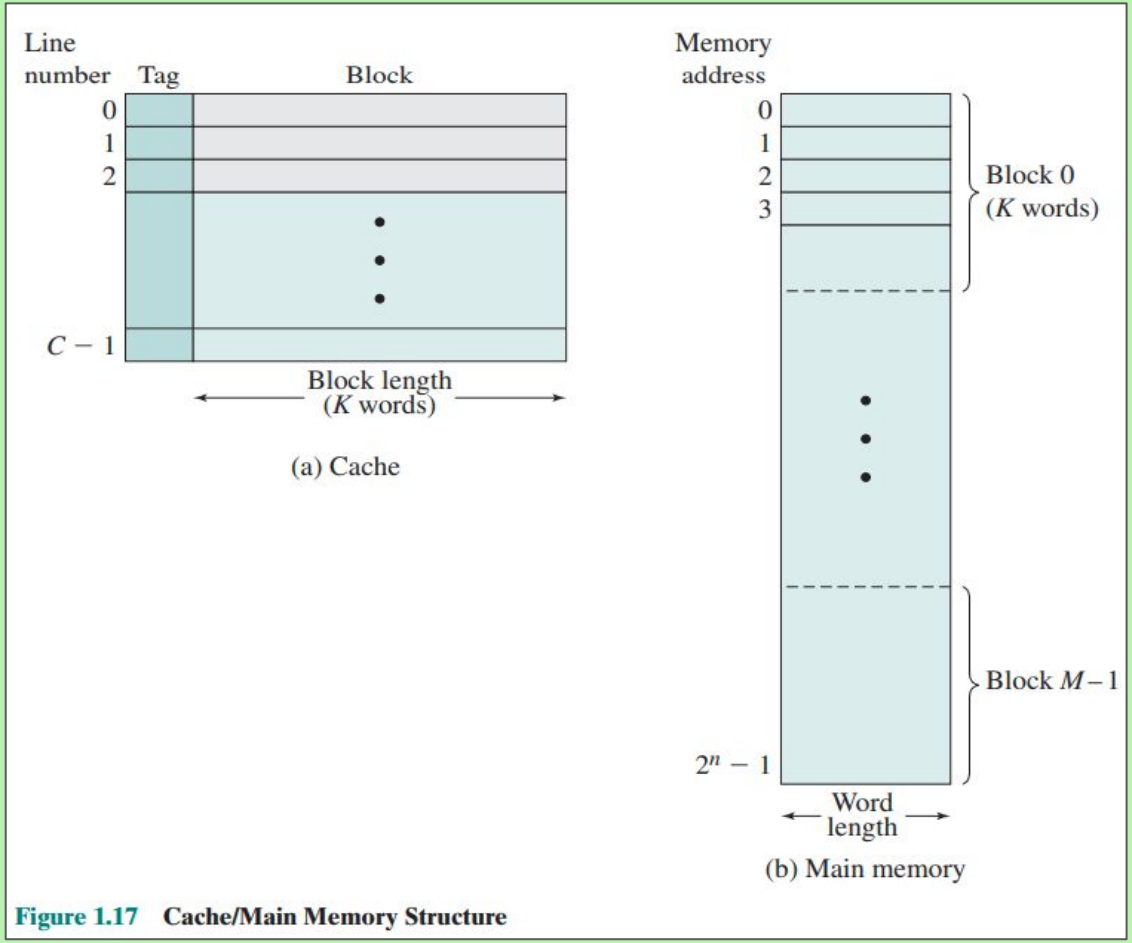


Figure 1.17 Cache/Main Memory Structure

CACHE MEMORY

- Cache size
- Block size
- Mapping function
- Replacement algorithm
- Write policy
- Number of cache levels

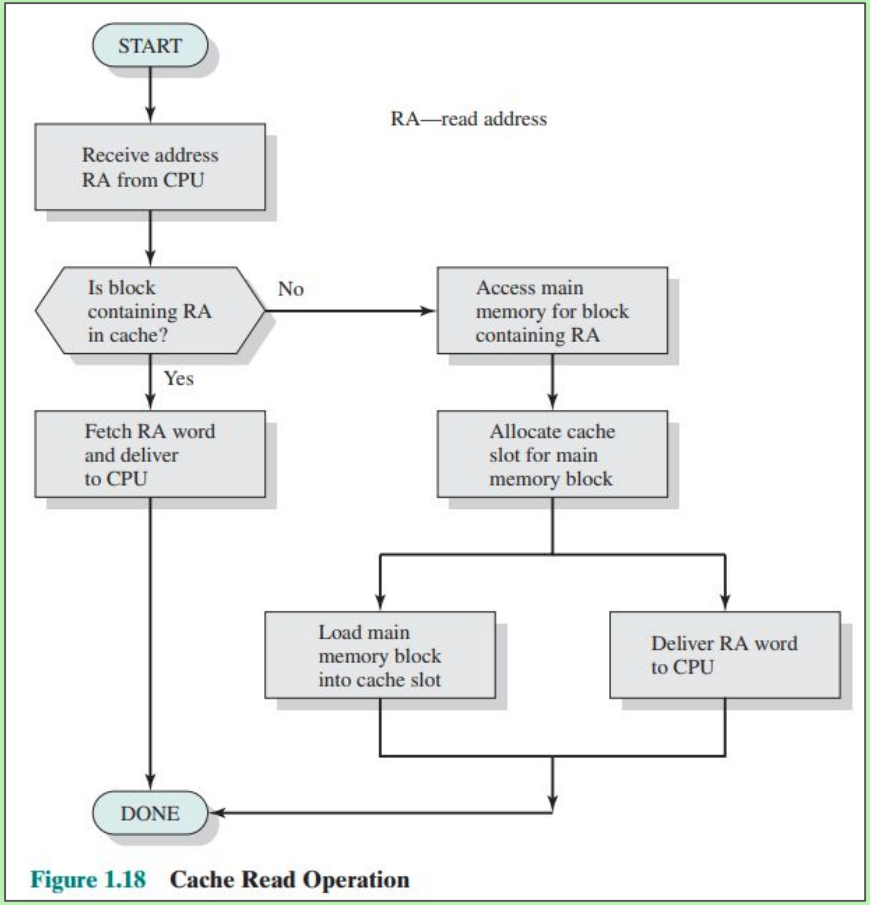


Figure 1.18 Cache Read Operation

DIRECT MEMORY ACCESS

- programmed I/O
- interrupt-driven I/O
- direct memory access (DMA)

1. When the processor wishes to read or write a block of data, it issues a command to the DMA module by sending the following information:
    - read or write is requested
    - the address of the I/O device involved
    - the starting location in memory to read data from or write data to
    - the number of words to be read or written

MULTIPROCESSOR AND MULTICORE ORGANIZATION

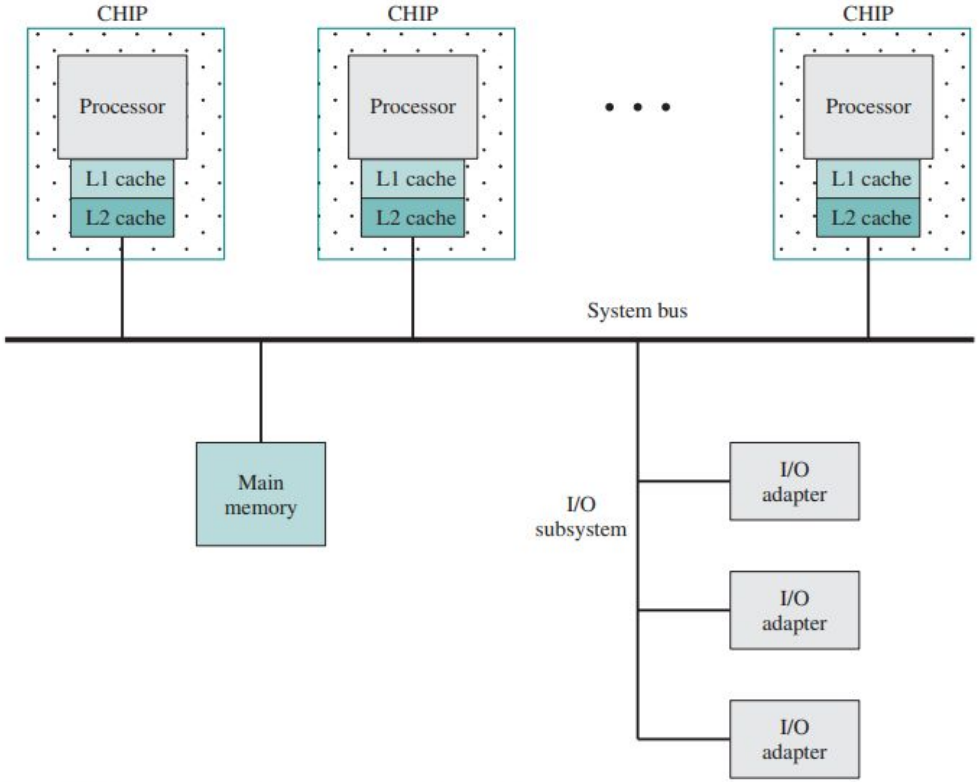


Figure 1.19 Symmetric Multiprocessor Organization

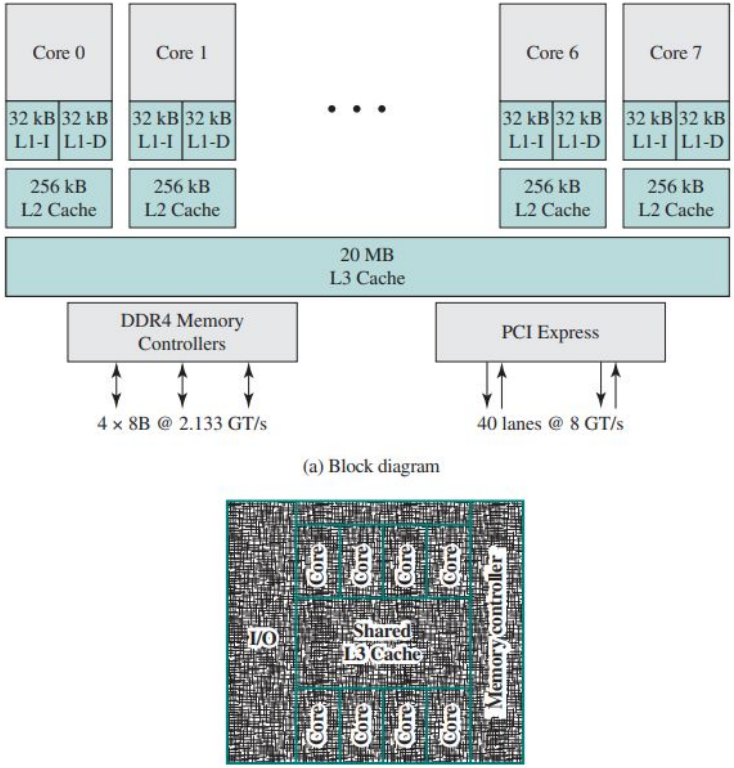


Figure 1.20 Intel Core i7-5960X Block Diagram

QUESTIONS

- **WS-Review Questions-ALL**
- **WS-Problem 1.1**
- **WS-Problem 1.2**
- **WS-Problem 1.3**