Name-Shantanu Deshporde

class - Second year CSE

Roll no . - 7

Date: 14 / 10 /2021



S1-07-SND



Enperiment No. 1B

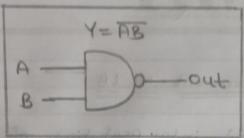
Am: Verification and interpretation of truth table for NAND and NOR gates.

Theory :

(1) NAND Gate +

This is a NOT-AND gate which is equal to an AND gates followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

A simple 2-input logic NAND gate can be constructed using RTL (Resistor-transistor-logic) switches connected together as shown below with the inputs connected directly to the transistor baser Either transistor must be cut-off or "OFF" for an output at Q.



Agure: logic symbol of NAND gate

A	В	6	
		100	
0	0	1	
0	Jain	1	-
solon	0	ille.	100
0 00	1	0	

figure: Truth table of MAND Gate

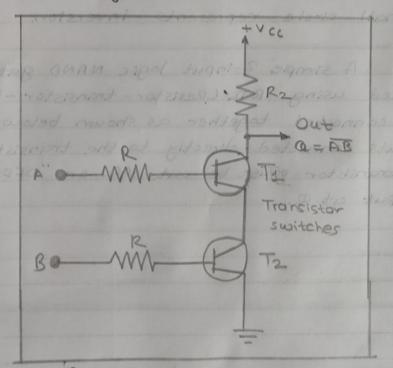


Figure: NAND gate through RTL logic.



A group of academic Research Institutions



Date: / /20

2) NOR Gate +

This is a NOT-OR gate which is equal to an or gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high. The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

A simple 2-input logic NOR gate can be constructed using RTL (Pesistor-transistor-logic)

Switches connected together as shown below with the inputs connected directly to the transistor bases.

Both transistors must be cut-off or "Off" for an output at Q.

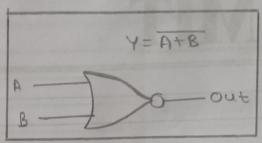


Figure: Symbol of Norgate

all non gate soloued by a parter the inputs are bigh. The symbol on the solon a sith a small circle on the output circle on the output.

On the output The Inal on the present.

figure: Truth table of NoRgate

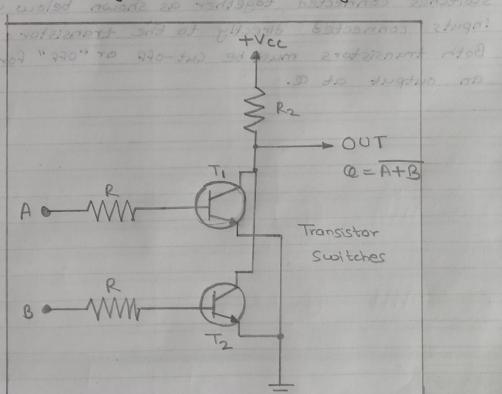
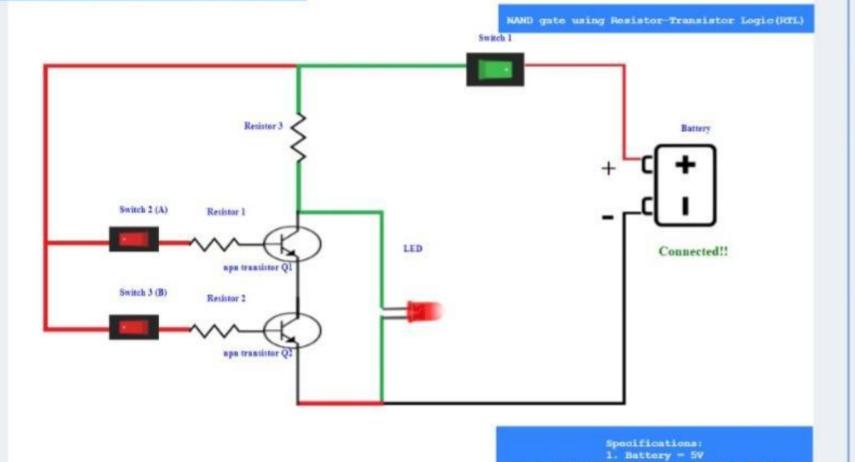


Figure: NOR gate through RTL Logic

Resistor R3 = 1 Kehm & R1 & R2 = 10 Kehm
 Transistors Q1 & Q2 = NFN 2M3904



Experiment to perform NAND gate on kit



3. Transistors Q1 & Q2 - NFW 2N3904



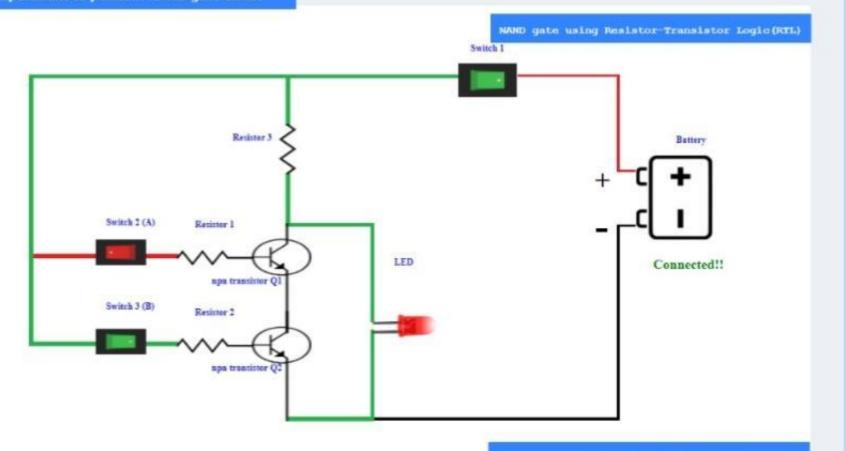
Experiment to perform NAND gate on kit NAMD gate using Resistor-Transistor Logic (RTL) Switch I Resistor 3 Battery Switch 2 (A) Resister I LED Connected!! npn transister Q1 Switch 3 (B) Resister 2 npn transister QI Specifications: 1. Battery = 5V 2. Resistor R3 = 1 Kohm & R1 & R2 = 10 Kohm

Resistor R3 = 1 Kohm 6 R1 6 R2 = 10 Kohm
 Transistors Q1 6 Q2 = NEW 2N3904

Experiment to perform NAND gate on kit NAMED gate using Resistor-Transistor Logic (RTL) Switch 1 Resistor 3 Battery Switch 2 (A) Resistor 1 LED Connected!! apa transister QI Switch 3 (B) Resistor 2 upa transister Q2 Specifications: 1. Battery = 5V



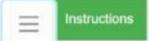
Experiment to perform NAND gate on kit



Specifications:

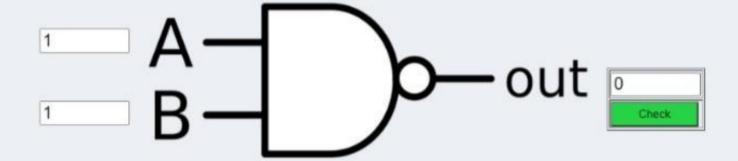
1. Battery = 5V

2. Resistor R3 = 1 Kohm & R1 & R2 = 10 Kohm 3. Transistors Q1 & Q2 = NPN 2N3904



S1-07-SND

Verification of truth table for NAND gate

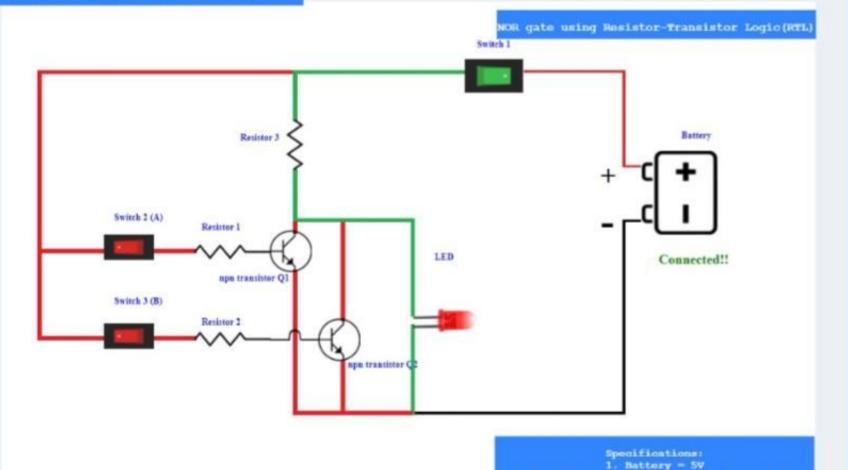


Serial No.	A	В	Output	Remarks
1	0	0	1	Correct
2	0	1	1	Correct
3	1	0	1	Correct
4	1	1	0	Correct

Reset

2. Resistor R3 = 1 Kohm & R1 & R2 = 10 Kohm 3. Transistors Q1 & Q2 = NFN 2N3904

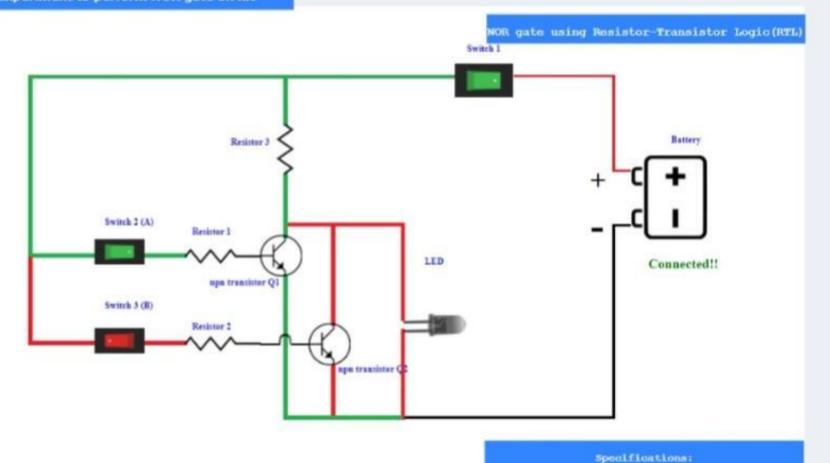
Experiment to perform NOR gate on kit



S1-07-SND

1. Battery - 5V
2. Resistor R3 - 1 Kohm & R1 & R2 - 10 Kohm
3. Transistors Q1 & Q2 - NFN 2N3904

Experiment to perform NOR gate on kit

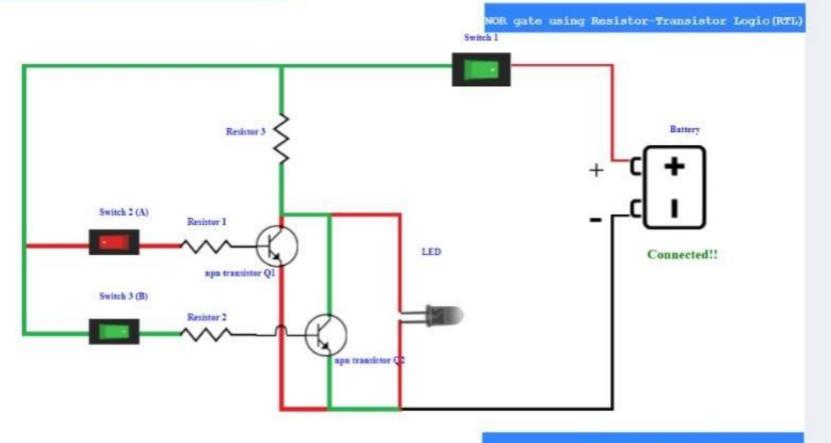




Experiment to perform NOR gate on kit NOR gate using Resistor-Transistor Logic(RTL) Switch 1 Battery Resistor 3 Switch 2 (A) Resistor 1 LED Connected!! apa transister Q1 Switch 3 (B) Resistor 2 npn transistor C Specifications: 2. Resistor R3 = 1 Kohm & R1 & R2 = 10 Kohm 3. Transistors Q1 & Q2 - NPN 2N3904

INSTRUCTIONS

Experiment to perform NOR gate on kit



Specifications: 1. Battery = 5V

Resistor R3 = 1 Kohm & R1 & R2 = 10 Kohm
 Transistors Q1 & Q2 = NFN 2N3904



S1-07-SND

Verification of truth table for NOR gate



Serial No.	A	В	Output	Remarks
1	0	0	1	Correct
2	0	1	0	Correct
3	1	0	0	Correct
4	1	1	0	Correct

Reset