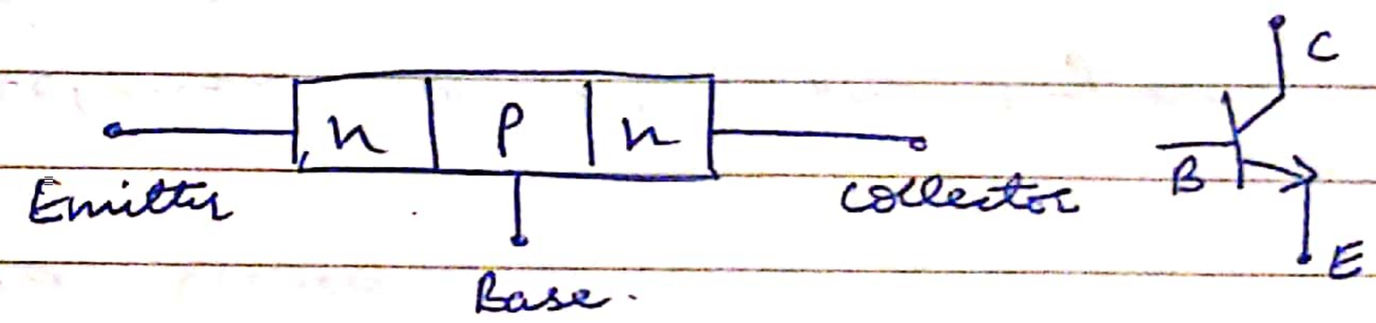
Transistors

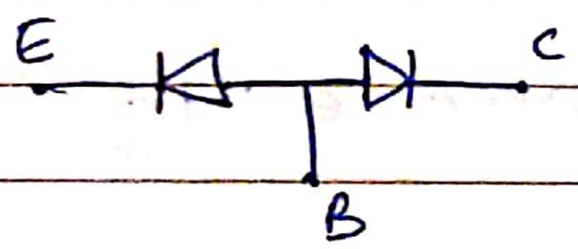
- Transistor has the property of Amplification.
- Because of Transistors electronic circuits are smaller more efficient and less expensive.

Transistor :-

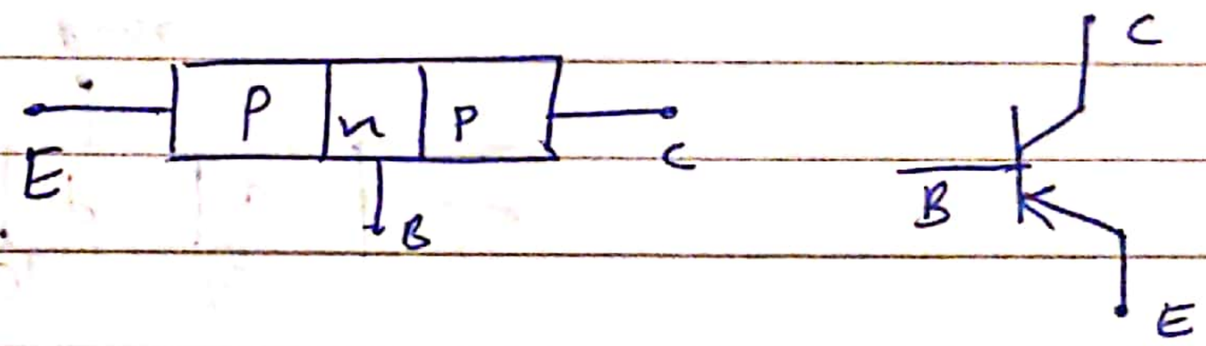
It consist of 2 - p-n junction. There are 2 types:
1) NPN transistor
2) PNP transistor.

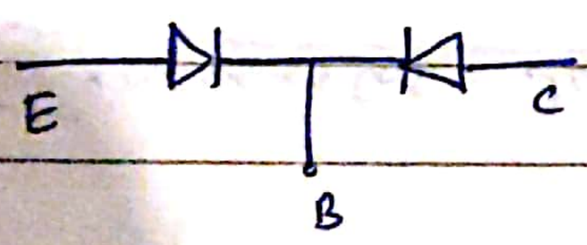
- NPN transistor –





- PNP transistor –





- Transistor —
  - → Unipolar Junction Transistor (Due to majority charge carrier)
  - → Bipolar Junction Transistor. (Due to minority & majority charge carriers.

Transistor Terminal :-

1) **Emitter** - It is heavily doped. It supplies majority carriers to other 2 regions.
It is always forward biased w.r.t base.

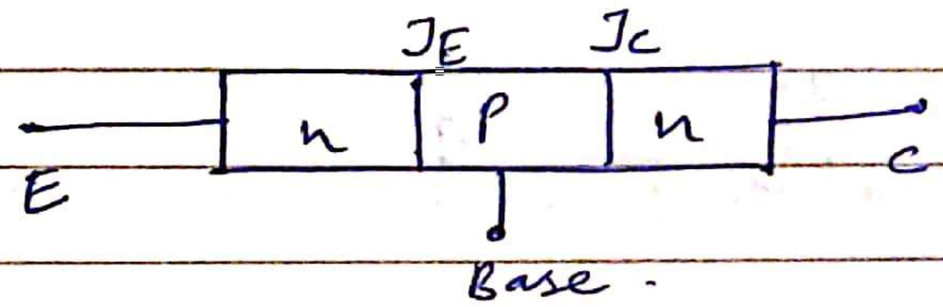
2) **Base :-**

It is lightly doped. It forms 2 p-n junction in the transistor.

3) **Collector :-**

It collects the charge carriers. It is always larger than the emitter and base of transistor. It is moderately doped.

Transistor Junction :-



J_E → Junction between emitter & base region. Forward biased.

J_C → Junction between collector & base region. Reverse biased.

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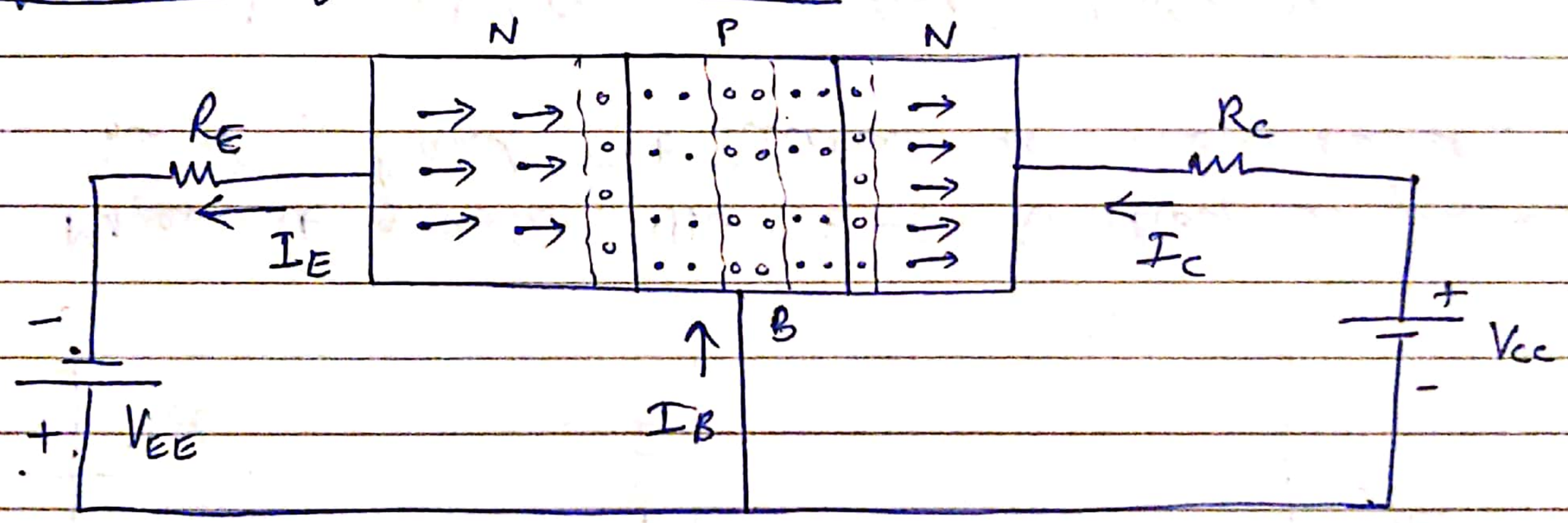
WKT, transistor has 2-PN junction, one is forward biased and other is reverse biased.

During fwd biased, low resistance path, and during reverse biased, high resistance path.

The weak signal is introduced in the low resistance circuit & output is taken from high resistance circuit.

Operation of NPN transistor



1) Emitter-base is forward biased.
Collector-base is reverse biased.

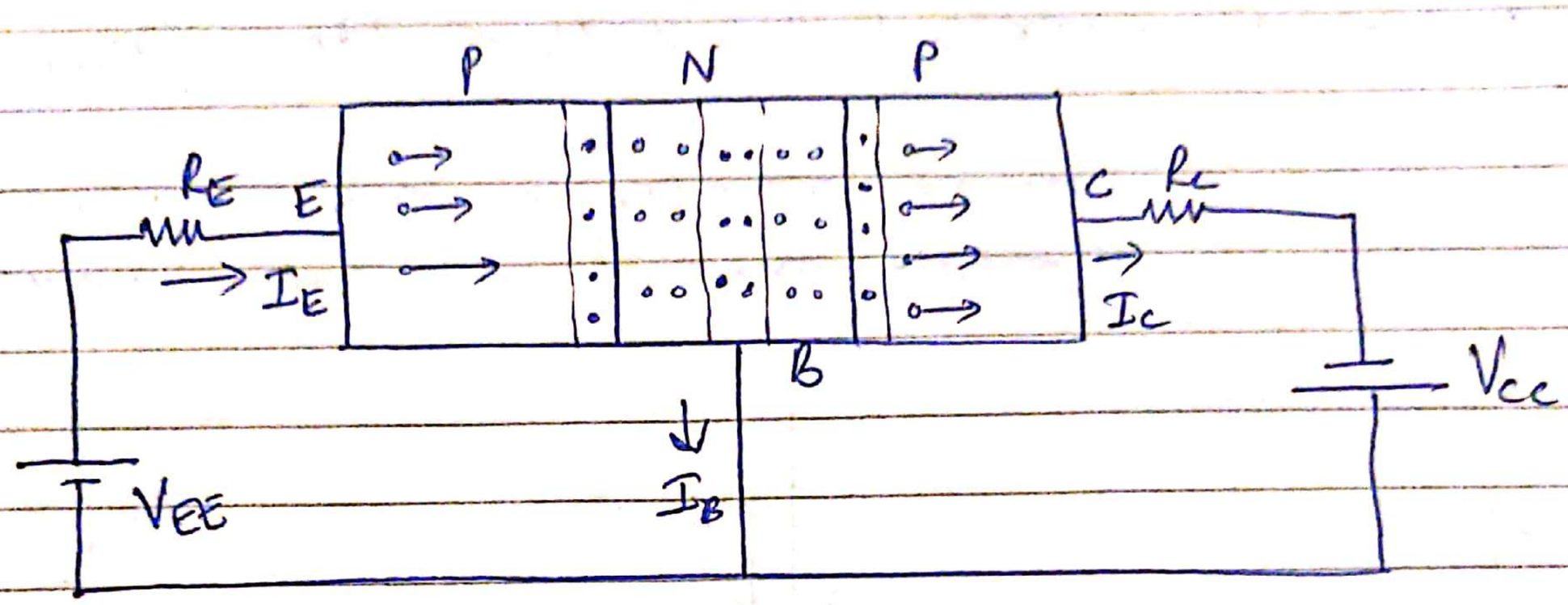
2) When $V_{EE} > V_B$ (barrier potential), forward bias of emitter to base junction causes e^- in N-region to flow towards base, the current is called emitter current I_E

3) As base region is lightly doped, only few electrons combine with holes & constitute base current I_B.

4) Most of electrons diffuse to collector region and constitute collector current I_C.

$$I_E = I_B + I_C.$$

Operation of PNP transistor



1) Movement of holes. The E-B junction is forward biased, and C-B junction is reverse biased.

2) When $V_{EE} > V_B$ (barrier potential), holes flow from emitter region to base region constituting I_E (emitter current).

3) Only few recombination takes place, as base is lightly doped. Most of holes diffuses into collector, constituting collector current.

$$I_E = I_B + I_C.$$

Another component of collector current in both NPN and PNP is due to thermally generated carriers, this current component is called reverse saturation current.

$$I_C = I_{C\,majority} + I_{CBO\,minority}$$
(mA) (μA/nA)

$$I_E = I_B + I_C \quad \text{—— (1)}$$

Dividing both side by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{\cancel{I_C}}{\cancel{I_C}}$$

$$\boxed{\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1} \quad \text{—— (2)}$$

WKT, $\beta = \frac{I_C}{I_B}$, $\alpha = \frac{I_C}{I_E}$ → current gain → Common base configuration

gain = $\frac{O/P}{I/P}$

current gain = $\frac{O/P\ current}{I/P\ current}$

Eq (2) becomes,

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$1/\alpha = \frac{1+\beta}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{\beta+1}} \quad \text{—— (3)}$$

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Eq ③, can be written as,

$$\alpha(1+\beta) = \beta.$$

$$\alpha + \alpha\beta = \beta.$$

$$\alpha = \beta - \alpha\beta.$$

$$\alpha = \beta(1-\alpha)$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}.}$$

The application of dc voltage across the transistor terminal is called biasing.

3 modes of transistor operation.

		E-B	C-B junction
1) Active (Amplifier).	—	Forward	Reverse
2) Saturation (closed switch)	—	Forward	Forward
3) Cut-Off (open switch)	—	Reverse	Reverse.

E-B is reverse biased & C-B is forward biased, region is called inverse active region.

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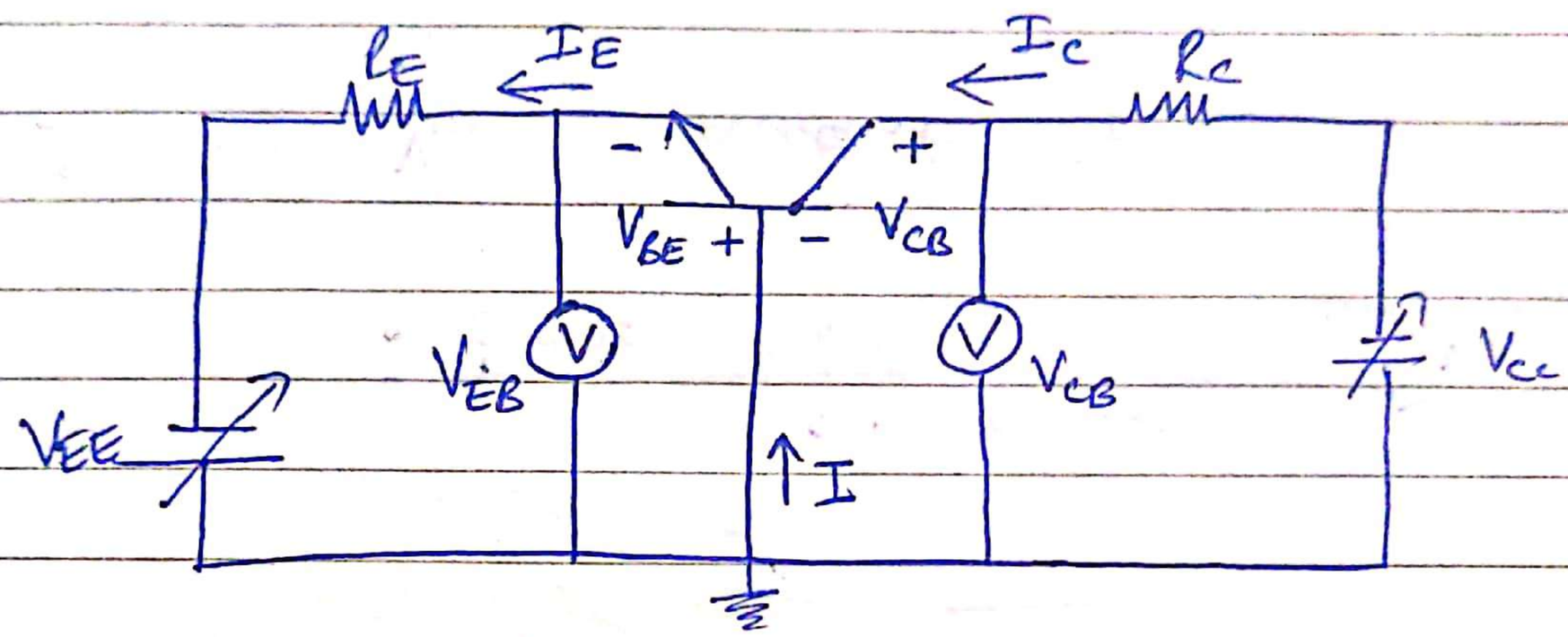
Transistor can be configured as Amplifier in 3 ways:-

3 types of configuration :-

1) common base configuration.
2) common emitter configuration.
3) common collector configuration.

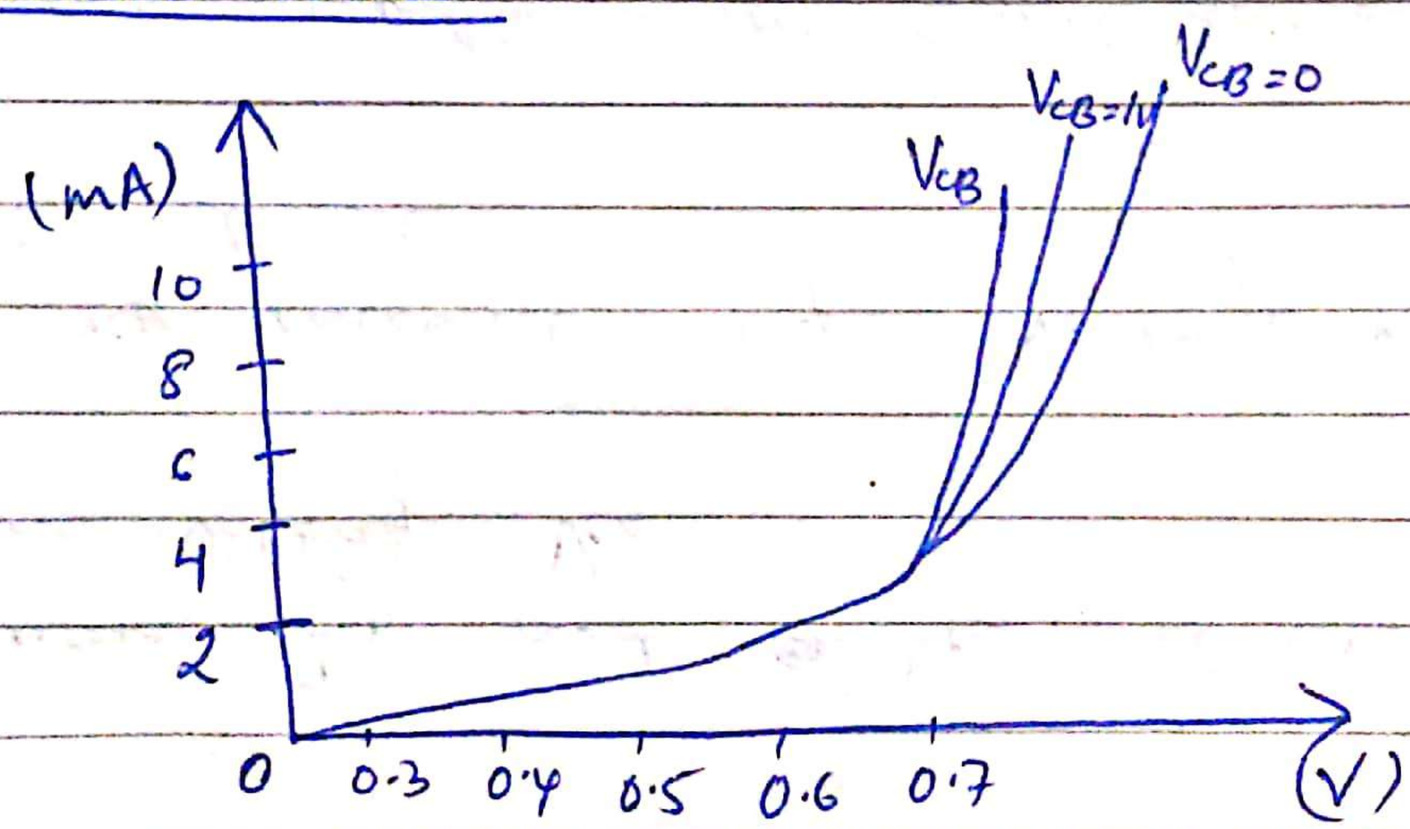
common base configuration.



- Emitter - base junction is forward biased and collector - base junction is reverse biased.

- I_E flows in input circuit and I_C flows in output circuit.

Input characteristics



1) Input is applied between emitter and base.
Output is measured between collector and base.

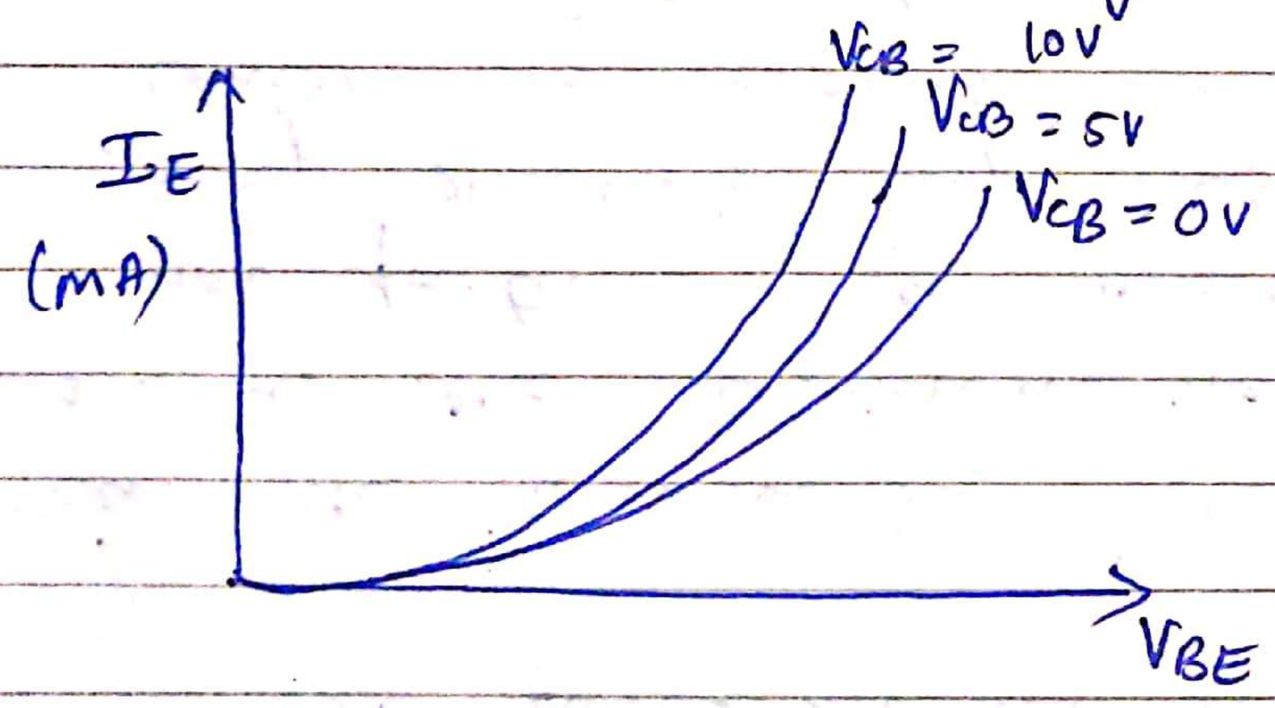
2) It is in active region, I_E is forward biased and I_C is reverse biased.

3) NPN transistor, I_E is away from transistor, I_B & I_C enters the transistor.

PNP transistor, I_E is entering the transistor and I_B & I_C is away from transistor.

4) Behaviour of common base configuration can be analyzed using input and output characteristics.

5) I_E is input current
V_{BE} is input voltage.



Fixed value of V_{CB}.

It is similar to the forward characteristics of PN junction diode.

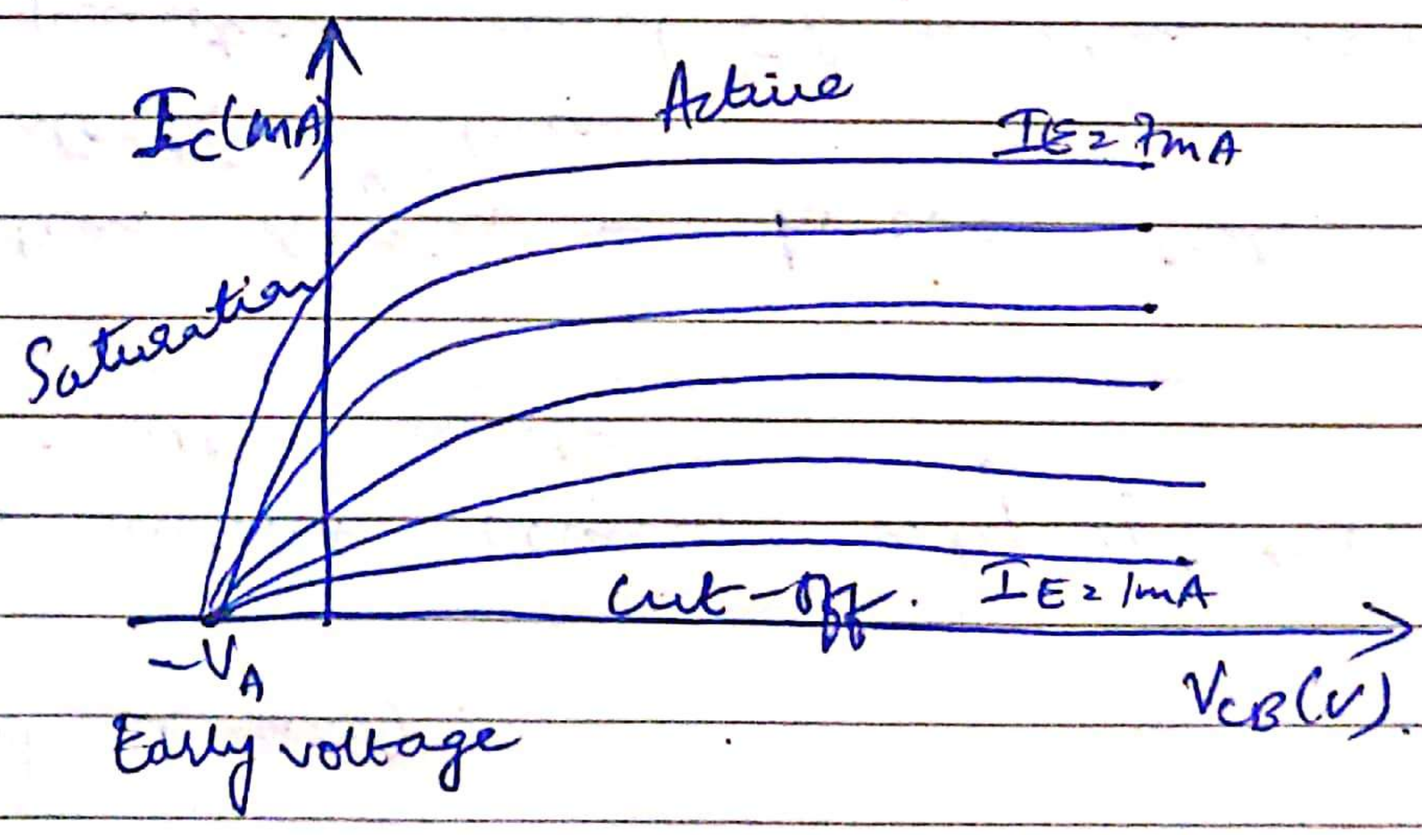
As the value of V_{CB} increases, the curve shifts towards left and I_E also increases.

Because, when C-B junction gets more reverse biased, the width of depletion region increases. Due to which base region will become narrower. So, less voltage is required to forward bias the emitter base junction.

$$\text{Input impedance} = \frac{\Delta V_{BE}}{\Delta I_E}$$

Input impedance is low, since small change in V_{BE}, give huge change in I_E.

6) I_C is output current.
V_{CB} is output voltage.
I_E is constant



3 regions of operation,

- Active region = More we increase the V_{CB}, the I_C remains constant.

$$I_C = \alpha I_E$$

$$\alpha = \frac{I_C}{I_E}$$

(current gain).

Collector current changes only if there is change in emitter current.

- Saturation region – As we reduce V_{CB}, I_C starts reduces.
  EB junction and CB junction is forward biased no current flows from EB to collector and current is less.

- cut off region – When, I_E is zero, even if, V_{CB} is increased, I_C remains zero.

I_C is due to minority charge carriers.

When emitter is open, the reverse saturation current I_{CBO}

$$I_{C_T} = I_C + I_{CBO}$$
$$= \alpha I_E + I_{CBO}$$

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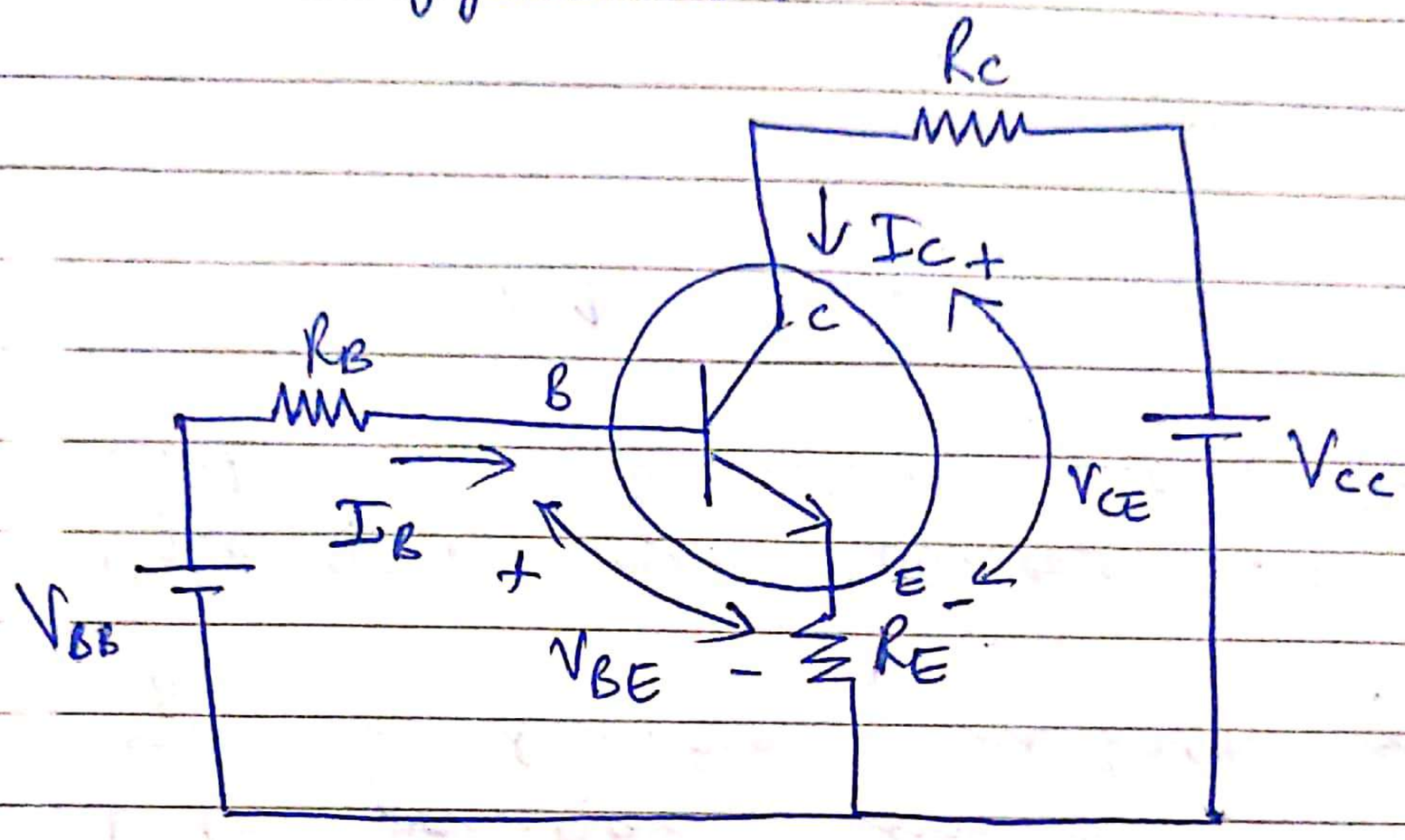
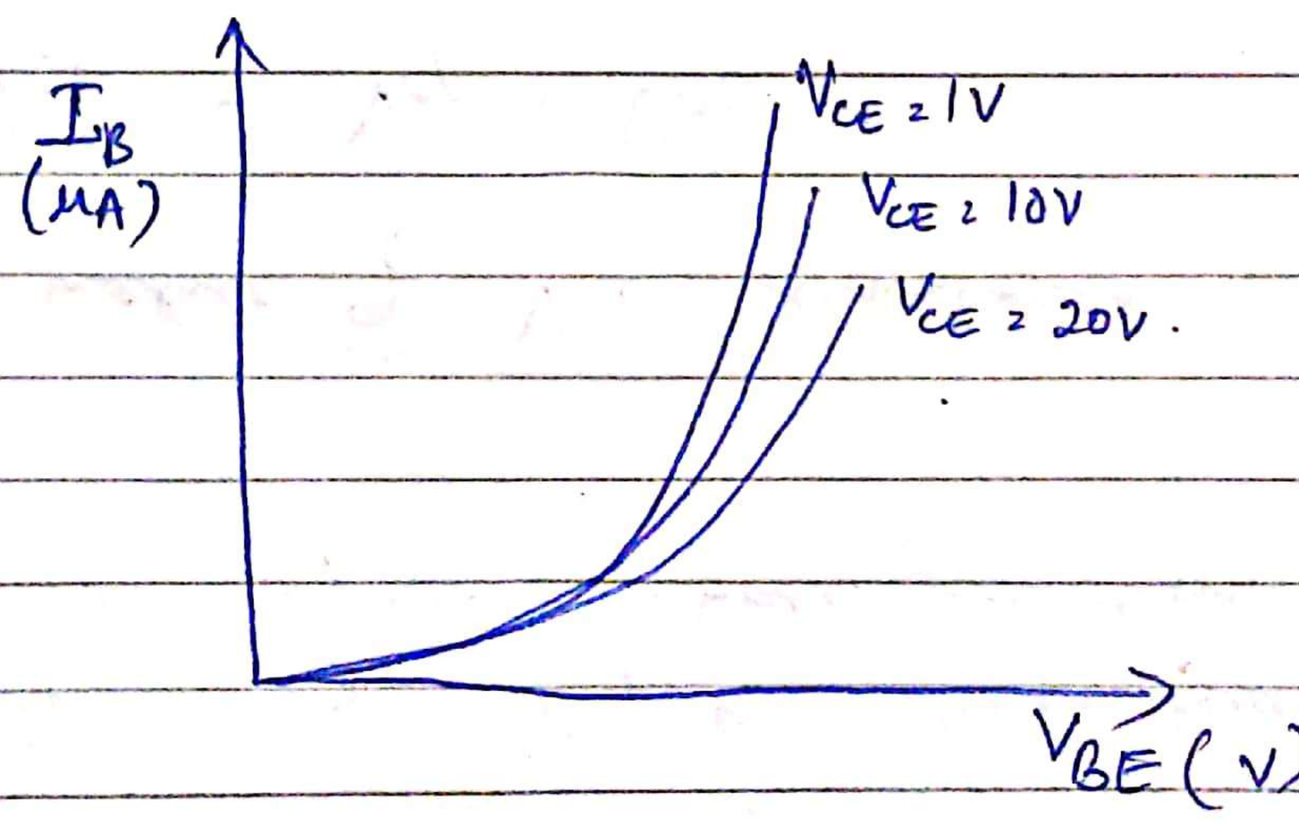
Common emitter configuration :-

- It is frequently used configuration and when BJT is used as an amplifier it is used in this configuration.



1) Base emitter junction is forward bias.
Collector emitter junction is reverse bias.

I/P characteristics ← I_B is input current, V_{BE} is input voltage
I_C is output current, V_{CE} is output voltage.
output characteristics. 2) Input characteristics



- It is similar to input characteristics of a diode, since emitter - base junction is forward biased.

- As the value of V_{CE} increases, I_B reduces.

$$V_{CE} = V_{CB} + V_{BE}.$$

For fixed value of V_{BE}, if we increase V_{CE}, then V_{CB} also increases.

As V_{CB} increases due to reverse bias applied, the base terminal also increases.

The depletion region formed between the B-C junction increases, the probability of recombination in base region will reduce.

Most of e^- get collected at collector terminal and due to which I_B will reduce.

- $V_{CE} \uparrow$, $I_B \downarrow$.

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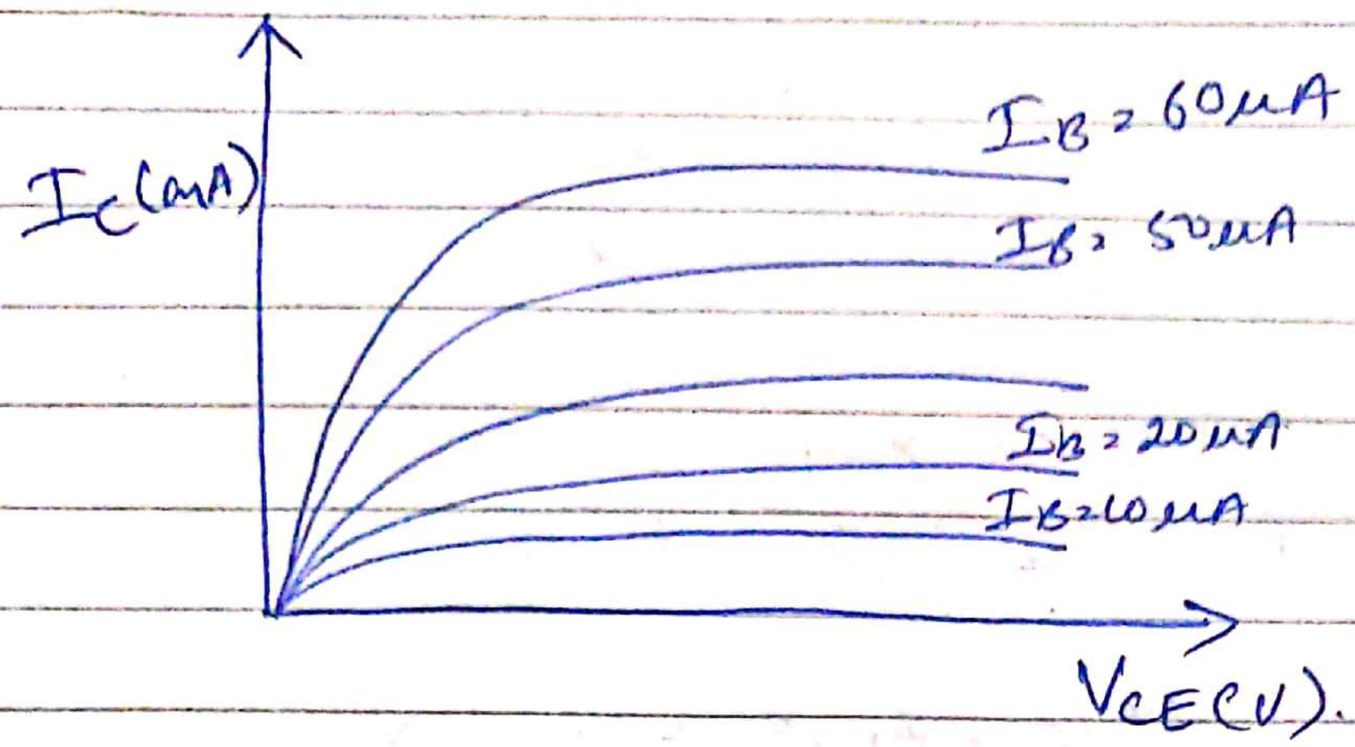
3) output characteristics.



Active region :-

As $I_B \uparrow$, $I_C \uparrow$, $V_{CE} \uparrow$, $I_C \uparrow$,

$V_{CE} \uparrow$, $V_{CB} \uparrow$, $\because V_{CE} = V_{CB} + V_{BE}$

Width of depletion region increases, effective base length ~~as~~ decreases, then probability of recombination reduces.

More e^- passes through the base.

I_B gets amplified by factor 'β'.

$$I_C = \beta I_B$$

β (current gain)

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B}$$

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Saturation region :-

As V_{CE} decreases, it gets close to zero, at that time the collector to base junction becomes forward biased.

Cut off

When $I_B = 0$, $I_C \neq 0$, and I_C is large.
when $I_E = 0$, collector current which exists is due to reverse saturation current.

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + I_C$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{\frac{\alpha}{1-\alpha} = \beta}$$

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$$I_C = \beta I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

β is high value.
$(1+\beta) I_{CBO}$ is high because of 'β'.

When $I_B = 0$, $I_C = \frac{1}{1-\alpha} I_{CBO}$

$(1-\alpha)$ will be very small, will be $0.95 \rightarrow 0.99$

$\frac{1}{1-\alpha}$ will be very large

When base terminal is open,

$$I_{CEO} = (\beta+1) I_{CBO}$$

Leakage current gets amplified by the factor of $\beta+1$.
if, $\beta = 99$,
$I_{CBO} = 1\mu A$.

$I_{CEO} = 100\mu A$.

i.e. the cut off region, there is large I_C.

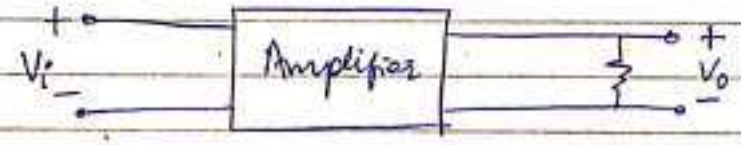
Advantages of CE configuration:-

1) Moderate current gain.
2) Moderate voltage gain
3) High power gain → sig amplification.
4) Moderate i/p impedance
5) Moderate o/p impedance

	CE	CB	CC
Z_i	$(1+\beta)r_e$	r_e	$\beta(r_e+R_E)$
Z_o	r_o	r_o	r_e
A_V	$-r_o/r_e$	r_o/r_e	$\simeq 1$
A_I	β	α	$-(1+\beta)$ $= -\beta$

Amplifiers

An amplifier is an electronic circuit that amplifies or magnifies or strengthens the amplitude of input signal without distortion



Let us assume, a small sinusoidal signal is applied to the amplifier, at the output of the amplifier the signal must remain ~~iss~~ sinusoidal in waveform and the frequency of the signal must remain same as input.

The ratio of output voltage to input voltage of amplifier is called the gain of the amplifier. (A_V)

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The ratio of output current to input current is called current gain of the amplifier. (A_I).

We express the gain in dB.

$$A_p = 10 \log \left[\frac{P_o}{P_I} \right]$$

$$P_o = \frac{V_o^2}{R_L}, \quad P_I = \frac{V_i^2}{R_L}$$

$$= \frac{V_o^2}{V_i^2} \qquad \text{if } R_L = R_i$$

$$= 10 \log \left[\frac{V_o^2}{V_i^2} \right]$$

$$\boxed{A_v (dB) = 20 \log \left[\frac{V_o}{V_i} \right]}$$

$$\boxed{A_{p(dB)} = 10 \log \left[\frac{V_o}{V_i} \right]}$$

$$\boxed{A_{I(dB)} = 20 \log \left[\frac{I_o}{I_i} \right]}$$

<u>Need for cascading of Amplifiers</u>

The current gain or voltage gain obtainable from a single transistor amplifier stage is usually inadequate for most of the applications. Hence several amplifiers are connected in cascade

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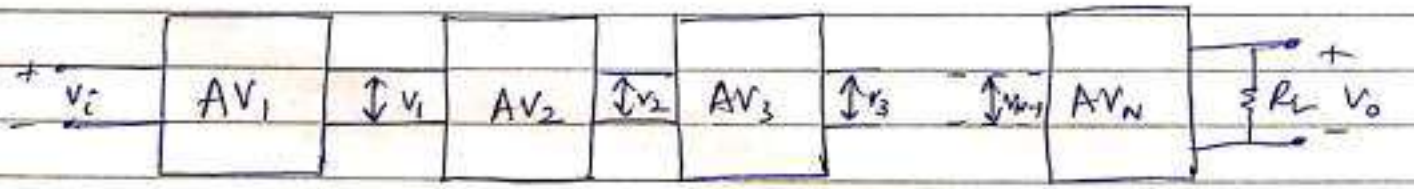
The amplifiers are connected such that the output of one stage forms the input of the next stage. Such cascade amplifiers permit realization of any desired voltage or current.

In the cascading of amplifiers an important consideration is the choice of elements coupling one stage to next one.

Different coupling methods are used in the different type of cascade amplifier such as RC coupled amplifier and transformer coupled amplifier.



Voltage of 1st stage $A_{V_1} = \frac{V_1}{V_i}$.

Voltage of 2nd stage, $A_{V_2} = \frac{V_2}{V_1}$

Voltage of 3rd stage, $A_{V_3} = \frac{V_3}{V_2}$

Voltage gain of Nth stage, $A_{V_N} = \frac{V_o}{V_{N-1}}$

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$\therefore$ Overall voltage gain $= A_v = \frac{V_o}{V_1}$

$$A_v = \frac{V_o}{V_{N-1}} \times \cdots \frac{V_3}{V_2} \times \frac{V_2}{V_1} \times \frac{V_1}{V_i}$$

$$= A_{v_N} \times \cdots A_{v_3} \times A_{v_2} \times A_{v_1}$$

$$\therefore \boxed{A_v = A_{v_1} \times A_{v_2} \times A_{v_3} \cdots A_{v_N}}$$

Overall voltage gain in dB.

$$(A_v)_{dB} = 20 \log_{10} [A_v]$$

$$= 20 \log_{10} [A_{v_1} \times A_{v_2} \times A_{v_3} \cdots \times A_{v_N}]$$

$$= 20 \log_{10} [A_{v_1}] + 20 \log_{10} [A_{v_2}] + \cdots 20 \log_{10} [A_{v_N}]$$

$$\boxed{(A_v)_{dB} = A_{v_{1dB}} + A_{v_{2(dB)}} \cdots + A_{v_N dB}}$$

Note:- 1) In decibels, its addition of gains
2) In Absolute number, its multiplication of gain

Each time the voltage gain increases or decreases by a factor of 2, the decibel voltage gain increases or decreases by 6dB.

Each time the A_v increases or decreases by a factor of 10, the decibel voltage gain increases or decreases by 20 dB.

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(1) The ~~out~~ output power from an amplifier is 50mW when the signal freq is 5KHz. The output power falls to 25mW. When freq is 20KHz calculate the power change in decibels,

Soln

$$\Delta P_o = 10 \log_{10}\left(\frac{P_2}{P_1}\right)$$

$$= 10 \log_{10}\left(\frac{25mW}{50mW}\right)$$

$$= -3dB.$$

(2) Calculate the power gain of an Amplifier with equal input and load resistance when $V_i = 100mV$ and $V_o = 3V$

Soln

$$A_{P(dB)} = 20 \log\left[\frac{V_o}{V_i}\right]$$

$$= 20 \log\left[\frac{3}{100m}\right].$$

$$= 29.54\ dB.$$

(3) The power gain of an amplifier is 20dB. The input power required to obtain an output power of 100W

$$(A_P)_{dB} = 10 \log_{10}\left[\frac{P_o}{P_i}\right]$$

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$$20 = 10 \log \left[\frac{100}{P_i}\right]$$

$$P_i = 1W.$$

(4) An amplifier has a voltage gain of 100 at 1KHz. The gain falls by 6 dB at 1MHz if the input is 3mW at 2MHz. Calculate the output voltage.

Soln: Gain in dB $= 20 \log_{10}(100) = 40 dB$.

Gain falls by 6dB $\therefore 40 - 6 = 34$ dB.

$$(A_V)_{dB} = 20 \log \left[\frac{V_o}{V_i}\right].$$

$$34 = 20 \log \left[\frac{V_o}{3mV}\right]$$

$$V_o = 0.1503V$$

$$\boxed{V_o \simeq 150.3mV}$$

(5) The output power of an amplifier with a power gain of 23 dB is 25W, the i/p power is,

$$A_{p(dB)} = 10 \log \left[\frac{P_o}{P_i}\right].$$

$$23 = 10 \log \left[\frac{25}{P_i}\right].$$

$$P_i = 0.125W \text{ or } 125mW$$

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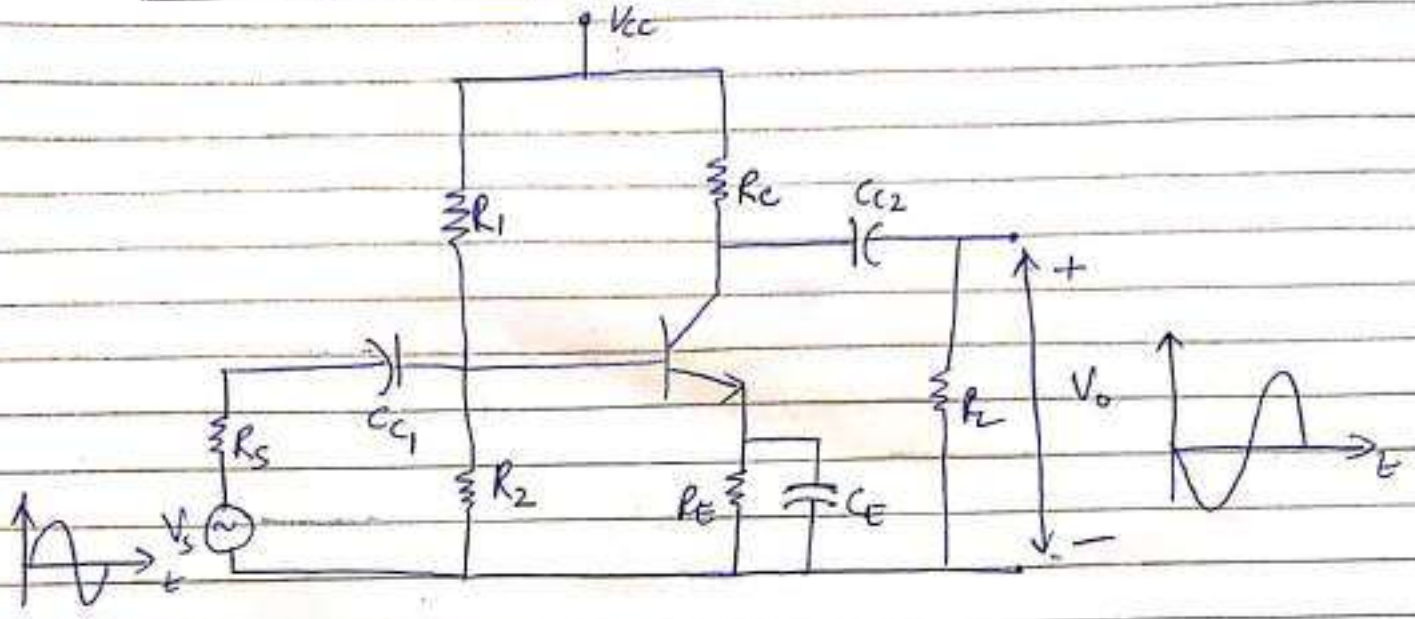
RC coupled amplifier



1) The resistors R_1, R_2, R_C, R_E form voltage divider bias circuit
2) The values of resistors are choosen such that, proper operating pt for CE amplifier.
3) operating point is choosen, device works in active region and acts as an amplifier.
4) There are 2 types of capacitors, $C_E \rightarrow$ bypass capacitors, C_{C1} & $C_{C2} \rightarrow$ coupling capacitors

WKT, Impedance of capacitor is given by,

$$X_C = \frac{1}{2\pi f C}$$

For DC sig, $f = 0$, $\therefore X_C = \infty$

For AC sig, we will have a signal freq. X_C will be low, capacitor acts as a short circuit.

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5) R_S is in parallel with R_2, this reduces the bias voltage at the base of the transistor and intern alters the collector current.

6) If we dont connect input capacitor C_{C1}. The dc signal which in the input of the source signal alters the biasing condition of transistor. The capacitor C_{C1} blocks any dc signal entering the transistor.

7) By connecting R_L directly to the amplifier, the dc levels of V_C and V_{CE} will change which again alters the operating condition of transistor.

8) The output coupling capacitor C_{C2} blocks dc signal entering load, and allows only ac signal.

9) R_E provides bias stabilization, it also reduces voltage gain
$C_E \rightarrow$ It gives low reactance path to the amplified ac signal which increases the output voltage gain.

10) Bypass capacitor acts as a short circuit for ac signal and allows us to create an ac ground in an amplifier without disturbing its Q-pt.

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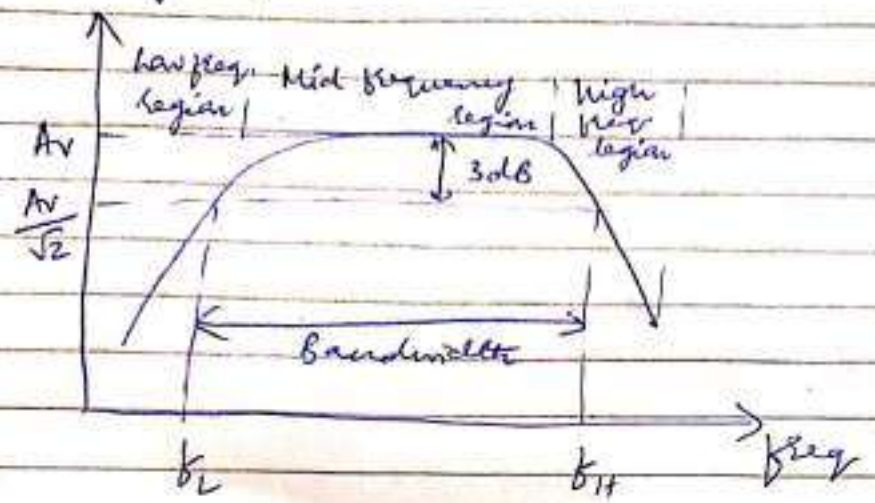
Frequency response



It can be divided into 3 regions :
(1) Low freq region.
(2) Mid freq region.
(3) high freq region.

Low freq region :-

The reactance of capacitor is given as,

$$X_C = \frac{1}{2\pi f C}$$

At low freq, X_C increases. This increase in X_C drops the signal voltage across the capacitor and intern reduces the circuit gain.

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Mid freq region :-

As the frequency increases, X_c becomes very small and the voltage gain will be maximum and it will be almost constant for certain range of frequencies.

High freq ~~range~~ region :-

At high freq the voltage gain decreases due to the influence of junction capacitance of the transistor. At high freq, the reactance of junction capacitance fall. When these reactances become small enough, they provide shunting effect as they are in parallel with the junction. This reduces the current gain intern the voltage gain.

Bandwidth of an Amplifier.

1) It is difference between f_H and f_L.
It specifies the range of frequencies over which the gain does not deviate more than 70.7% of maximum gain at mid frequency range.

2) The 2 frequencies f_H and f_L are referred as half power frequencies

3) They are called half power points because the gain or output voltage drops to 70.7% of maximum value.

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(2) A Si-transistor has its $I_{co} = 6nA$ and $\alpha = 0.98$. If $I_B = 0$, and $V_{CE} = 4V$ then $I_C = ?$

Soln

$$I_C = \frac{I_{co}}{1-\alpha} = 300nA$$

(b) A N-P-N transistor has $I_{co} = 30nA$, $I_B = 0$, $V_{CE} = 4V$ and $I_C = 30\mu A$. value of $\beta = ?$

Soln

$$I_C = \beta I_B + (1+\beta) I_{co}$$

$$= (1+\beta) I_{co}$$

$$\beta = 999$$

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If the output voltage gain is expressed in dB scale, then to find the cut off frequencies we have to come down 3dB from maximum gain

$$(A_f)_{dB} = 20 \log \left[\frac{70.7}{100}\right]$$

$$= -3dB.$$

(6) (a) Three amplifiers of voltage gain 20dB, 26dB and 32dB are cascaded to obtain an output voltage of 2V. Calculate the input voltage needed.

Soln

$$A_{dB} = A_{1dB} + A_{2dB} + A_{3(dB)}$$
$$= 78dB.$$

$$A_{dB} = 20 \log \left(\frac{V_o}{V_i}\right)$$

$$78 = 20 \log_{10} \left(\frac{2}{V_i}\right)$$

$$V_i = 0.25mV.$$

(b) An amplifier having a power gain of 17dB delivers a power output of 40W to a load of 1KΩ. Calculate (i) the input power needed, (ii) the input voltage needed, if the voltage gain of amplifier is 35dB.

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Soln

$A_p(dB) = 17\,dB$, $A_v(dB) = 38\,dB$.

$P_o = 40W$

$R_L = 1K\Omega$, $P_i = ?$, $V_i = ?$

$$A_p = 10 \log\left(\frac{P_o}{P_i}\right)$$

$$17\,dB = 10 \log\left(\frac{40}{P_i}\right)$$

$$P_i = 0.79\,W.$$

$$P_o = V_o^2/R_L$$

$$40 = \frac{V_o^2}{1K\Omega}$$

$$V_o^2 = 40K\Omega$$

$$= 200V.$$

$$A_v = 20 \log\left(\frac{V_o}{V_i}\right)$$

$$38 = 20 \log\left(\frac{200}{V_i}\right)$$

$$1.9 = \log\left(\frac{200}{V_i}\right)$$

$$10^{1.9} = \frac{200}{V_i}$$

$$V_i = \frac{200}{79.43} = 2.51V$$

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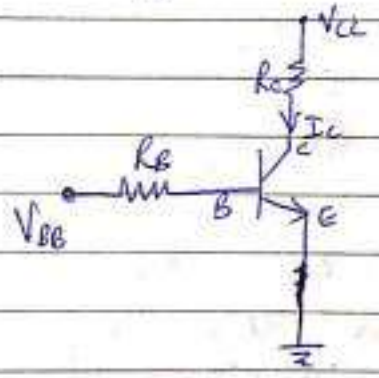
Transistor as a switch: (Computer & control applications)

BJT can be used as a switch in cut-off / saturation region. Let us consider, fixed bias configuration



When $V_{BB} = 0$, or less than V_{BE}, then $i_b = 0$, WKT, $i_c = \beta i_b \approx 0$.

No voltage drop across R_C.

$V_{CE} = V_{CC}$

BJT is operating in cut off region.

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- When $V_{BB} \neq 0$, it might work in active or Saturation region.

In Saturation region, V_{CE} is very low (0.1-0.2)
I_C will be maximum.

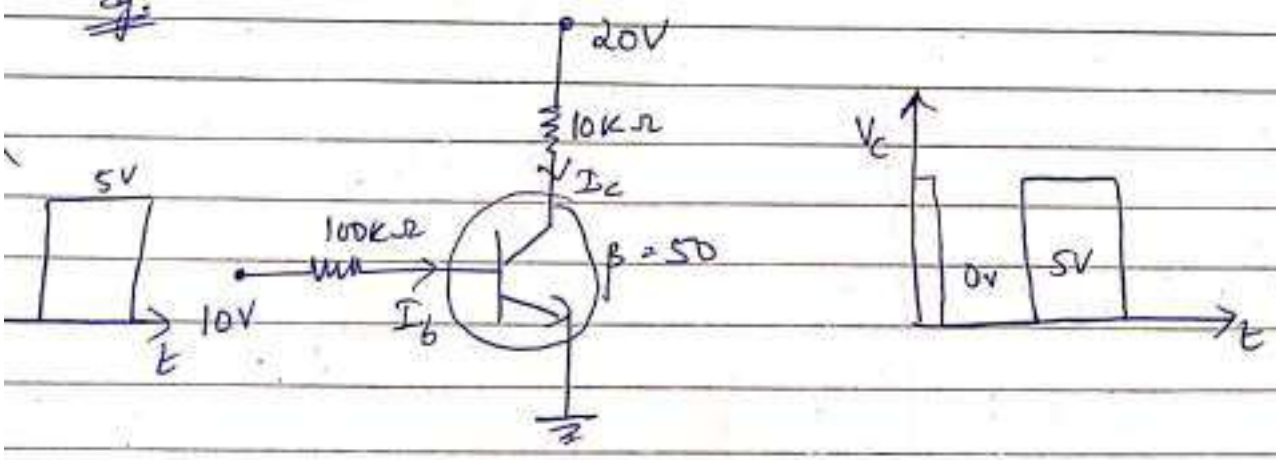
$$I_{C(sat)} = \frac{V_{CC}}{R_C}$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B}$$

$I_C = \beta I_B$. (Assume, BJT is in active region)

$I_C > I_{Csat}$, then it is in saturation region

Eg:-



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