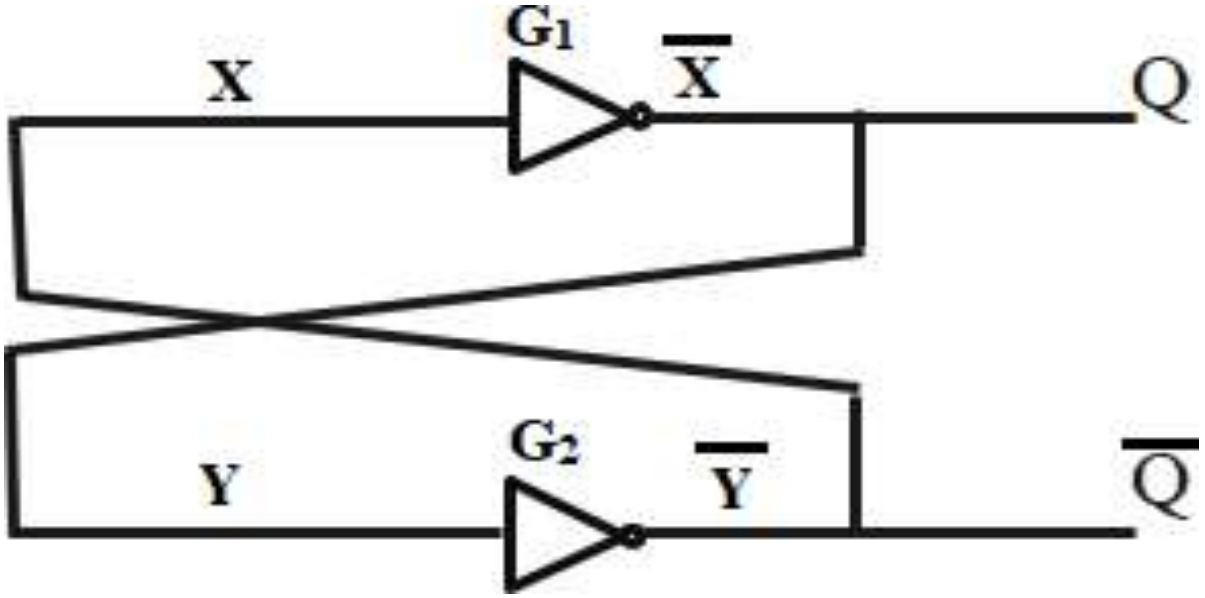
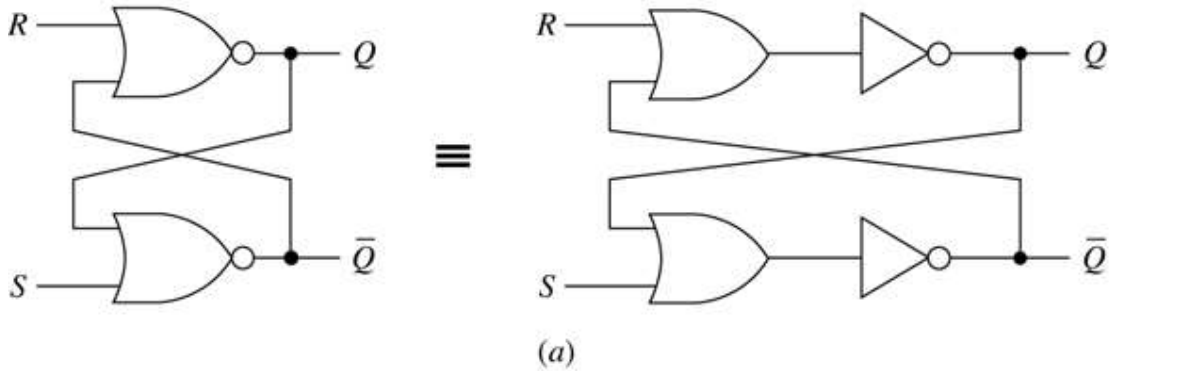
Basic bistable element.

Figure 6.1



SR latch. (*a*) Logic diagrams. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

Figure 6.2

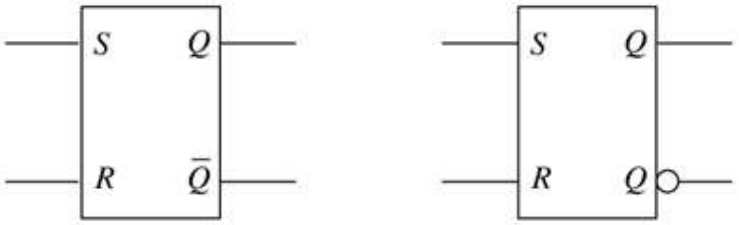


(*a*)

Inputs		Outputs	
S	*R*	Q^+	$\bar{Q}^+$
0	0	*Q*	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0*	0*

*Unpredictable behavior will result if inputs return to 0 simultaneously

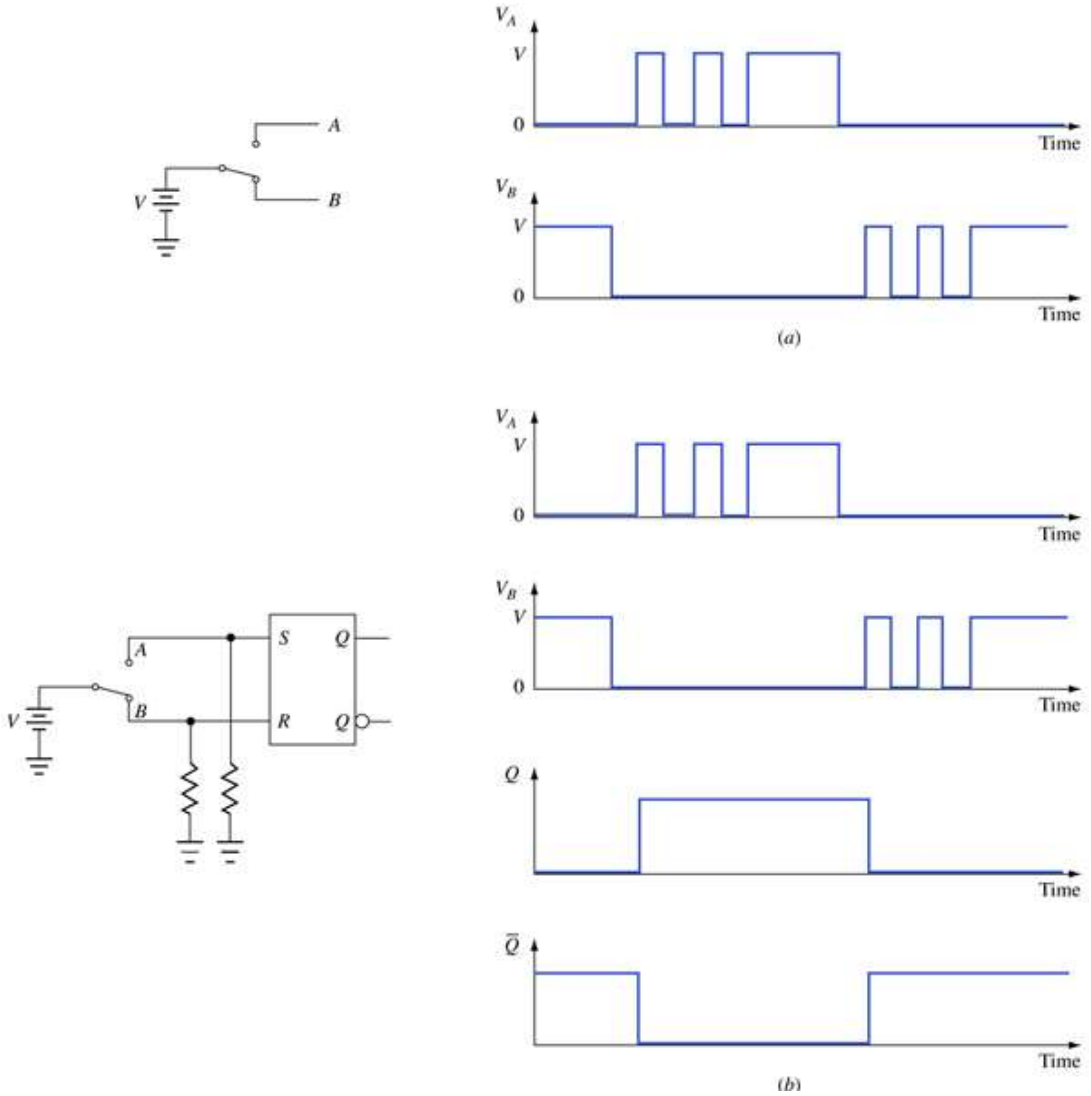
(*b*)



(*c*)

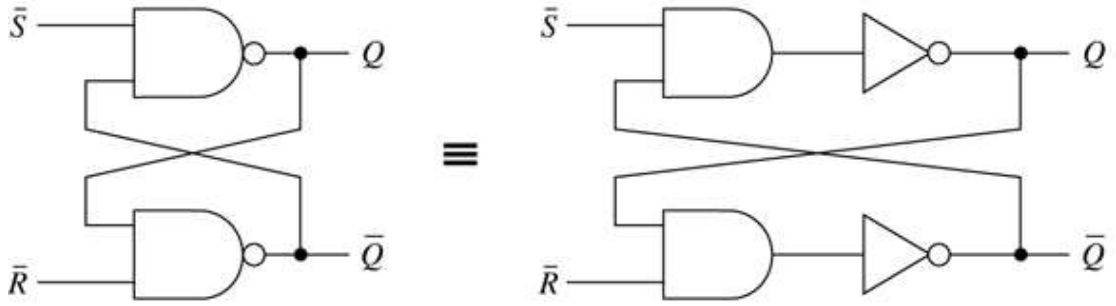
An application of the *SR* latch. (*a*) Effects of contact bounce. (*b*) A switch debouncer.

Figure 6.3



$\bar{S}\bar{R}$ latch. (*a*) Logic diagrams. (*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

Figure 6.4

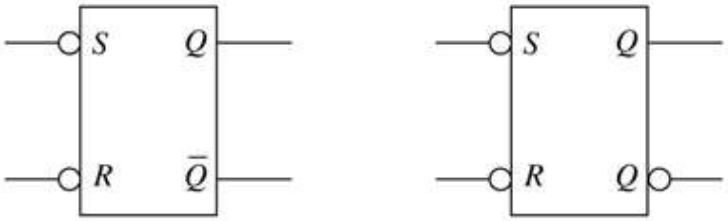


(*a*)

Inputs		Outputs	
$\bar{S}$	$\bar{R}$	Q^+	$\bar{Q}^+$
0	0	1*	1*
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

*Unpredictable behavior will result if inputs return to 1 simultaneously

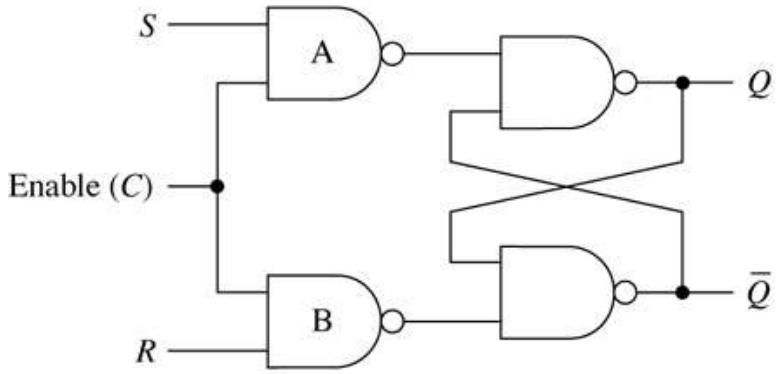
(*b*)



(*c*)

Gated *SR* latch. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

Figure 6.5

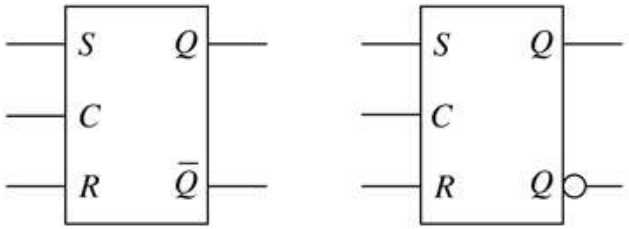


(*a*)

Inputs			Outputs	
S	*R*	*C*	Q^+	$\overline{Q}^+$
0	0	1	*Q*	$\overline{Q}$
0	1	1	0	1
1	0	1	1	0
1	1	1	1*	1*
X	X	0	*Q*	$\overline{Q}$

*Unpredictable behavior will result if *S* and *R* return to 0 simultaneously or *C* returns to 0 while *S* and *R* are 1

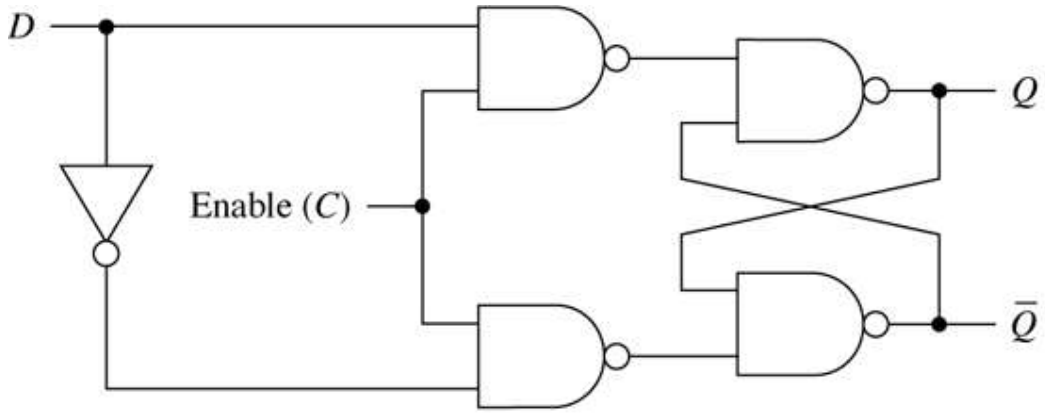
(*b*)



(*c*)

Gated *D* latch. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

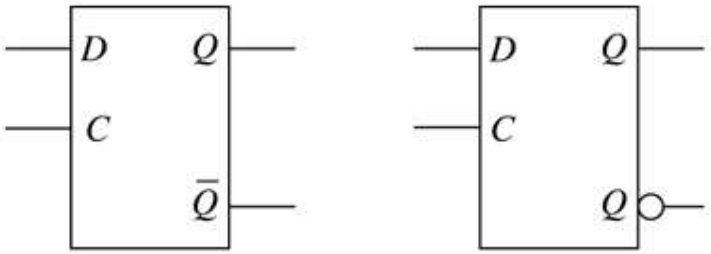
Figure 6.6



(*a*)

Inputs		Outputs	
D	*C*	Q^+	$\overline{Q}^+$
0	1	0	1
1	1	1	0
X	0	*Q*	$\overline{Q}$

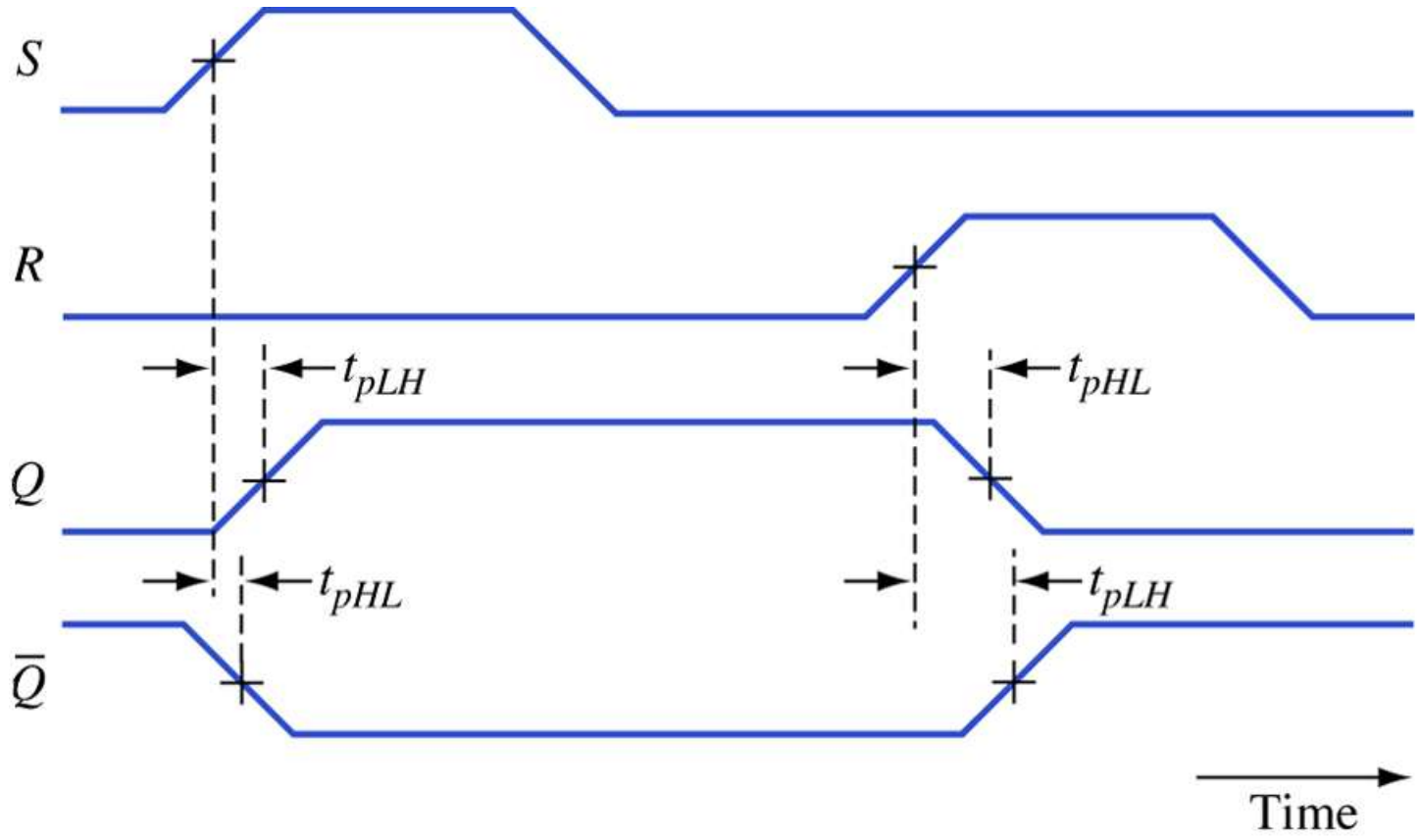
(*b*)



(*c*)

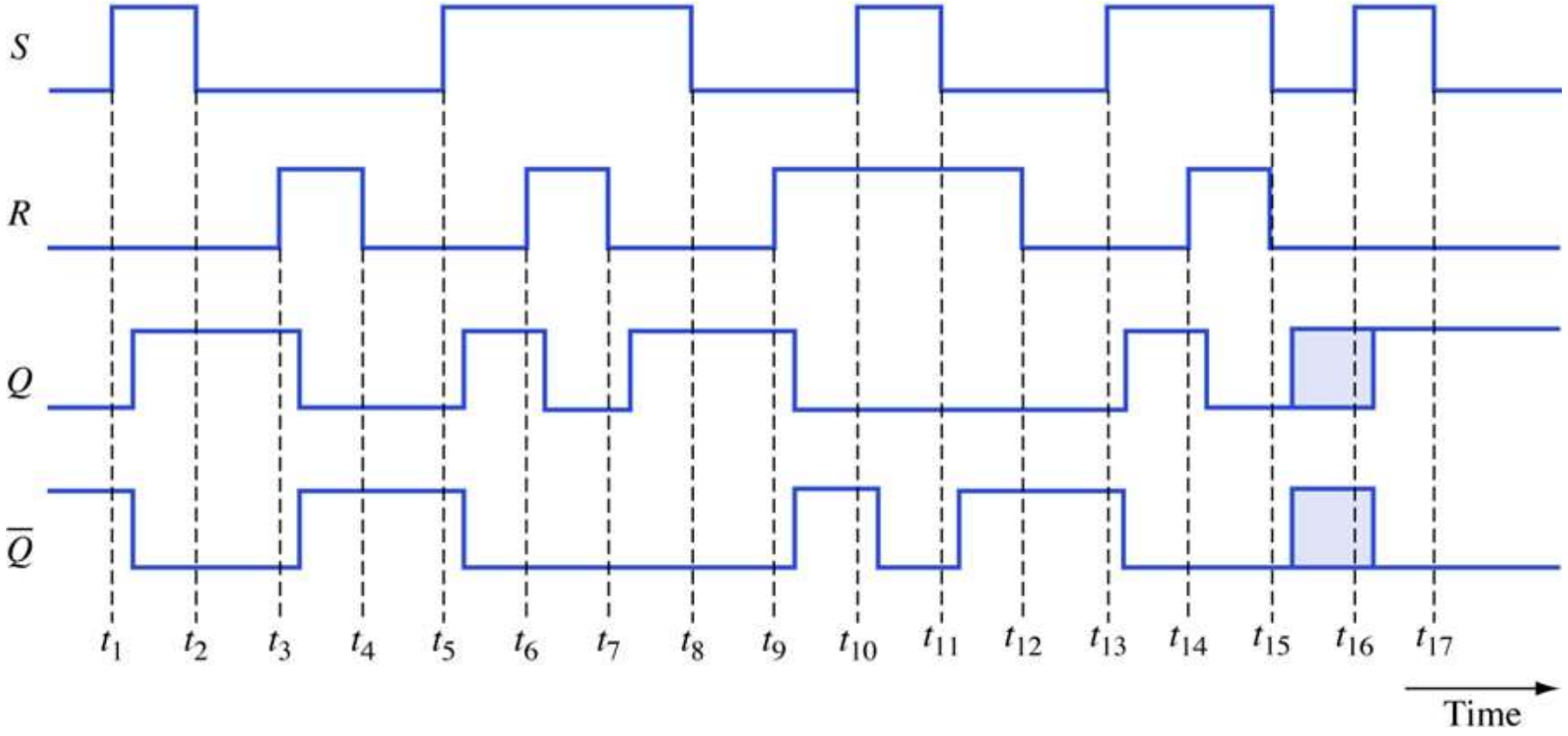
Propagation delays in an *SR* latch.

Figure 6.7



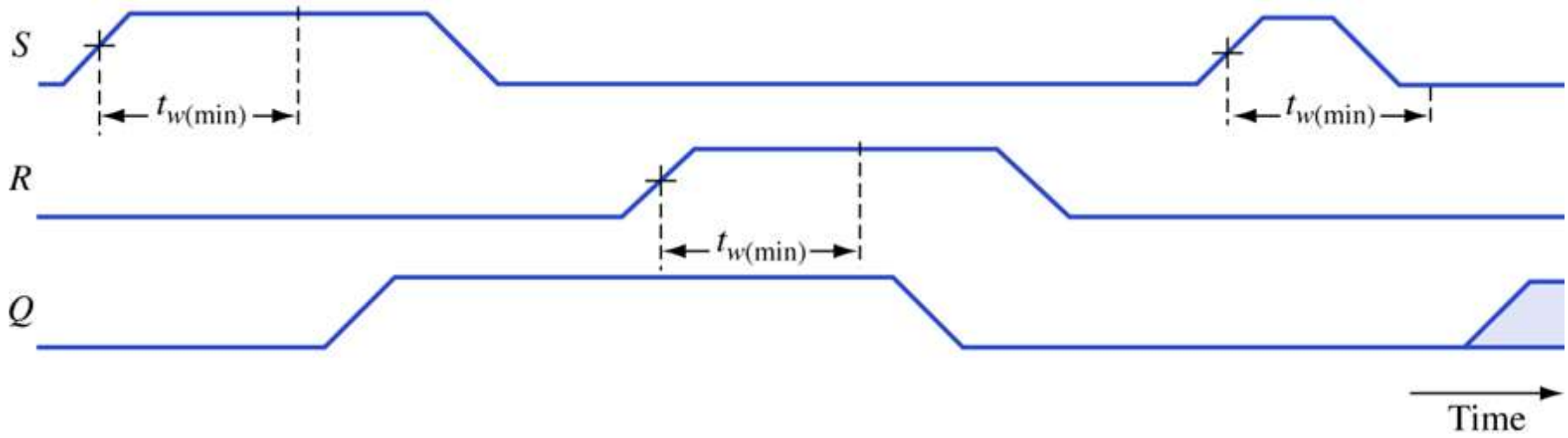
Timing diagram for an *SR* latch.

Figure 6.8



Minimum pulse width constraint.

Figure 6.9



Timing diagram for a gated *D* latch.

Figure 6.10

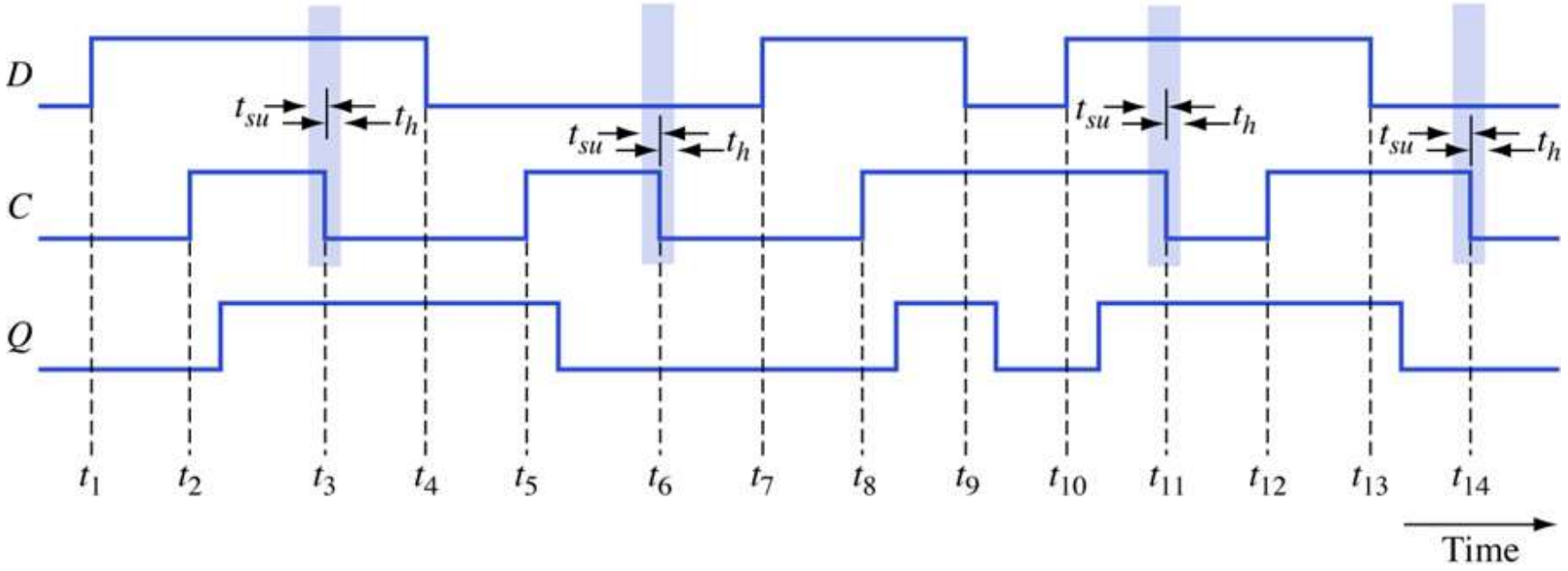
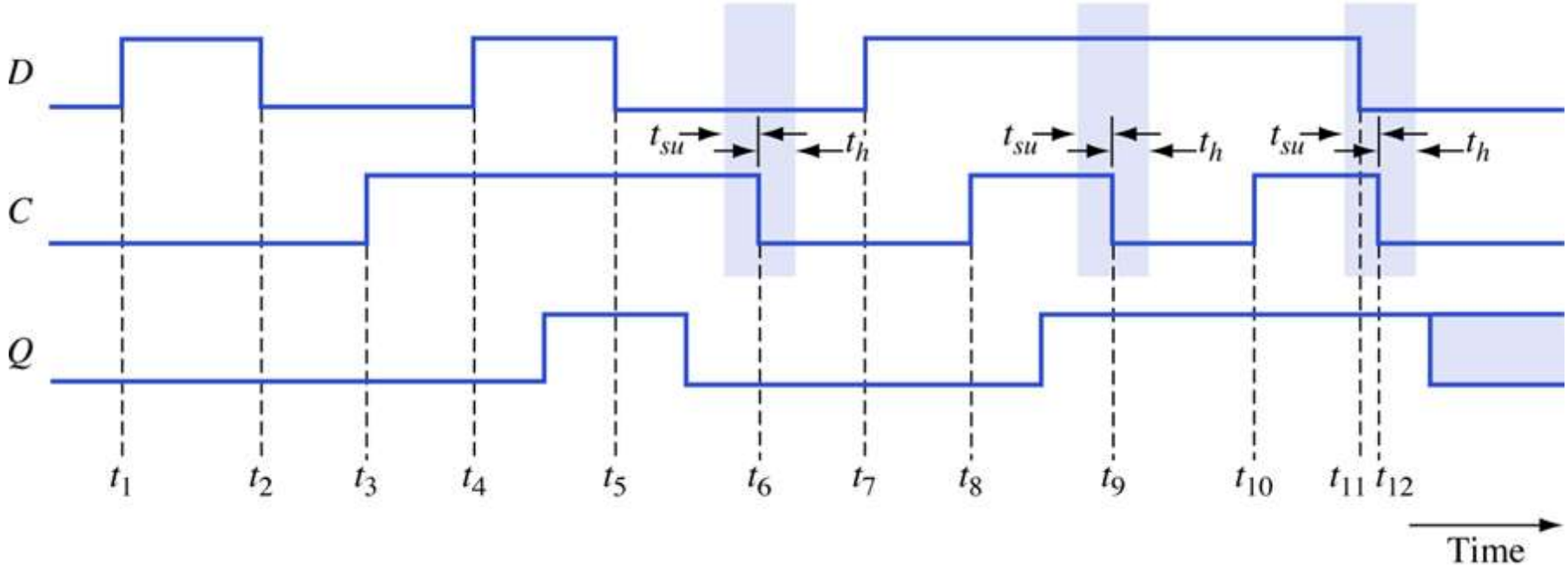


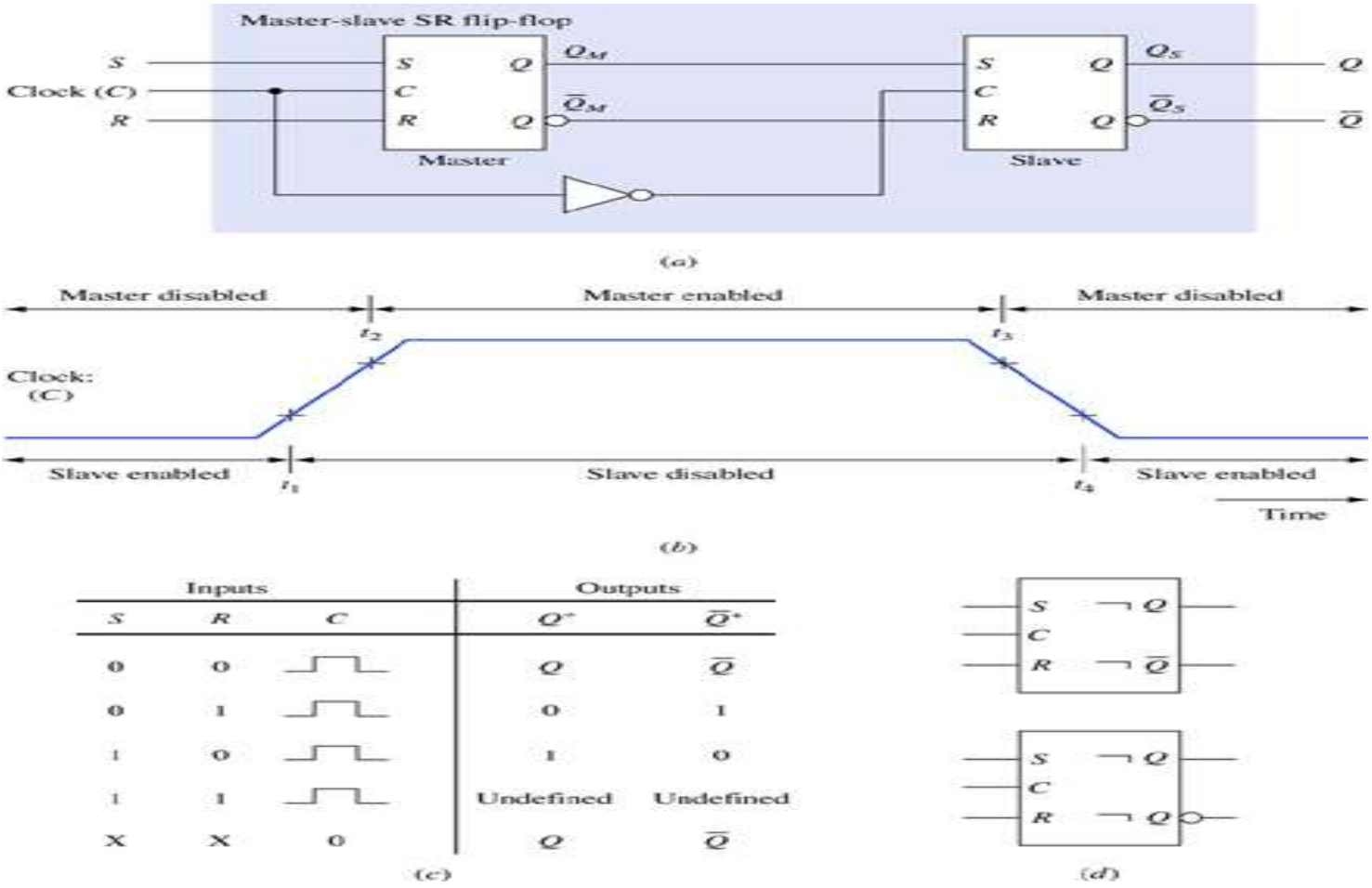
Illustration of an unpredictable response in a gated *D* latch.

Figure 6.11



Master-slave *SR* flip-flop. (*a*) Logic diagram using gated *SR* latches. (*b*) Flip-flop action during the control signal. (*c*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

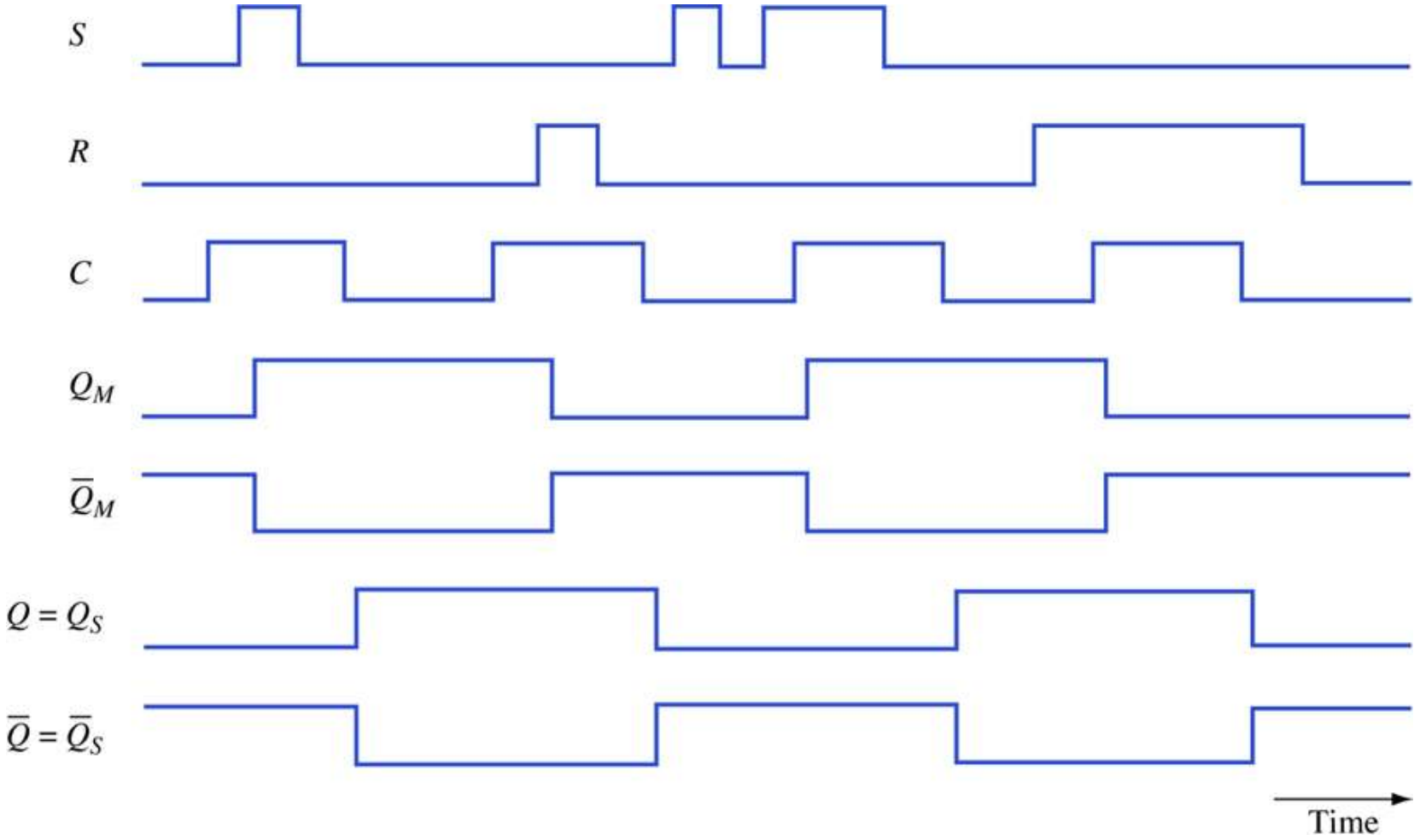
Figure 6.12



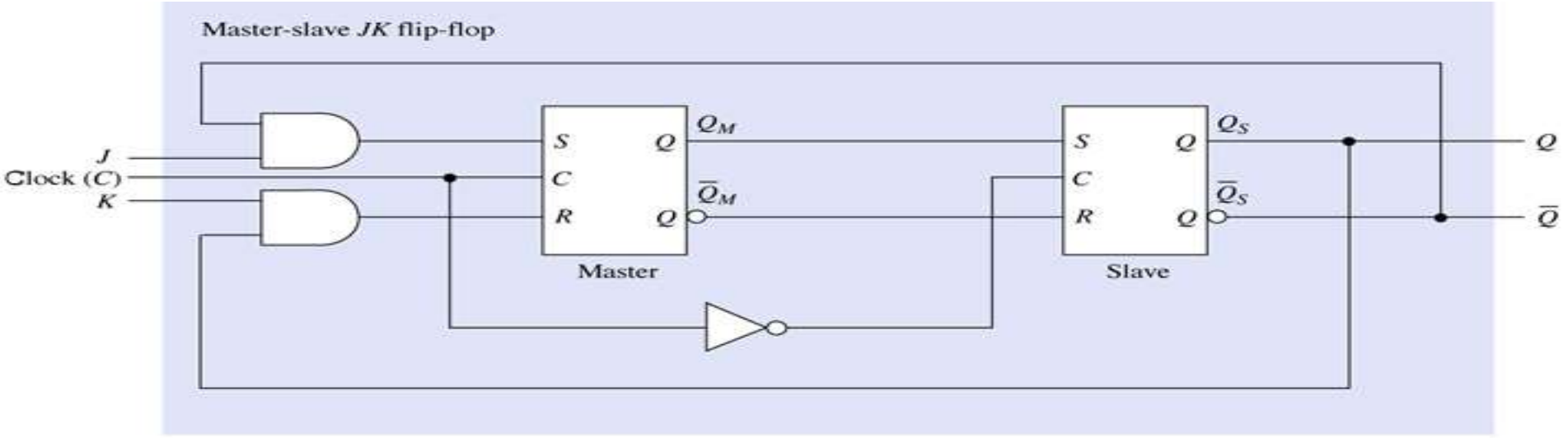
S	R	C	Q^+	$\overline{Q}^+$
0	0	⊓	Q	$\overline{Q}$
0	1	⊓	0	1
1	0	⊓	1	0
1	1	⊓	Undefined	Undefined
X	X	0	Q	$\overline{Q}$

Timing diagram for a master-slave *SR* flip-flop.

Figure 6.13



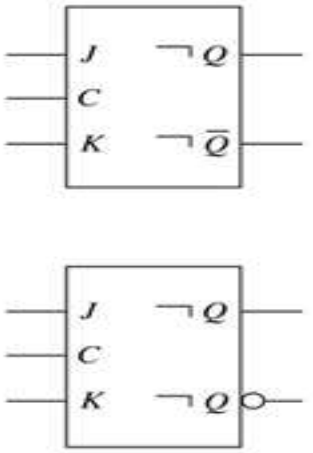
Master-slave *JK* flip-flop. (*a*) Logic diagram using gated *SR* latches. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.



(*a*)

Inputs			Outputs	
J	*K*	*C*	Q^+	$\overline{Q}^+$
0	0	⎍	*Q*	$\overline{Q}$
0	1	⎍	0	1
1	0	⎍	1	0
1	1	⎍	$\overline{Q}$	*Q*
X	X	0	*Q*	$\overline{Q}$

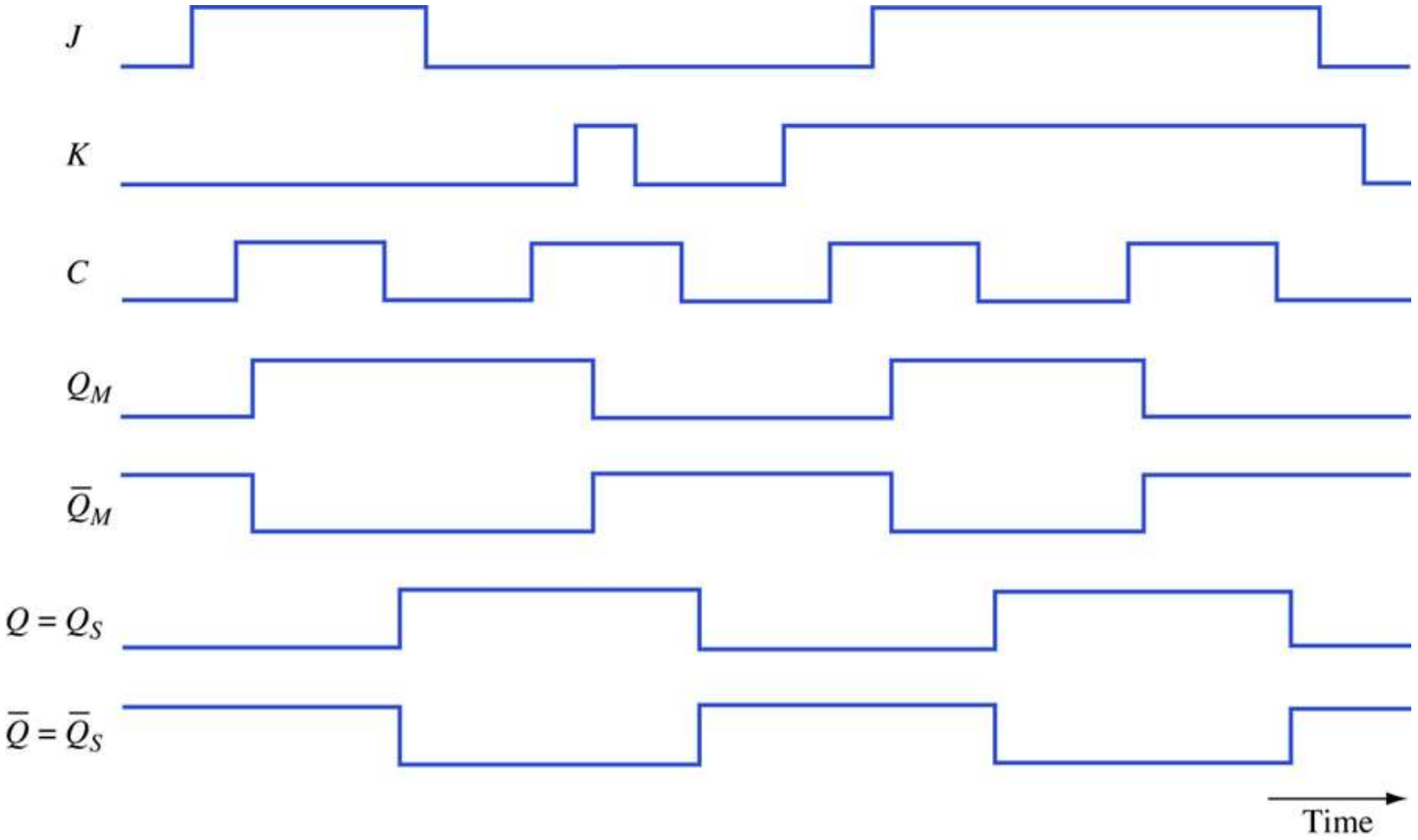
(*b*)



(*c*)

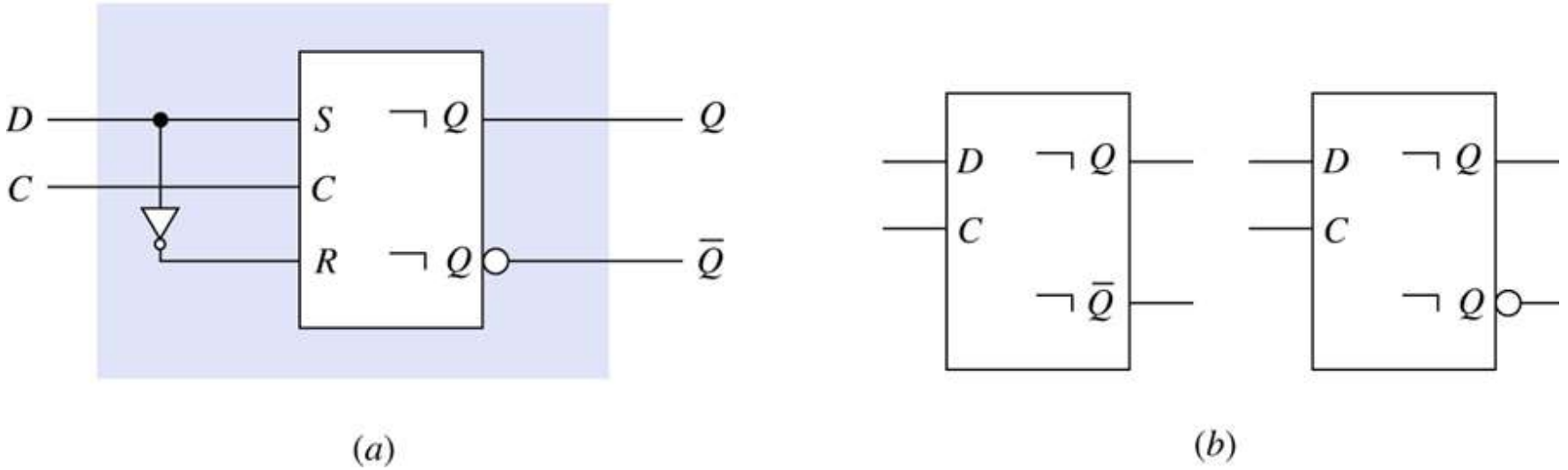
Timing diagram for master-slave *JK* flip-flop.

Figure 6.15



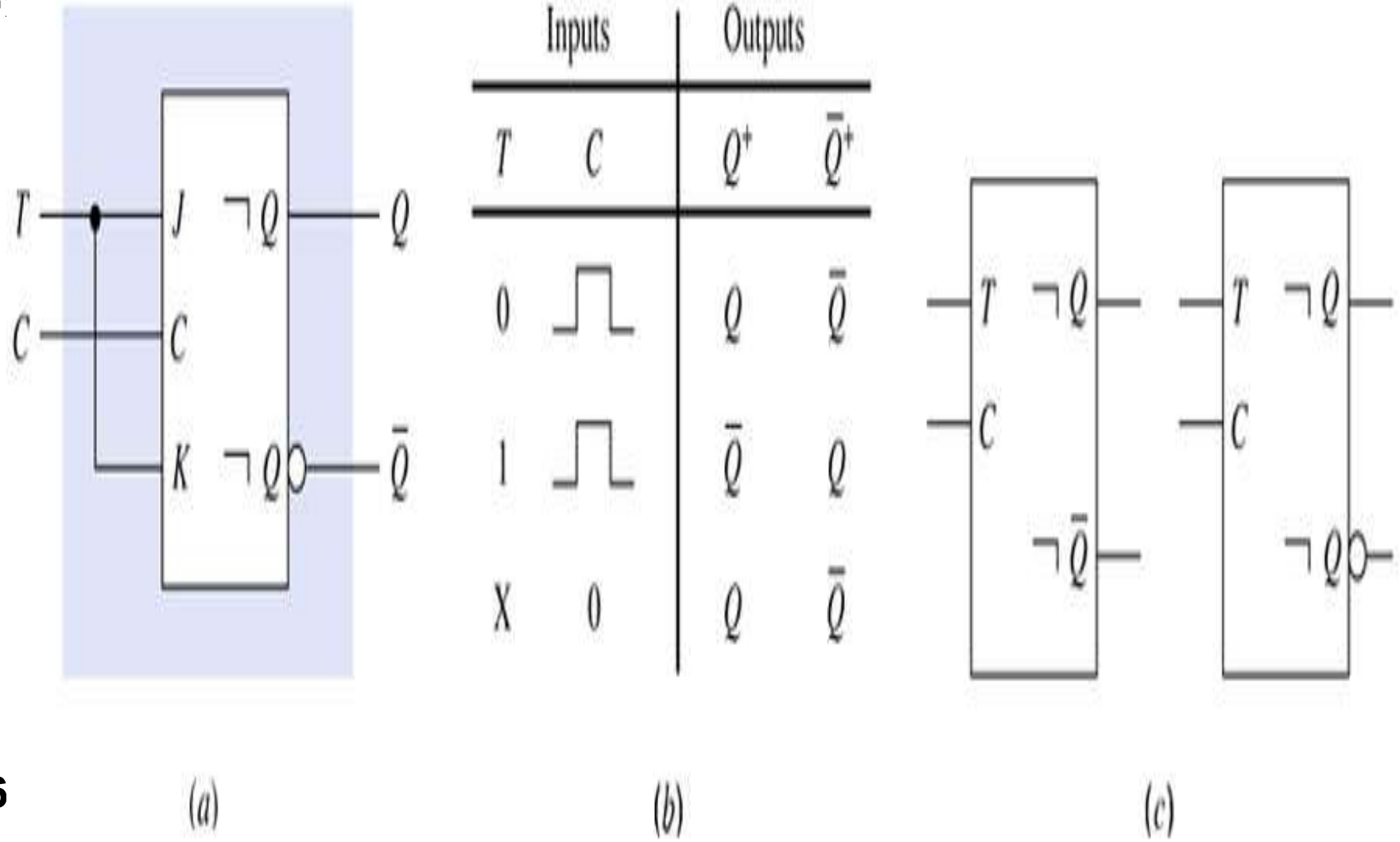
Master-slave *D* flip-flop. (*a*) Logic diagram using master-slave *SR* flip-flop (*b*) Two logic symbols.

Figure 6.16



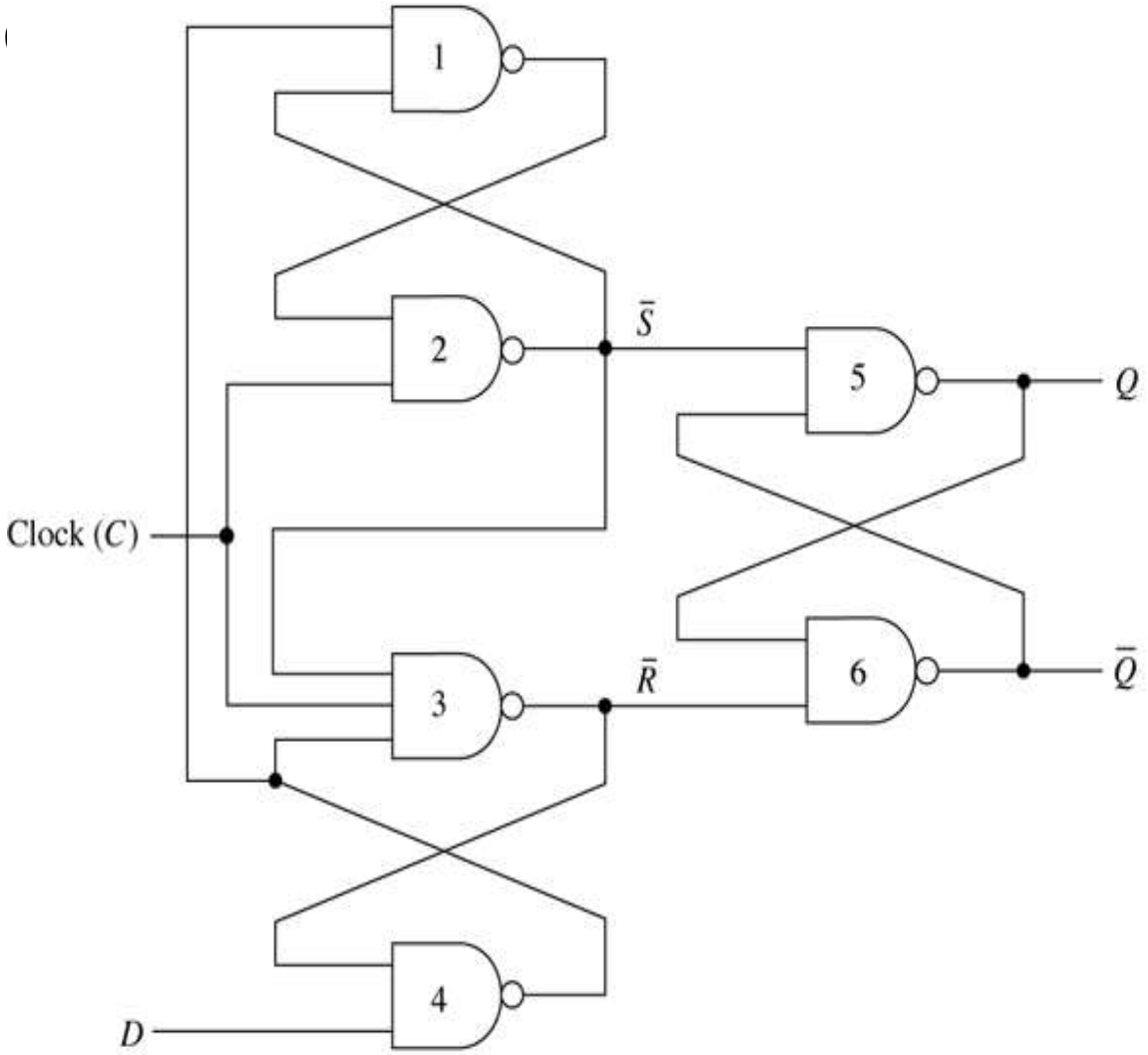
Master-slave *T* flip-flop. (*a*) Logic diagram using a master-slave *JK* flip-flop. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

F



Positive-edge-triggered *D* flip-flop. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

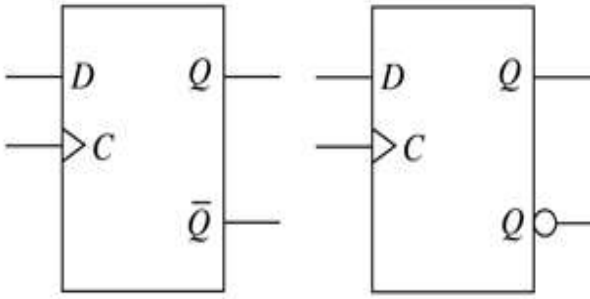
Figure



(a)

Inputs		Outputs	
D	C	Q^+	$\bar{Q}^+$
0	↑	0	1
1	↑	1	0
X	0	Q	$\bar{Q}$
X	1	Q	$\bar{Q}$

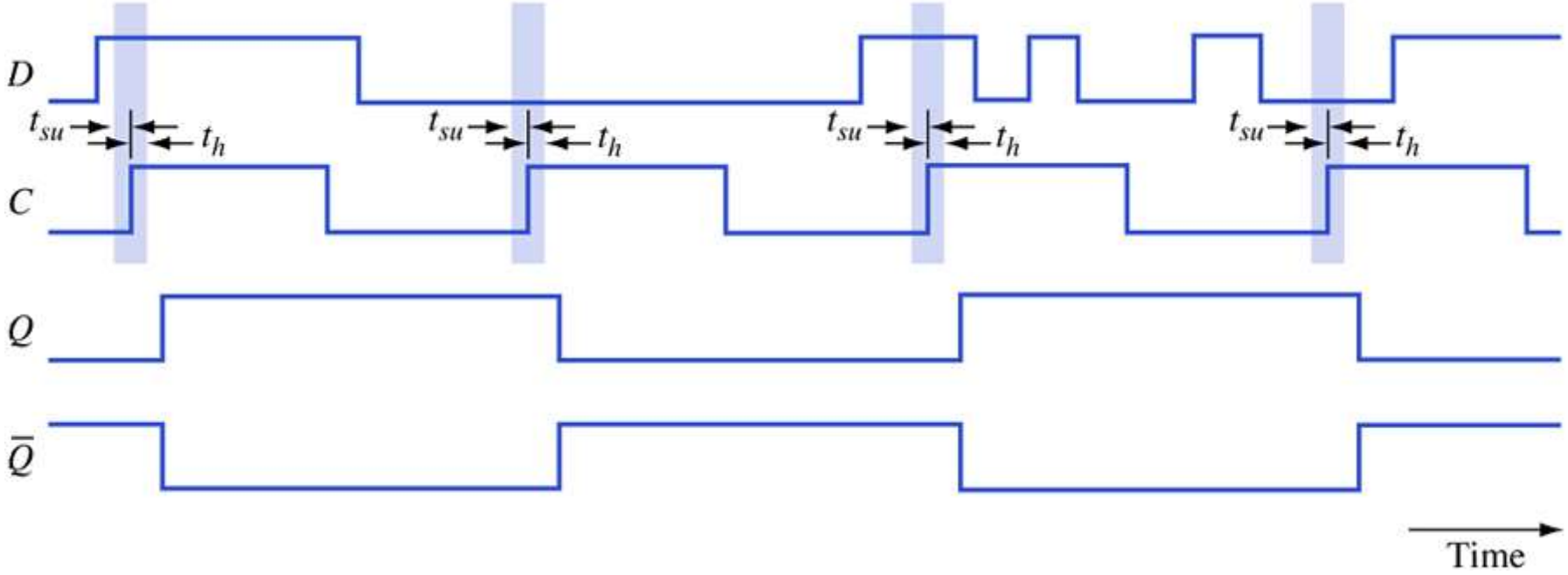
(b)



(c)

Timing diagram for a positive-edge-triggered *D* flip-flop.

Figure 6.19

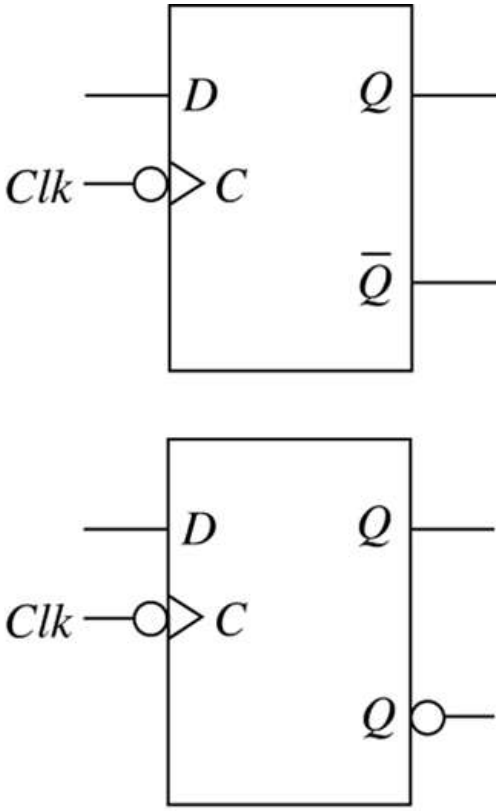


Negative-edge-triggered *D* flip-flop. (*a*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*b*) Two logic symbols.

Figure 6.20

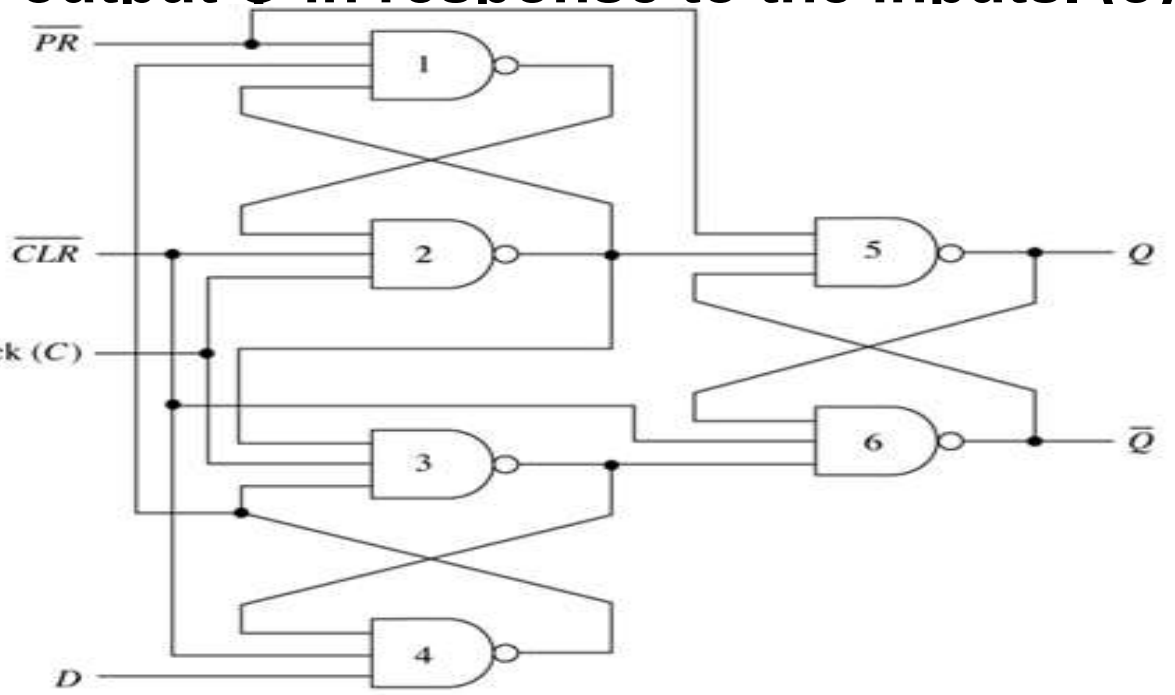
Inputs		Outputs	
D	*Clk*	Q^+	$\overline{Q}^+$
0	↓	0	1
1	↓	1	0
X	0	*Q*	$\overline{Q}$
X	1	*Q*	$\overline{Q}$

(*a*)



(*b*)

Positive-edge-triggered *D* flip-flop with asynchronous inputs. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

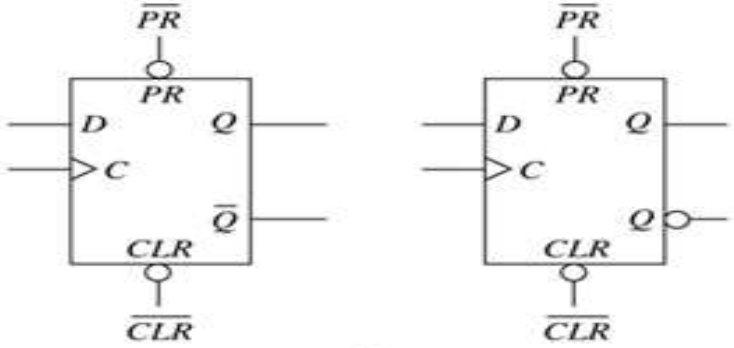


(*a*)

Inputs				Outputs	
$\overline{PR}$	$\overline{CLR}$	*D*	*C*	Q^+	$\overline{Q}^+$
0	1	X	X	1	0
1	0	X	X	0	1
0	0	X	X	1*	1*
1	1	0	↑	0	1
1	1	1	↑	1	0
1	1	X	0	*Q*	$\overline{Q}$
1	1	X	1	*Q*	$\overline{Q}$

*Unpredictable behavior will result if $\overline{PR}$ and $\overline{CLR}$ return to 1 simultaneously

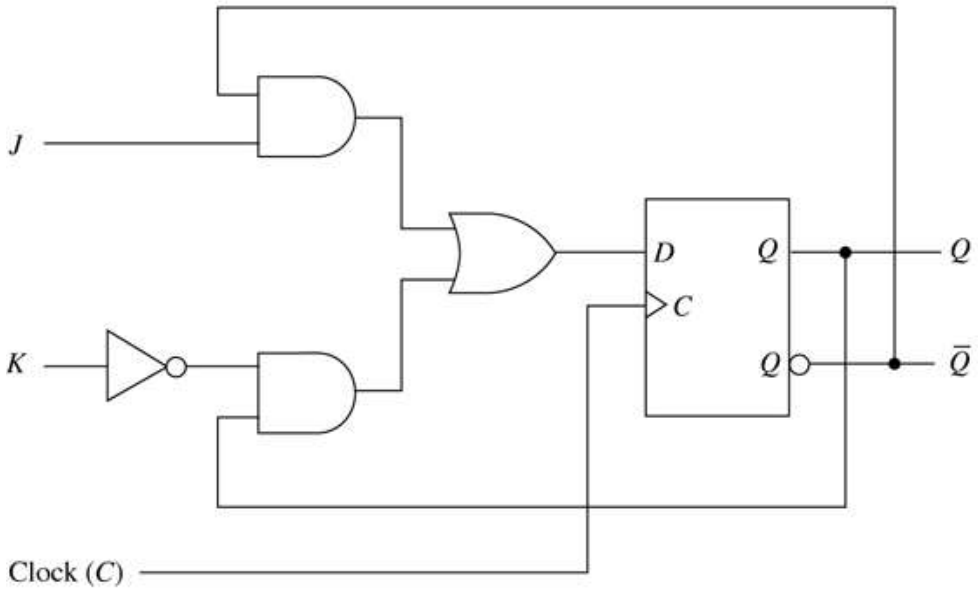
(*b*)



(*c*)

Positive-edge-triggered *JK* flip-flop. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output Q in response to the inputs. (*c*) Two logic symbols.

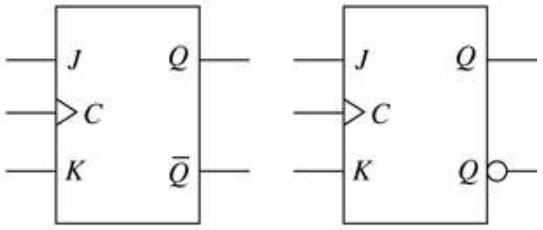
Figure 6.22



(a)

Inputs			Outputs	
J	K	C	Q^+	$\overline{Q}^+$
0	0	↑	Q	$\overline{Q}$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}$	Q
X	X	0	Q	$\overline{Q}$
X	X	1	Q	$\overline{Q}$

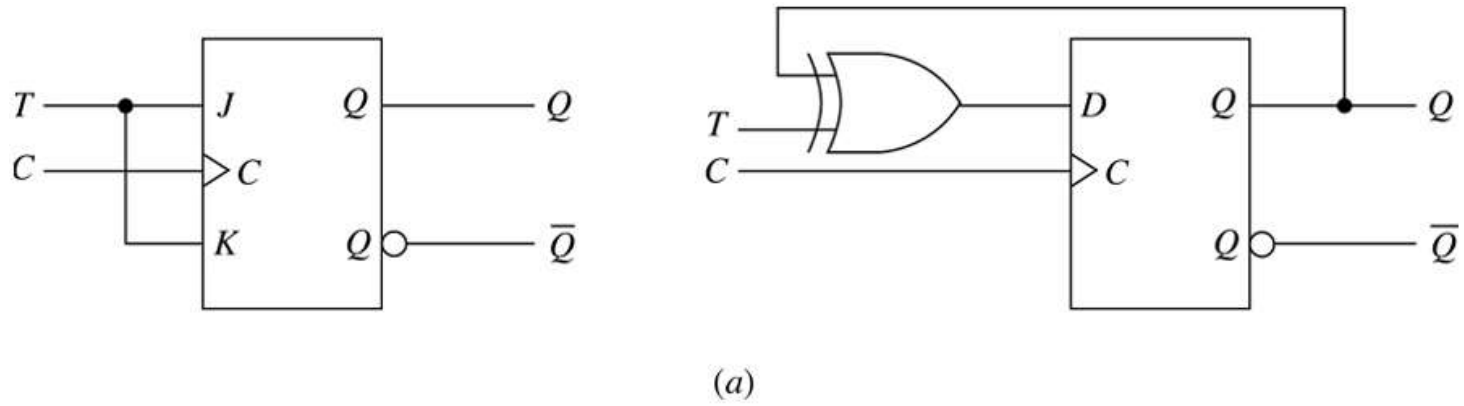
(b)



(c)

Positive-edge-triggered *T* flip-flop. (*a*) Logic diagram. (*b*) Function table where Q^+ denotes the output *Q* in response to the inputs. (*c*) Two logic symbols.

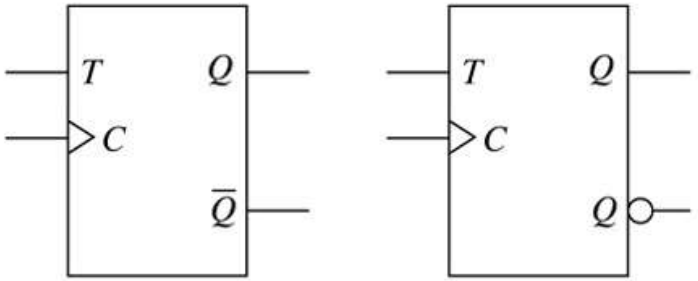
Figure 6.23



(*a*)

Inputs		Outputs	
T	*C*	Q^+	$\overline{Q}^+$
0	↑	*Q*	$\overline{Q}$
1	↑	$\overline{Q}$	*Q*
X	0	*Q*	$\overline{Q}$
X	1	*Q*	$\overline{Q}$

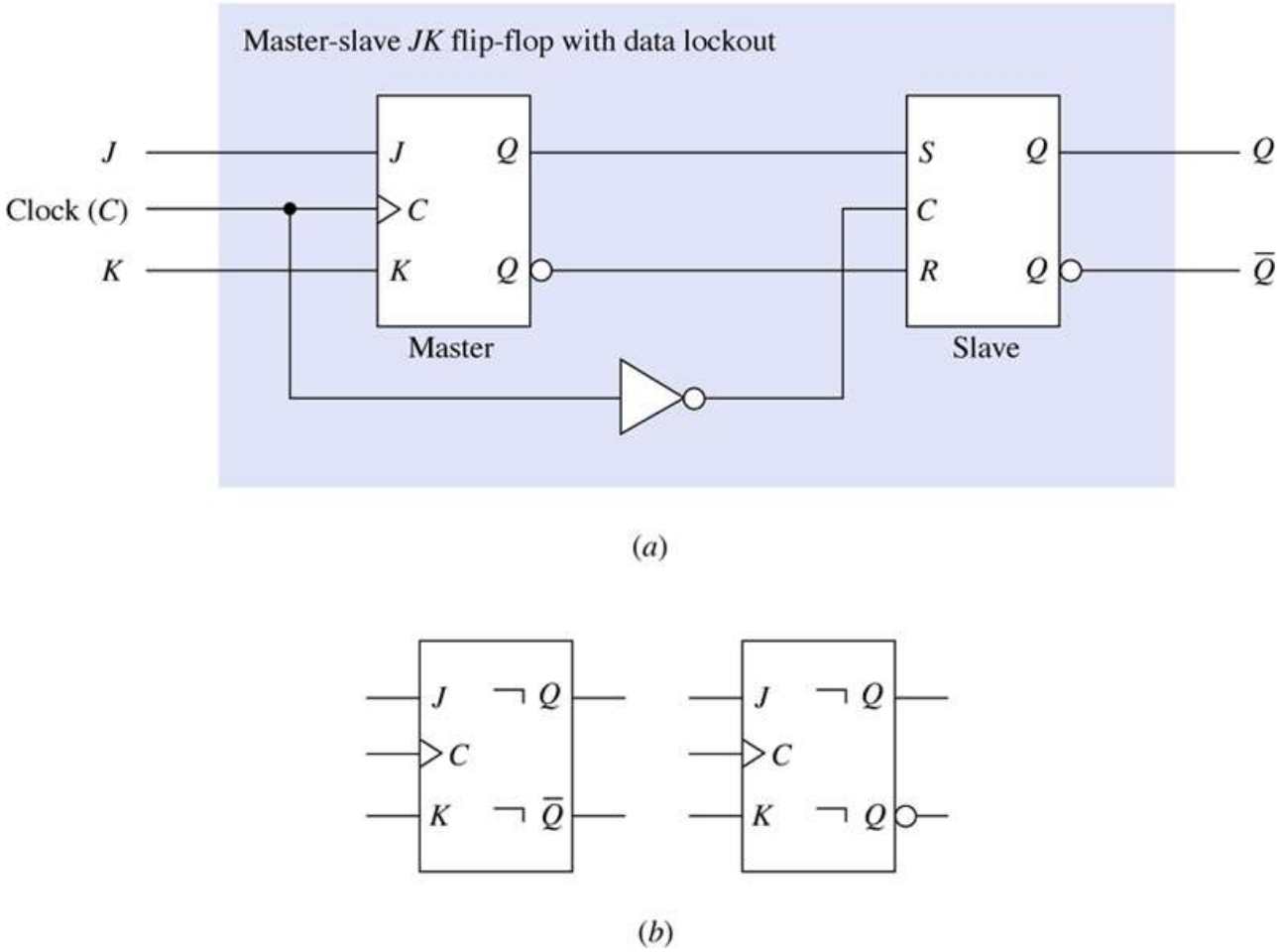
(*b*)



(*c*)

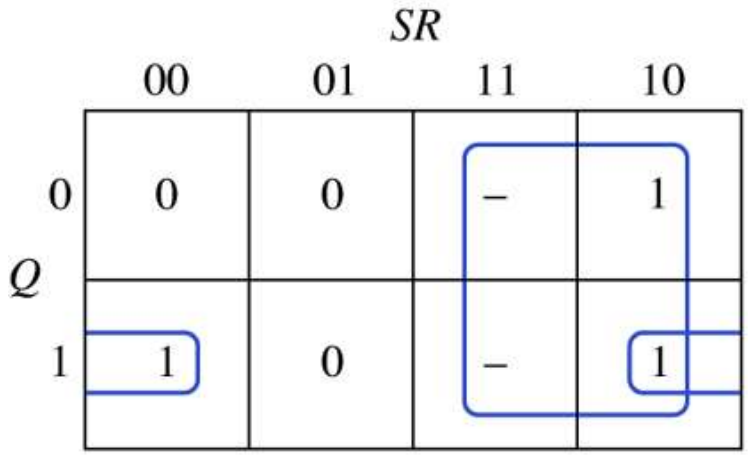
Master-slave *JK* flip-flop with data lockout. (*a*) Logic diagram. (*b*) Two logic symbols.

Figure 6.24



Characteristic equations. (*a*) Derivation of characteristic equation for an *SR* flip-flop. (*b*) Summary of characteristic equations.

Figure 6.25



$Q^+ = S + \bar{R}Q \quad (SR = 0)$

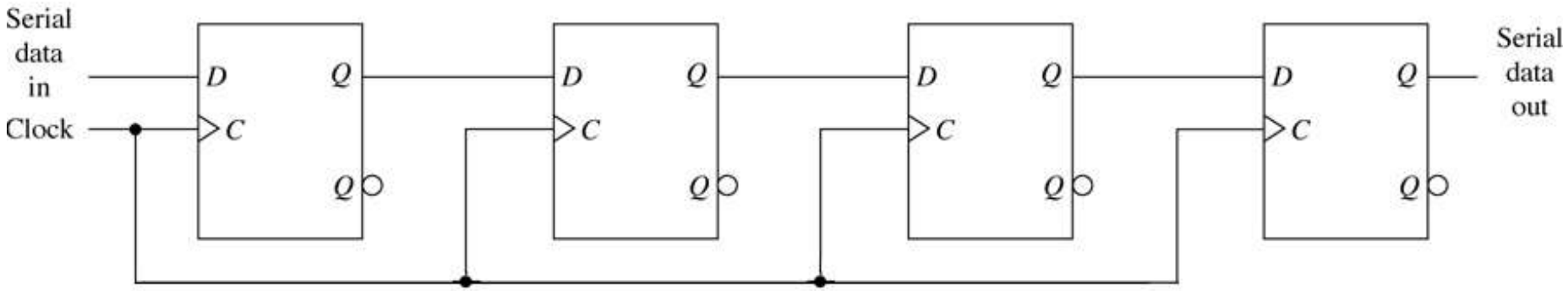
(*a*)

Flip-flop type	Characteristic equation
SR	$Q^+ = S + \bar{R}Q \quad (SR = 0)$
JK	$Q^+ = J\bar{Q} + \bar{K}Q$
D	$Q^+ = D$
T	$Q^+ = T\bar{Q} + \bar{T}Q = T \oplus Q$

(*b*)

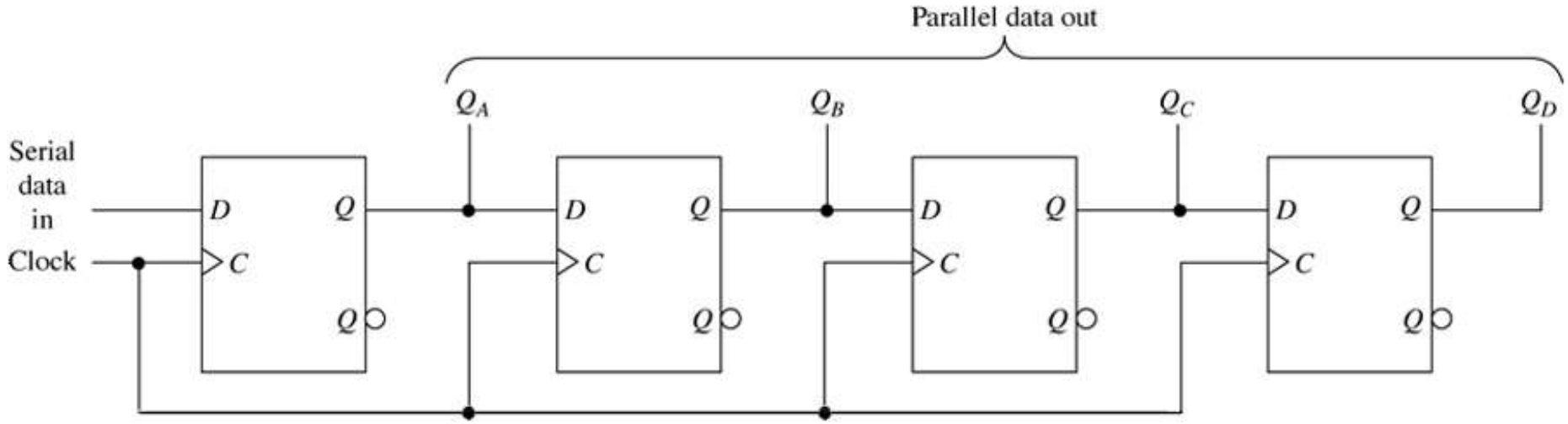
Serial-in, serial-out unidirectional shift register.

Figure 6.26



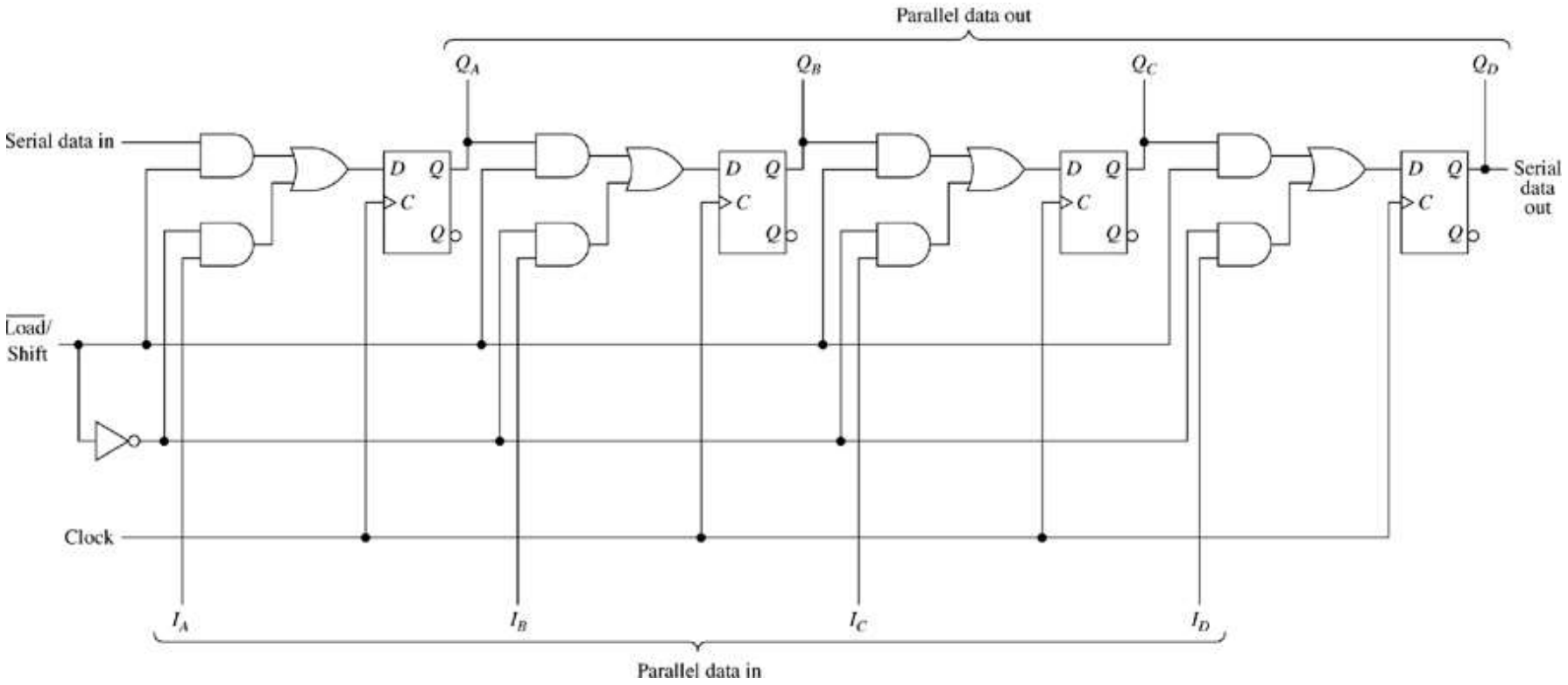
Serial-in, parallel-out unidirectional shift register.

Figure 6.27



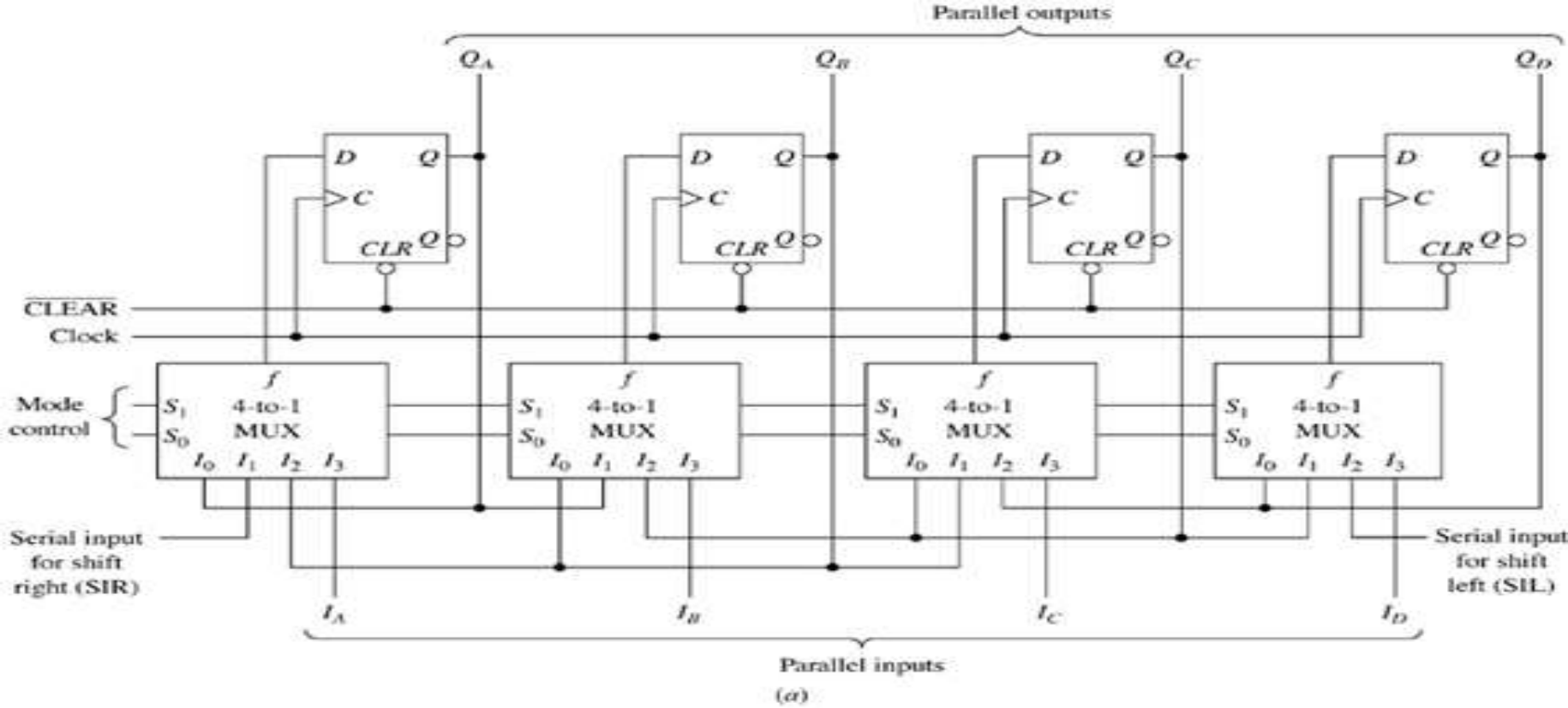
Parallel-in unidirectional shift register.

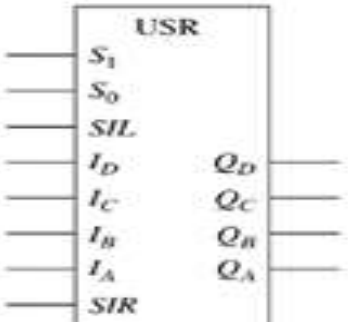
Figure 6.28



Universal shift register. (*a*) Logic diagram. (*b*) Mode control. (*c*) Symbol.

Figu



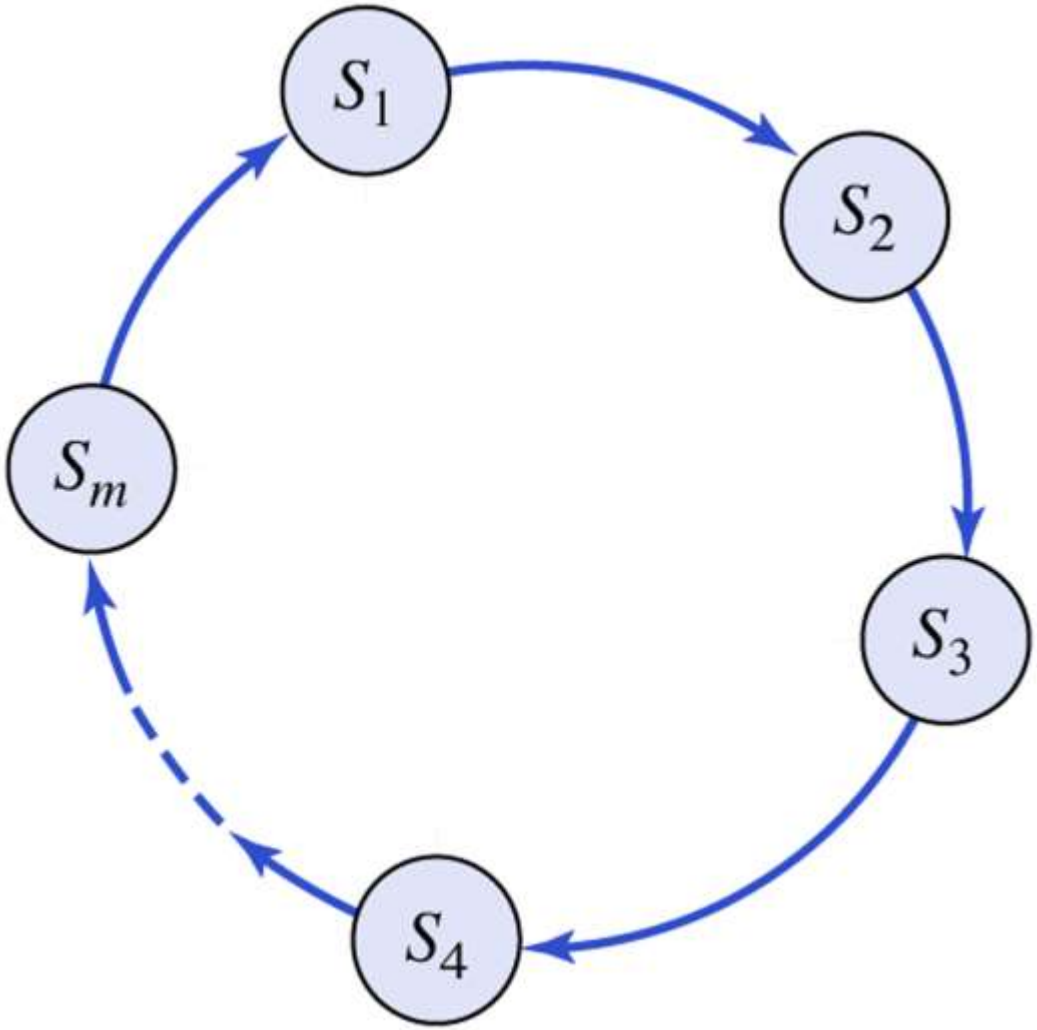


6-2

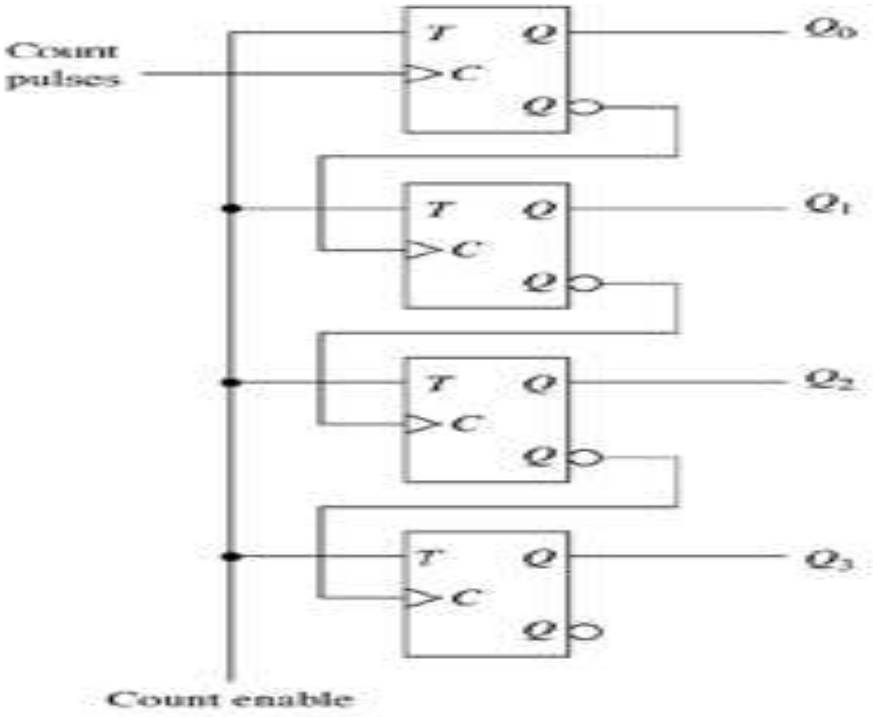
Select lines S_1	S_0	Register operation
0	0	Hold

State diagram of a counter.

Figure 6.30



Four-bit binary ripple counter. (*a*) Logic diagram. (*b*) Timing diagram. (*c*) Counting sequence.

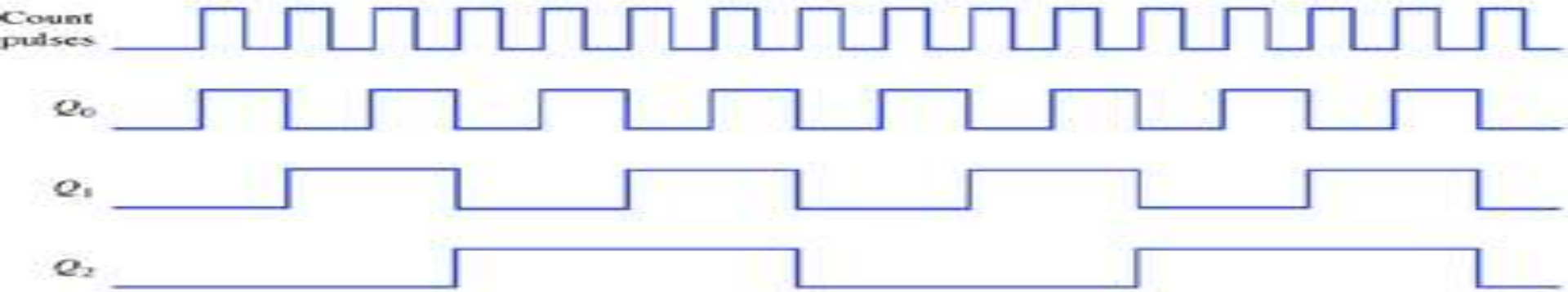


(*a*)

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0

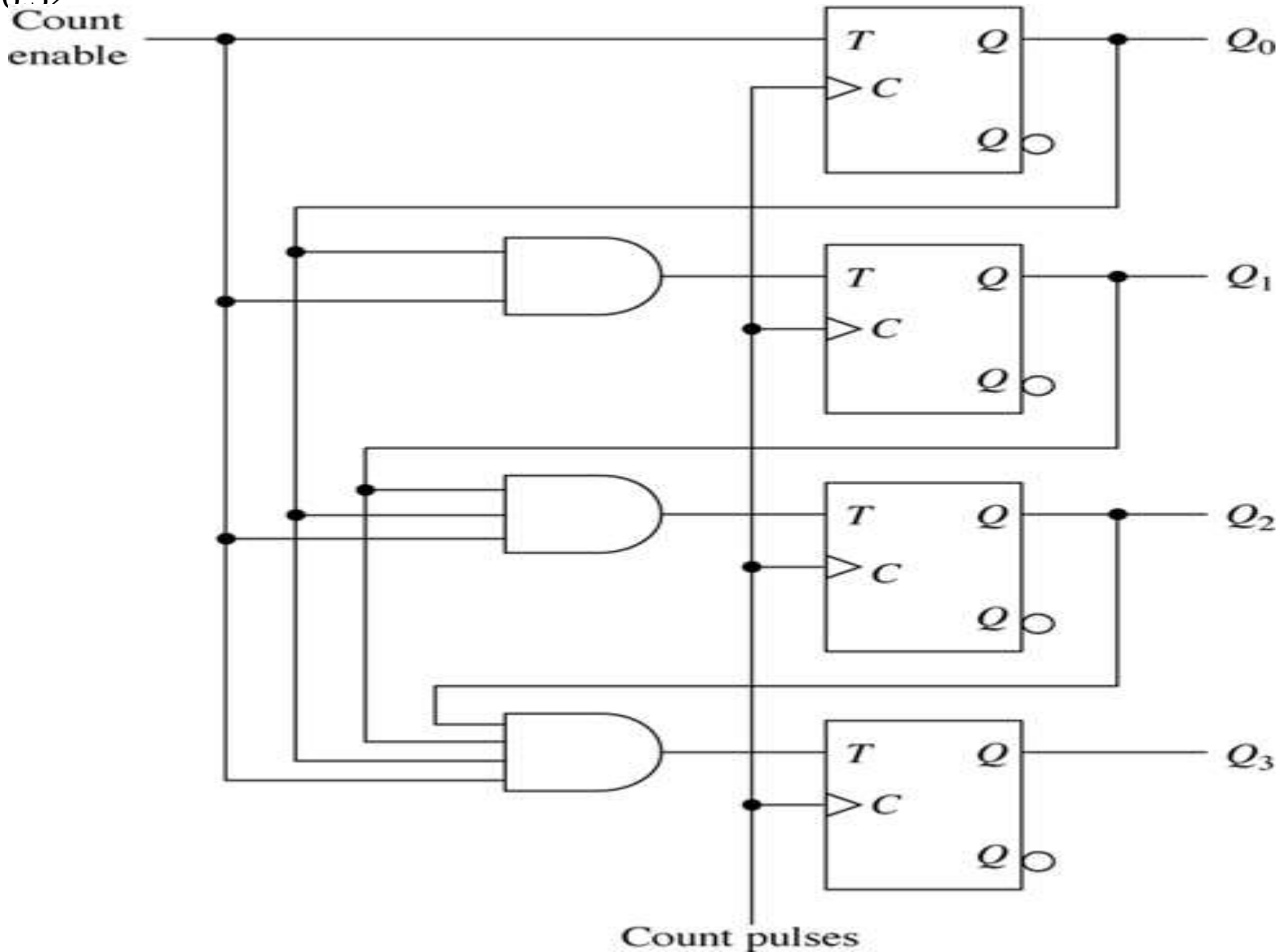
etc.

(*c*)



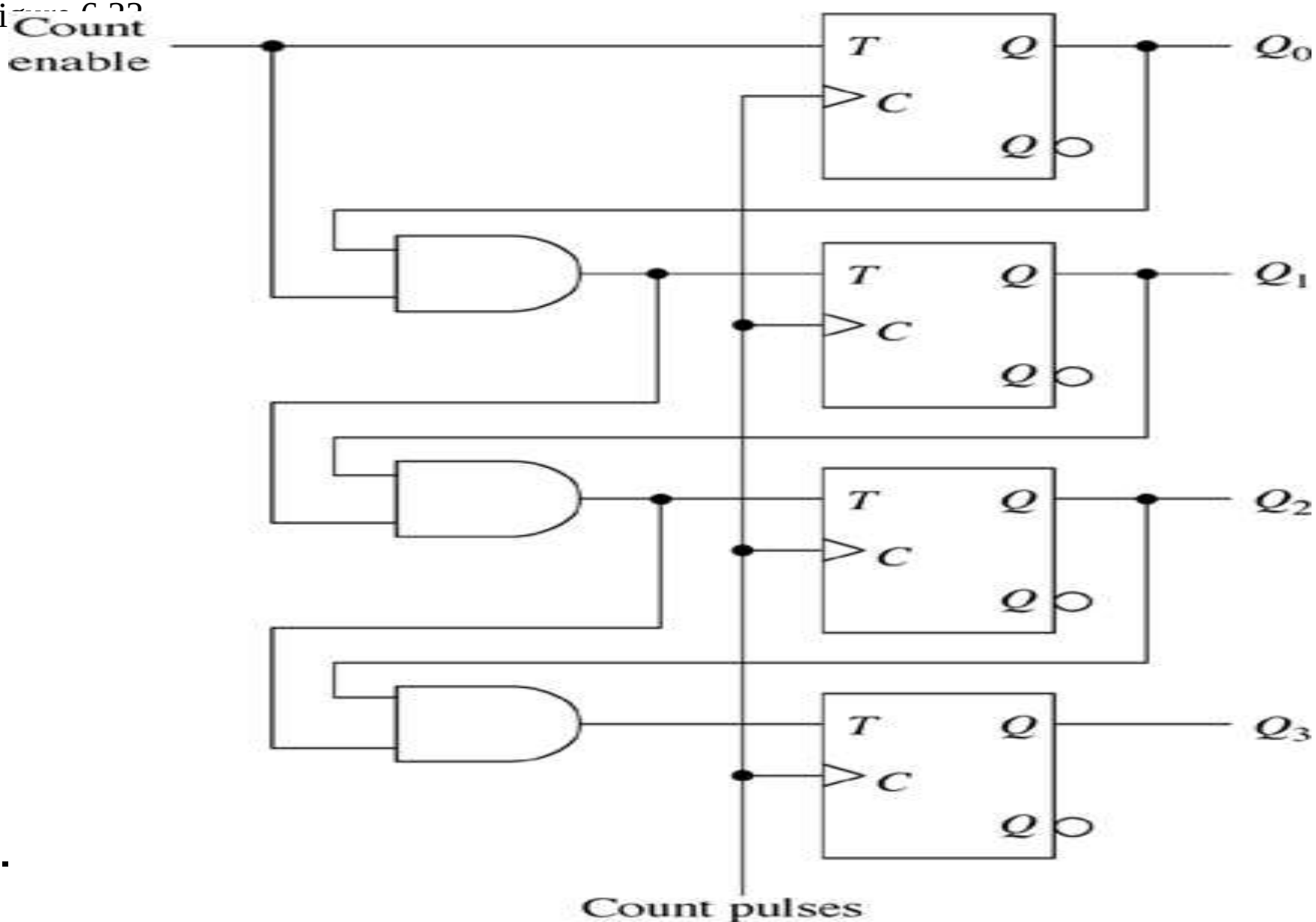
Four-bit synchronous binary counter.

Figure 6.32



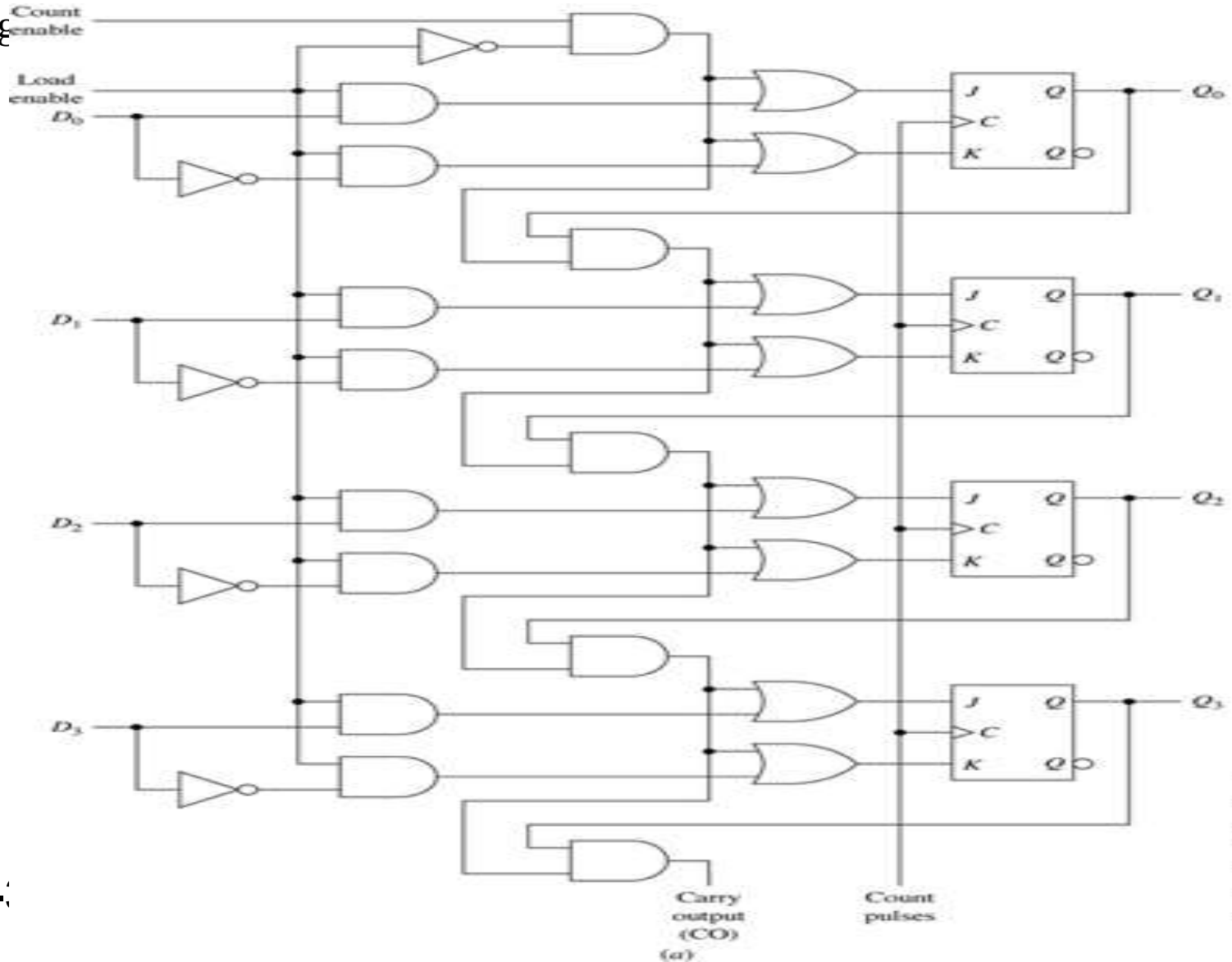
Four-bit synchronous binary counter variation.

Figure 6.22



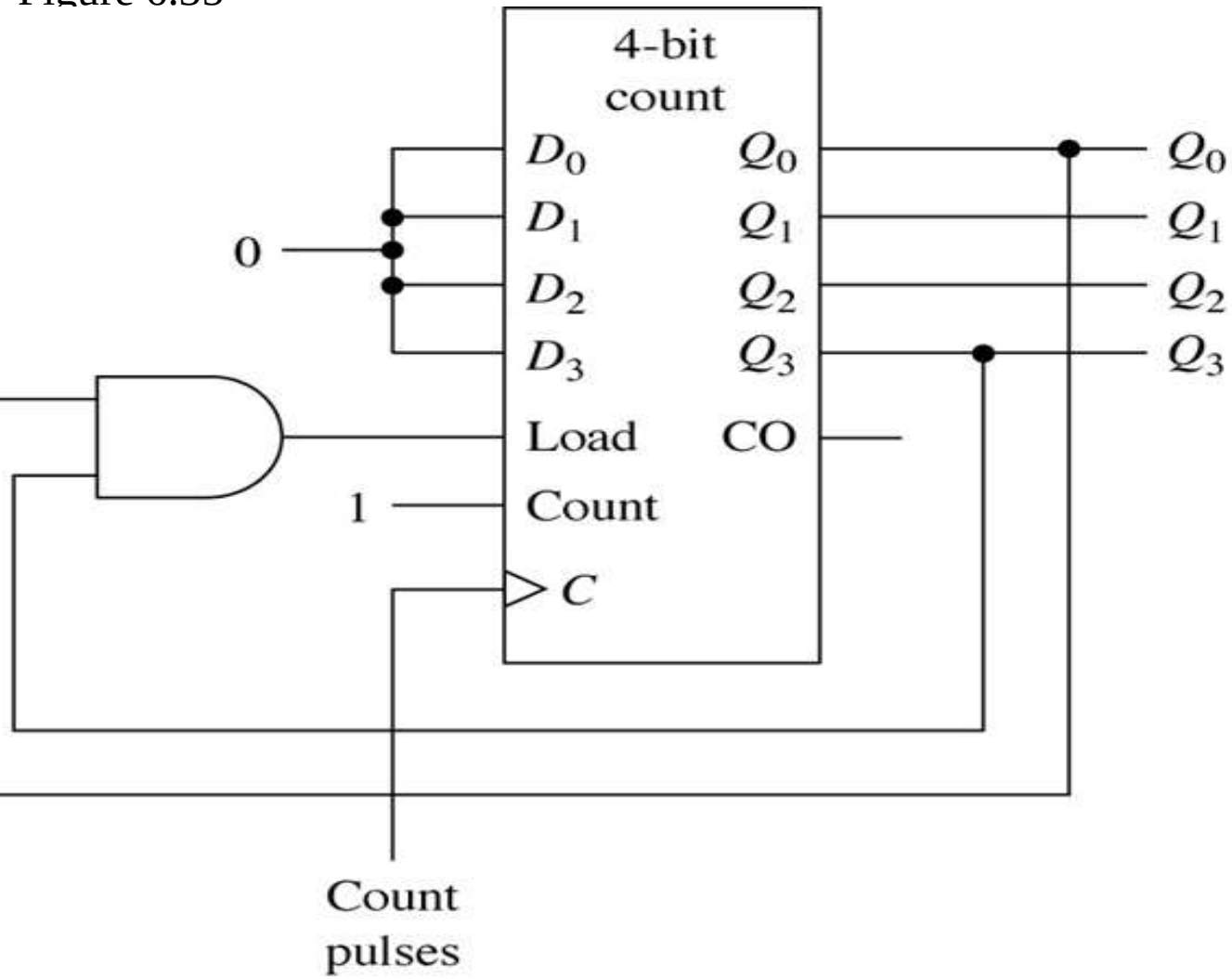
Four-bit synchronous binary counter with parallel load inputs. (*a*) Logic diagram. (*b*) Symbol.

Fig



Synchronous mod-10 counter. (*a*) Connections. (*b*) Counting sequence.

Figure 6.35



(*a*)

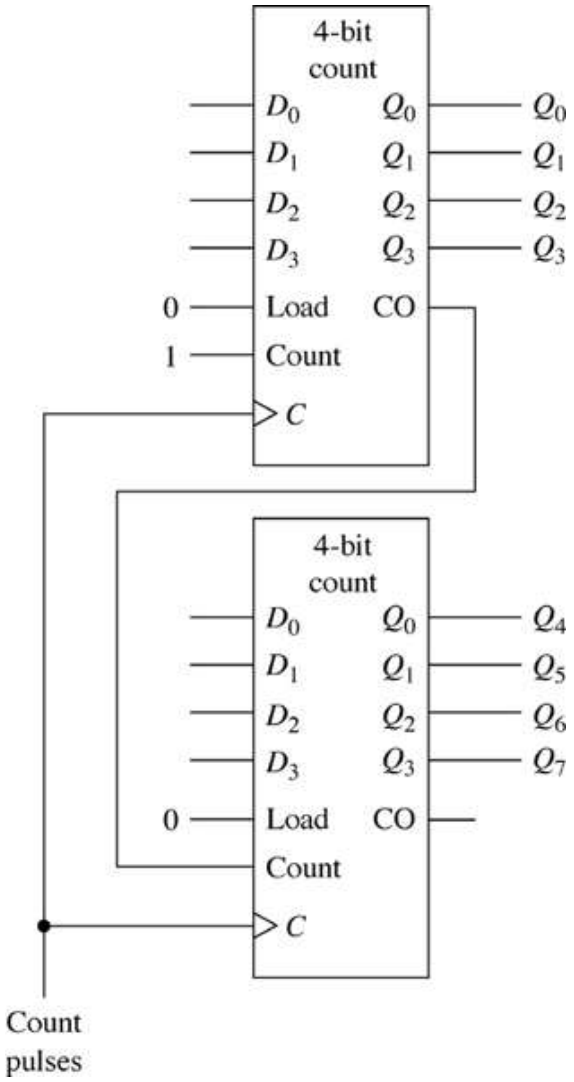
Q_3	Q_2	Q_1
0	0	0
0	0	0
0	0	1
0	0	1
0	1	0
0	1	0
0	1	1
0	1	1
1	0	0
1	0	0
0	0	0

etc.

(*b*)

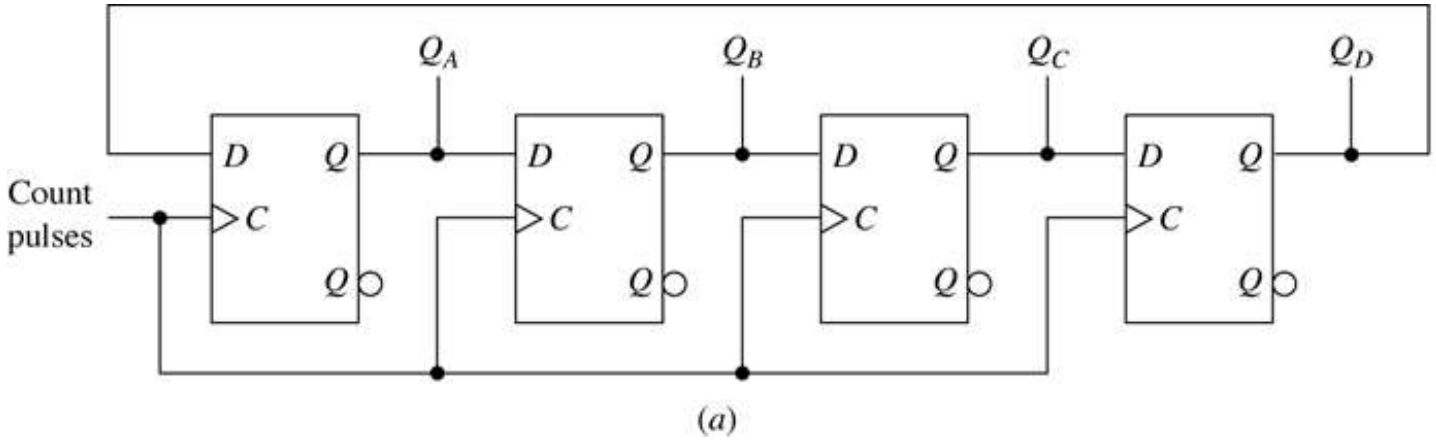
8-bit synchronous binary counter constructed from two 4-bit synchronous binary counters.

Figure 6.36



Mod-4 ring counter. (*a*) Logic diagram. (*b*) Counting sequence.

Figure 6.37



(*a*)

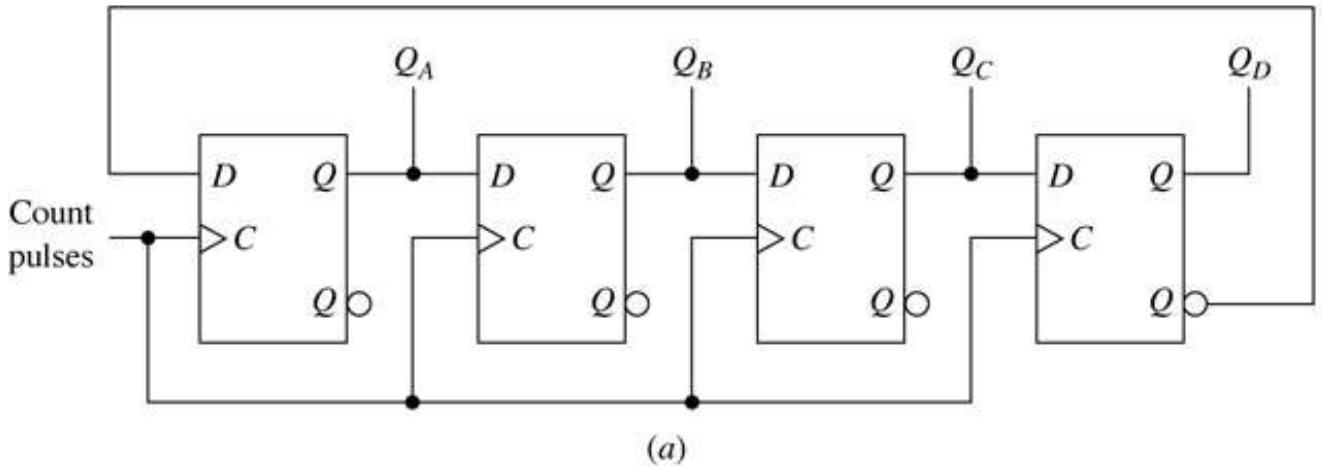
Q_A	Q_B	Q_C	Q_D
1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1
1	0	0	0

etc.

(*b*)

Mod-8 twisted-ring counter. (*a*) Logic diagram. (*b*) Counting sequence.

Figure 6.38



(*a*)

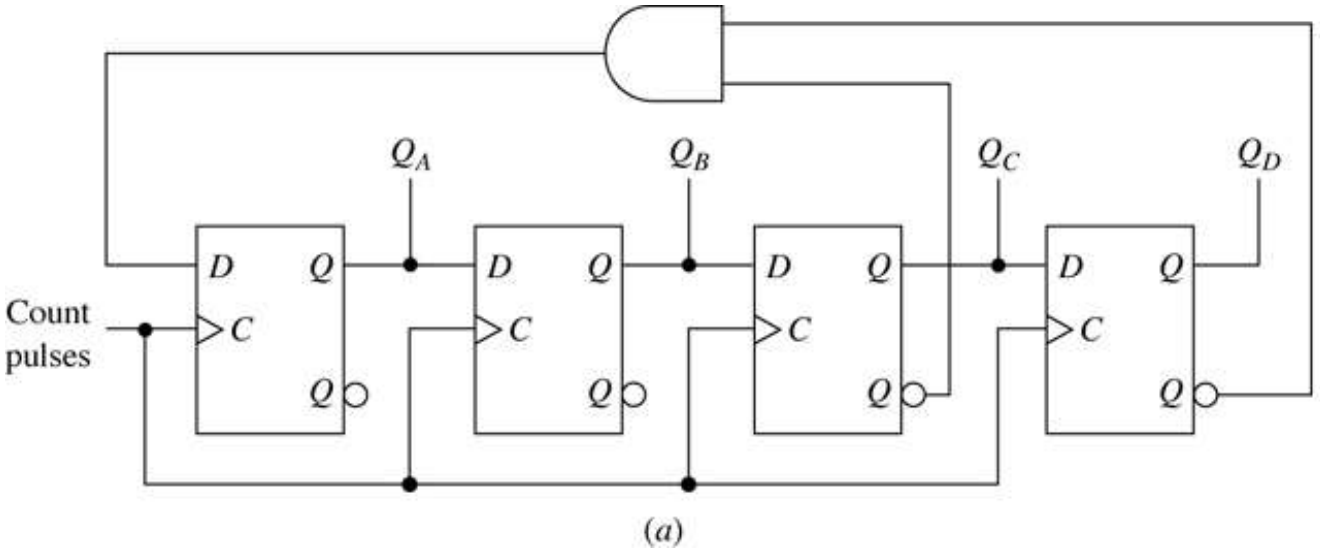
Q_A	Q_B	Q_C	Q_D	And-gate inputs
0	0	0	0	$\overline{Q}_A\overline{Q}_D$
1	0	0	0	$Q_A\overline{Q}_B$
1	1	0	0	$Q_B\overline{Q}_C$
1	1	1	0	$Q_C\overline{Q}_D$
1	1	1	1	Q_AQ_D
0	1	1	1	$\overline{Q}_AQ_B$
0	0	1	1	$\overline{Q}_BQ_C$
0	0	0	1	$\overline{Q}_CQ_D$
0	0	0	0	

etc.

(*b*)

Mod-7 twisted-ring counter. (*a*) Logic diagram. (*b*) Counting sequence.

Figure 6.39



(*a*)

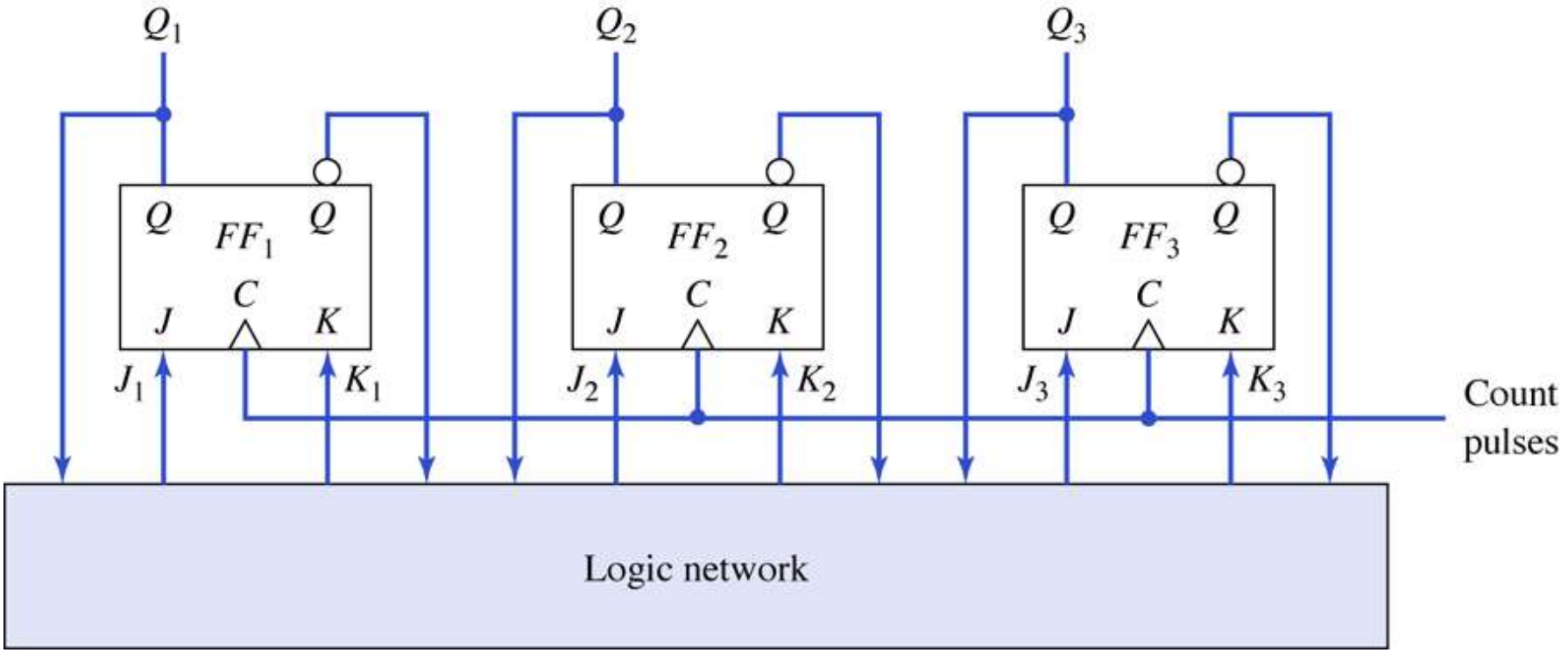
Q_A	Q_B	Q_C	Q_D	And-gate inputs
0	0	0	0	$\overline{Q}_A\overline{Q}_D$
1	0	0	0	$Q_A\overline{Q}_B$
1	1	0	0	$Q_B\overline{Q}_C$
1	1	1	0	$Q_C\overline{Q}_D$
0	1	1	1	$\overline{Q}_AQ_B$
0	0	1	1	$\overline{Q}_BQ_C$
0	0	0	1	$\overline{Q}_CQ_D$
0	0	0	0	

etc.

(*b*)

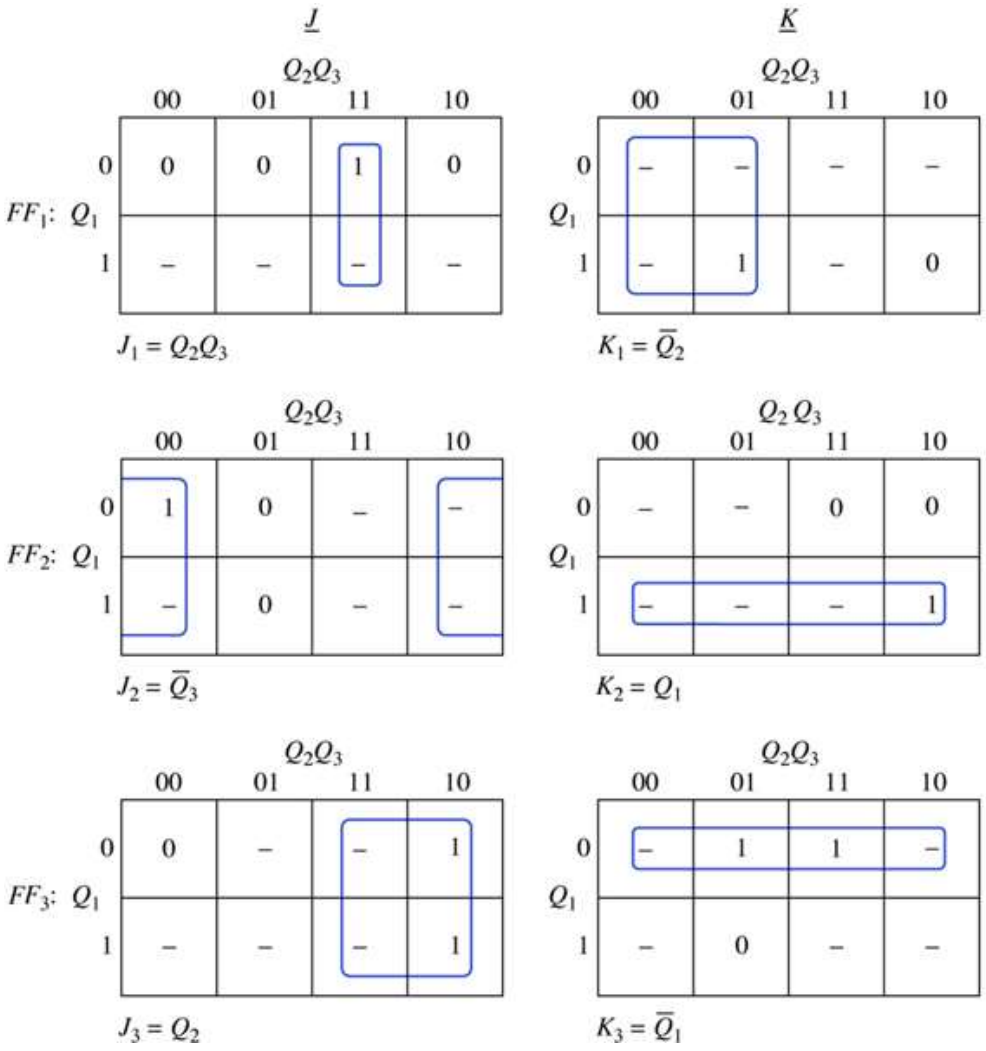
General structure of a synchronous mod-6 counter using positive-edge-triggered *JK* flip-flops.

Figure 6.40



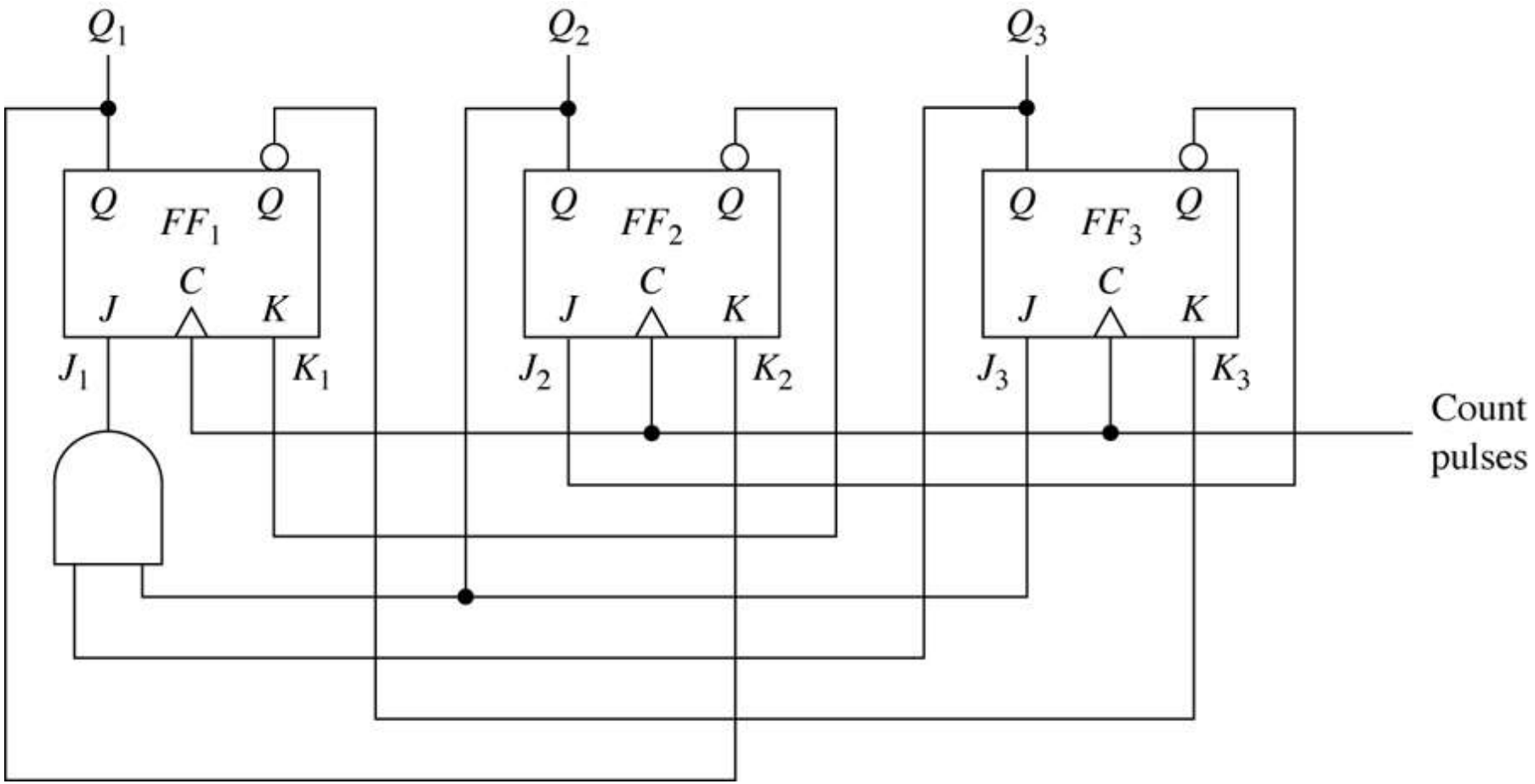
Determination of the minimal-sum expressions for a synchronous mod-6 counter using clocked *JK* flip-flops.

Figure 6.41



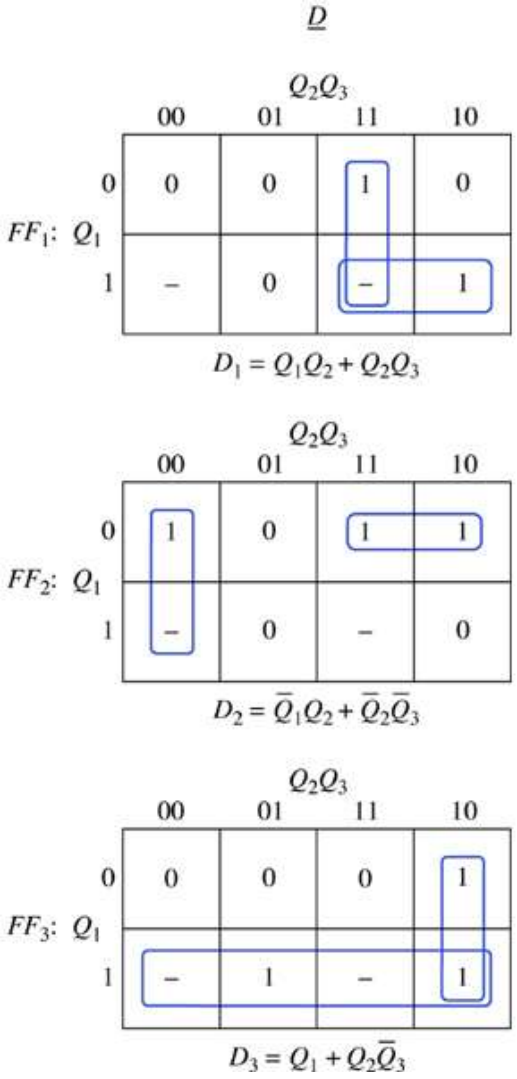
Logic diagram of a synchronous mod-6 counter.

Figure 6.42



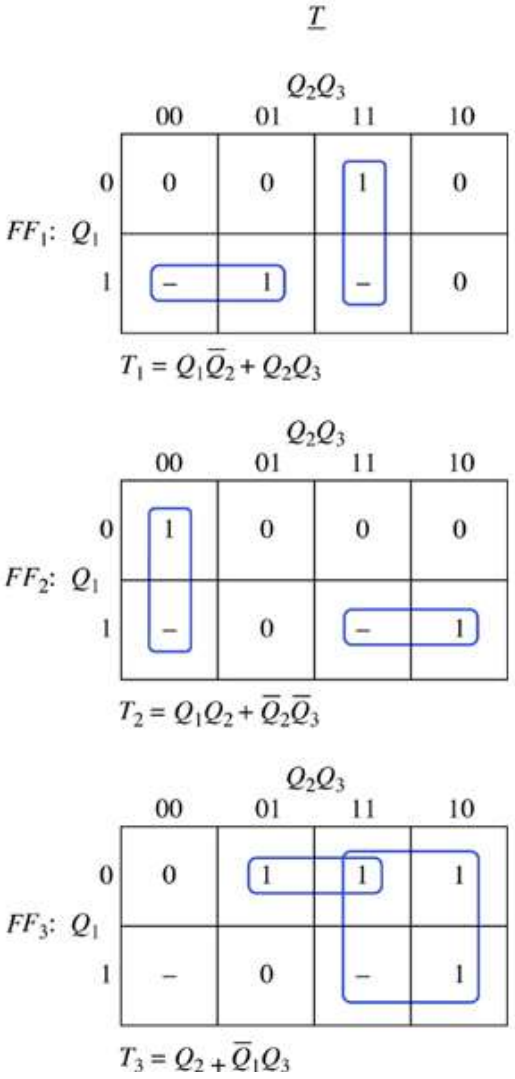
Determination of the minimal-sum expressions for a synchronous mod-6 counter using clocked *D* flip-flops.

Figure 6.43



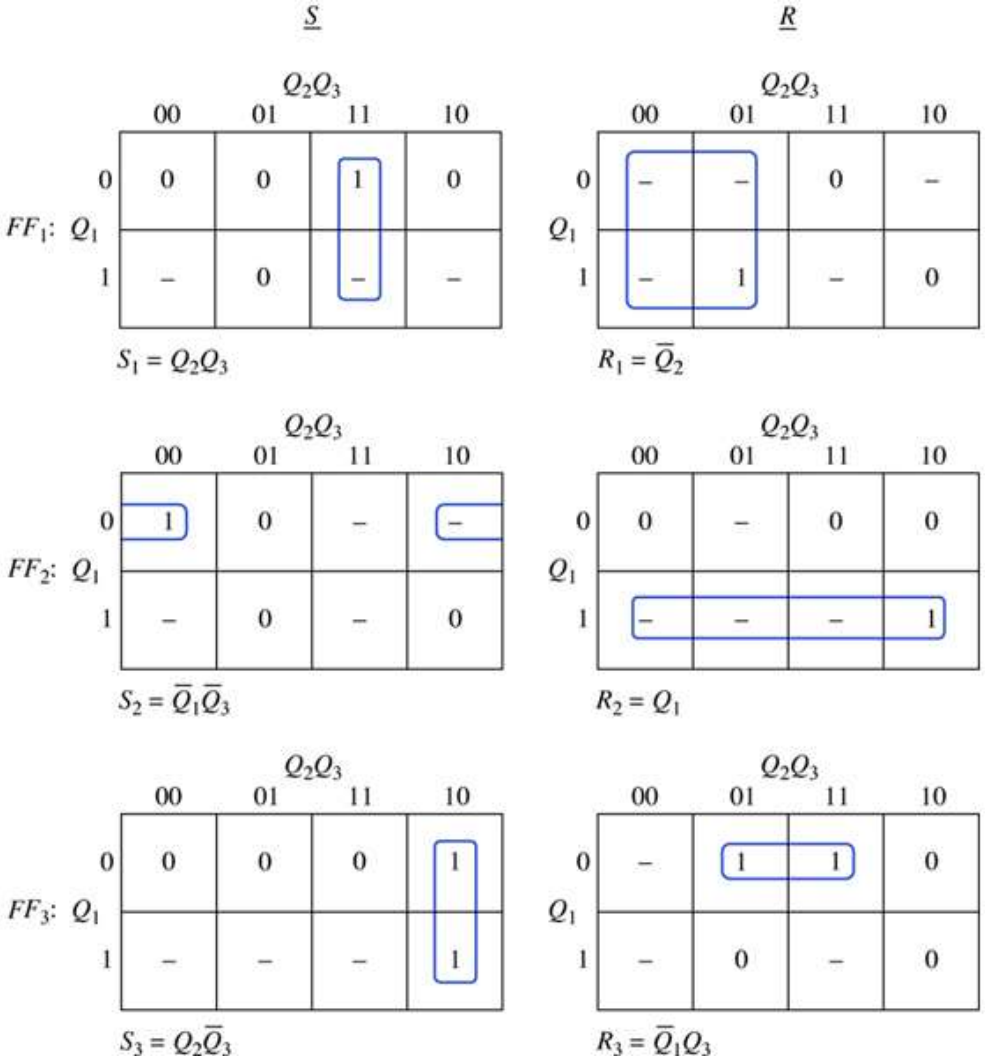
Determination of the minimal-sum expressions for a synchronous mod-6 counter using clocked *T* flip-flops.

Figure 6.44



Determination of the minimal-sum expressions for a synchronous mod-6 counter using clocked *SR* flip-flops.

Figure 6.45



Complete state diagram for the synchronous mod-6 counter of Fig. 6.42.

Figure 6.46