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FCSD – Foundations Of Computer System Design

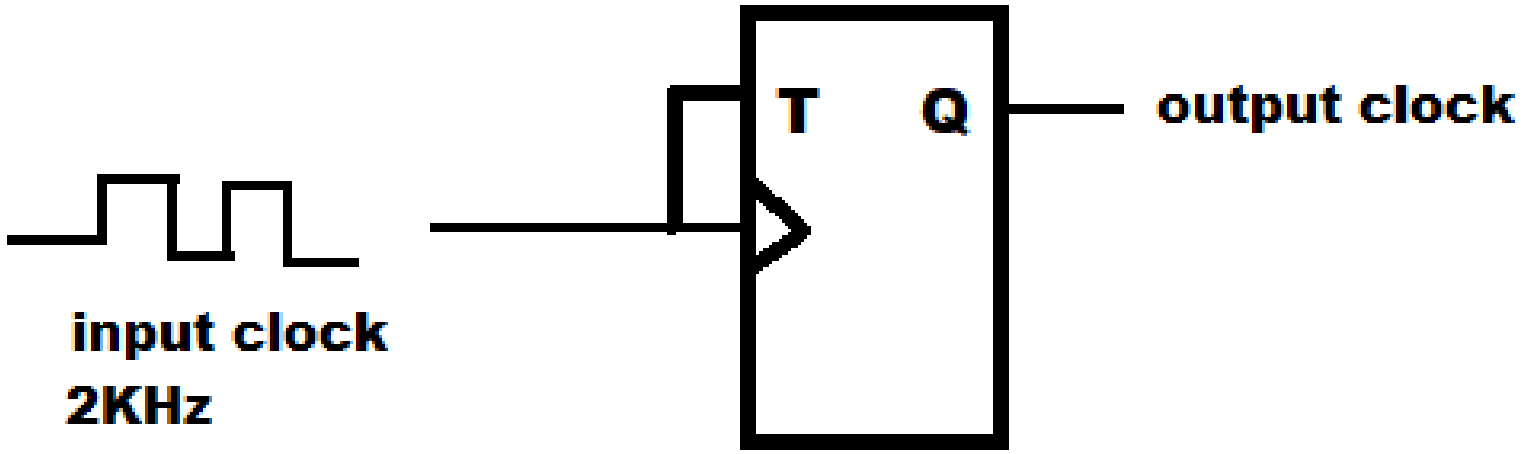
Unit 2 : Logic Design Using Sequential Circuits

Flip-Flops and Applications - The Basic Bistable Elements,
Latches, Timing Considerations, Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops), Edge Triggered Flip-Flops, Characteristic Equations, Registers - SISO, SIPO, PISO, PIPO and Universal Shift Register

Unit 2 : Applications of FlipFlops

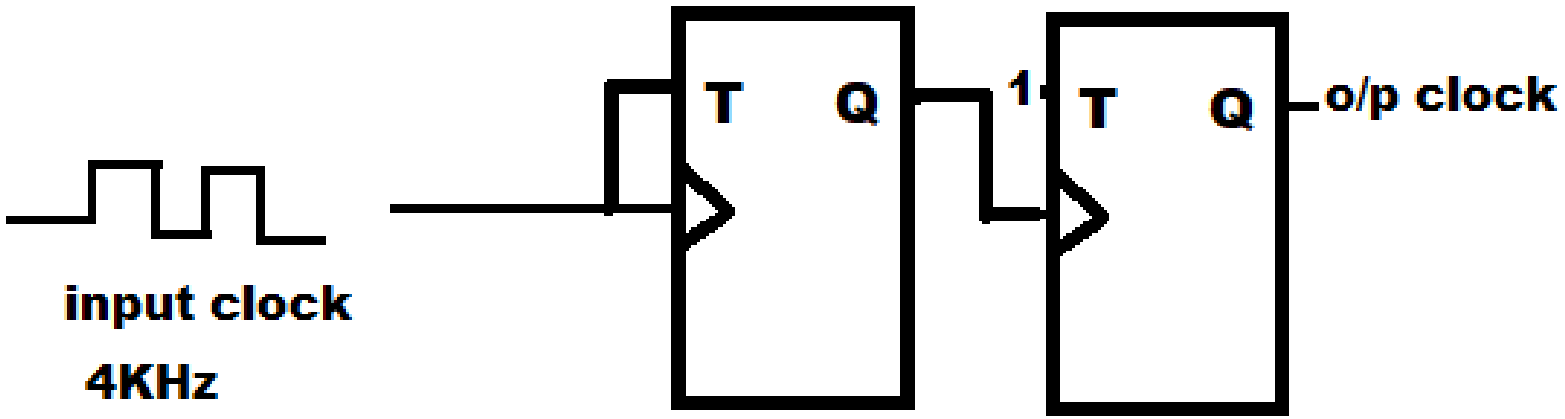
Applications of FlipFlops: Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers. Design of Synchronous Counters and Self-Correcting Counters

- CIE/SEE Quiz Question solutions
- Reference: Chapter 6 – Flip Flops and Simple Flip Flop Applications
  (Book:Donald D.Givone, "Digital Principles and Design",
  Tata McGraw-Hill, 2003 ISBN-13: 0-07- 252503-7)



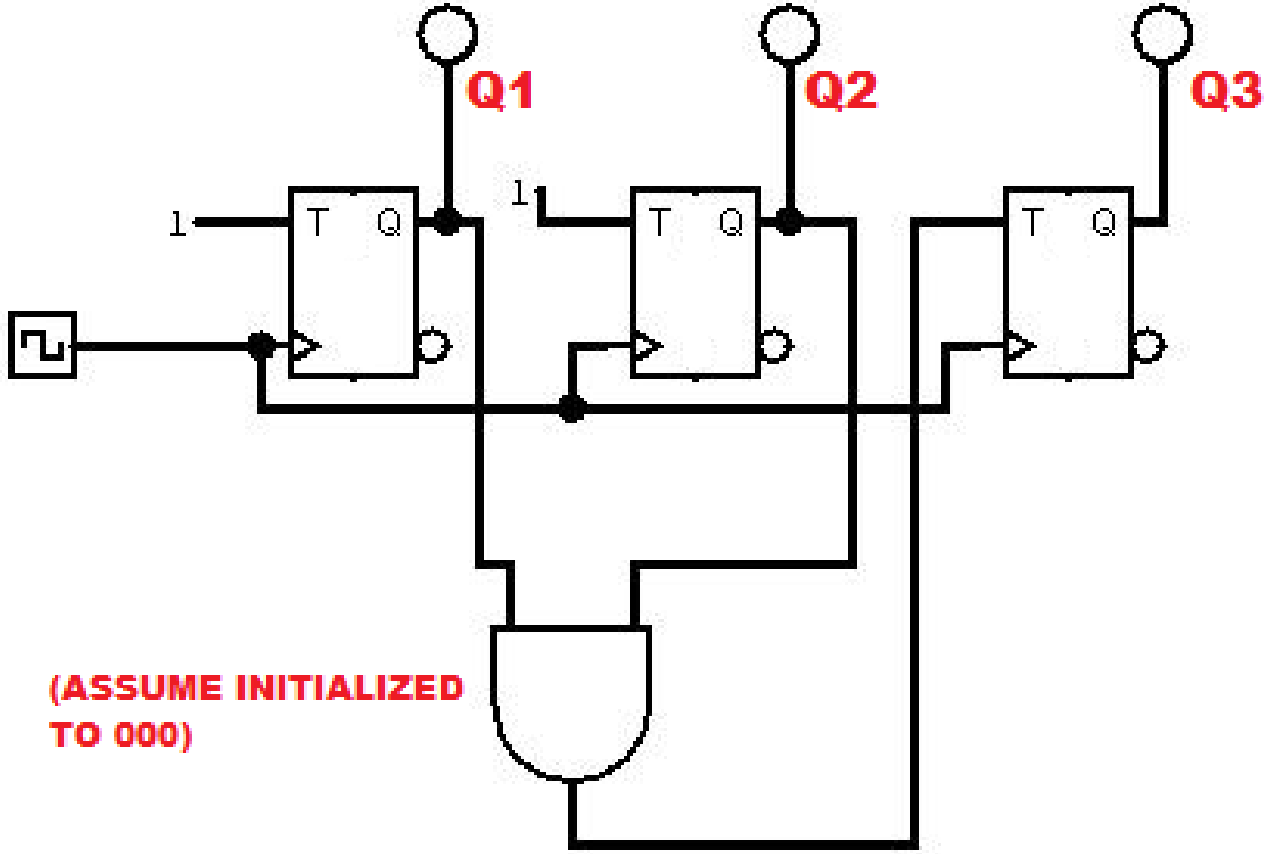
A. Output clock frequency – 2KHz
B. Output Clock frequency – 1KHz
C. Output Clock frequency – 4KHz
D. No change happens in the output

(ans – B)



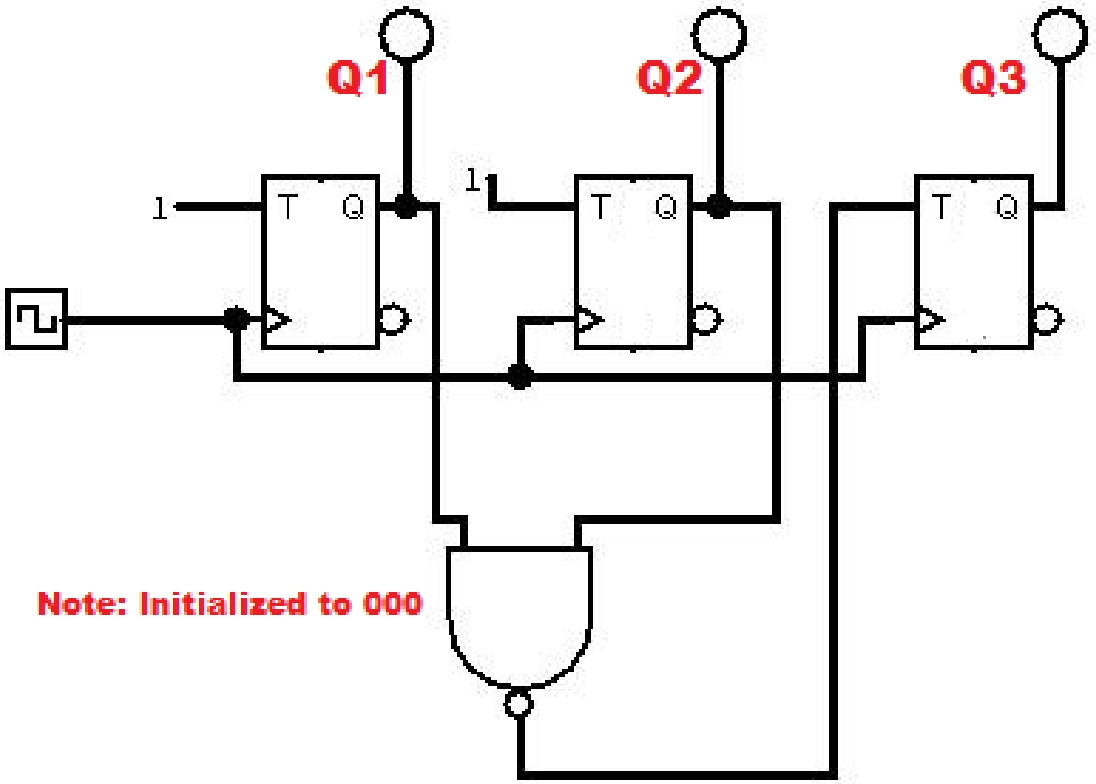
A. Output clock frequency – 1KHz
B. Output clock frequency – 2KHz
C. Output clock frequency – 4KHz
D. No change happens in the output

(ans – A)



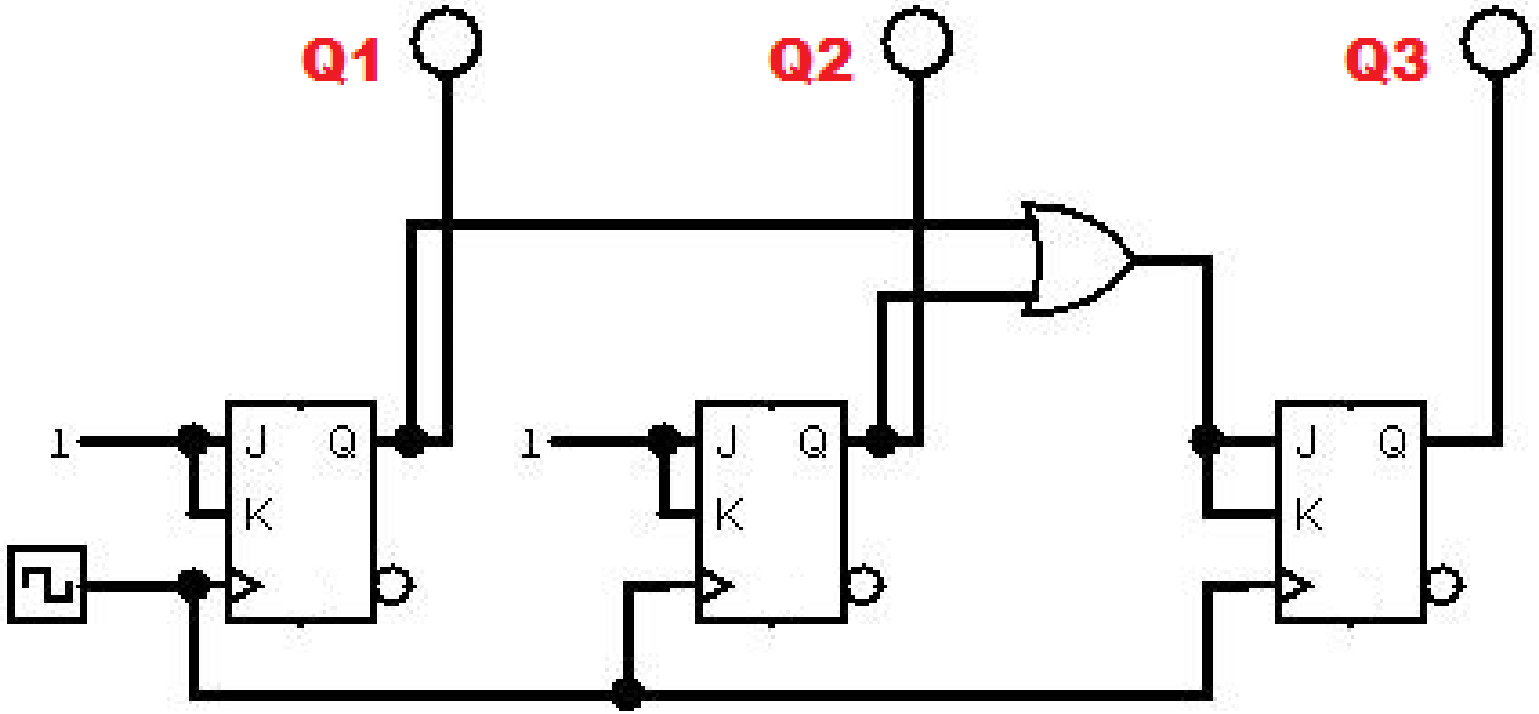
A. Valid Counting Sequence: 001,110,100,111
B. Valid Counting Sequence: 000,110,001,111
C. Valid Counting Sequence: 111,100,001,000
D. Valid Counting Sequence: 001,110,000,111

(ans – B)



A. Valid Counting Sequence: 001,110,100,111
B. Valid Counting Sequence: 001,110,100,111
C. Valid Counting Sequence: 000,001,111,110
D. Valid Counting Sequence: 000,111,001,110

(ANS – d)



A. Valid Counting Sequence: 000,111,110,001
B. Valid Counting Sequence: 000,111,001,110
C. Valid Counting Sequence: 000,110,001,111
D. Valid Counting Sequence: 000,001,110,111

(ANS – C)

Indicate the number of FlipFlops required to build Mod-8 Ring Counter

A. 4 T flip-flops
B. 8 T flip-flops
C. 4 D flip-flops
D. 8 D flip-flops

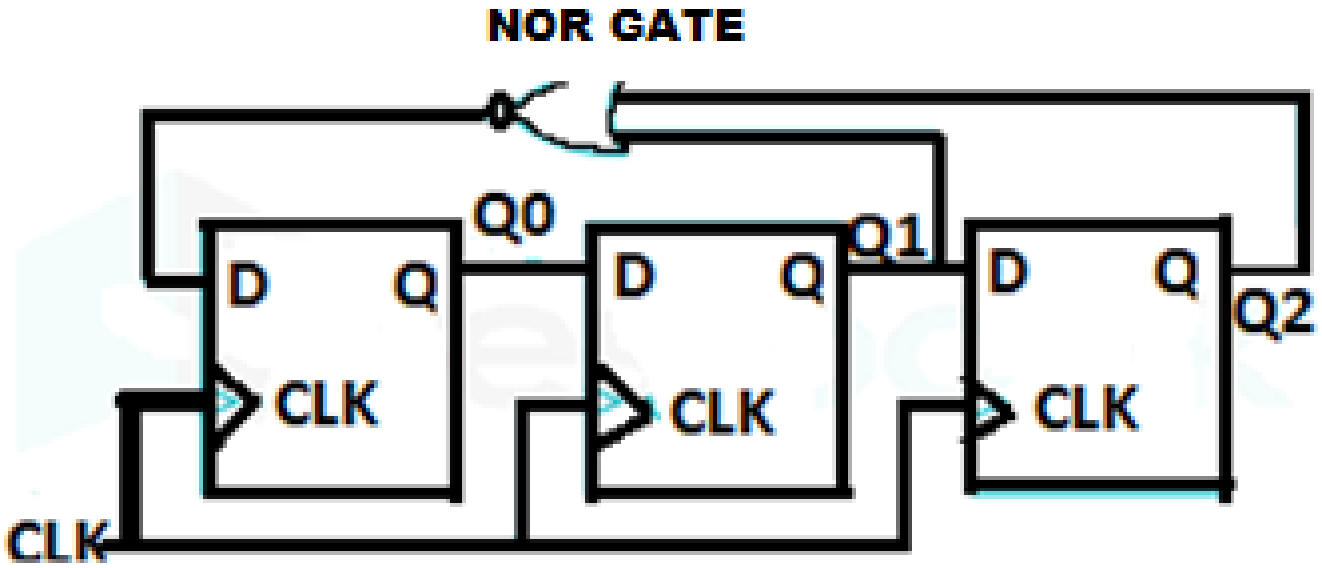
(ans – D)

Indicate the number of FlipFlops required to build Mod-8 Johnson Counter

A. 4 T flip-flops
B. 8 T flip-flops
C. 4 D flip-flops
D. 8 D flip-flops

(ans – C)

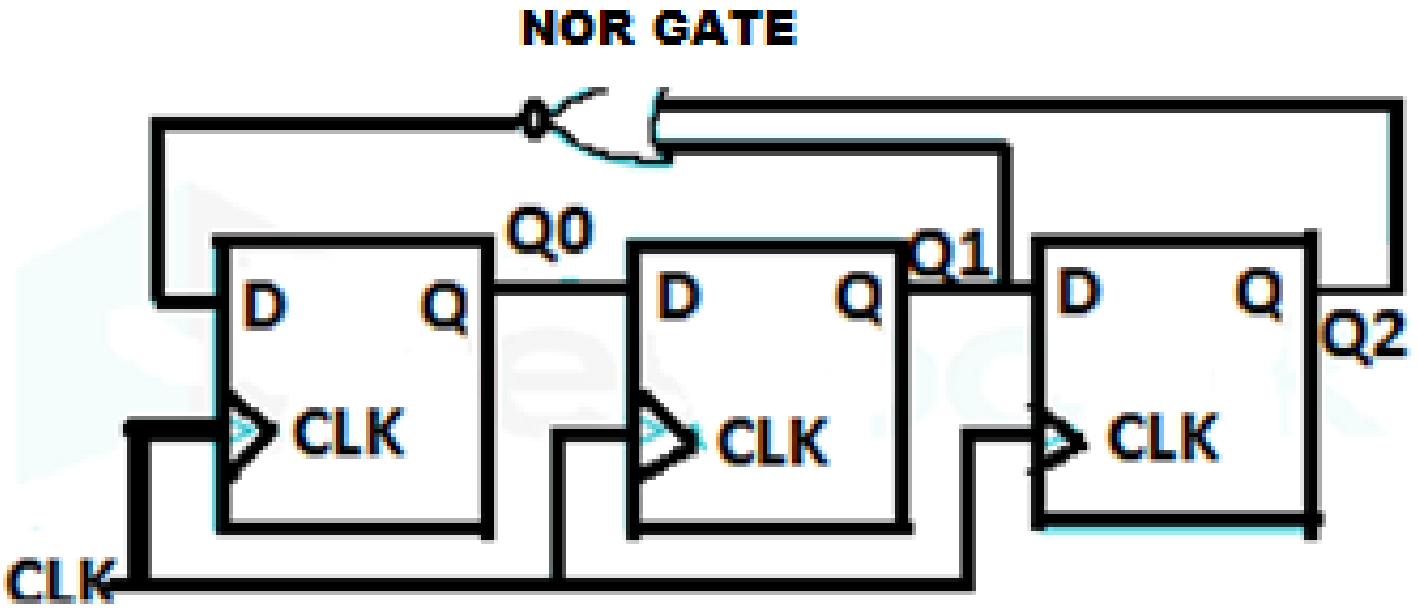
Give the Mod vaue of the following Counter



A. 6
B. 5
C. 4
D. 8

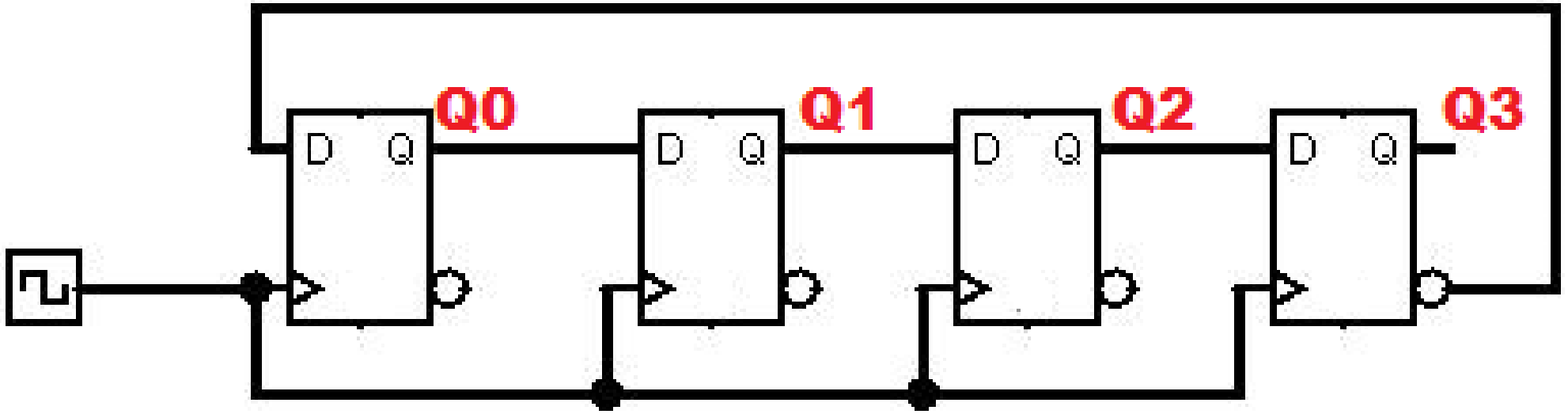
(ans – B)

Counting Sequence ?
(assume initialized to 000)



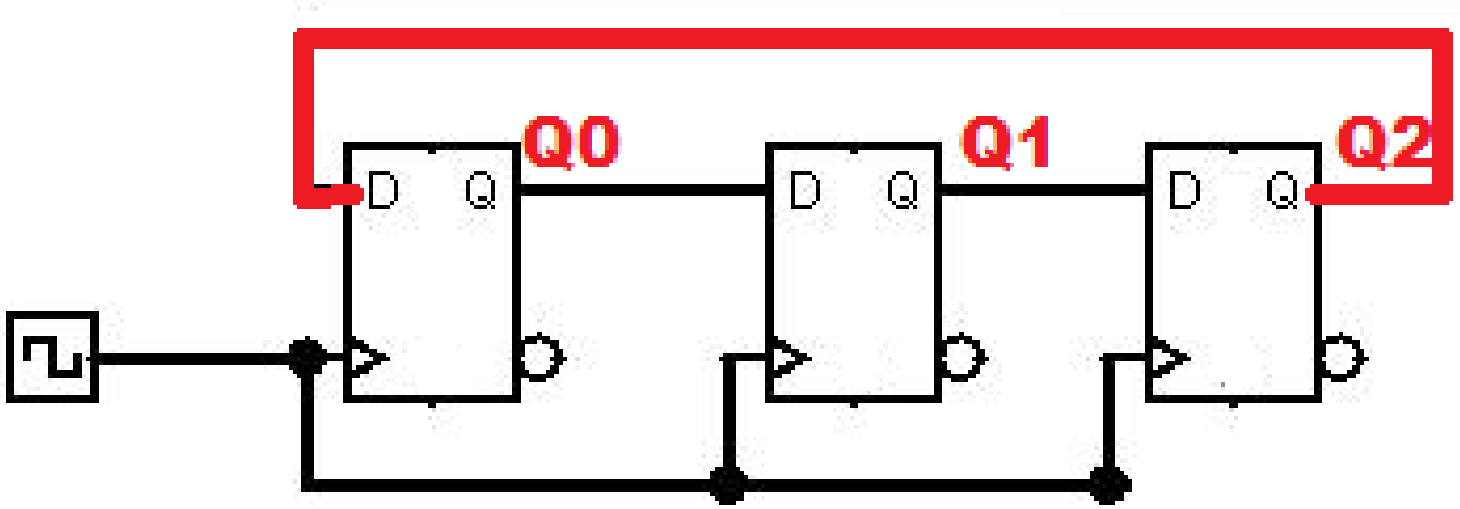
A. Valid Counting Sequence: 000,100,110,011,001
B. Valid Counting Sequence: 000,110,100,011,001
C. Valid Counting Sequence: 100,011,001,000
D. Valid Counting Sequence: 100,110,011,000

(ans – A)



A. MOD VALUE OF ABOVE COUNTER IS 4
B. MOD VALUE OF ABOVE COUNTER IS 2
C. MOD VALUE OF ABOVE COUNTER IS 8
D. MOD VALUE OF ABOVE COUNTER IS 2(POWER)4= 16

(ANS – C)



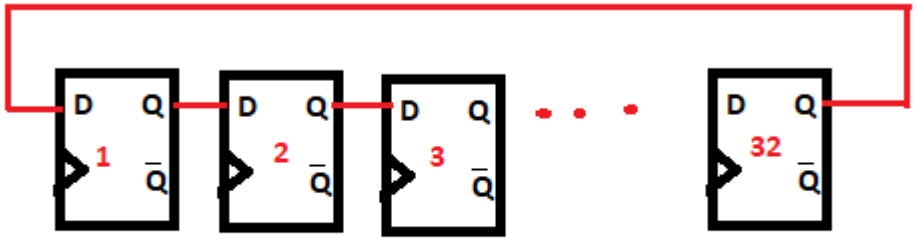
A. Ring Counter with Mod value 3, initial value=000
B. Twister Ring Counter with Mod Value = 2 x 3=6
C. Ring Counter with sequence:100,010,001 (if initial value is 100)
D. Jhonson counter with Mod 3, with initial value 001

(ANS – C)

Give one Advantage of Ring Counter. Design a Mod 32 Ring Counter Using D Flip-Flops. (Yr.2023)

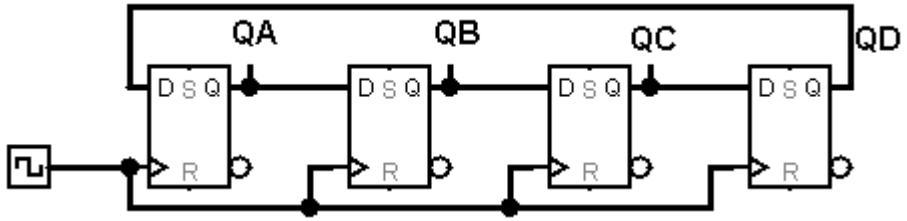
Ans: Does not require decoder circuit, because looking at 1 flipflop status, we get to know the state of the counter.

For Mod-32 We need 32 D FFs.

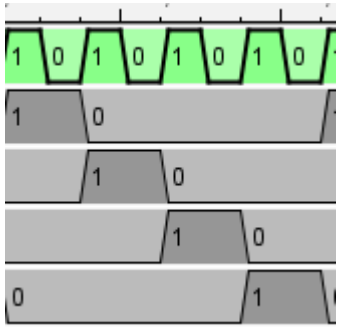


Basics Of Ring Counter....

A Ring Counter is circular shift register which is initialized so that only one of its flip flops is in the logic 1 state, while others are in 0 states. For each clock pulse, the 1 is shifted to its adjacent flip-flop. Because of this, Ring counter designed using N flip-flops has N states. (.Ex: Ring counter with 4 FFs, have 4 states, hence Mod-4 counter).



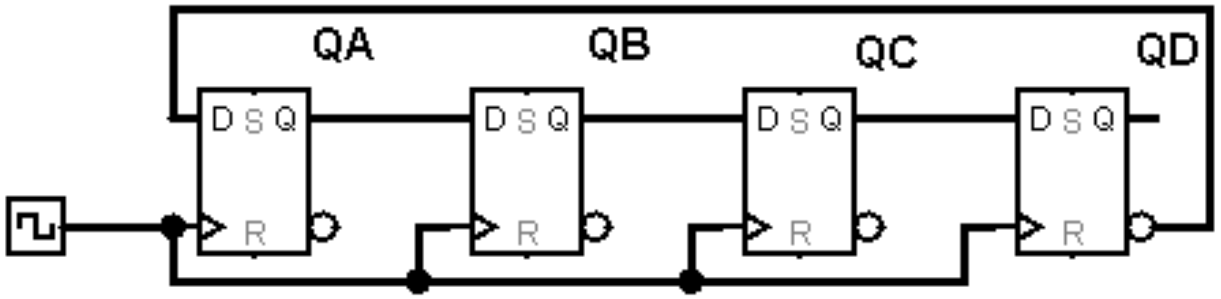
States	Q_A	Q_B	Q_C	Q_D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1



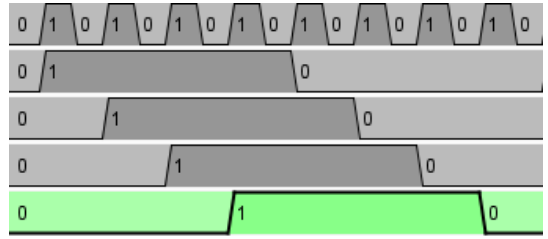
Advantage: Although the ring counter is not efficient in the number of FFs used, it provides a decoded output. That is, **to detect any particular state in the counting sequence, it is only necessary to interrogate the output of a single FF**. Ex: the 0001 state is readily detected by observing the output terminal Qd. Whenever logic 1 value appears at this terminal, the state of the counter is known to be 0001. Similarly, the determination of any other state only requires observing the output of a single FF.

Johnson Counter

Twisted Ring Counter / Johnson Counter
In this counter unlike Ring counter, compliment of the right most flip-flop *QD serves as input to the left most flip flop. Johnson counter, of N flip flops provide 2*N states, hence it is MOD-2N counter. Ex: with 4 FFs, it is MOD-8 counter (8 states) as shown in the figure. Assumed, counter starts with counting sequence QA-QB-QC-QD = 0000 state.

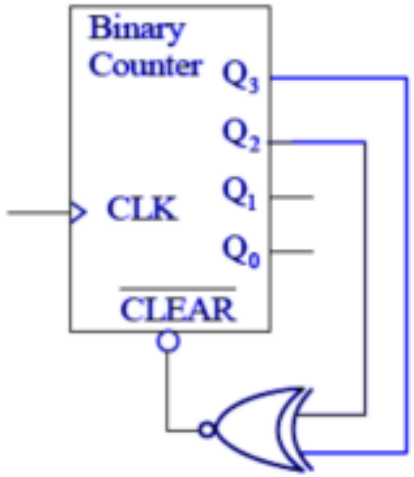


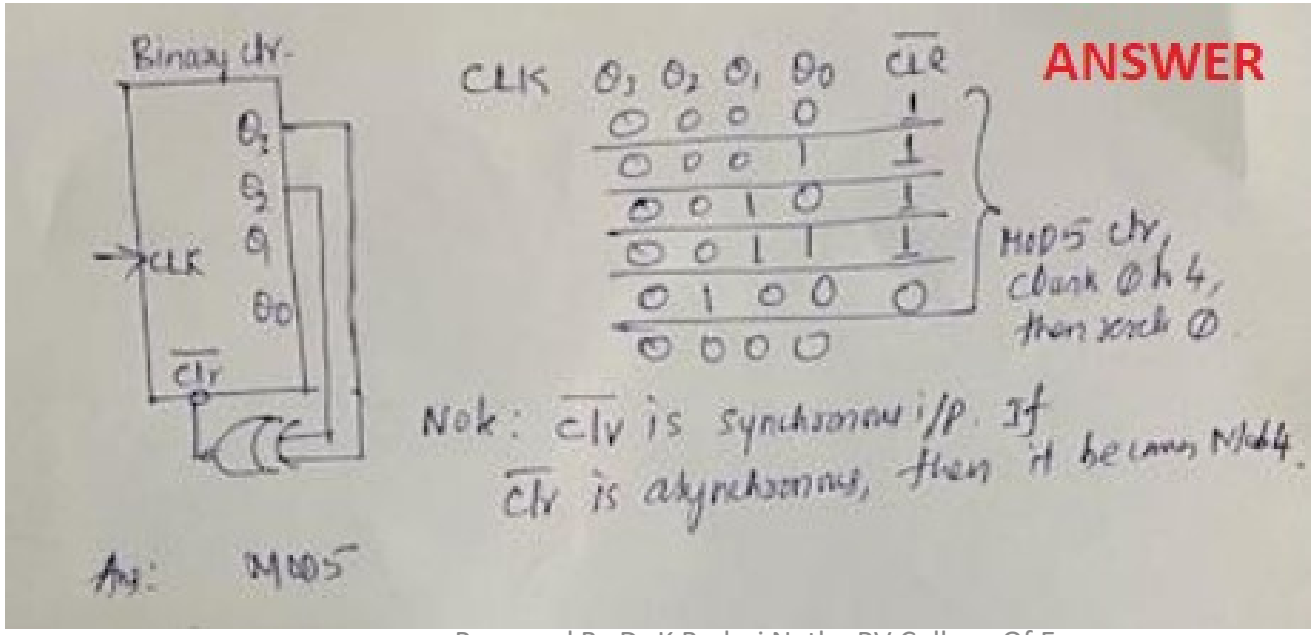
States	Q_A	Q_B	Q_C	Q_D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1



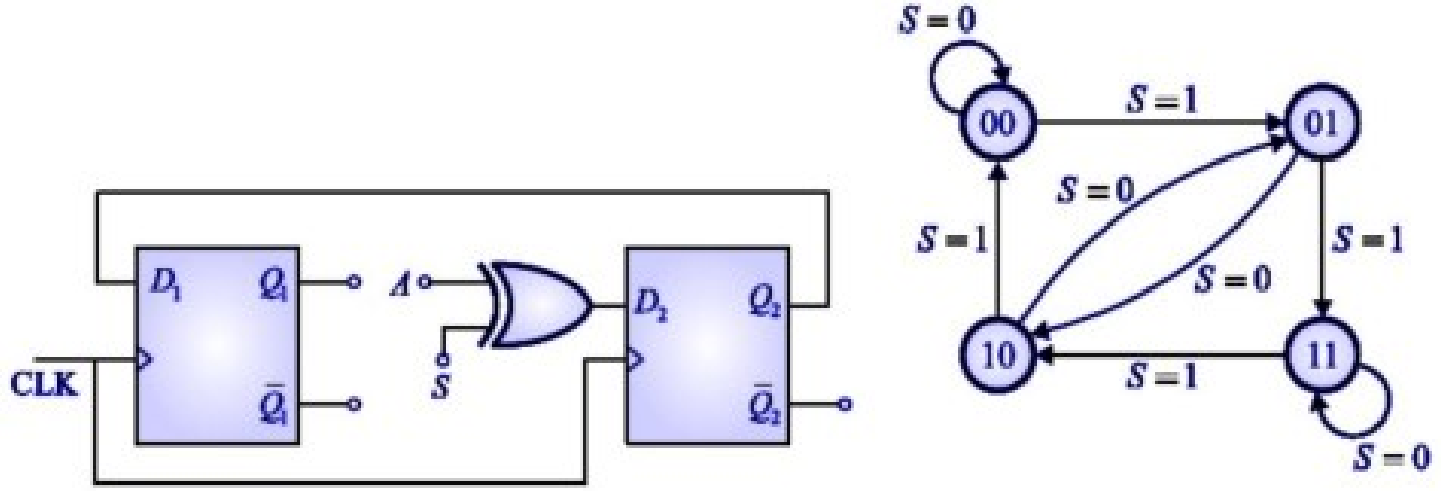
Advantage: Provides more number of states compare to ring counter and reduced decoding ckt. Unlike the ring counter, to detect any particular state in the counting sequence of a twisted-ring counter, it is necessary to incorporate some logic elements. From the table it can be noted that, only single 2 input AND gate is required to obtain a decoded output. Ex: State 1000 is decoded by :Qa,*Qb (as this combination Qa=1,Qb=0 is unique and this exists only for this state)

The figure shows a binary counter with synchronous clear input, Show what will the mod value of the counter.



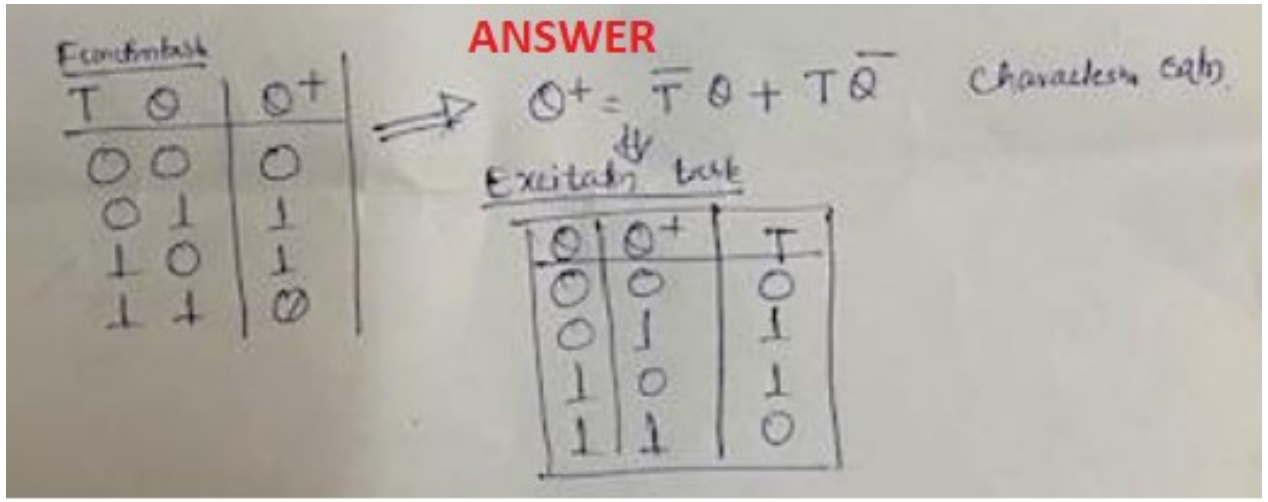


The digital logic shown in the figure, satisfies the given state diagram, when Q1 is connected to input A of the XOR gate. Suppose the XOR gate is replaced by an XNOR gate, connecting A to which option preserves the state diagram?



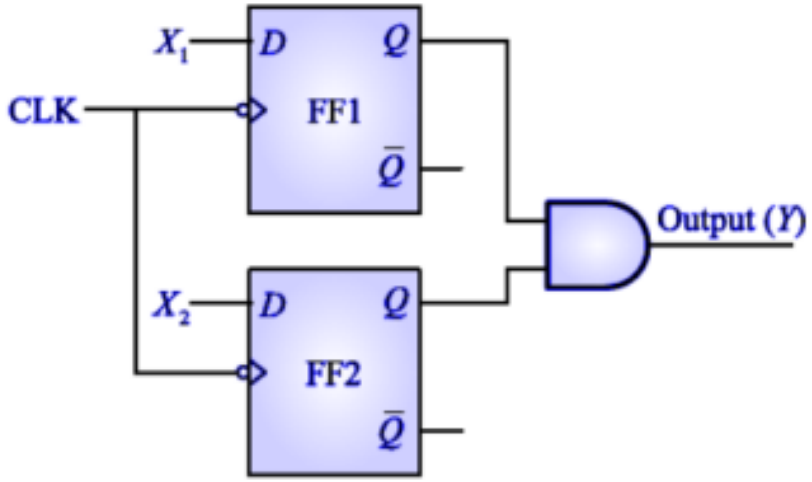
Input A should be connected to Q1’

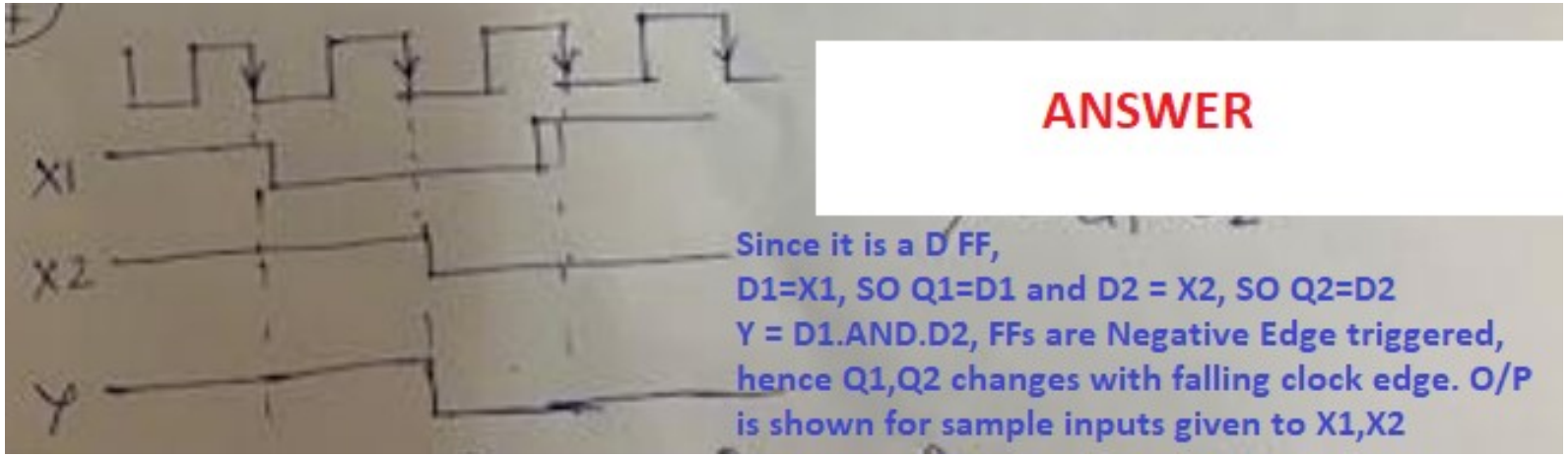
Derive the characteristic equation and Excitation table for a T flip flop
(refer page nos. 329 -331 Givone ref book, for all characteristic equation derivations

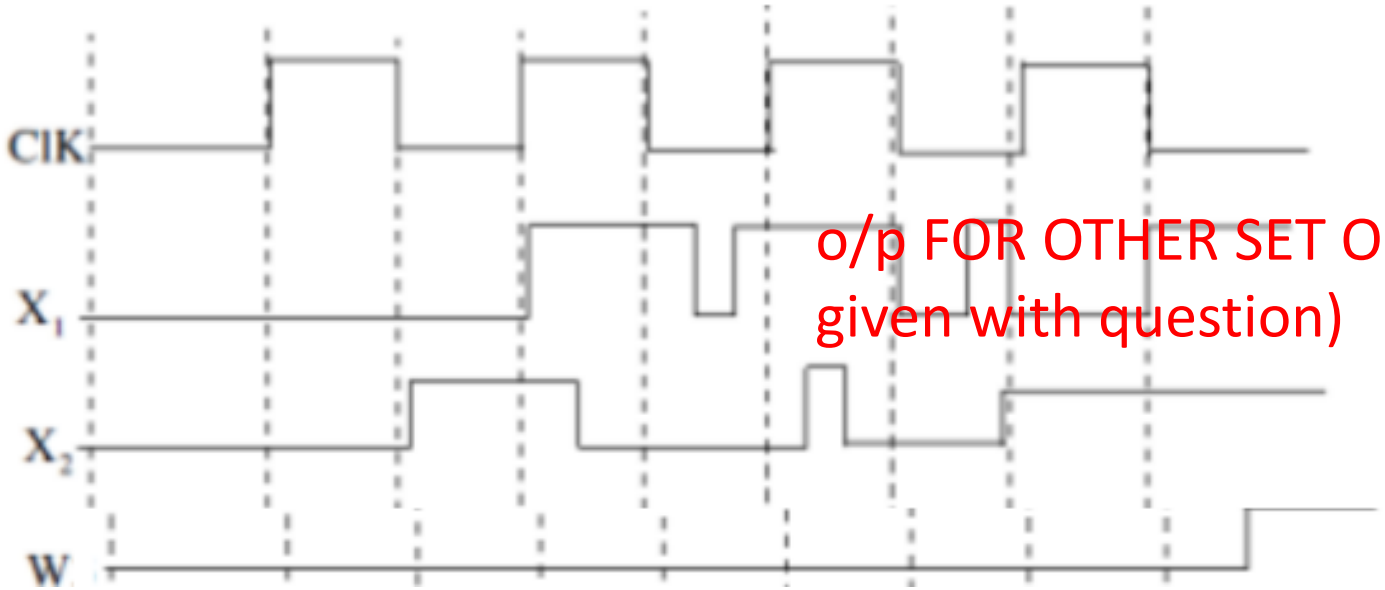


Note: Excitation Table for a Flip-Flop is also referred as Application Table

For the circuit shown, draw the wave form for output Y







o/p FOR OTHER SET OF DATA (some times waveforms may be given with question)

Design a mod 9 asynchronous counter using JK flipflops.

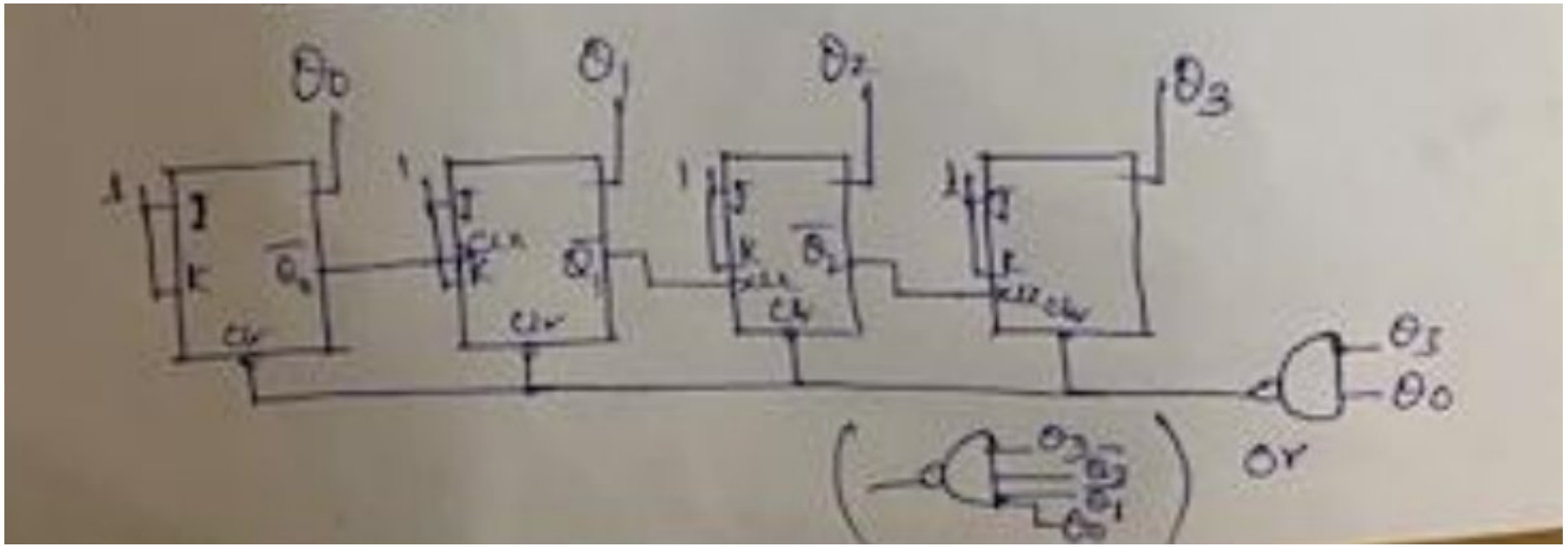
Since JK flip flop is given, convert to T ff, by making J=K=1

Mod -9 Asynchronous 4 ffs are required

Total states = 9 ; No. FFs Reqd = 4(with 3 - Max 8, with 4 Max 16 we get, so4) ; Total States: 9 (0000 to 1000)

	Q0	Q1	Q2	Q3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0

9	1	0	0	1

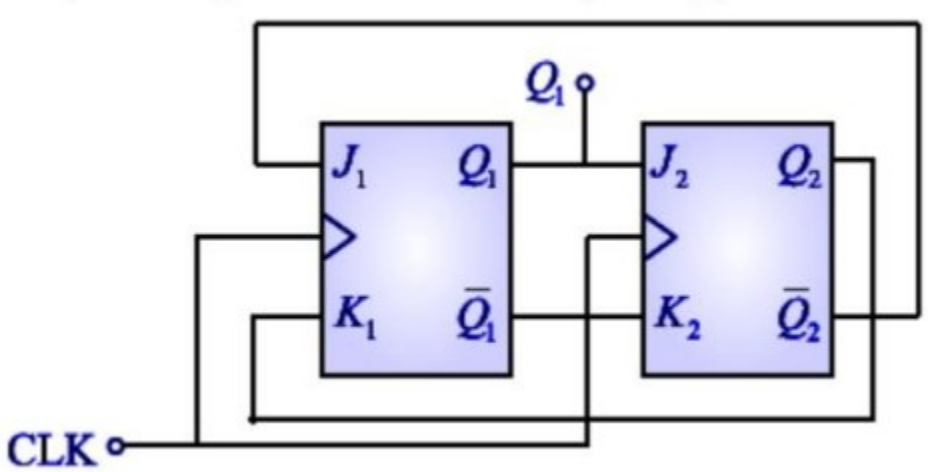


When counter completes 8 (1000), it would have finished 9 states(including 0000 state), and now when it reaches 9 (1001), it should clear the counter and start from 0000.

We should decode the value of 1001 using NAND gate, and apply the output to active low clear input. Since, *CLR is asynchronous input, it immediately resets the output and enter to state 0000. (for a very short time it will be in state 9, it is almost negligible compare the clock puluse width).

1 0 0 1 -> NAND GATE INPUTS -> Q0 AND Q3 (We can invert and use Q1 and Q2 also, if required, but in this case Q0=1 and Q3=1 is unique combination only for state 9, hence checking for Q0 and Q3 is enough).

The outputs of the two flip flops Q1, Q2 in the figure shown below are initialized to 0,0. Calculate the Sequence generated at Q1 upon the application of the clock signal is



We can solve these types of problems by the following method.

1. Identify the Flip Flop type, and use its characteristic equation to find its next state.

2. Write Present state of FF, I/Ps for each flip flop (excitation variables), Next State of FF. Calculate the next state of FF, by using Excitation variable values and characteristic equation.

3. Based on the initial values given in the question, take the values for present state (if not given take it 0). Find out the next state for first row, then that becomes the present state (second row). When all states complete stop the process (maximum number of states is based on number of flip flops, or when state repeats stop the process).

Solution for the given Question:

From the diagram, we can write FlipFlop inputs,

J1 = *Q2, K1 = Q2

J2 = Q1, K2 = *Q1

and using characteristic equations for JK flip-flop, next state can be written as

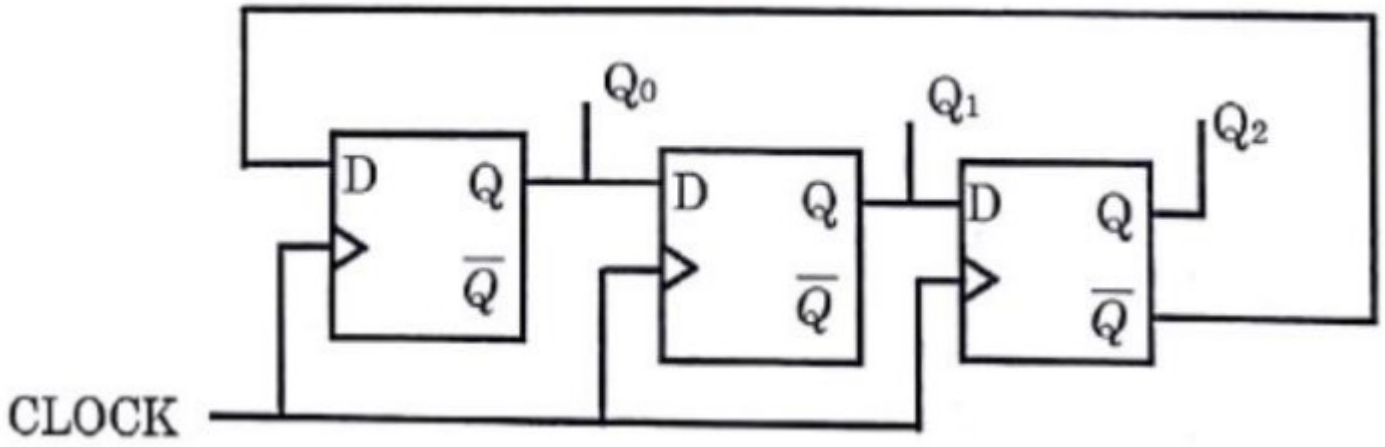
Q1+ = J1.*Q1 + *K1.Q1 ; Q2+ = J2.*Q2 + *K2.Q2

Now, we can prepare table to find out the different states of this circuit/counter

Present State		Excitation Variables				O/P		
Q1	Q2	J1(*Q2)	K1(Q2)	J2(Q1)	K2(*Q1)	Q1+	Q2+	
0	0	1	0	0	1	1	0	(initially Q1,Q2 are Zero, use equations to find out Q1+,Q2+ using J/K/Q)
1	0	1	0	1	0	1	1	(next state of first row, becomes pressent state for second row)
1	1	0	1	1	0	0	1	(next state of second row, becomes present state for 3rd row)
0	1	0	1	0	1	0	0	(stop here, as max 4 states for 2 flip flops, and now states repeat...)

So, output sequence appers at Q1 is -> 0 1 1 0 0 1 1 0... . (So total 4 different states, Mod 4 counter)

What is the value of the register formed from D flipflops using Q0, Q1 and Q2 as output after 14 cycles.



Since it is Johnson counter, let us assume initial value of Q0,Q1,Q2 is 000. Then for every 6 clocks (3*2 = 6 states), sequence repeats. Let us write the sequence.

1 clock – 100,
2 clock - 110
3 clock - 111
4 - 011
5 - 001
6 - 000

Now these will repeat (7 to 12), 100,110,111,011,001,000, again repeat 100 (13^{th} clock), 110 (after 14^{th} clock)