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Dr. M. S. Sheshgiri Campus, Belagavi

Department of Electronics and Communication Engineering

Sensior Design Project Report on

" Design and Analysis of a Low-Power 6T SRAM Cell "

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2025

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that project entitled **" Design and Analysis of a Low-Power 6T SRAM Cell "** is a bonafide work carried out by the student team of **" Sakshi More (02FE22BEC075) , Sejal Jadhav(02FE22BEC086), Sanket Kammar (02FE23BEC406), Aditya Donk(02FE23BEC409) "**. The project report has been approved as it satisfies the requirements with respect to the Sensior Design project work prescribed by the university curriculum for B.E. (VII Semester) in Department of Electronics and Communication Engineering of KLE Technological University Dr. M. S. Sheshgiri CET Belagavi campus for the academic year 2025-26.

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-The project team

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Abstract

The design and analysis of a low-power 6T SRAM cell are essential for modern VLSI systems that require high performance, minimal power consumption, and compact area utilization. This project focuses on comparing the performance of the 6T SRAM cell implemented in 45nm, 90nm, and 180nm CMOS technologies. Using Cadence Virtuoso, the SRAM cell is designed, simulated, and analyzed across these technology nodes to evaluate key parameters such as power consumption, delay, and area efficiency. The results show that technology scaling significantly influences device behavior — smaller nodes like 45nm provide faster operation and reduced dynamic power, while larger nodes like 180nm offer improved stability but consume more area and power. The comparative analysis emphasizes the trade-offs between speed, power efficiency, and area optimization in different process technologies, providing valuable insights for selecting the most suitable design for advanced VLSI applications.

1 Introduction

In modern VLSI design, Static Random Access Memory (SRAM) is one of the most critical components used for high-speed data storage in processors, cache memory, and embedded systems. The 6T SRAM cell, consisting of six transistors, is widely preferred due to its simple structure, fast access time, and low power operation. As technology scales down from 180nm to 90nm and 45nm, transistor dimensions shrink, leading to faster operation and lower dynamic power consumption. However, this scaling also introduces challenges such as leakage current, variability, and reduced stability. Therefore, an in-depth analysis of SRAM performance at different technology nodes is essential to achieve an optimal balance between speed, power efficiency, and area utilization. This project focuses on the design and comparative analysis of a low-power 6T SRAM cell across these three technology nodes using Cadence Virtuoso to understand the impact of scaling on overall performance and design efficiency.

2 Objectives:

- To design a 6T SRAM cell with optimized transistor sizing for minimum power consumption.
- To analyze the performance parameters such as power, delay, and static noise margin (SNM).
- To compare the 6T SRAM cell performance across different technology nodes (180 nm, 90 nm, and 45 nm).
- To implement and simulate the SRAM cell using industry-standard EDA tools (e.g., Cadence Virtuoso).
- To evaluate the trade-offs between speed, stability, and power efficiency.
- To verify the design through LVS, DRC, and post-layout simulations ensuring accuracy and manufacturability.
- To develop a low-power and high-performance memory design suitable for modern VLSI systems.

3 Literature Survey

3.1 Design, modeling and comparative analysis of SRAM performance and functionality under the Subthreshold regime for various technologies

Many researchers have focused on improving the 6T SRAM cell design for low power and high-speed applications. Studies show that scaling from 180 nm to 45 nm technology reduces delay and power consumption but increases leakage. Vasudeva Reddy et al. analyzed SRAM performance under subthreshold operation, emphasizing power–stability trade-offs. Modified architectures like Schmitt-trigger and FinFET-based SRAMs further enhance stability and energy efficiency. Overall, technology scaling and optimized transistor sizing are key to achieving reliable and efficient SRAM designs for modern VLSI systems.

3.2 Design and optimization of 6T SRAM cell at different technology nodes using CMOS for Low power and high-speed neural network computation

Recent studies have focused on designing and optimizing 6T SRAM cells across different technology nodes to achieve low power, high speed, and improved stability. Researchers like Swatantra Kumar and Vasudeva Reddy analyzed 6T SRAM performance at 180 nm, 90 nm, 45 nm, and 22 nm using Cadence tools, showing that delay and power decrease as technology scales down. However, challenges such as leakage current and reduced noise margin increase at smaller nodes. Various designs, including FinFET and Schmitt-trigger-based SRAMs, have been proposed to enhance energy efficiency and stability. Overall, scaling and transistor optimization remain key to reliable and efficient SRAM operation in modern VLSI applications.

3.3 Design and Performance Analysis of 6T SRAM cell on 90nm technology

Researchers have extensively analyzed 6T SRAM cell designs to improve speed, stability, and power efficiency at different technology nodes. Studies by Mehak Zargar et al. and Swatantra Kumar et al. show that scaling from 180 nm to 22 nm significantly reduces delay and power consumption but increases leakage and variability. Various techniques like FinFET, MTCMOS, and low-leakage design approaches have been proposed to enhance stability and minimize power loss. Vasudeva Reddy et al. further emphasized transistor sizing and SNM optimization for better performance. Overall, technology scaling and design optimization play a vital role in developing efficient low-power SRAMs for modern VLSI systems.

3.4 Performance Analysis of Low Power 6T SRAM Cell in 180nm and 90nm

Researchers have extensively studied 6T SRAM cells to achieve low power and high-speed performance across various CMOS technologies. C. Ashok Kumar et al. analyzed 6T SRAM using 180 nm and 90 nm nodes, showing that as technology scales down, power consumption and delay reduce while speed improves. The study also highlights the importance of transistor sizing and layout optimization for stable read/write operations. Other researchers have proposed advanced low-power techniques like power gating and multi-threshold transistors to minimize

leakage. Overall, technology scaling enhances SRAM efficiency but introduces challenges like reduced stability and higher leakage currents.

3.5 Design and Performance Analysis of 6T SRAM Cell on Different CMOS Technologies

The reviewed literature on 6T SRAM cell design across different CMOS technologies highlights its importance in modern VLSI systems due to its high speed, low power consumption, and stability. Several studies, such as Seevinck et al. (1987) and Grossar et al. (2006), analyzed static noise margin, read stability, and write ability for nanoscale SRAMs. Later works by Steegen (2005) and Kumar et al. (2016) emphasized scaling benefits, showing reduced power dissipation with smaller feature sizes. Comparative analyses of multi-transistor SRAM structures (6T–10T) demonstrated trade-offs in area, delay, and leakage performance. Overall, the transition from 90 nm to 50 nm technologies enhances speed and energy efficiency, making 6T SRAMs optimal for high-performance, low-power applications.

4 Project Planning:

4.1 Gantt Chart:

This Gantt chart represents the project timeline for designing and analyzing a 6T SRAM cell. The Literature Survey begins in Week 2 of August and continues through Week 4, followed by defining the Problem and Need Statement during Weeks 2–3. The Schematic Design starts in early September and runs through Week 3, after which Simulation and Analysis are conducted in Week 3. The Layout Design phase spans from late September to early October, followed by DRC, LVS, and P-EX checks during Weeks 1–3 of October. Finally, Final Documentation takes place from late October to early November, marking the completion of the project workflow.

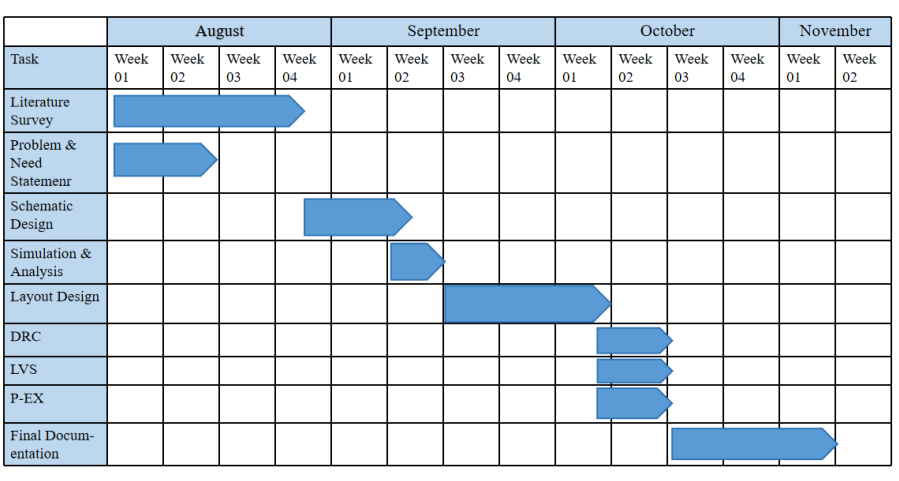

Figure 1: Gantt Chart

4.2 Work Breakdown Structure:

This Work Breakdown Structure (WBS) illustrates the systematic workflow for the project "Design and Analysis of a Low-Power 6T SRAM Cell." It is divided into six major phases — Project Initiation, Planning and Analysis, Design, Implementation, Testing Optimization, and Documentation Presentation. The project begins with defining the problem, objectives, and software scope through a literature survey. Then, tools and requirements are analyzed, and a Gantt chart is prepared for scheduling. The Design phase focuses on schematic creation, simulation setup, and optimization. In the Implementation phase, EDA tools are configured, and the layout design and LVS/DRC verification are performed. The Testing Optimization phase ensures functional accuracy, performance efficiency, and parasitic extraction. Finally, the Documentation Presentation phase involves preparing reports, presentations, and final reviews to complete the project.

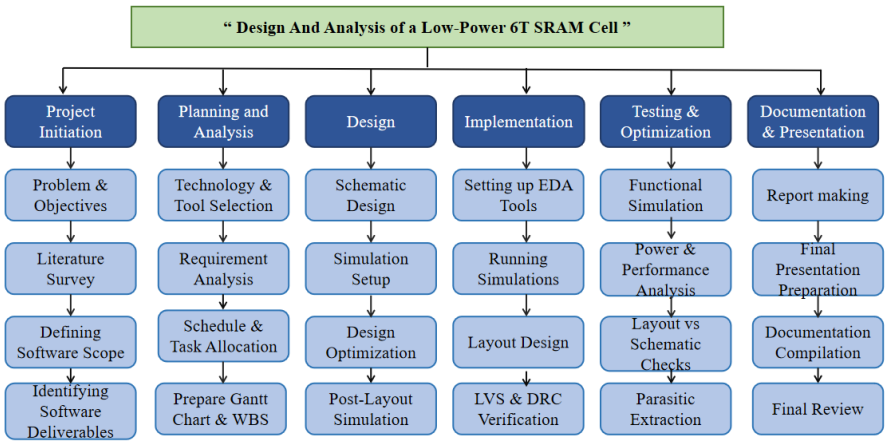

Figure 2: Work Breakdown Structure

4.3 Block Diagram:

This block diagram outlines the step-by-step process of designing and analyzing a 6T SRAM cell across different CMOS technologies. The process starts with Technology Selection, where 45 nm, 90 nm, and 180 nm nodes are chosen to compare performance variations. In Schematic Design, the SRAM circuit is modeled using these technologies to study transistor behavior. During Simulation, parameters like read/write delay, power dissipation, and stability are analyzed for each node. The Layout Designing stage converts the schematic into its physical layout for fabrication. Testing Verification (using DRC and LVS) ensures that the layout follows design rules and matches the schematic. Finally, in Result Analysis, the performance results show that as technology scales down from 180 nm to 45 nm, speed improves and power consumption decreases, demonstrating the benefits of advanced CMOS scaling.

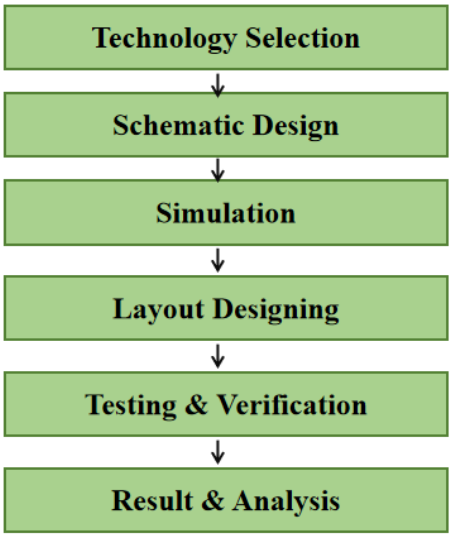

Figure 3: Block Diagram

4.4 Circuit Diagram:

The 6T SRAM cell consists of six MOS transistors. Four transistors (M1–M4) form two cross-coupled inverters that store one bit of data, while two access transistors (M5 and M6) connect the cell to the bit lines (BL and BL) during read and write operations. The word line (WL) controls the access transistors, enabling or isolating the cell. This configuration ensures stable data storage as long as the supply voltage (VDD) is maintained.

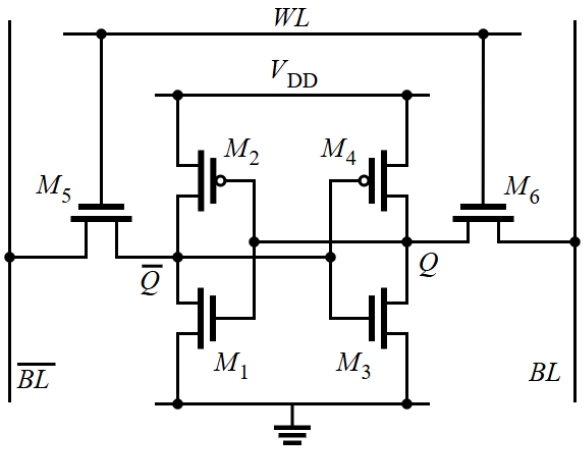

Figure 4: Circuit Diagram

5 Methodology:

5.1 Selection of Technology Nodes:

- The 6T SRAM cell is designed and analyzed using 180 nm, 90 nm, and 45 nm CMOS technologies to study the impact of technology scaling on performance parameters like area, power, and delay.

5.2 Schematic Design:

- A standard 6T SRAM cell is constructed using two cross-coupled inverters and two access transistors. The schematic is implemented in Cadence Virtuoso using respective BSIM/PDK models for each technology node.

5.3 Transistor Sizing and Simulation Setup:

- Proper transistor sizing ratios (pull-up, pull-down, and access transistors) are chosen for stable read/write operations. The design is simulated using Spectre Simulator to measure read/write delay, static and dynamic power.

5.4 Layout Design and Verification:

- The layout of the 6T cell is created for each technology node and verified through DRC and LVS checks. Parasitic extraction (PEX) is performed to include real physical effects in post-layout simulations.

5.5 Performance Evaluation:

- The extracted layouts are simulated to evaluate area utilization, power dissipation, and propagation delay. The results for all three technology nodes (180 nm, 90 nm, 45 nm) are compared to analyze improvements due to scaling.

5.6 Result Analysis:

- The comparison highlights that as the technology node decreases, cell area and power consumption reduce, and speed improves, validating that technology scaling enhances performance but introduces leakage challenges.

6 Application:

6.1 Memory-Based Applications:

6.1.1 Cache Memory

6T SRAM cells are widely used in cache memories of microprocessors and microcontrollers due to their high speed and low access time. They provide faster data retrieval compared to DRAM, making them ideal for L1 and L2 caches.

6.1.2 Embedded Memory

The designed low-power SRAM cell can be integrated into embedded systems and System-on-Chip (SoC) architectures to store frequently accessed data efficiently with minimal energy consumption.

6.2 Low-Power Device Applications:

6.2.1 Portable and IoT Devices

Low-power 6T SRAM cells are suitable for portable electronics, IoT devices, and wearable systems, where battery life and energy efficiency are critical design parameters.

6.2.2 Mobile and Consumer Electronics

The optimized SRAM design can be used in smartphones, tablets, and digital cameras for fast buffering and temporary data storage with minimal leakage current.

6.3 Computational Applications:

6.3.1 Artificial Intelligence and Machine Learning

In AI and ML accelerators, SRAM serves as the on-chip memory for storing weights and activation data, offering faster access speeds for real-time inference operations.

6.3.2 DSP and GPU Architectures

6T SRAM is employed in Digital Signal Processors (DSPs) and Graphic Processing Units (GPUs) to handle large volumes of data for parallel computations efficiently.

6.4 VLSI and Advanced Computing Systems:

6.4.1 Low-Power VLSI Circuits

The proposed SRAM design can be integrated into low-power VLSI systems for applications requiring reduced energy per operation, such as biomedical or aerospace electronics.

6.4.2 High-Speed Computing Platforms

Due to its fast access time, the 6T SRAM is suitable for high-speed computing and communication systems, improving the overall processing efficiency.

7 Results:

The 6T SRAM cell was successfully designed and simulated using 180 nm, 90 nm, and 45 nm CMOS technologies. The results show that as the technology node scales down, cell area and power consumption decrease, while speed and performance improve. The read and write delays are significantly lower at 45 nm compared to 90 nm and 180 nm. However, leakage current and noise margin issues increase with scaling. Overall, the 45 nm SRAM cell demonstrates the best trade-off between power efficiency, stability, and speed, making it suitable for modern low-power VLSI applications.

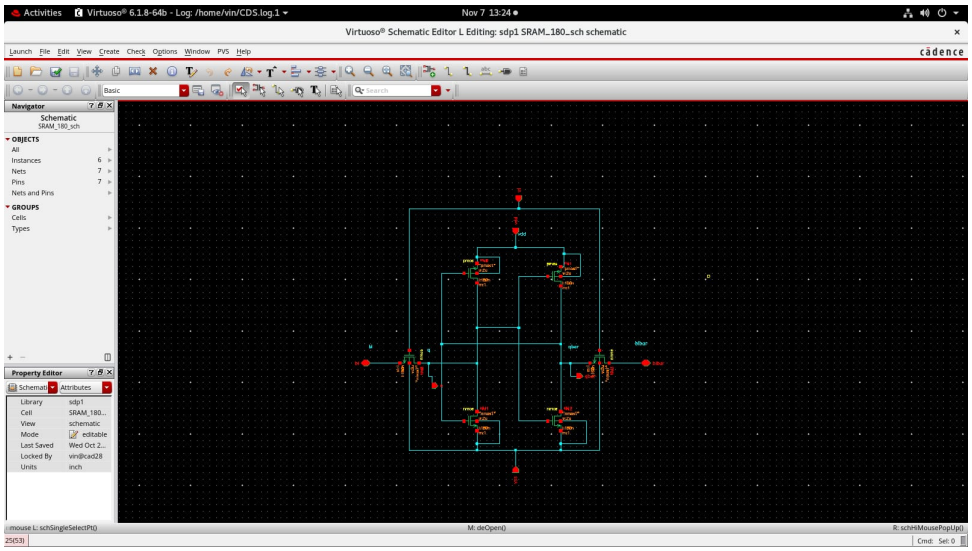

Figure 5: Schematic of 6T SRAM using 180nm technology

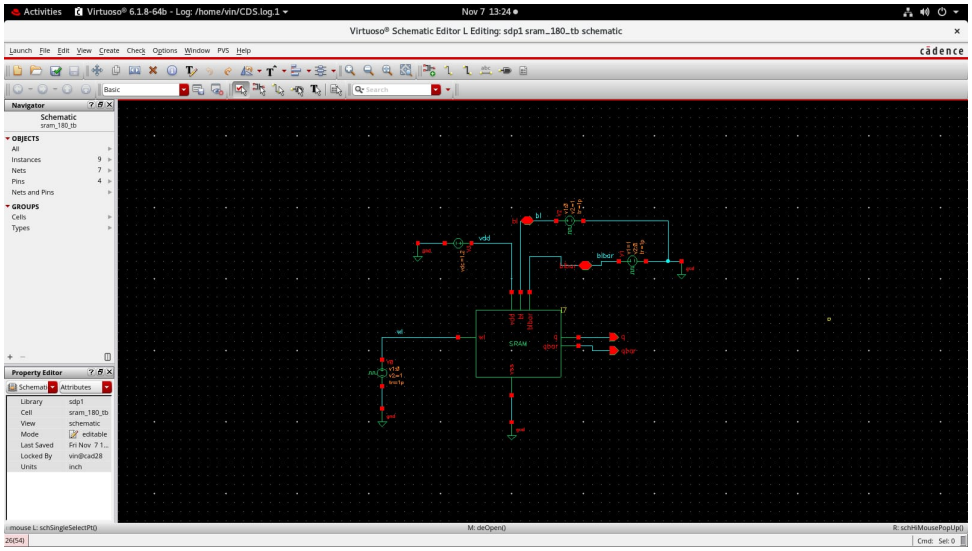

Figure 6: Test Bench of 6T SRAM bitcell using 180nm

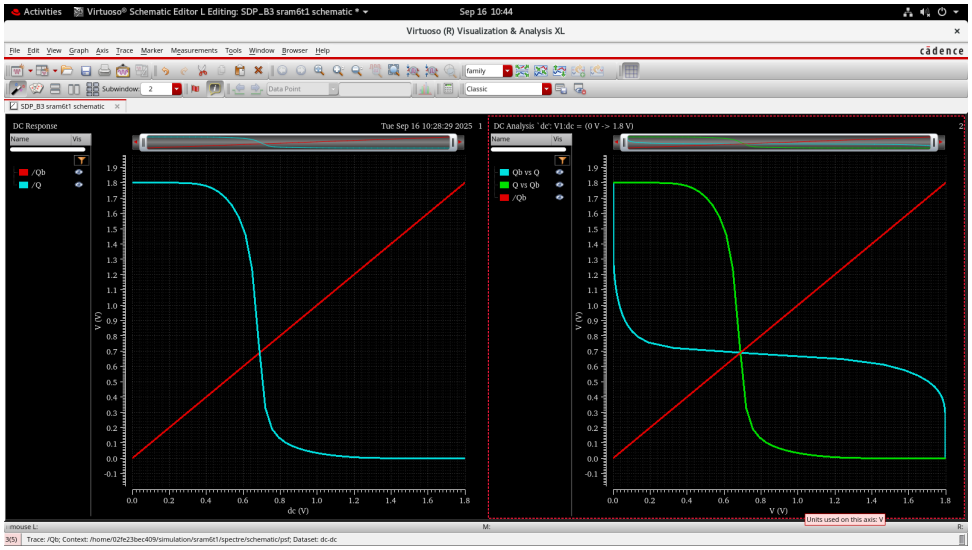

Figure 7: DC analysis(Butterworth wave) of 6T SRAM bitcell using 180nm

Figure 8: Transient analysis of 6T SRAM bitcell using 180nm

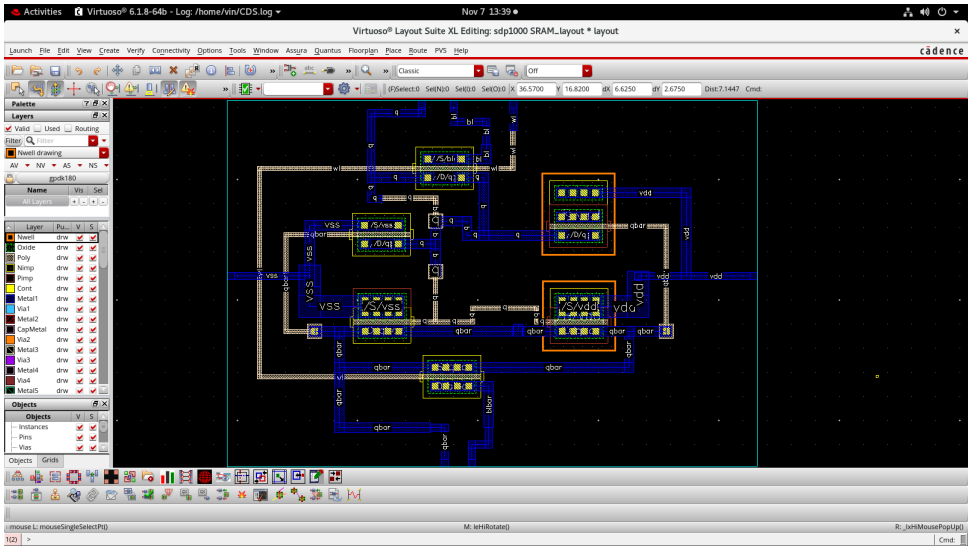

Figure 9: Layout of 6T SRAM bitcell using 180nm

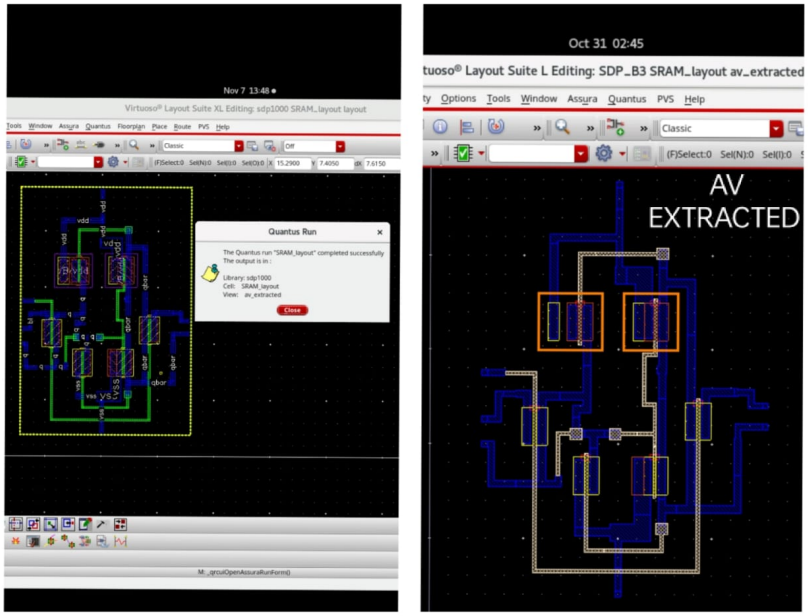

Figure 10: AV Extracted view of 6T SRAM bitcell using 180nm

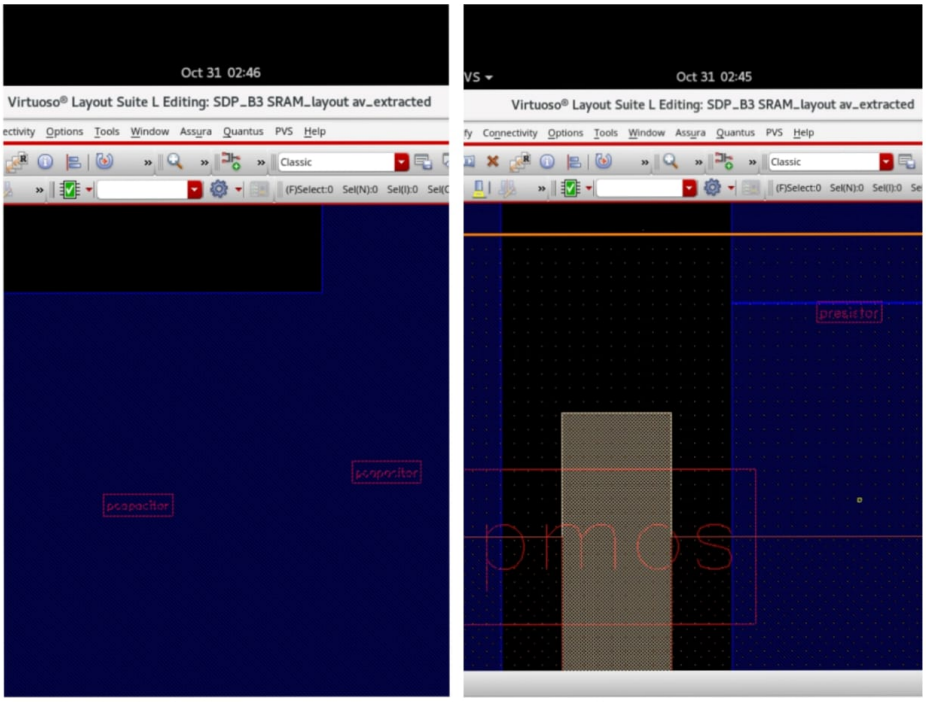

Figure 11: Parasitic resitors and capacitors of 6T SRAM bitcell using 180nm

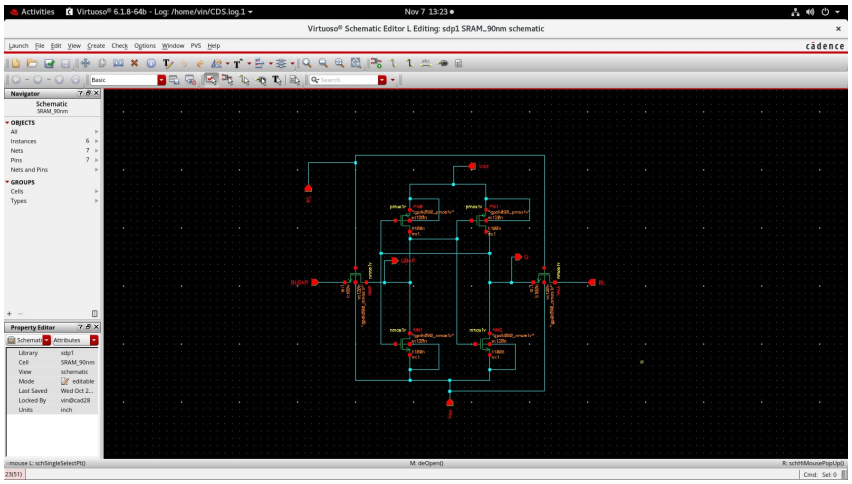

Figure 12: Schematic of 6T SRAM using 90nm technology

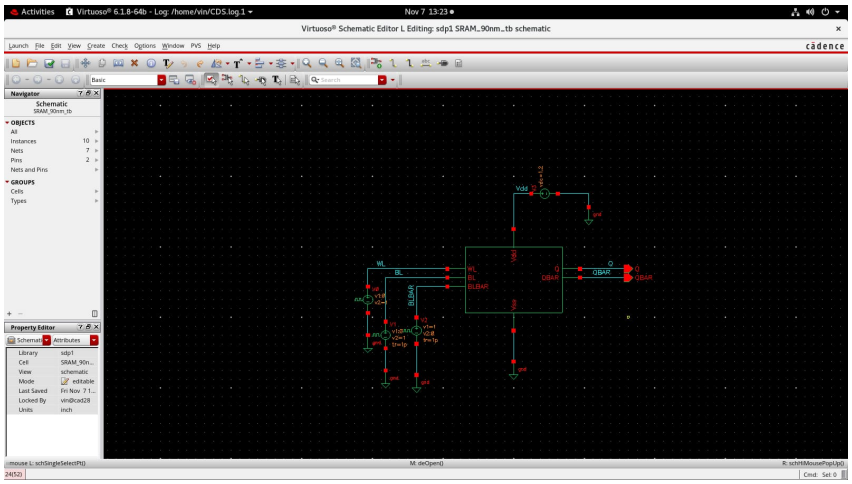

Figure 13: Test Bench of 6T SRAM bitcell using 90nm

Figure 14: Transient Analysis of 6T SRAM Bitcell using 90nm Technology

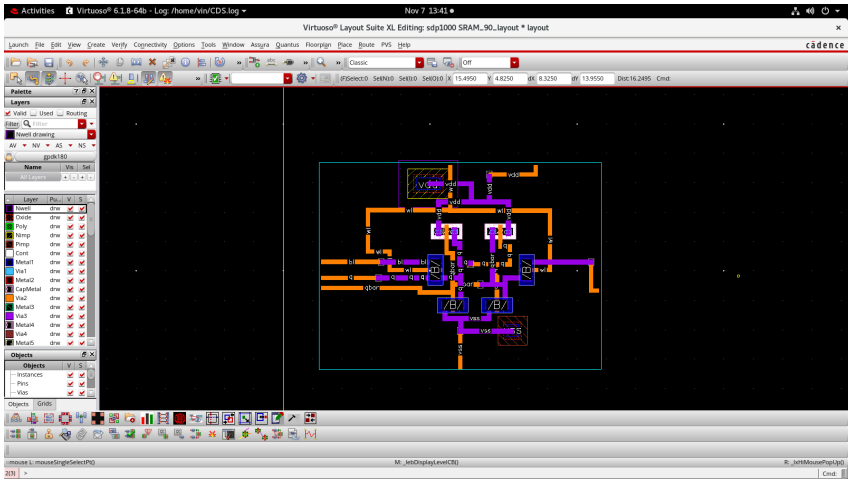

Figure 15: Layout of 6T SRAM bitcell using 90nm

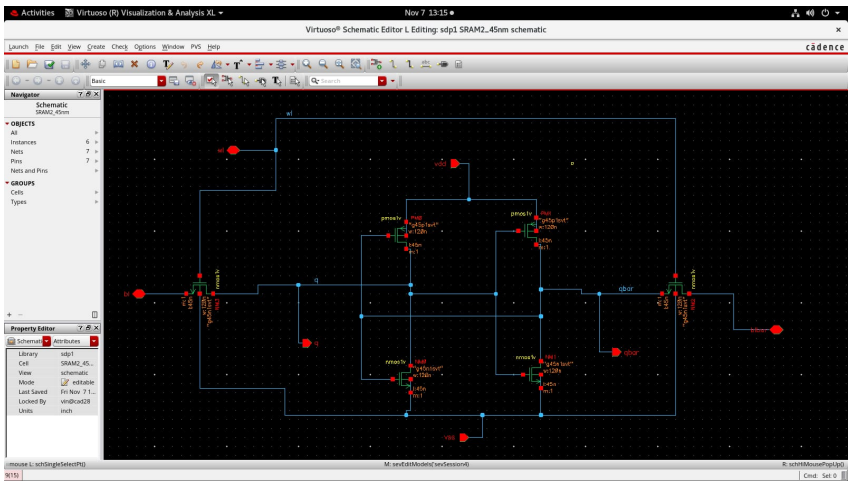

Figure 16: Schematic of 6T SRAM using 45nm technology

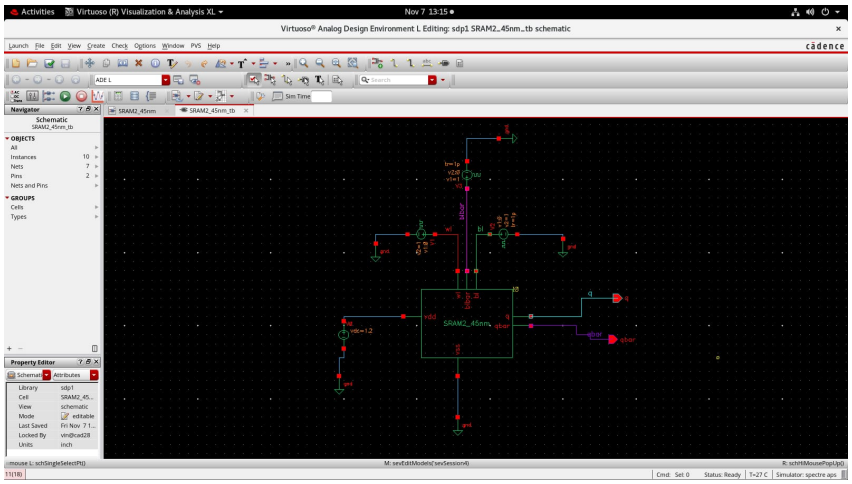

Figure 17: Test Bench of 6T SRAM bitcell using 45nm

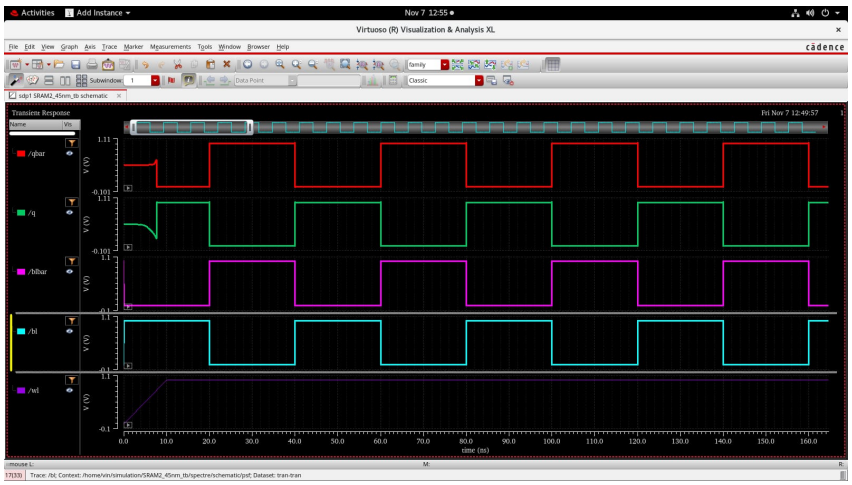

Figure 18: Waveform for Transient Analysis of Write Operation in 6T SRAM Bitcell in 45nm Technology

8 Write Delay and Power Comparison of 6T SRAM Across Technology Nodes :

8.1 180 nm Technology

VDD	Measurement	Literature paper values	Practical values
1.0V	Rising to Falling Delay (1→0)	0.255 ns	0.240 ns
1.0V	Falling to Rising Delay (0→1)	0.500 ns	0.410 ns
1.2V	Rising to Falling Delay (1→0)	0.166 ns	0.180 ns
1.2V	Falling to Rising Delay (0→1)	0.358 ns	0.340 ns
1.2V	Avg Power at Q	–	0.599 mW
1.2V	Avg Power at $\overline{Q}$	–	0.598 mW

Table 1: Write delay and power comparison of 6T SRAM at 180 nm node.

8.2 90 nm Technology

VDD	Measurement	Literature paper values	Practical values
1.0V	Rising to Falling Delay (1→0)	0.0912 ns	0.098 ns
1.0V	Falling to Rising Delay (0→1)	0.1403 ns	0.100 ns
1.2V	Rising to Falling Delay (1→0)	0.067 ns	0.039 ns
1.2V	Falling to Rising Delay (0→1)	0.119 ns	0.100 ns
1.2V	Avg Power at Q	–	0.625 mW
1.2V	Avg Power at $\overline{Q}$	–	0.403 mW

Table 2: Write delay and power comparison of 6T SRAM at 90 nm node.

8.3 45 nm Technology

VDD	Measurement	Literature paper values	Practical values
1.0V	Rising to Falling Delay (1→0)	0.062 ns	0.019 ns
1.0V	Falling to Rising Delay (0→1)	0.082 ns	0.020 ns
1.2V	Rising to Falling Delay (1→0)	0.0378 ns	0.011 ns
1.2V	Falling to Rising Delay (0→1)	0.0477 ns	0.020 ns
1.2V	Avg Power at Q	–	0.586 mW
1.2V	Avg Power at $\overline{Q}$	–	0.610 mW

Table 3: Write delay and power comparison of 6T SRAM at 45 nm node.

9 Conclusion

The project successfully demonstrates that technology scaling plays a vital role in improving SRAM efficiency. The 45 nm technology offers better performance in terms of speed and power consumption, making it ideal for low-power and high-speed applications. The 90 nm node provides a balanced trade-off between stability and power, while 180 nm offers higher noise immunity with larger area and delay. Thus, optimized transistor sizing and design techniques are essential to ensure reliable and energy-efficient SRAM operation in advanced VLSI systems.

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