DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGG.

Head of Department Profile

Name :- Dr. Smt Prerana VijayKumar Rathod

Present Post Held:- Head of Department (Electronics and Telecommunication)

Membership no. of professional Organization/ Bodies:-

- **Life member of Indian Society for Technical Education (ISTE)**
- **Associate Member of The Institution of Engineers (IEI-India) **

Part A:-Educational Qualifications (Degree Onwards)

Sr No.	Exam Passed	Name of Institute	Name of University	Year of Passing	% of Marks
1	B.E (Electronics & Telecommunication)	Maharashtra Institute of Technology,Pune	Pune University	May 1991	66%
2	M. Tech (VLSI Technology)	Department of Electronics	North Maharashtra University	May 2007	78.25%
3	Ph.D (Electronics Engg)		SKVM's NMIMS, Mumbai	July 2014	

Part B:-Previous Experience

a) Teaching Experience:-

Sr. No	**Period**		**Post held**	**Nature of appointment**	**Nature of post**	**Pay Scale**
	From Date	To date				
1	22-06-2018	Till date	Head of Department, Government Polytechnic, Nashik	Regular	Teaching Research and Administration	Level 13A1
2	27-10-2016	21-06-2018	Head of Department, Government Residential, Womens, Polytechnic, Latur.	Regular	Teaching Research and Administration	37400-67000 with an AGP of Rs. 9000
(3)	5-8-2001	26-10-2016	Designations held were Lecturer, Associate Professor, Professor, and in position of Head of Department and Academic Dean	Regular	Teaching and Research and Administration	Last drawn salary was with basic pay scale of 37400-67000 with an AGP of Rs. 10000

b) Industrial Experience:-

Sr. No	Period		Post held	Name of Company	Work Profile
	From Date	To date			
1	16-08-1991	9-02-1992	Trainee Engineer	Sejda TV, Nashik	Quality assured production by testing television receivers
2	10-2-1992	29-12-2000	Research & Development Engineer and Consultant	NATELCO, Nasik and STMF Consultancy services	Developed EPBAX, types of telephone instruments, test jigs for telecom products & microprocessor based systems

Participation in Training Programmers in last three Years:-

Sr.No.	Name of Training Program Attended	Duration of Training Program & Date	Name of Training Program sponsor	Venue of Training Program
1	Outcome Based Education (OBE) Philosophy and NBA Awareness	One week 9-01-2017 to 13-01-2017	Directorate of Technical Education, Maharashtra State, Mumbai	Government Polytechnic Pune.
2	Research Methodology and Optimization Techniques	One week 30-01-2018 to 03-02-2018	Directorate of Technical Education, Maharashtra State, Mumbai	Government Polytechnic, Nashik.
3	Foundation Training Programme for Class-I Officers of Directorate of Technical Education	6 Week 12-02-2019 to 25-03-2019	Directorate of Technical Education, Maharashtra State, Mumbai	Yashwantrao Chavan Academy of Development Administration
4	NPTEL Online Certification in Product Design and Innovation	4 Week Jan-Feb 2020	Swayam, Indian Institute of Technology, Guwahati	Online
5	Python Workshop	One day 22-06-2019	`Teaching Learning Centre(ICT) at IIT, Bombay	K.C.E. Society, COEIT , Jalgaon

Details of papers published in National & International Conference
Journal Papers:

- G.Phade, **Prerana Jain** and B.K. Mishra ,'Modeling of Optical Effects of MOSFET with EKV3 in MATLAB" *in InJoREST - International Journal of Research in Engineering Science & Technology*,Vol 1 No.1, pp 55-61, June 2010.
- **Prerana Jain**, B.K. Mishra and G. Phade," Power Gain Analysis of Optically Illuminated MOSFET", *International Journal of Computer Applications'* Vol 51 No 16, August-2012, pp.50-54. (00975-8887)
    - **Publisher and Place of Publication:** Published By FCS® (Foundation of Computer Science) USA.
- **Prerana Jain** and, B.K. Mishra," C-V Investigation in Optically Illuminated MOSFET ", *International Journal of Engineering Research and Applications*, ,Vol. 2, No 6, pp.1282-1288, November-December 2012, , (2248-9622)
    - **Publisher and Place of Publication:** Published By IJERA ,India.
- **Prerana Jain** and B.K. Mishra," An Investigation of DC Characteristics in Multifinger Optically Illuminated MOSFET", *International Journal of Computer Applications'* Vol 61-No 2, January -2013. , pp.12-17. (00975-8887).
    - **Publisher and Place of Publication:** Published By FCS® (Foundation of Computer Science) USA.
- **Prerana Jain** and B.K. Mishra," Evaluation of Optically Illuminated MOSFET characteristics by TCAD Simulation" , *International Journal of VLSI Design and Communication Systems*', (VLSICS)Vol 4 No 2, April 2013, pp11-25.
    - **Publisher and Place of Publication:**Academy And Industry Research Collabration Centre (AIRCC),India.
- **Prerana Jain** and B.K. Mishra," High frequency noise performance in OG-MOSFET", *Journal Of Electron Devices*,Vol No.18,August 2013,pp 1531-1536,(1682-3427)
    - **Publisher and Place of Publication:**Perpignan University,France

- A.J.Patil, **Prerana Jain** and Ashwini Pachpande, "Automatic Brain Tumor Detection Using K-Means and RFLICM" in International Journal of Innovative Research in Science,

Engineering and Technology (IJIRSET),Volume 3-Issue 12,DECEMBER 2014, pp 13896-13903 ISSN ONLINE(2278-8875) PRINT (2320-3765)

  - **Publisher and Place of Publication:** Ess & Ess Research Publications, Chennai-600070, Tamilnadu, India

- Khairnar Vinayak Prakash, Abhijeet Kumar and **Prerana Jain, "**Circumventing Short Channel Effects in FETs: Review**"** International Journal of Computer Applications ,(IJCA) Volume 117 - Number 17**,** May 2015 (pp-24 -30), (2321-7545)
  - **Publisher and Place of Publication:** Published By FCS® (Foundation of Computer Science) USA.
- **Prerana Jain,** A.J.Patil and Mayuri Thakre," Floating point Arithmetic, International Journal of Scientific Research and Education(IJSRE***)***, Volume 3, Issue 07, July 2015, pp 3929-3936 (2321-7545)
- **Prerana Jain,** A.J.Patil, Prasad Kulkarni, " Development of Economical Monitoring system for vehicle security, International Journal of Innovations and Advancements in computer Science ,Volume 4, Issue -7,pp 64-67(2347-8616)
  - **Publisher and Place of Publication:**Academic Science,New Dehli
- Khairnar Vinayak Prakash, Abhijeet Kumar and **Prerana Jain,"** Simulation And Characterization Of Silicon Nanowire FET Using SILVACO TCAD", IJRIT International Journal Of Research In Information Technology, Volume 3, Issue 8, August 2015, Pg. 91-98 (2001-5569)
- **Prerana Jain,** A.J.Patil and Mayuri Thakre, " Synthesis and Simulation of Floating point Multipliers", International Journal of Advance Foundation and Research in Computer (IJAFRC), Volume 2, Issue 11, November - 2015. (2348 – 4853)

International Conferences:

- **Prerana Jain**, B.K. Mishra and S.C. Patil, " Capacitance Modeling of Optically Gated MOSFET' *in proceedings of ACM, ICWET 10 (International Conference and Workshop on Emerging Trends in Technology),* Pages 887-891 , ISBN: 978-1-60558-812- doi: 10.1145/1741906.1742109.
- B.K. Mishra, **Prerana Jain**, G.Phade and S.C. Patil," Optically Controlled Transconductance Amplifier", *in proceedings of ACM, ICWET 11(International Conference and Workshop on Emerging Trends in Technology),* ICWET 2011", Pages 1139-11423,ISBN:978-1-4503-0449-8 ,doi: 10.1145/1980022.1980266 .
- G.Phade, B.K. Mishra and **P. Jain,**" Small Signal Modeling of Illuminated MOSFET for RF application" *in proceedings of ACM, ICWET 11(International Conference and Workshop on Emerging Trends in Technology),* ICWET 2011", Pages 1114-1119ISBN:978-1-4503-0449-8 ,doi: 10.1145/1980022.1980262 .
- **Prerana Jain**, Mishra B.K. and G, Phade, "AC performance of optically controlled MOSFET" in *proceedings of IEEE Students conference Electrical, Electronics and Computer Science* (SCEECS), 2012, ISBN: 978-1-4673-1516-6, doi :10.1109/SCEECS.2012.6184825,March-2012.
- **Prerana Jain**, Mishra, B.K. and G. Phade, "S parameters of optically illuminated MOSFET," in *proceedings of International Conference on Advancements in Engineering & Management* (ICAEM-2012) pp 9-12,February-2012.
- Gaytri M Phade, B K Mishra and **Prerana Jain, "**Modeling of Optically Tailored Noise Parameters of MOSFET", *in proceedings on International Conference in Computational Intelligence (ICCIA2012)* iccia(8):-, March 2012.
- Mukesh Mahajan, Prasant Ingale, P.N.Jain, "FPGA Implementation of ARM Processor", *in proceedings of International Conference on Recent Technologies,* at Institute of knowledge college of Engineering, Pune, Feb 9-11, 2012.
- Tanay Dahale, Prashant Ingale , P.N.Jain, "Simulation and Analysis of Silicon Nanaowire Transistor" in proceedings of *International Conference on Recent Technologies,* at Institute of Knowledge college of Engineering, Pune Feb 9-11, 2012.
- Prerana Jain and A.J. Patil, "Implementation of two dimensional DCT core by pipelining" *in proceeding of International Conference on "Science, Engineering and*

Spirituality" (ICSES-10) , on April 1st & 2nd, 2010, at SES College of Engineering, Navalnagar, Dhule (MS).

- Archana Shewale and Prerana Jain, " Face recognition using neutral network" *in proceeding of "International Conference on Science, Engineering and Spirituality*", (ICSES-10), on April 1st & 2nd, 2010, at SES College of Engineering, Navalnagar, Dhule (MS).
- **Prerana Jain,** A.J. Patil and Gayatri M Phade," FPGA Implementation of a Two Dimensional DCT Core" in *proceeding of International Conference on on Emerging Techniques in Computing, Electronics, Embedded System & VLSI Design*, on March 21-22, 2008, at Ahmednagar.
- Gayatri M Phade, R.S. Jahagirdar and Prerana Jain, "Intelligent Reflectometer for flexible pavement" at International Conference on Advances in Computing at Anuradha Engineering, February 25-26,2008, College, Chikli.

National Conferences:

- B.K. Mishra **,Prerana Jain**, and G.Phade, "I-V characterization of Optically Gated MOSFET" *in proceedings of National conference on Emerging Trends(NCET -10)* ,pp 183-187, March-2010.
- B.K. Mishra, G.Phade, and **Prerana Jain**, "InGaAs MISFET capacitances under illumination" *in proceedings National conference on Emerging Trends –(NCET-10),*pp158-160, March-2010.
- **Prerana Jain**, B.K. Mishra, G. Phade ,"RF performance of Optically Gated MOSFET" *in proceedings National conference on Emerging Trends –(NCET-10),*pp 57-61, March-2011.
- **Prerana Jain and** Archana Shewale," ERP and Web technology" *in proceedings of National conference on Computing, Communication, Electronica"* on 8-9 February, at KCE's College of Engineering and Information Technology, Jalgaon.

Areas Of Interest For Research:

- Semiconductor Device Modelling.
- VSLI Design: Front end and Back-end.

Professional Activities:

- Organizer & Convener of various workshops (PSPICE, Automation etc), conferences (ACME) etc. at Institute and University level.
- Invited to deliver expert lectures by North Maharashtra University, Government and Private institutes in Maharashtra
- Invited as reviewer, session chair and judge for conferences and technical events.
- Worked as Subject expert, Paper–setter and Examiner for various university at
- under-graduate and post graduate level.
- Successfully completed workshop on 'High Impact Teaching skills' conducted by WIPRO and Dale Carnegie Associates.
- Trained on Virtuoso Custom IC Design Flow at Cadence Training Centre, Bangalore.
- Coordinator for Avishkar-2013 where 10 groups were shortlisted for university and two groups represented university at State level.
- Actively involved in syllabus revision at Institute, MSBTE and university level.

Selections/Honours/Achievements:.

- First rank in M Tech (VLSI Technology) in North Maharashtra University.
- 21st ranking in merit list of HSC in Pune Board.
- Final year graduation project sponsored by Motorola, USA.

Extra Curricular Activities:

- Counselling and guidance to parents of mentally retarded children

Dr. Prerana Vijaykumar Rathod