Series/Parallel MOS Networks and MOS Current Dividers

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All experiments were conducted in LTspice.

Experiment 1: Transistor Matching

Q	I_s	V_{T0}	κ
1	2.1038mA	0.6758	0.6353
2	2.0305mA	0.6760	0.6326
3	2.0449mA	0.6763	0.6328
4	2.0854mA	0.6734	0.6353

Extracted I_s, V_{T0}, and κ from EKV fit

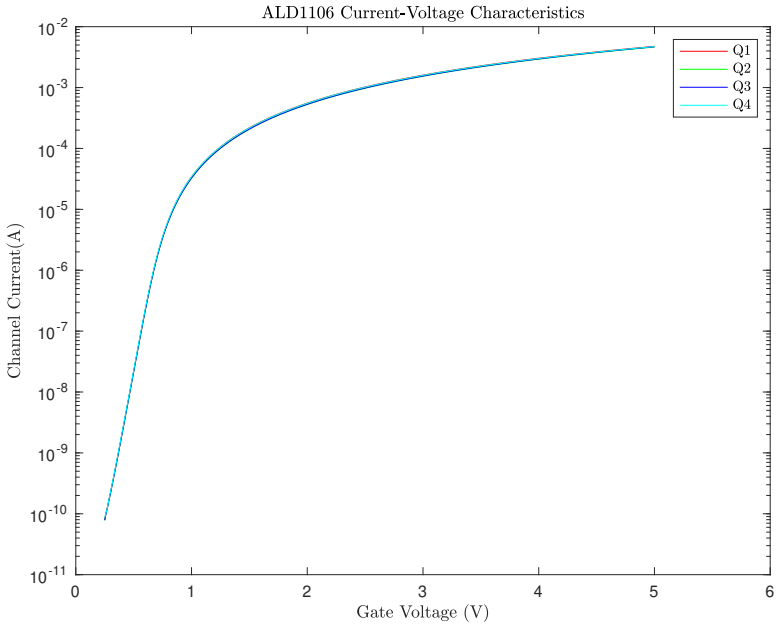


Figure 1: Channel Current vs Gate Voltage

The transistors match fairly well. Q1 and Q4 are more similar and Q2 and Q3 are more similar. This could be attributed to the physical location of the transistor circuits in relation to each other on the actual ALD chip. Q4 matches relatively poorly in weak and moderate inversion based on our percent difference graph. The other three transistors match well on the weak inversion region and at the higher end of strong inversion regions. Zoomed out, our Current Voltage characteristic curves are nearly identical.

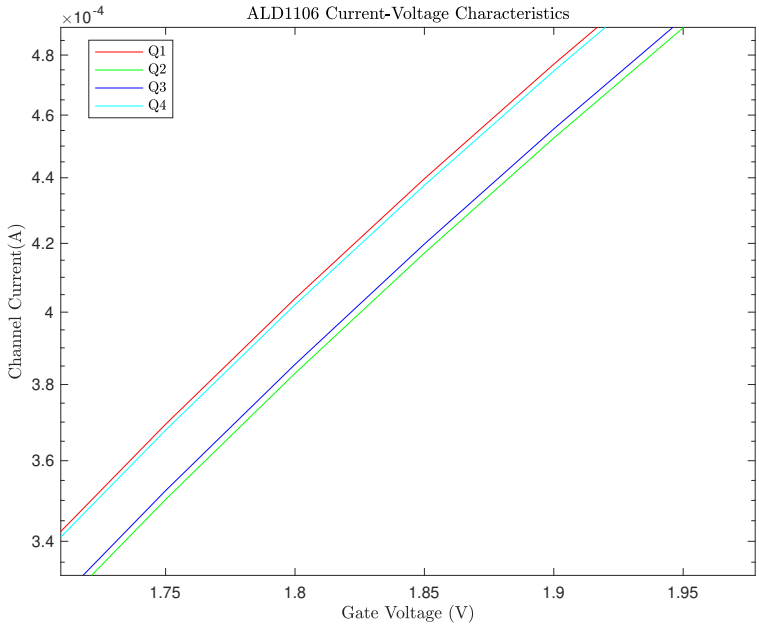


Figure 2: Zoomed view to show that the curves aren't identical

Experiment 2: MOS Transistors in Series and Parallel

For the parallel setup, the channel current does look to be consistently about twice of the individual. But, it is a little difficult to tell from Figure 6 or Figure 5. Similarly for the series setup, it looks reasonably close to 1/2.

From Figure 7 we can see the the parallel behaviour is actually very consistent for strong inversion. There is a small blip when in weak inversion and in the Ohmic region, however even that is within 5%. Figure 8 shows that the series behavior is really consistent in the Ohmic region of operation. There is a skew trendline when the device is in saturation however, it is again within 5% of the expected behaviour.

Experiment 3: MOS Current Dividers

The LTspice schematics used to simulate both setups is shown Figures 9a and 9b - note that in each subfigure there are two schematics, the left being setup A and the right being setup B. Both subfigures show the same two schematics; they differ in the Spice directives used for simulation. We only pull data from one divider setup per each subfigure.

Because LTspice gives us ideal transistors with identical strength ratios, using the default transistors to simulate a current divider would not be very interesting. To 'spice' it up, we changed the transistor multiplicity parameter for one transistor in each setup, sweeping it through a linear range of five values. In the spice directive used to accomplish this, we've labeled the multiplicity parameter being swept foo. We swept the parameter for each setup. As the multiplicity parameter affects the strength ratio as seen in the equation below, we are calling the effective strength ratio of the changed transistor as Ms, where s is the default strength ratio in LTspice. Furthermore, as the unchanged transistor uses the default strength ratio, we can call the strength ratio of the changed transistor as $s_2 = Ms_1$, where s_2 is the strength ratio of the changed transistor, and s_1 that of the unchanged transistor.

$$s_{\text{effective}} = Ms_{\text{base}}$$

For each setup we obtained five ITCs, one per each sweep - these are shown in Figures 10 and 11. Along with the simulation data are their according fits; each fit is also labeled with the extracted divider

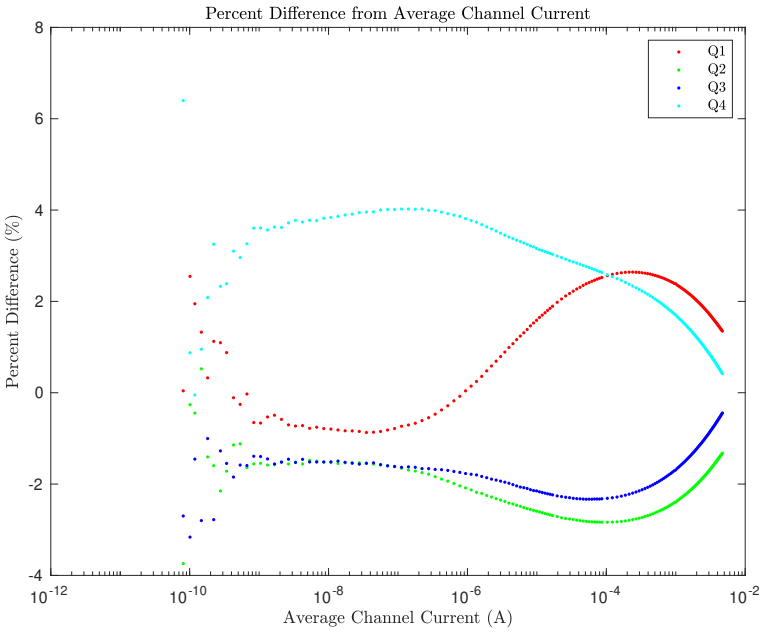


Figure 3: Percent Difference in Channel Current

ratio value. Comparisons of the extracted divider ratio and actual divider ratio for each setup are shown in Table 1, shown below. This shows that for each setup, the actual and extracted ratios match exactly. Additionally, we note that as expected, the ratios for the two experiments are the same. All current divider ratios are dimensionless.

Setup A		
s_2	Actual Ratio	Extracted Ratio
$0.5s_1$	0.33	0.33
$0.75s_1$	0.43	0.43
$1.0s_1$	0.50	0.50
$1.25s_1$	0.56	0.56
$1.5s_1$	0.60	0.60
Setup B		
s_2	Actual Ratio	Extracted Ratio
$0.5s_1$	0.33	0.33
$0.75s_1$	0.43	0.43
$1.0s_1$	0.50	0.50
$1.25s_1$	0.56	0.56
$1.5s_1$	0.60	0.60

Table 1: Table of Actual vs. Extracted Divider Ratios

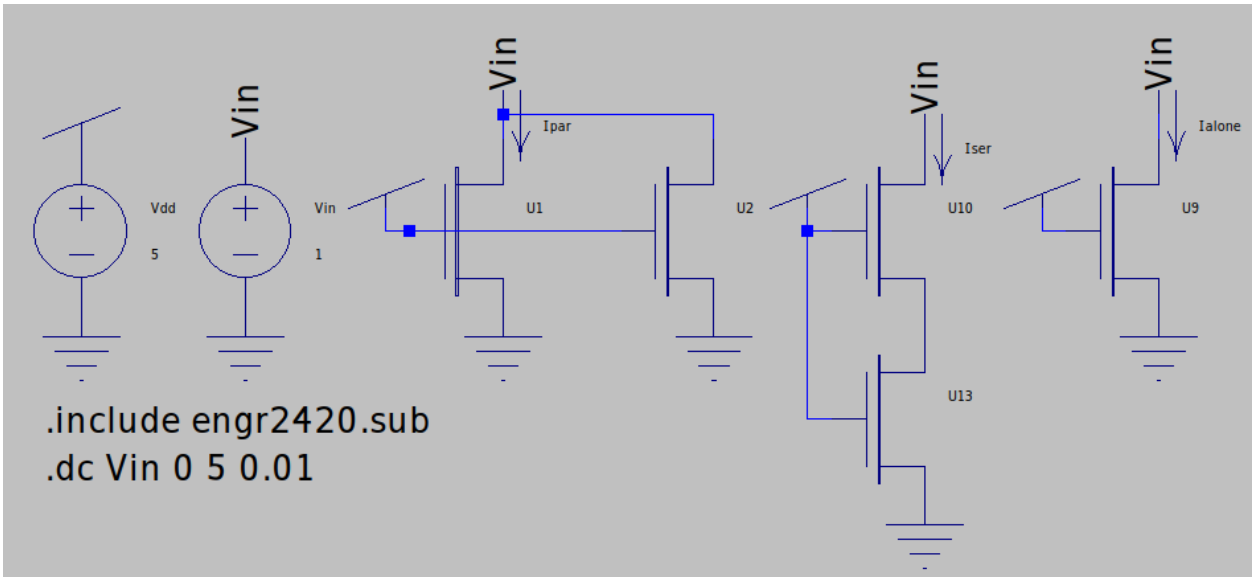


Figure 4: Schematic for exp 2
For this experiment, data from Brad's experimental setup was used

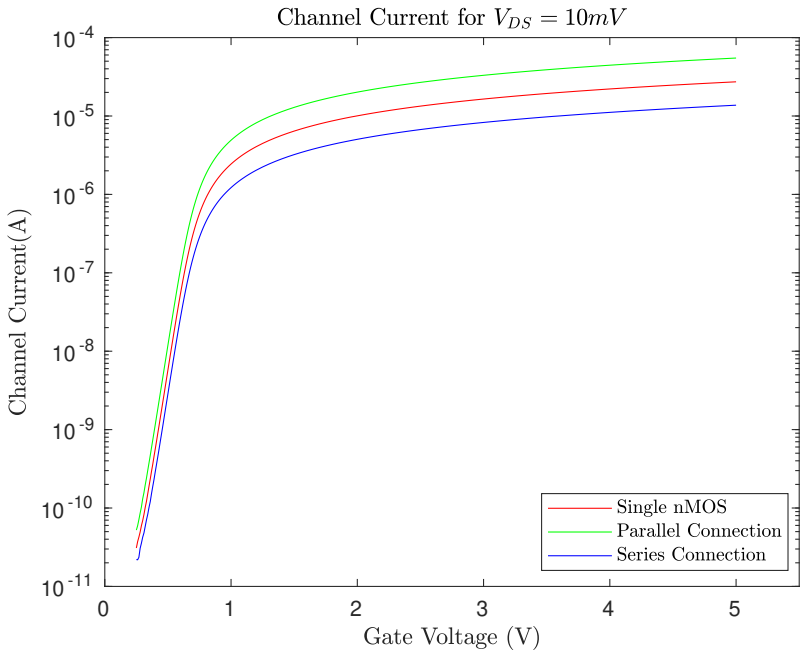


Figure 5: Channel Current in Ohmic Region

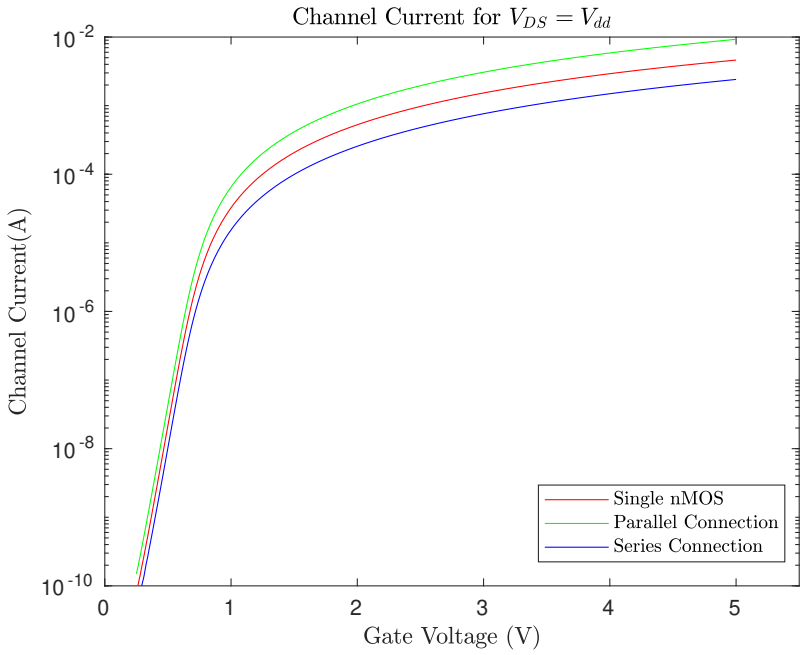


Figure 6: Channel Current in Saturation Region

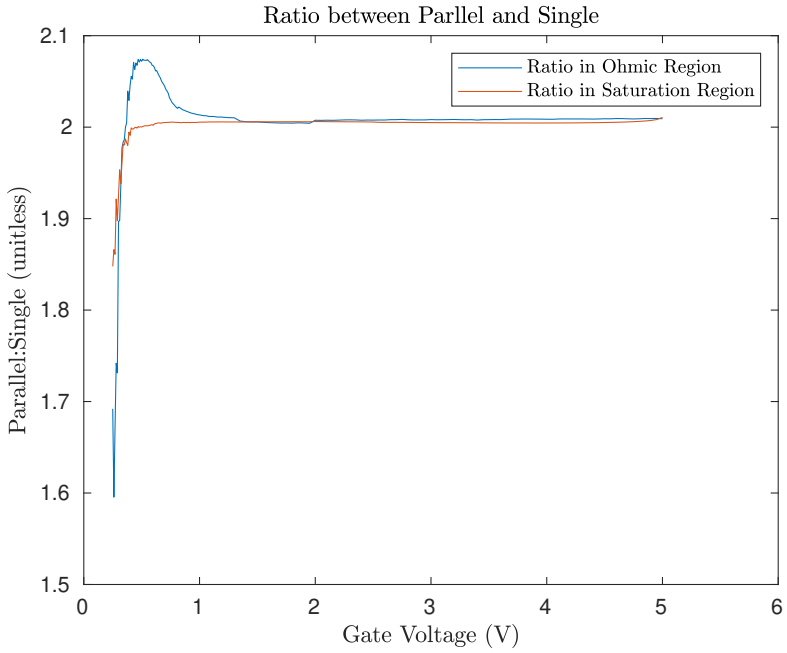


Figure 7: Ratio between Parallel and Single

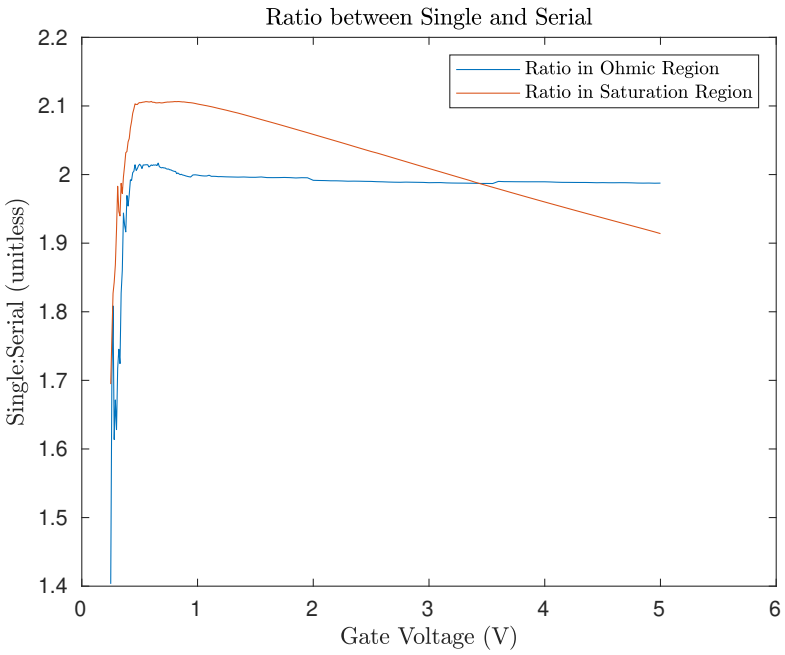
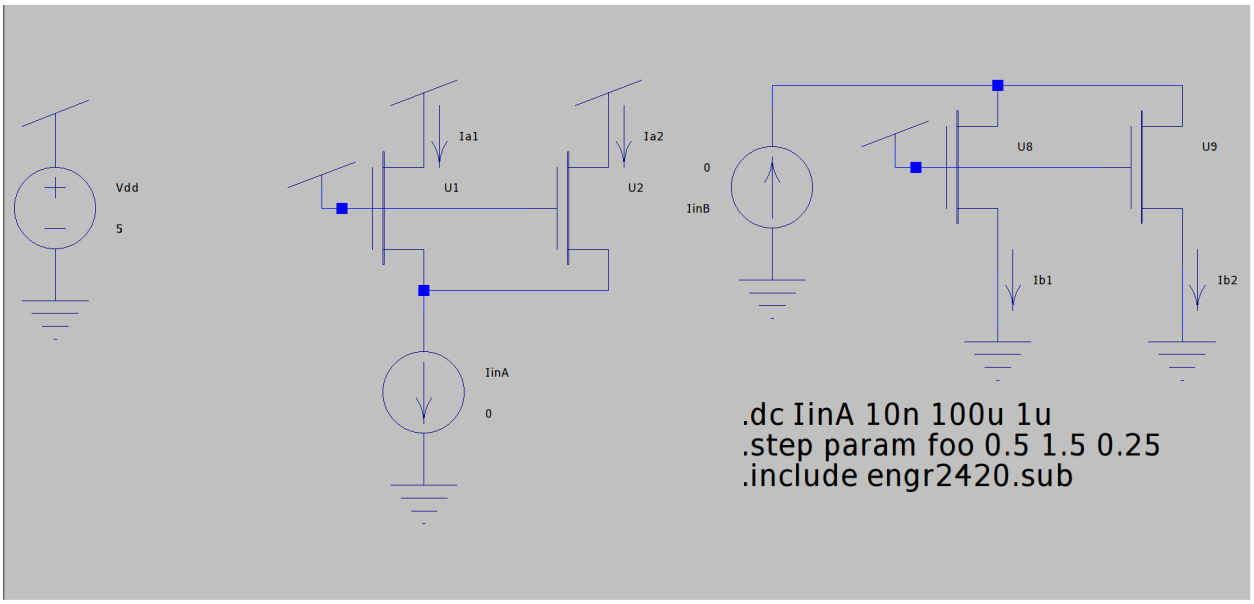
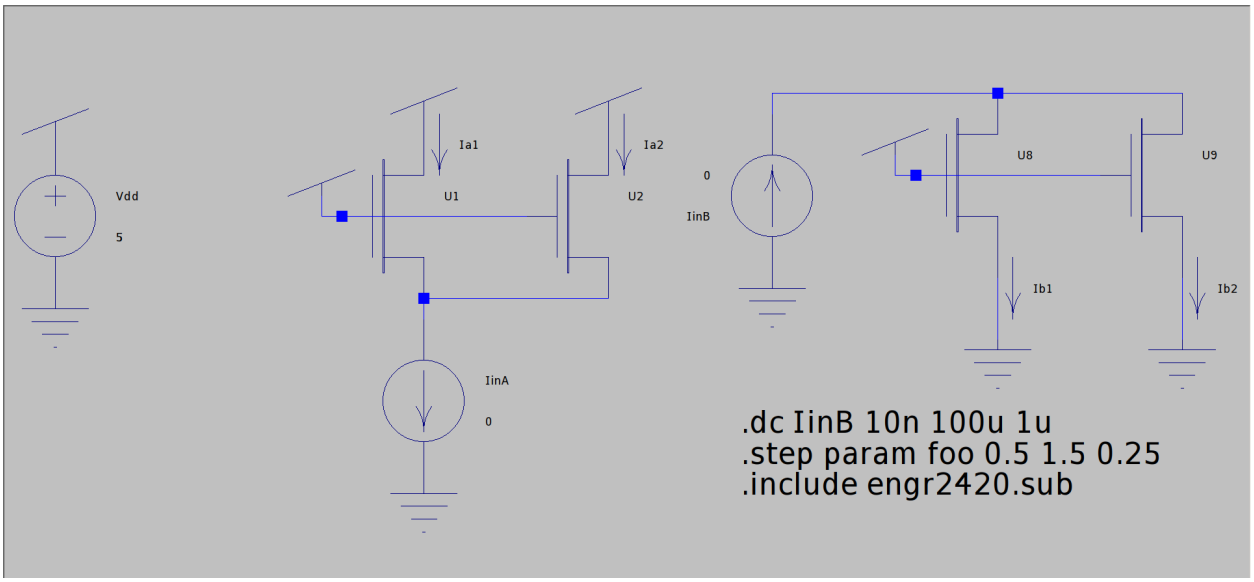


Figure 8: Ratio between Single and Single



(a) Current Dividier Setup A



(b) Current Dividier Setup B

Figure 9: LTspice schematic for exp 3's current divider setups

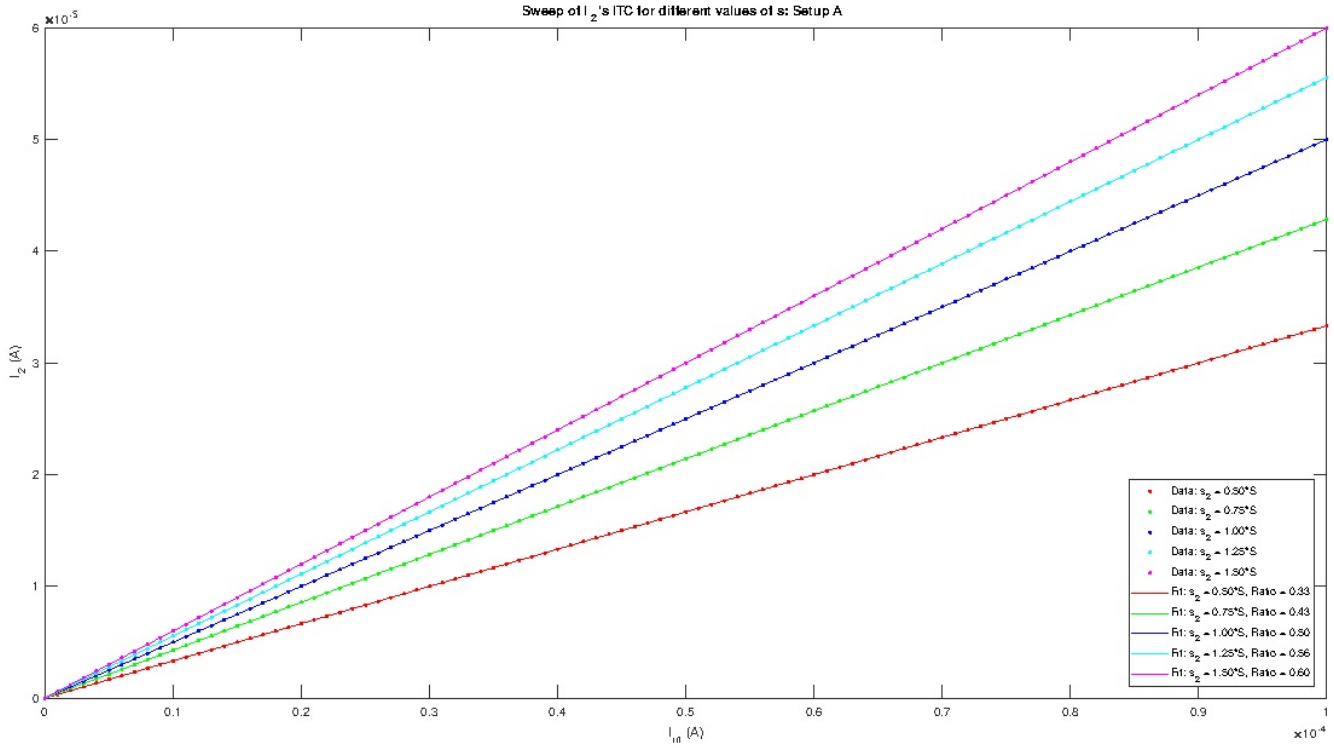


Figure 10: Current Divider ITC for setup A: Sweeping s_2

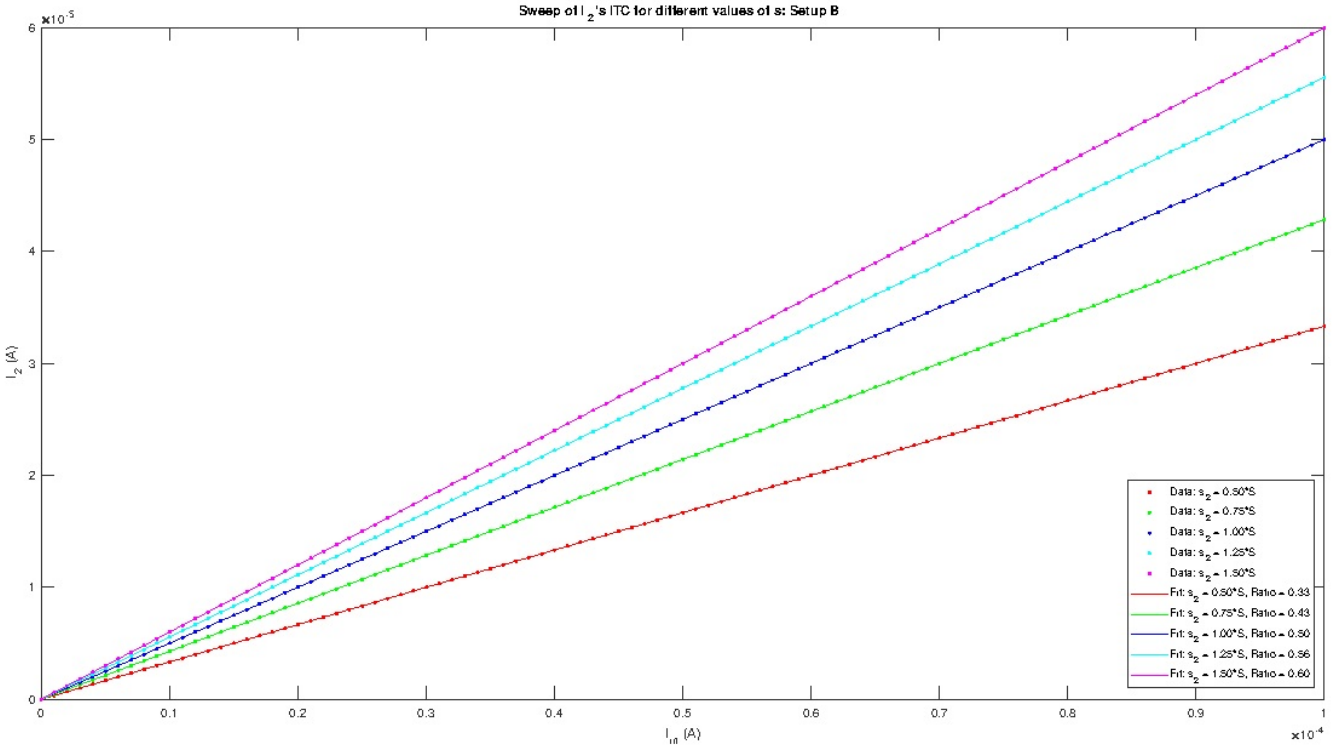


Figure 11: Current Divider ITC for setup B: Sweeping s_2