Translinear Circuits

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All experiments were conducted in LTspice.

Experiment 1

We used the LTspice schematic setup seen in Figure 1 for this first experiment. After running the sweeps, we fit the EKV model to the output data and extracted the parameter values for κ, I_s, and V_T. Plotting the fits against the actual data on a semilog-y scale results in the two graphs seen in Figures 2 and 3 for the nMOS and pMOS transistors, respectively, where we see that the EKV model matches well with each transistor response. (The fit parameters are listed in the figure titles).

Likewise, the values for the transconductance gain g_m was extracted, and plotted on a log-log scale against the current, along with the theoretical fits from the Weak Inversion and Strong Inversion models. These are seen in Figures 4 and 5 for the nMOS and pMOS transistors. The fits for both transistors match their according sections very well, i.e. the weak inversion model fits match the weak inversion portion of the responses very well, and likewise for the strong inversion model.

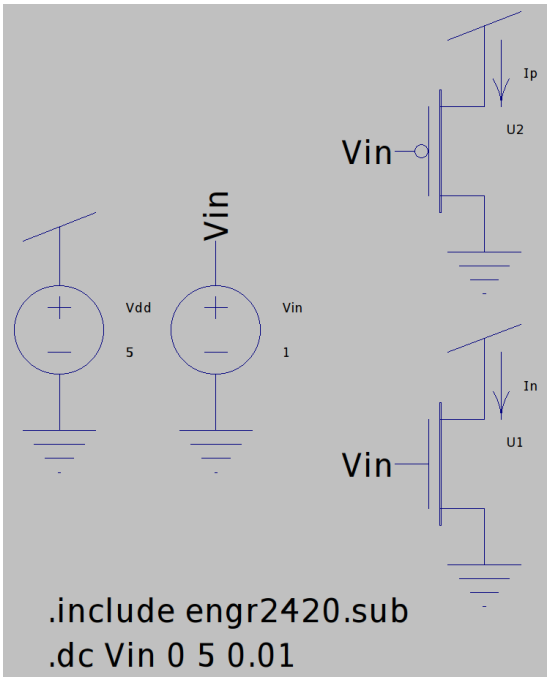


Figure 1: LTspice setup schematic

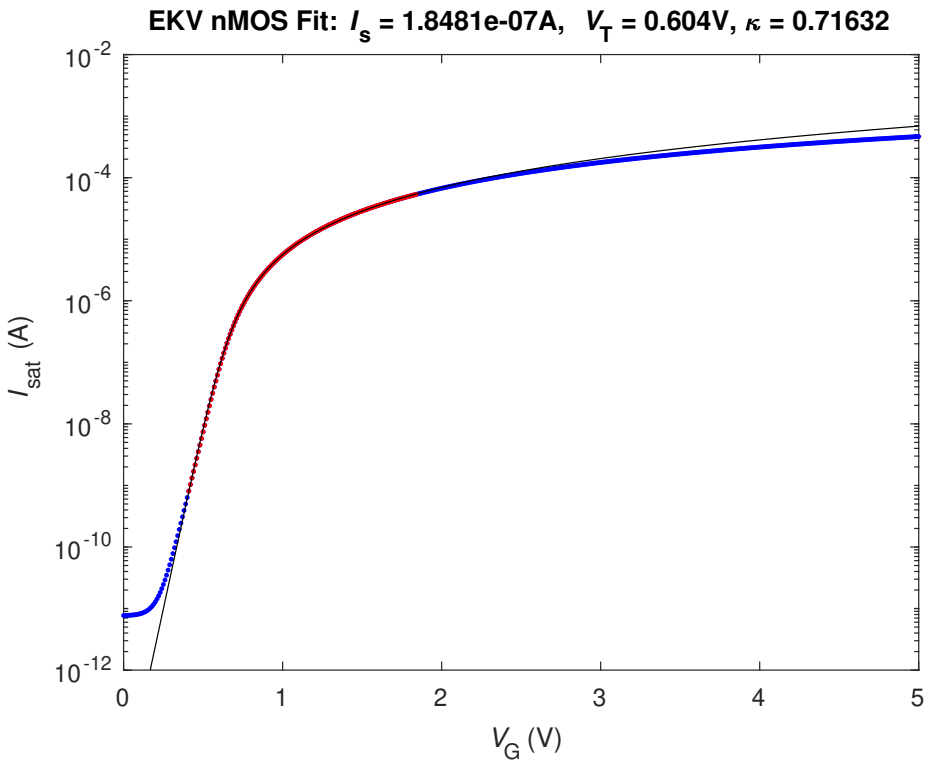


Figure 2: EKV fit for an nMOS transistor

Experiment 2

The slope of the exponential in the Weak Inversion regime for the nMOS is -34.681A/V. This is flipped on our graph so we could generate our fit line. The slope of the pMOS is 37.114A/V. The characteristics obtained from this experiment yielded slightly different values, but all on the same order of magnitude as those obtained from experiment 1. For our nMOS, we got an I_s value of 2.72e-8, a V_T value of 1.12V and a K value of 1.08. For our pMOS, we got an I_s value of 2.84e-8, a V_T value of 1.2V and a K value of 1.1.

The theoretical fits match the data very well in the WI and SI regions.

Experiment 3

It is generally a good assumption that a transistor's intrinsic gain is much larger than unity as seen in Figure 16. $G_m * r_o$ will also be significantly above unity because κ is .7 for both types of transistors. We believe that the transistor has a significant gain associated with changes in V_g

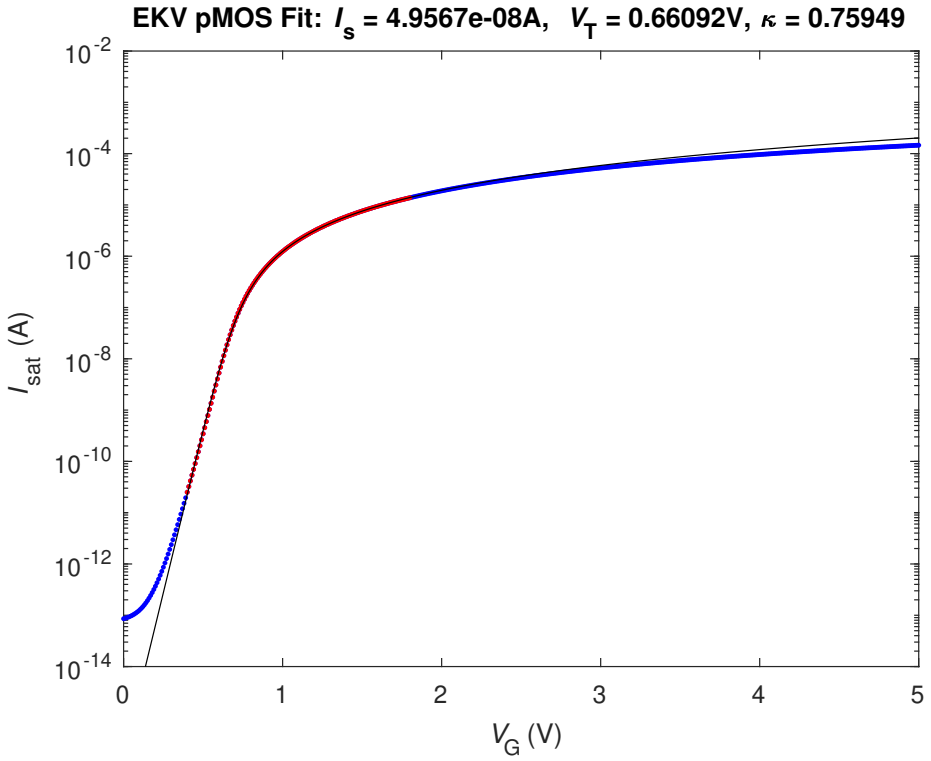


Figure 3: EKV fit for a pMOS transistor

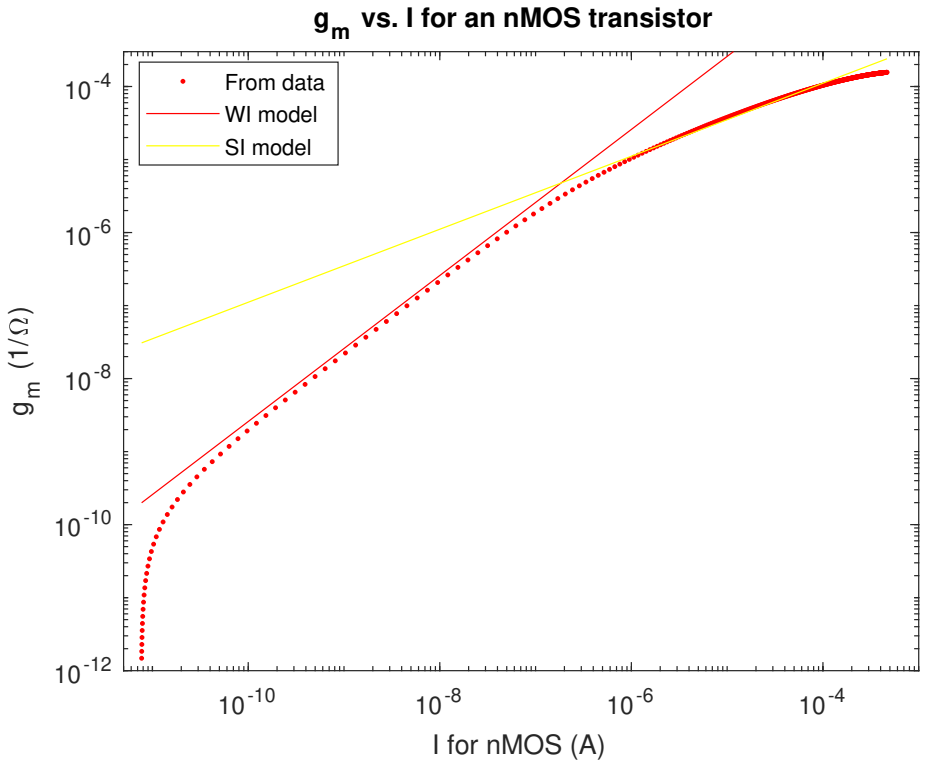


Figure 4: g_m vs. I for an nMOS transistor

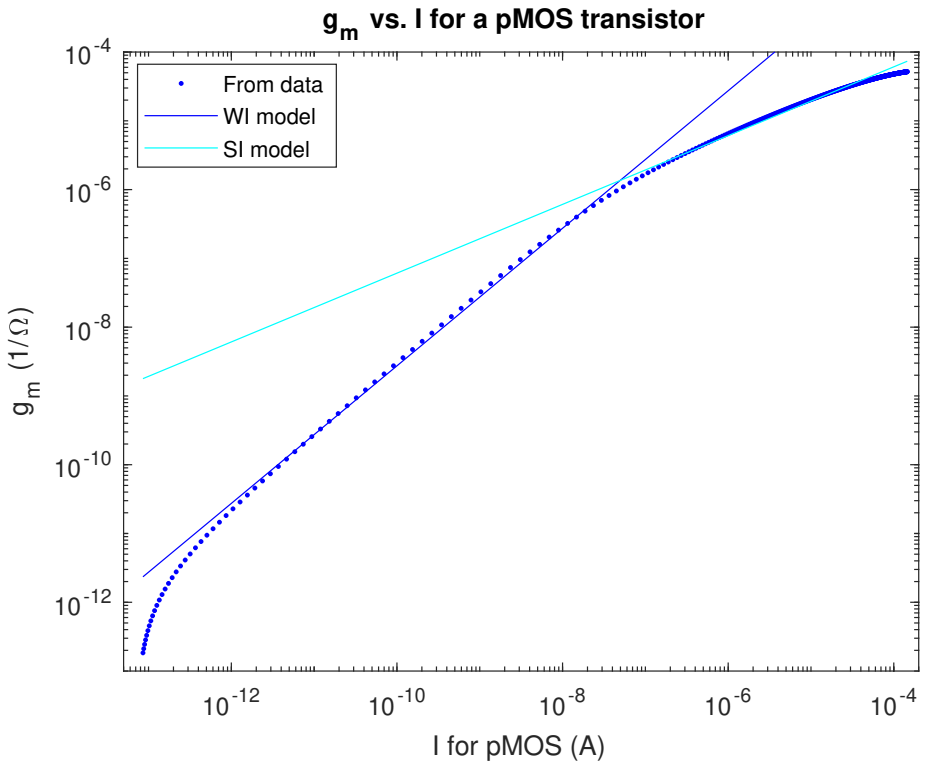


Figure 5: g_m vs. I for a pMOS transistor

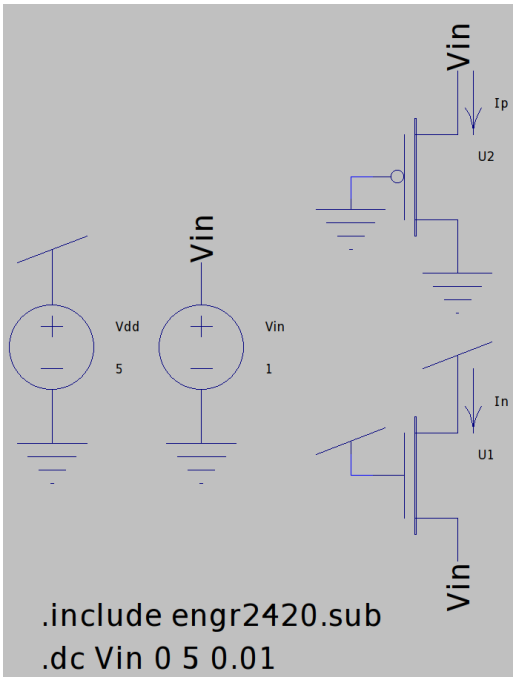


Figure 6: LTspice setup schematic exp 2

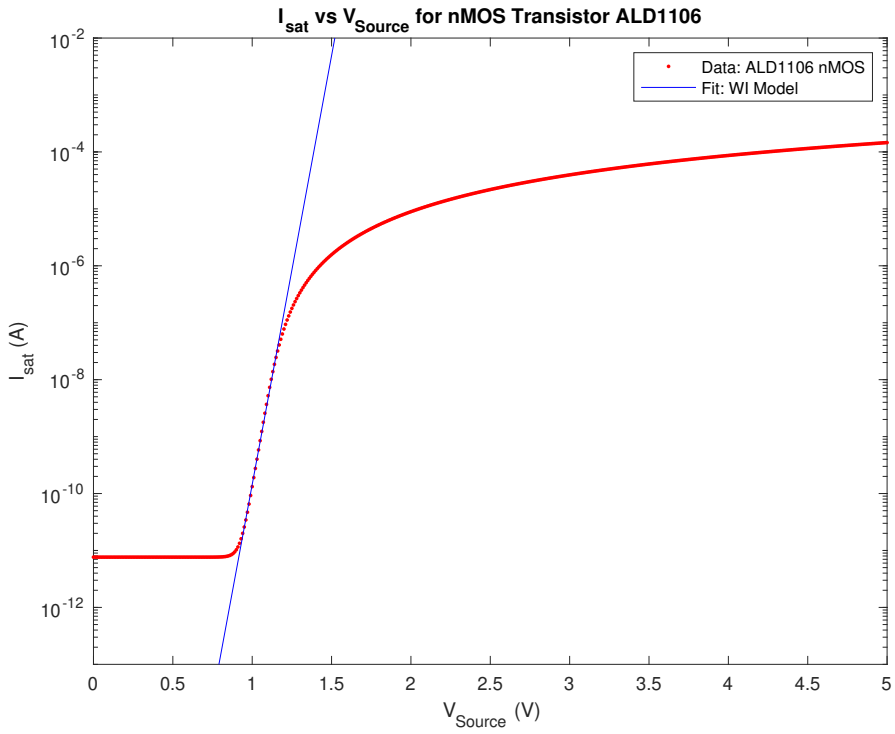


Figure 7: I_sat vs. V_{source} for an nMOS transistor

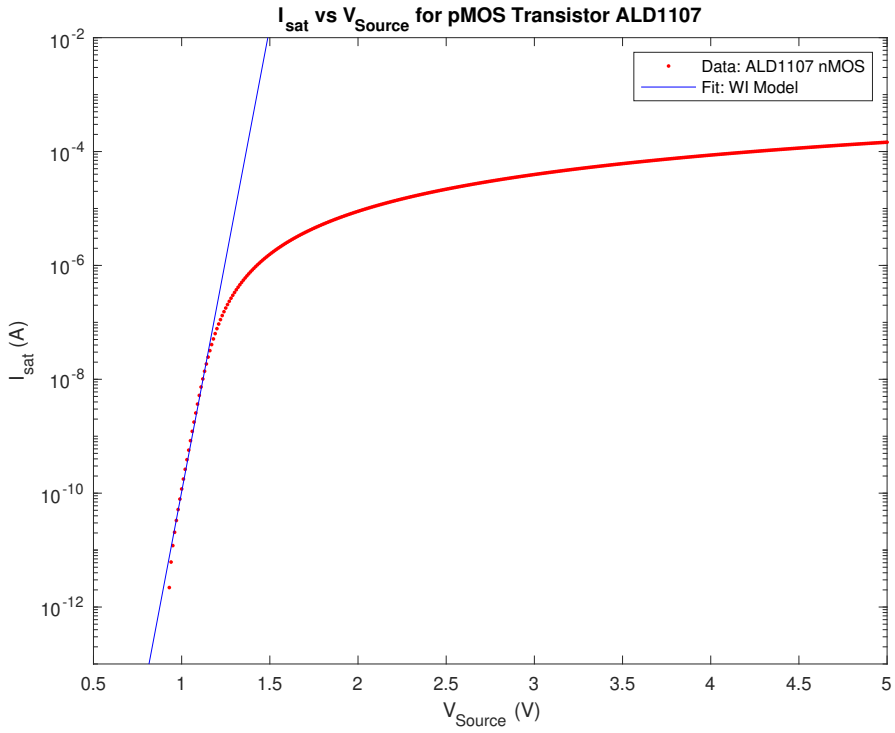


Figure 8: I_sat vs. V_{source} for an pMOS transistor

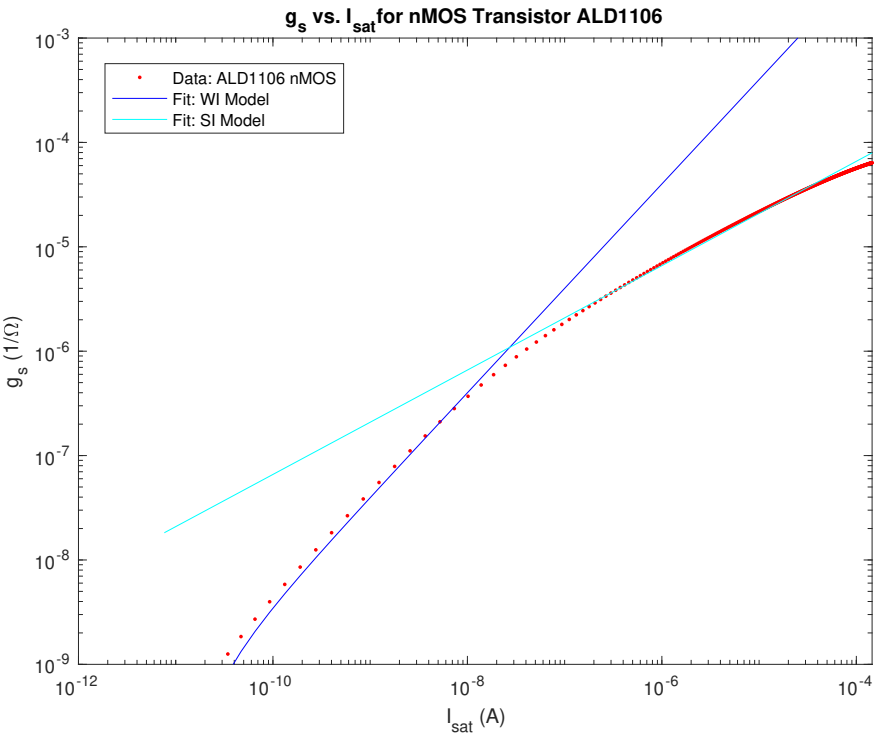


Figure 9: g_s vs. I for an nMOS transistor

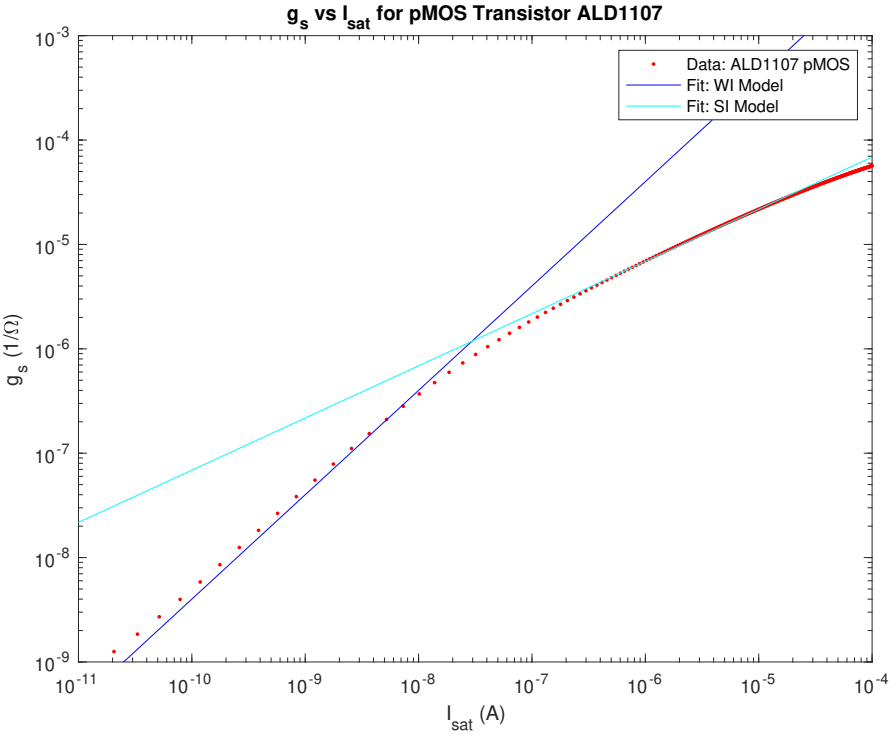
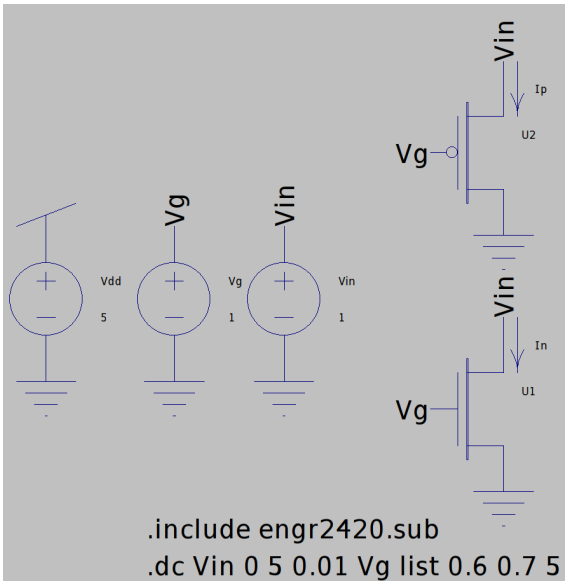
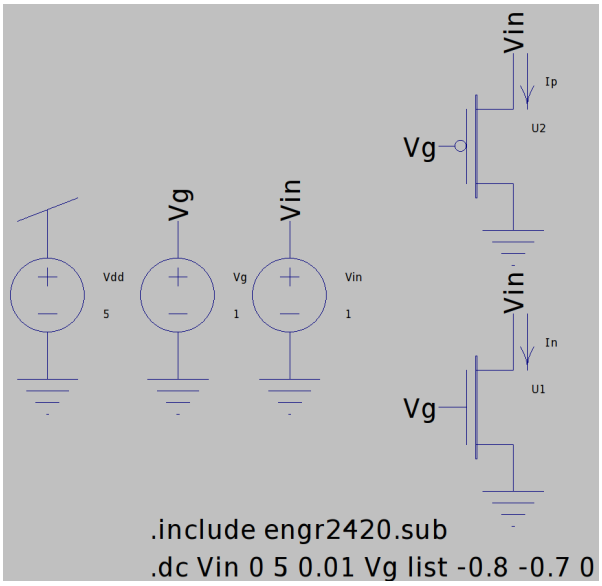


Figure 10: g_s vs. I for a pMOS transistor



(a) nMOS setup



(b) pMOS setup

Figure 11: LTspice setup schematic exp 3

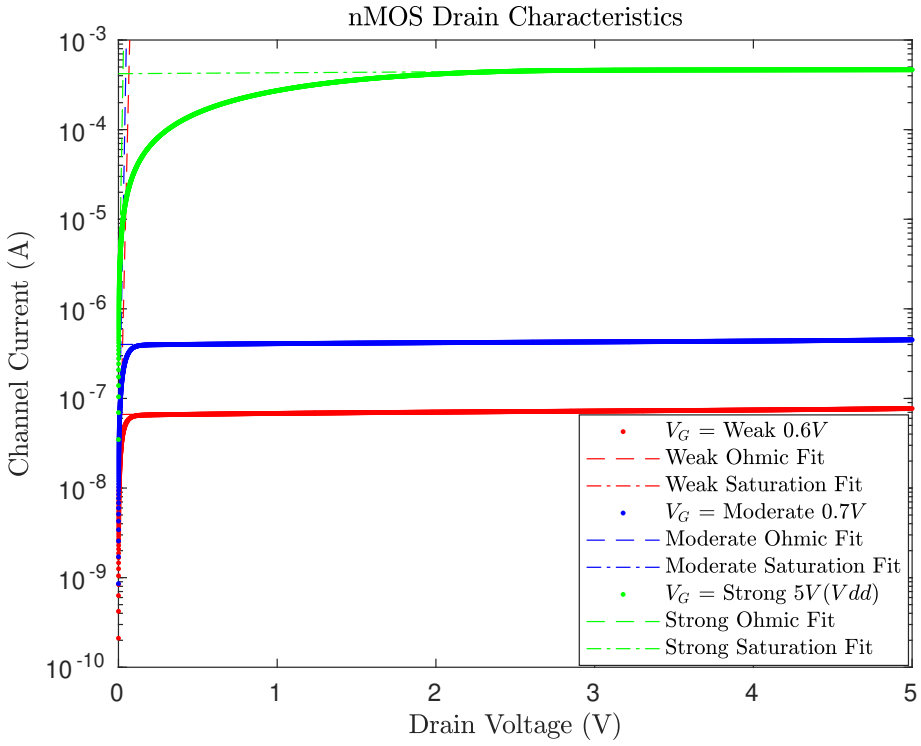


Figure 12: Drain Characteristics for nMOS transistor

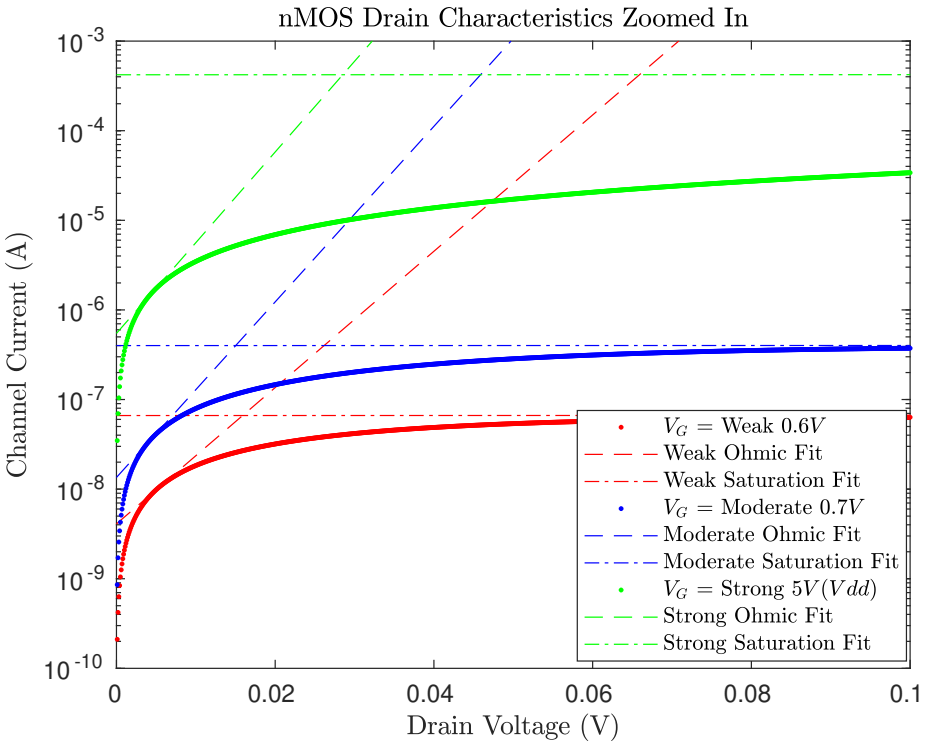


Figure 13: Drain Characteristics for nMOS transistor zoomed in

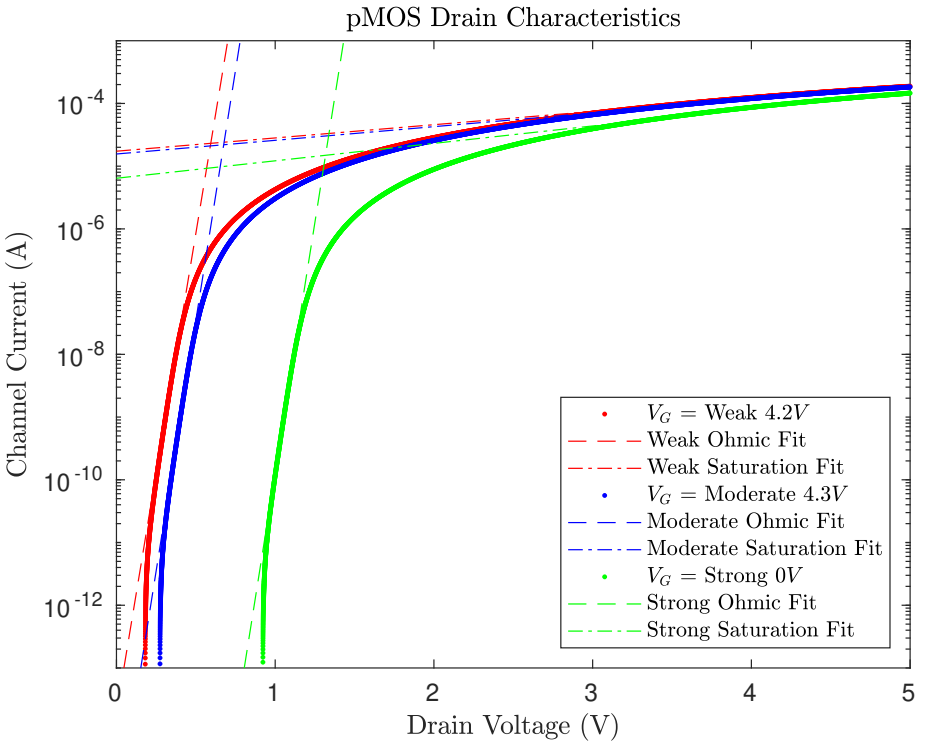


Figure 14: Drain Characteristics for pMOS transistor

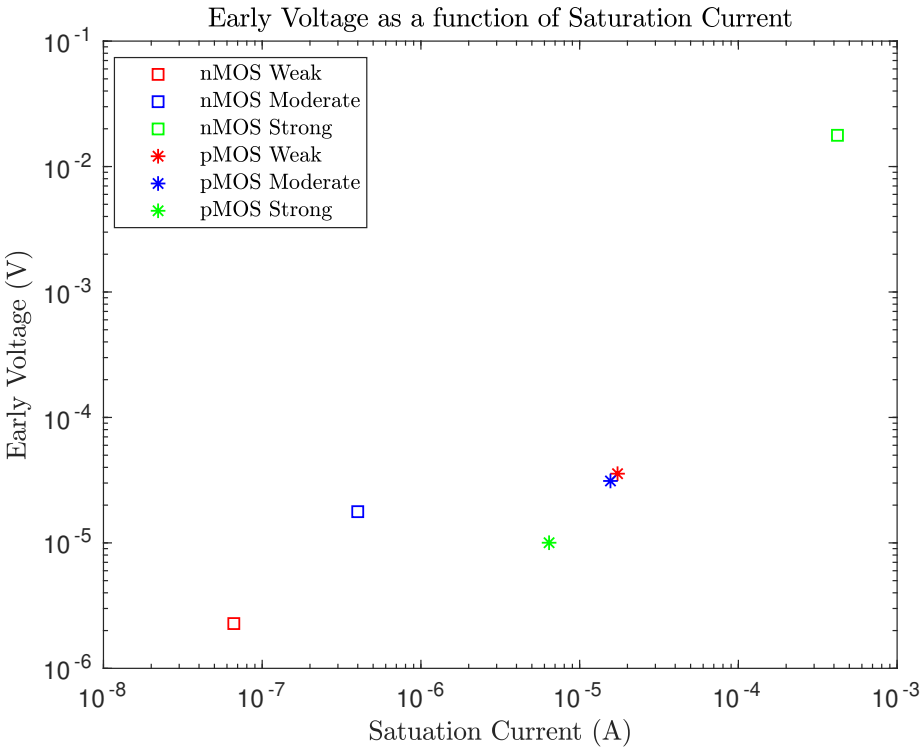


Figure 15: Early Voltage as a function of Saturation Current

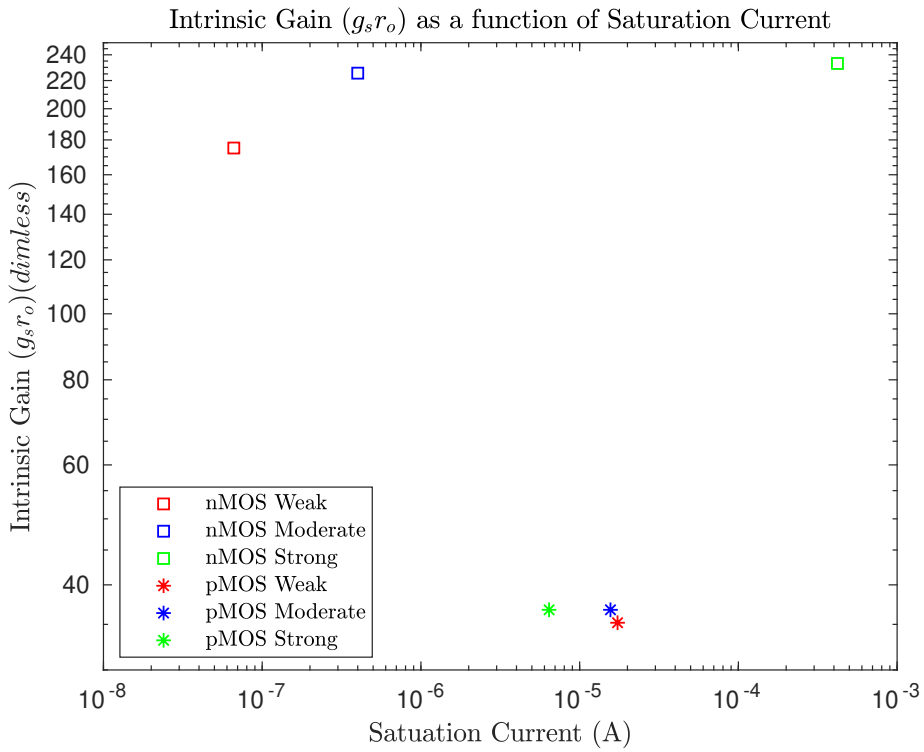


Figure 16: $g_s r_o$ Intrinsic Gain as a function of Saturation Current