FACULTY OF ENGINEERING & TECHNOLOGY,
UNIVERSITY OF LUCKNOW
B.TECH. SEMESTER - IV, 2023-24
Branches: ECE, CSE & AI

Student's Roll No.....

Subject Code: EC-301 **Subject Title: Digital Circuits & Logic Design**
Time: 1 Hrs. **Full Marks:** 20
Note: Attempt questions from each section as per instructions.

SECTION A

1. ***Attempt all parts of this question. Each part carries 1 mark.*** **(1 x 5=5)**
   a) What are universal logic gates? Why they are called as universal logic gates?
   b) Explain in brief ASCII code.
   c) Implement XNOR gate using NAND gate.
   d) Convert $(BF.34)_{16}$ into equivalent binary and octal code.
   e) Convert $(35.35)_{10}$ into equivalent hexadecimal code.

SECTION B

Attempt any THREE questions of the following. Each question carries equal marks. **(5 x 3=15)**

2. Simplify the given expression using Boolean theorems:
   $$F(A, B, C) = \bar{A}BC + B\bar{C} + \bar{A}B\bar{C} + \bar{A}B + A\bar{C} + ABC.$$
3. Generate the Hamming code for the message bit 111011. Also check whether received code word 1110010011 is erroneous or not. If yes, then find out that position. (even parity)
4. Find out the minterms and maxterms of given expression:
   $$F(A, B, C, D) = AB+CD.$$

OR

Perform subtraction (A-B) between A=1011 and B=1110 using 2's complement method and BCD addition (A+B) between A= 6 and B=8.

5. Explain and classify binary codes in detail with suitable examples.

OR

Simplify the following Boolean function using K-map and also implement the simplified function using logic gates:
$$F(A, B, C, D) = \sum m(0,2,4,5,7,10,11,13,14,15) + \sum d(1,8,12).$$

Department of Electronics and Communication Engineering,
Faculty of Engineering & Technology, University of Lucknow
2nd Mid Term Exam (2023-24)
Digital Circuits and Logic Design (EC-301)

M.M.: 20 **Time: 1 HOUR**

NOTE: Attempt all the questions. **Roll. No.....**

SECTION-A

1. **Note: Attempt all the parts.** **(1x5=5)**

a) Differentiate combinational and sequential circuits.
b) Design XOR and XNOR gate using 2:1 MUX.
c) Define race-around condition only.
d) Give the excitation tables for S-R and J-K flipflops.
e) Calculate total time required in load and shift by a 4-bit SISO shift register if each flip-flop has 10 ns propagation delay.

SECTION-B

Note: Attempt any three questions. **(5x3=15)**

2. Design a 4-bit magnitude comparator with its output expressions.
3. Design a 16:1 MUX using 4:1 MUX only. Also, implement the given function using 4:1 MUX taking A&B as select lines:
   $F(A,B,C,D) = \Sigma m(0,1,2,4,5,8,10,12,14)$.
4. Draw and explain PISO shift right register with its timing diagram.
5. Draw and explain ring and Johnson counters with their timing diagrams.

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B.Tech. IIIrd Semester Examination, 2023

DIGITAL CIRCUITS AND LOGIC DESIGN

Paper : EC–301

Time : 3 Hours] [*M.M. : 70*

Note :– Answer any *five* questions. All questions carry equal marks.

1. (a) What do you understand by weighted and non-weighted binary codes ? Convert Gray code 1101 to equivalent excess-3 code.

(b) What are universal logic gates ? Why are they called as universal logic gates ? Design XNOR gate and AND gate using NOR gates.

2. (a) Find out the minterms and maxterms for the given function :

$$F(A, B, C, D) = AB + CD$$

(b) Simplify the following Boolean function 'F' together with don't-care condition and also implement the simplified function using NAND gate only :

$F(A, B, C, D) = \Sigma m(1, 3, 5, 7, 9) +$

$d(A, B, C, D) = \Sigma m(6, 12, 13)$

3. (a) Simplify the following function using tabulation method :

$F(A, B, C, D) = \Sigma m(1, 4, 6, 7, 8, 9, 10, 11, 15)$

(b) Perform the subtraction (A – B) using 1's complement method where A = 1011 and B = 1110. Also, draw its circuit diagram.

4. (a) Write the BCD equivalent of $(AB)_{16}$. Perform BCD addition between A = 7 and B = 9 with its circuit diagram.

(b) Design a 16 : 1 multiplexer using 4 : 1 multiplexer. Also, implement the following Boolean function using 4 : 1 MUX taking C and D as select line :

$F(A, B, C, D) = \Sigma m(0, 1, 2, 3, 4, 6, 8, 10, 12, 13, 14, 15)$

5. (a) Draw and explain a 4-bit magnitude comparator with its output expressions.

(b) Differentiate between characteristic table and excitation table. Explain race-around condition in detail with its remedies.

6. (a) Perform the following conversions :

(i) J-K flipflop to T flipflop

(ii) D flipflop to J-K flipflop

(b) Explain 4-bit ring counter and Johnson counter using D-flipflop with its timing diagrams.

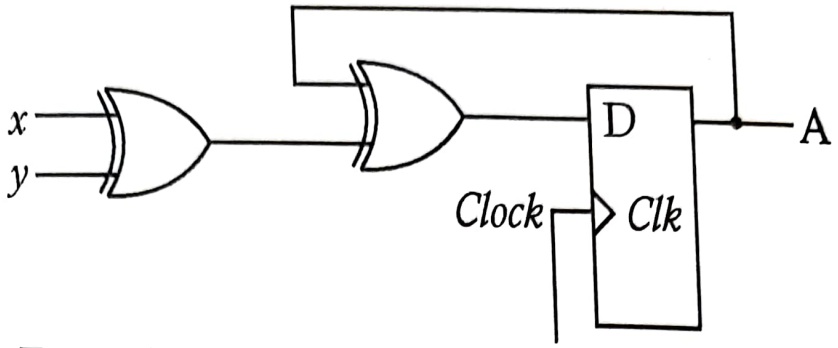
7. (a) Design 4-bit synchronous counter using D flipflop and also trace its timing diagram.

(b) Design Modulo-14 synchronous counter using S-R flipflops.

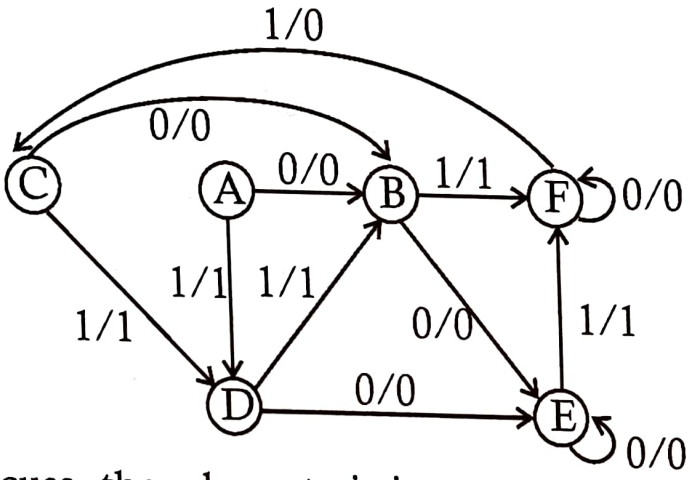
8. (a) Draw and explain 4-bit PISO shift-left register using D-flipflop.

(b) Differentiate between synchronous and asynchronous sequential circuits. Calculate total time required in load and shift by 4-bit PISO shift register if each flipflop has 15 ns propagation delay.

9. (a) Derive state table and state graph for the following circuit diagram :



(b) Draw the reduced state graph by first deriving its reduced state table of the following state graph :



10. (a) Discuss the characteristic parameters of a logic family. Calculate the fan-out of an inverter having the following specifications : $I_{OH\ max} = -0.4mA$, $I_{OL\ max} = 8mA$, $I_{IH\ max} = 20\mu A$, $I_{IL\ max} = -0.1mA$.

(b) Implement the following function using PROM, PLA and PAL :

$F(A, B, C, D) = \Sigma m(0, 3, 6, 9, 10, 12, 14, 15)$