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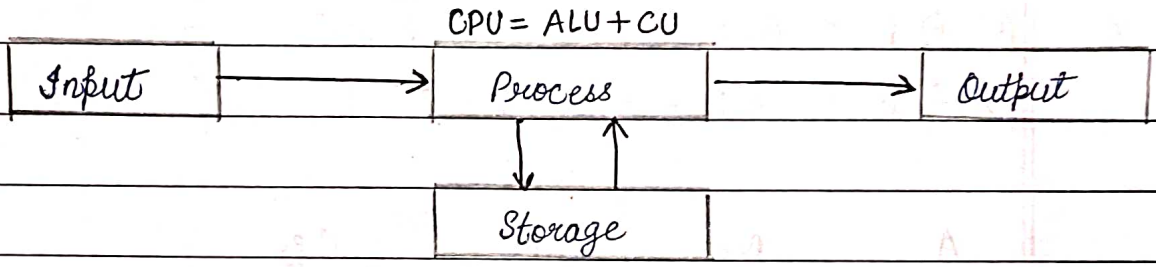
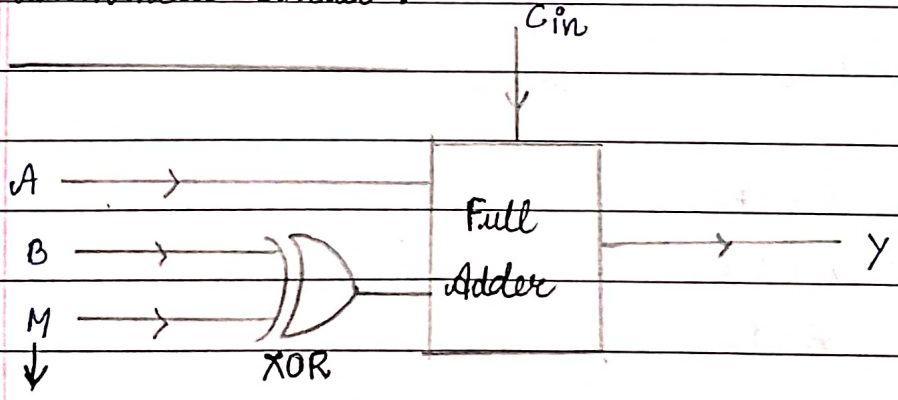
Unit : 1



Basic Amenities of Computer Organisation :

- ALU
- ALU operations
- Control design
- I/O organization
- Storage

Arithmetic Circuit :



(Control value / Control Input)

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★ $B \oplus 0 = \bar{B}.0 + \bar{\bar{B}}.\bar{0} = 0 + B = B$

★ $B \oplus 1 = \bar{B}.1 + B.\bar{\bar{0}} = \bar{B} + 0 = \bar{B}$

$(A \oplus B = \bar{A}.B + A.\bar{B})$ & $(\bar{0} = 1)$ & $(\bar{1} = 0)$

A	B	M	C_{in}	Y
A	0	0	0	Transfer (A)
A	0	0	1	Increament (A+1) /Dec.
A	B	0	0	Addition (A+B)
A	B	0	1	Addition with Carry (A+B+1)
A	B	1	0	Subtraction with Borrow (A+$\bar{B}$)
A	B	1	1	A+$\bar{B}$+1 (Subtraction)

★ A+1 = A-1

∵ A+1 = A+0+1
= A+$\bar{1}$+1
= A-1

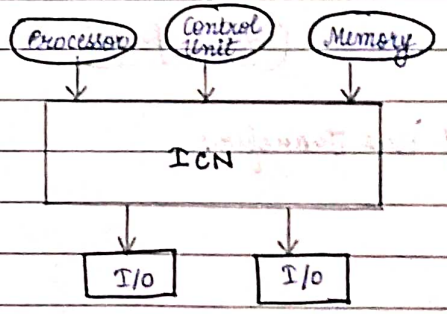
→ System Bus : 1) Address Bus
2) Data Bus
3) Control Bus

Memory $\xrightarrow[\text{operation}]{\text{Read}}$ Processor

Processor $\xrightarrow[\text{operation}]{\text{Write}}$ Memory

→ Registers : 1) MAR : Memory Address Register

2) MDR : Memory Data Register



• To perform Read and Write operations MAR and MDR are used.

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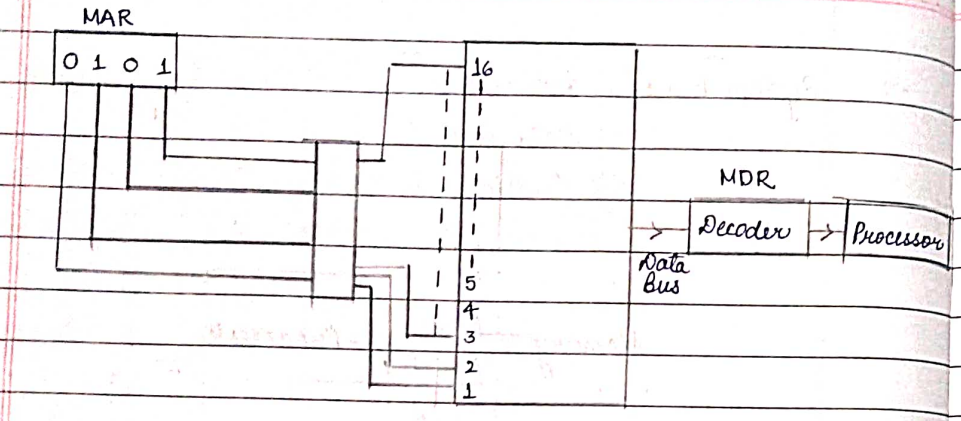
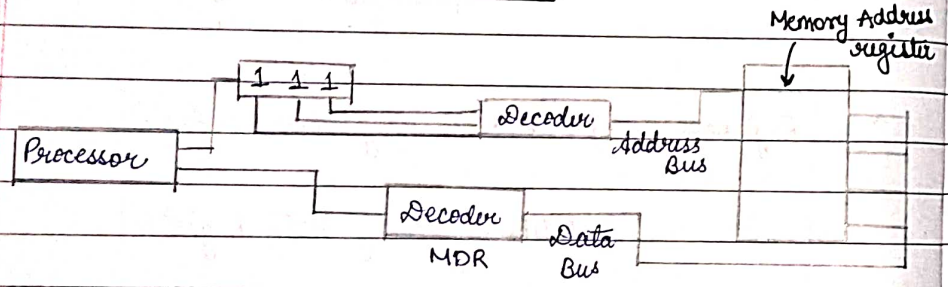


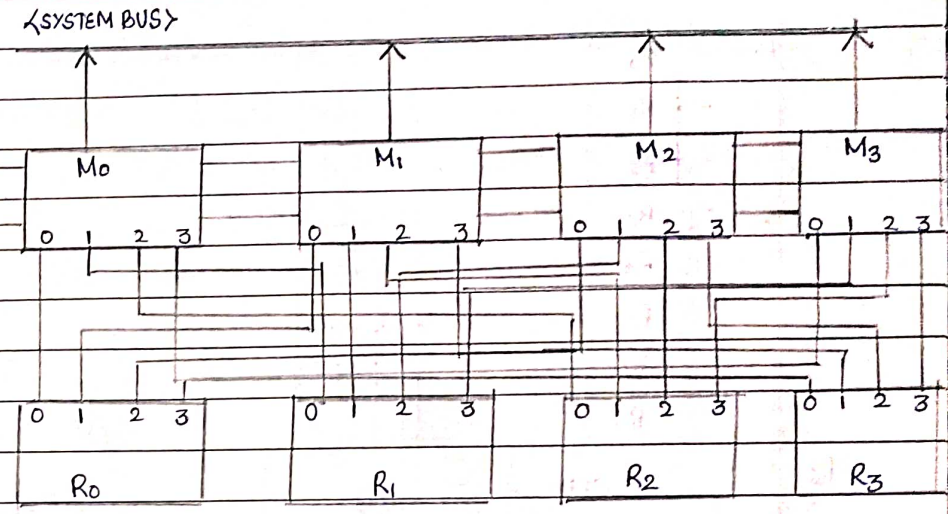
(Read operation)



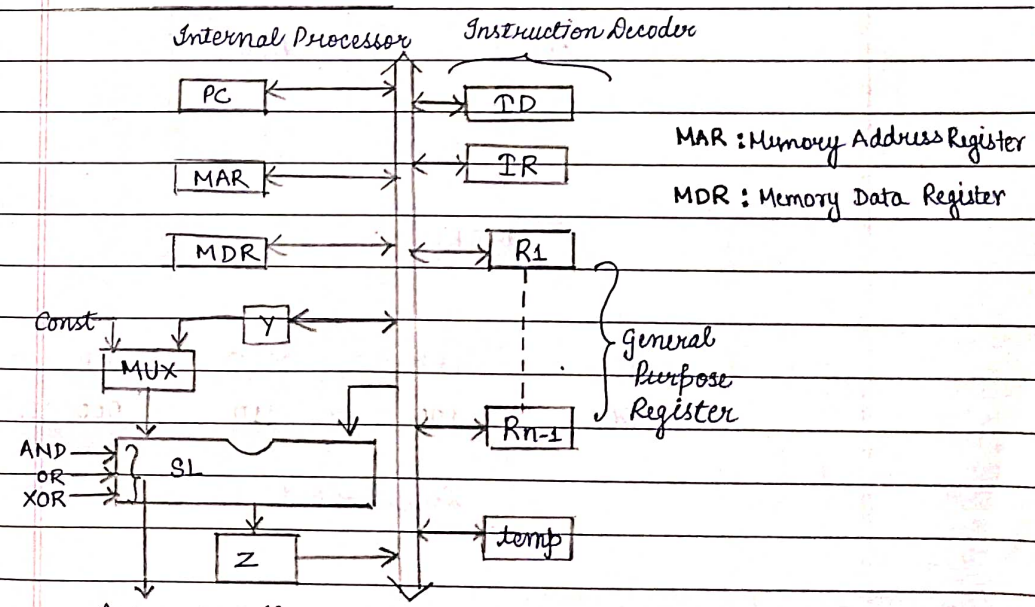
(Write operation)

Two Types of Bus Transfer:

a) By Multiplexer
b) By Decoder



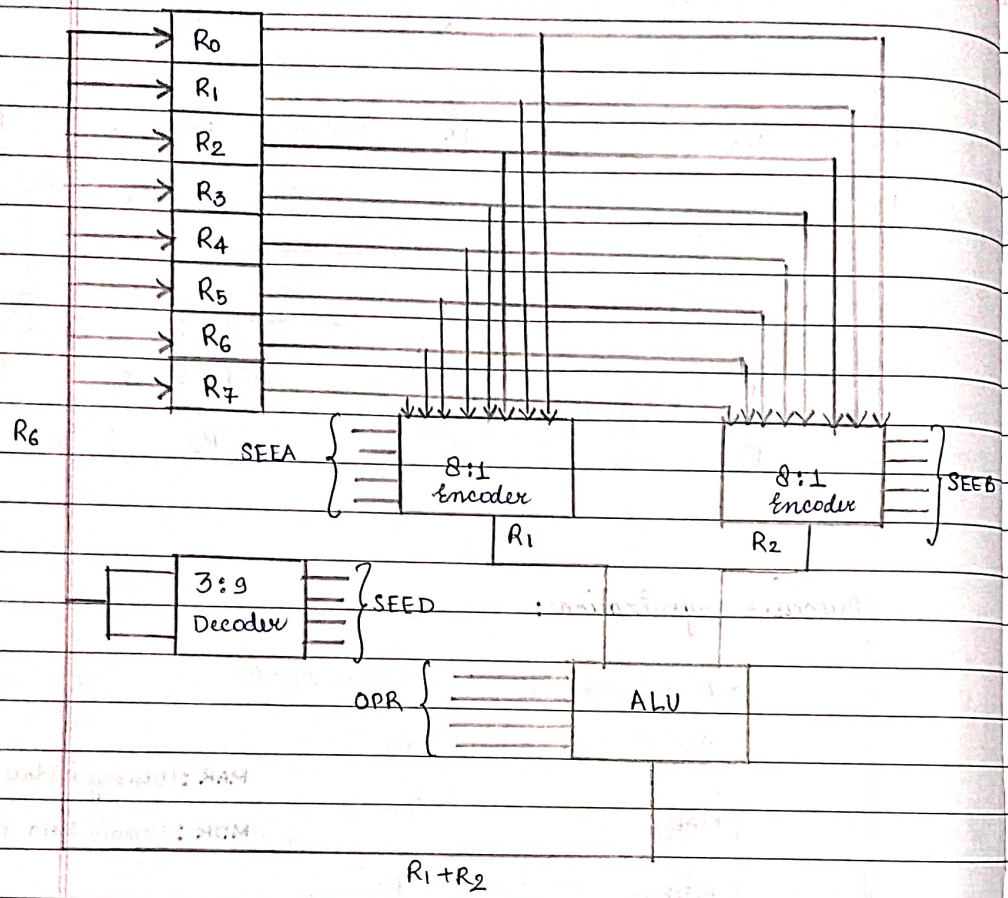
Processor Organization:



MAR : Memory Address Register

MDR : Memory Data Register

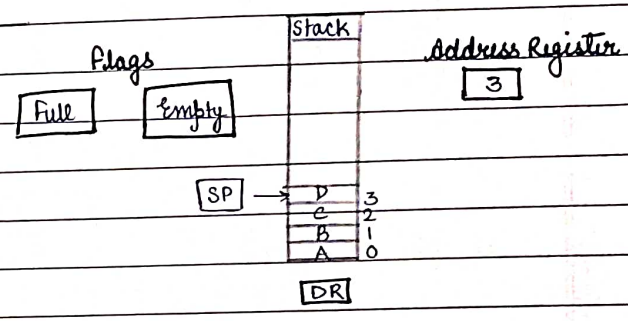
General Register Organization



SEEA	SEEB	SEED	OPR
001	100	110	000

Control Word

Stack Organization:



* Push operation:

1) SP ← SP+1
2) M[SP] ← DR
3) If SP=0; full ← 1
4) Empty ← 0

* Pop operation:

1) DR ← M[SP]
2) SP ← SP-1
3) If SP=0; Empty ← 1
4) full ← 0

Addressing Modes

* Immediate
* Direct
* Indirect
* Register Direct
* Register Indirect

Instructions: Combination of operations and operands.

* Number of subinstructions required to run an Instruction, are referred to as Microinstructions.