Pipeline in Computer Architecture

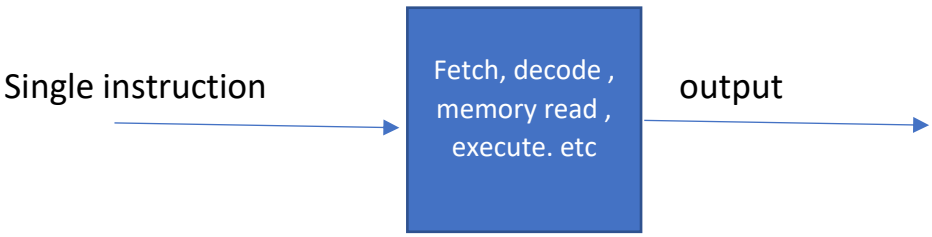
A program consists of several number of instructions. These instructions may be executed in the following two ways-

- Non-Pipelined Execution
- Pipelined Execution

Non-Pipelined Execution

In non-pipelined architecture,

- All the instructions of a program are executed sequentially one after the other.
- A new instruction executes only after the previous instruction has executed completely.
- This style of executing the instructions is highly inefficient.



Process stage

Assume we have four instruction in a program. If number of clock cycle for executing one instruction = 4 clock cycle and one clock cycle time is 3 sec, then-

Number of clock cycle required for execution of four instruction=4 x 4

= 16 clock cycle

CPU time= clock cycle x clock cycle time

Time taken for executing '4' instructions = 16 x 3=48 sec.

Pipelined Execution

In pipelined architecture, Multiple instructions are executed parallelly. This style of executing the instructions is highly efficient.

Instruction Pipelining- Instruction pipelining is a technique that implements a form of parallelism called as instruction level parallelism within a single processor.

A pipelined processor does not wait until the previous instruction has executed completely. Rather, it fetches the next instruction and begins its execution.

Pipelined Architecture-

In pipelined architecture,

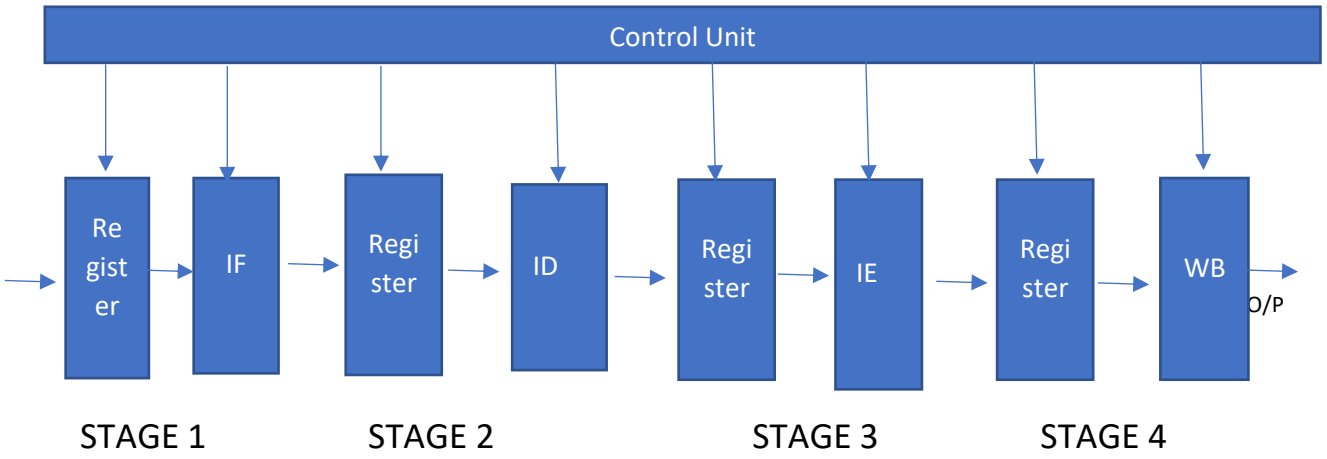
- The hardware of the CPU is split up into several functional units.
- Each functional unit performs a dedicated task.
- The number of functional units may vary from processor to processor.
- These functional units are called as stages of the pipeline.
- Control unit manages all the stages using control signals.
- There is a register associated with each stage that holds the data.
- There is a global clock that synchronizes the working of all the stages.
- At the beginning of each clock cycle, each stage takes the input from its register.
- Each stage then processes the data and feed its output to the register of the next stage.

Four-Stage Pipeline-

In four stage pipelined architecture, the execution of each instruction is completed in following 4 stages-

- Instruction fetch (IF)
- Instruction decode (ID)
- Instruction Execute (IE)

- Write back (WB)



Stage-1: First functional unit performs instruction fetch. It fetches the instruction to be executed.

Stage-2: Second functional unit performs instruction decode. It decodes the instruction to be executed.

Stage-3: Third functional unit performs instruction execution. It executes the instruction.

Stage-4: Fourth functional unit performs write back. It writes back the result so obtained after executing the instruction.

Assume four instruction in a program

I1

I2

I3

I4

Program execution

Clock cycle	CC1
WB	
IE	
ID	
IF	I1

Clock cycle	CC1	CC2
WB		
IE		
ID		I1
IF	I1	I2

Clock cycle	CC1	CC2	CC3
WB			
IE			I1
ID		I1	I2
IF	I1	I2	I3

Clock cycle	CC1	CC2	CC3	CC4
WB				I1
IE			I1	I2
ID		I1	I2	I3
IF	I1	I2	I3	I4

Clock cycle	CC1	CC2	CC3	CC4	CC5
WB				I1	I2
IE			I1	I2	I3
ID		I1	I2	I3	I4
IF	I1	I2	I3	I4	

Clock cycle	CC1	CC2	CC3	CC4	CC5	CC6
WB				I1	I2	I3
IE			I1	I2	I3	I4
ID		I1	I2	I3	I4	
IF	I1	I2	I3	I4		

Clock cycle	CC1	CC2	CC3	CC4	CC5	CC6	CC7
WB				I1	I2	I3	I4
IE			I1	I2	I3	I4	
ID		I1	I2	I3	I4		
IF	I1	I2	I3	I4			

In pipelined architecture,

- Instructions of the program execute parallelly.
- When one instruction goes from nth stage to (n+1)th stage, another instruction goes from (n-1)th stage to nth stage.

Assuming there are four instruction and one clock cycle time is 3 sec.

Number of clock cycle required to execute four instruction = 7 clock cycle

CPU time= clock cycle x clock cycle time

Time taken for executing ‘4’ instructions = 7 x 3=21 sec.

EXECUTING THE PROGRAM USING NON-PIPELINING

Program execution

Clock cycle	CC1	CC2	CC3	CC4	CC5	CC6	CC7	CC8	CC9	CC10	CC11	CC12	CC13	CC14	CC15	CC16
WB				I1				I2				I3				I4
IE			I1				I2				I3				I4	
ID		I1				I2				I3				I4		
IF	I1				I2				I3				I4			