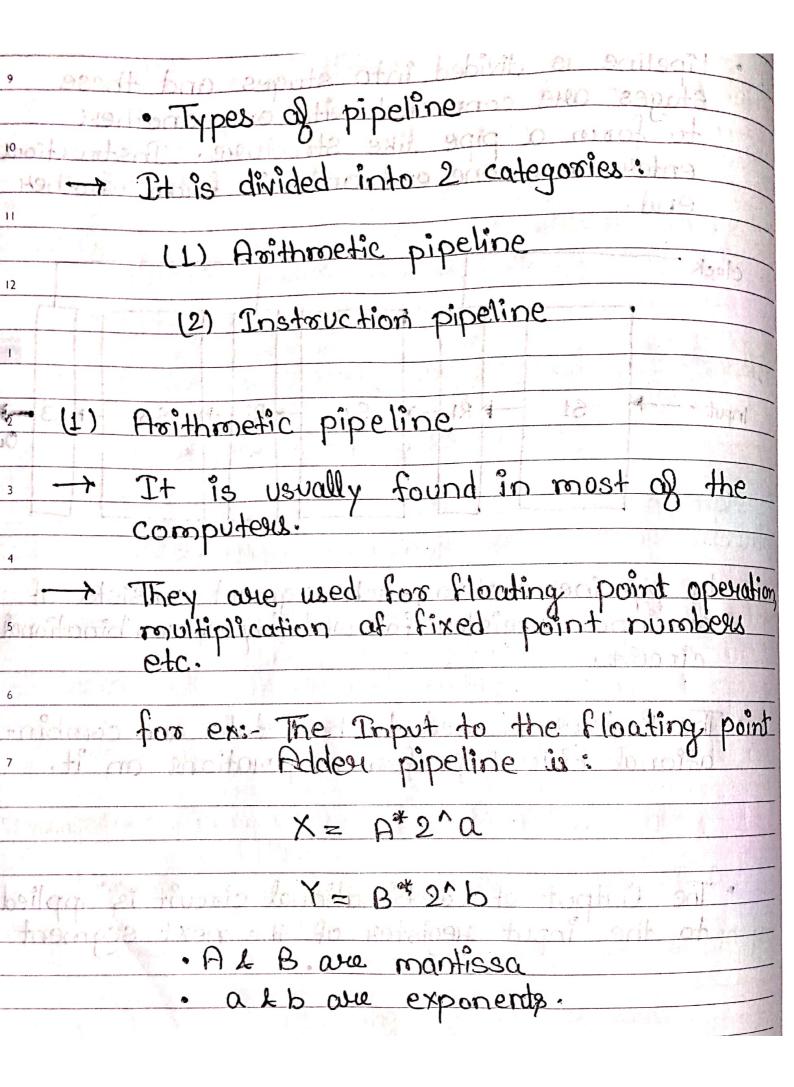
Pipeline is divided into stages and these stages are connected with one another to form a pipe like structure. Instructions enter from one end and exit from another end. clock S2 ₱ R3 R2 Input 51 N RI Output · In pipeline system, each segment consists of an input suggister followed by a combinational circuit. · The Register is used to hold data and combinational circuit performs operations on it. Sunday 17 · The Output of combinational circuit is applied to the input siegister of the next segment.



(2) Instruction pipeline
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a la thic chrosm of coetxuctions—cull De.
executed by overlapping fetch, decode
and execute phases of an instruction
executed by overlapping fetch, decode and execute phases of an instruction cycle.
This type of technique is used to increase the throughput of the computer System
the throughput of the computer System
almostered training and amiliarated of
-> An instruction pipeline neads instruction
from the memore while previous instruct.
ion are boing executed in other segments
An instruction pipeline heads instruction from the memory while previous instruction ion one being executed in other segments of the pipeline. Thus we can execute multiple instructions simultaneously.
or the pipeline. mos significations.
4 multiple instauctions should be
10 10 marco efficient if the
the pipeline will be 1810se Citicient
instruction cycle is divided into seguents
The pipeline will be more efficient if the instruction cycle is divided into segments of equal duration.
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Total expose the topically their was
Fresholisten tropers out good in
Pipeline Conflicts
WHO OB WAR
There are some factors that cause the

pipeline to deviate its normal performance. Some of these factors are given below:

1) Timing Variations

of time. This puroblem generally occurs in instructions have different operands steppendents and thus different processing time.

2) Data Hazards

when several instructions are in partial execution, and if they deference same data then the problem arises. We must ensure that next instruction does not attempt to access data before the current instruction, because this will lead to incorrect desults.

3) Breanching

instruction must know what that instruction is. If the present instruction is a conditional branch, and its result will lead us to the next instruction, then the next instruction may not be known until the current one is processed.

4) Interrupts

Interrupts set unwanted instruction into the instruction stream. Interrupts effect the execution of instruction.

5) Data Dependency

open the Hesult of a phevious instruction but this Hesult us not yet available.

