14.12.23

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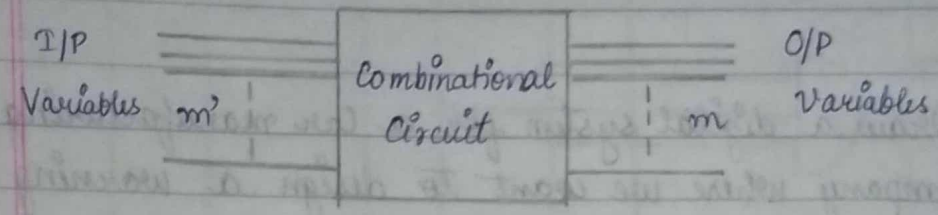
Unit: 2 Combinational and Sequential Circuit

Combinational Circuit:



- When logic gates are connected together to produce a specified output in certain specified combinations of Input Variables with no memory involved, then the resulting circuit is called combinational circuit.

- Output depends only upon present Input

- Combinational circuit performs operations that can be specified logically by a set of Boolean functions. A combinational circuit may have m' binary Inputs and m binary Outputs.
Example: Half Adder, Full Adder, Half Subtractor, Full Subtractor, Multiplexer, Demultiplexer, Encoder, Decoder (Code Convertor).

How To design Combinational Circuit:

- Analyse the given problem and identify number of Input and Output Variables.

- Write truth table based upon specification of problem.

- Convert Truth Table in Minimised Boolean Expression using K-Map.

11/9 - Draw Logic Circuit for the above obtained Output Expression.

Que Ques- Draw a digital system for a car manufacturing company where we want to design a warning signal for a car. There are 3 inputs: Lights of the car (a), Day or Night (b), Ignition on or off (c)

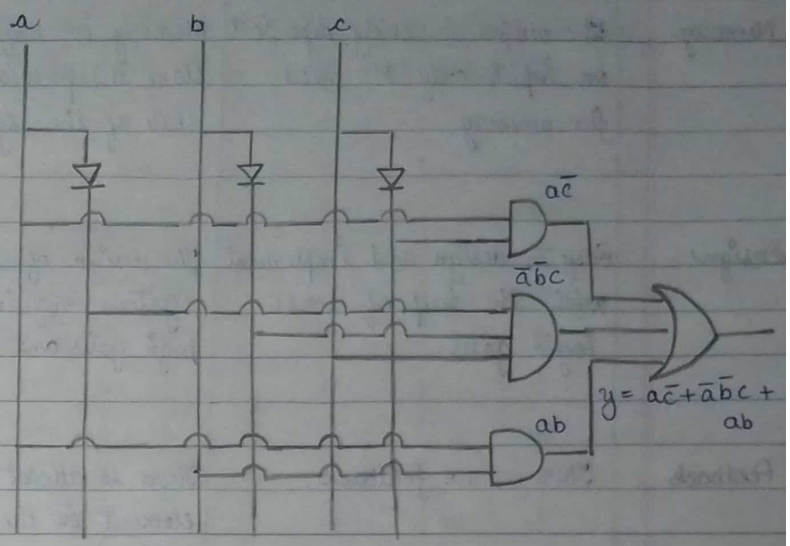
a	b	c	W
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

We have to minimize $\Sigma m(1, 4, 6, 7)$

a \ bc	00	01	11	10
0	0	1 (1)	3	2
1	1 (4)	5	1 (7)	1 (6)

Minimised Boolean Expression,

$y = a\bar{c} + \bar{a}\bar{b}c + ab$



Ques- Difference between combinational circuit and sequential circuit.

Parameters	Combinational Logic Circuits	Sequential Logic Circuits
Definition	At any instant of time, the output is only dependent on the current state of the inputs.	At any instant of time, the output is determined by inputs and previous outputs.
Time dependency	Time is not an important parameter	Time is an important parameter. For timing and synchronizing of different circuit elements, a clock signal is necessary.

Memory	The output is solely dependent on inputs only. No need for memory.	Memory is required to store the previous state of the system.
Design	Easy to design and implement with the help of basic logic gates.	The design of these systems requires basic logic gates and flip flops.
Feedback	There is no feedback.	There is atleast one memory element in the feedback path.
Hardware & Cost	They are easier to implement but costly, due to hardware. This implementation requires more hardware.	They are difficult to implement but less costly than sequential circuits.
Speed	They are faster since all inputs are applied at the same time.	They are slower, because of the secondary inputs. So, there is a delay in between inputs. And the output is gated by a clock signal.

Ques- Design a digital system where output is 1 only when the input variable is greater than 100.

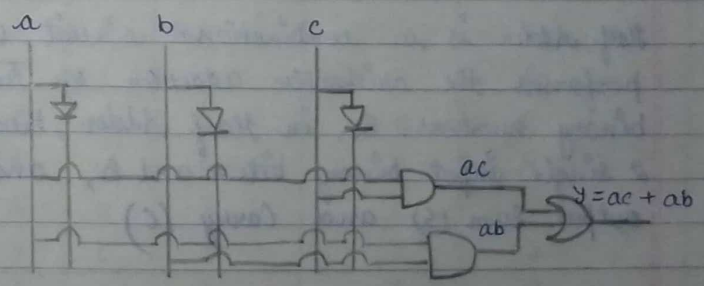
a	b	c	Output
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

We have to minimize $\Sigma m(5,6,7)$

a \ bc	00	01	11	10
0	0	1	3	2
1	4	1 (5)	1 (7)	1 (6)

Minimized Boolean Expression is,

$$y = ac + ab$$



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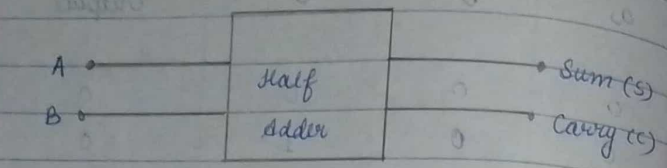
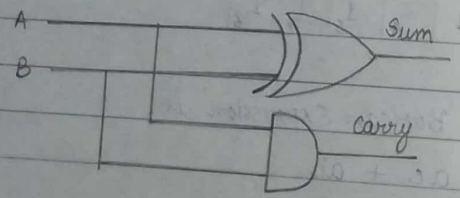
Half Adder :-

Block Diagram of Half Adder;



Truth Table :-

Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



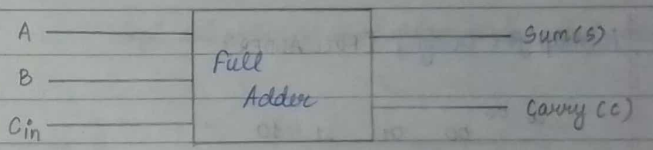
Half Adder is a combinational circuit, which performs the arithmetic addition of two 1 bit binary numbers. So, in Half Adder, there are 2 single input binary bits A and B, and two output Sum (S) and Carry (C)

Full Adder :-

Full Adder is a combinational logic circuit that performs the arithmetic sum of 3 input bits.

When A_n and B_n are the nth order bits of A & B respectively, and C_{in} is the carry generated from the addition of (n-1) th order bits. It consists of 3 input bits denoted by A (first operand), B (second operand), C_{in} (represent carry from the previous lower significant position).

Block diagram of Full Adder :

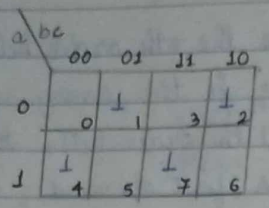


Truth Table :

Inputs			Output	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

NOTE: Half Adder :- (Works on 2 inputs) Full Adder :- (Works on 3 inputs)

K map for Sum ; [FULL ADDER]



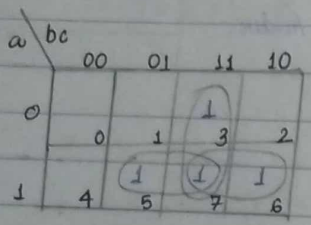
$= a\bar{b}\bar{c} + \bar{a}\bar{b}c + abc + \bar{a}b\bar{c}$

$= \bar{a}(\bar{b}c + b\bar{c}) + a(\bar{b}\bar{c} + bc)$

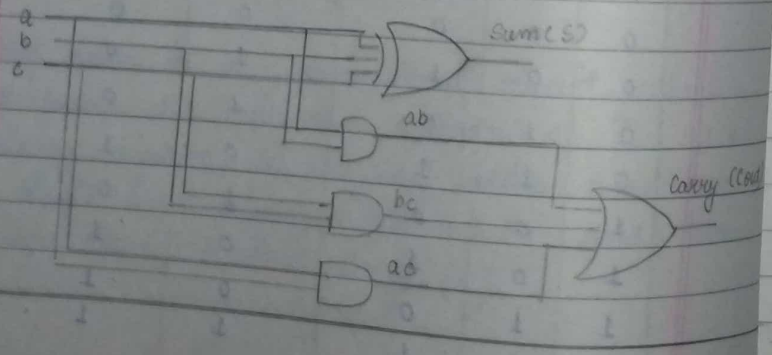
$= \bar{a}(b \oplus c) + a(\overline{b \oplus c})$

$= a \oplus b \oplus c$

K map for Carry ; [FULL ADDER]

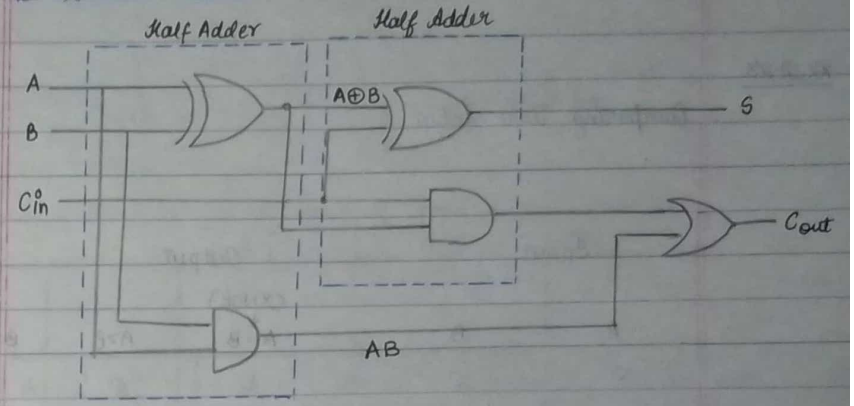


$= ab + bc + ac$

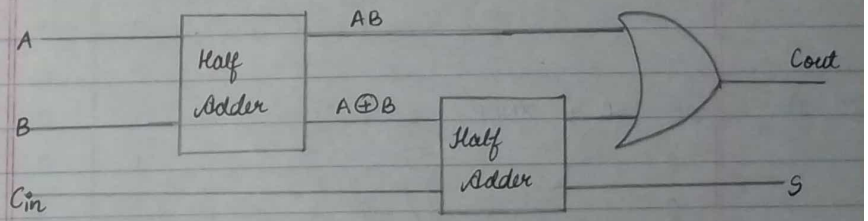


Ques) Design a Full Adder using the half adder.

The logic diagram of the full adder using two half adders is shown below:



Logic Diagram of Full Adder using Half Adder



Block diagram of Full Adder using Half Adder

From the logic diagram, it is clear that we require two XOR gates, two AND gates and one OR gate for the implementation of a full adder circuit using Half adders.

However, the implementation of full adder using half adder has a major disadvantage that is increased

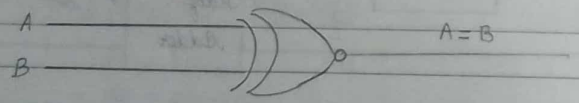
propagation delay. That means, the input bits must propagate through several gates in succession that increases the total propagation delay of the full adder circuit.

22.12.23

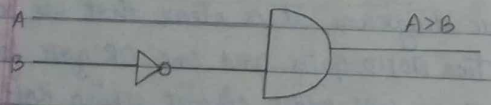
Comparing Two input

Input		Output		
		(XNOR) ↓		
A	B	A=B	A>B	B>A
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

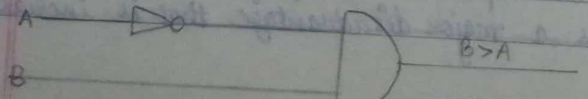
1) For A=B ; XNOR



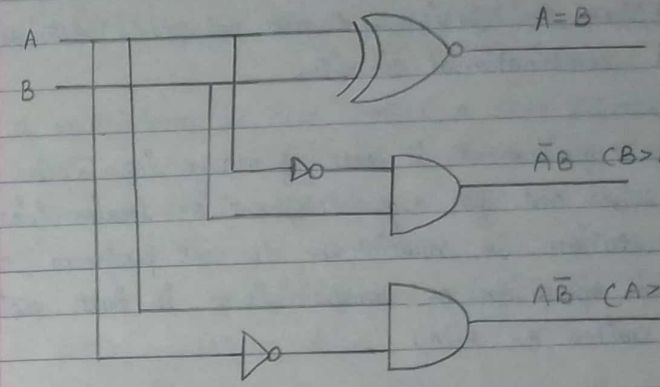
For A>B ; $A\bar{B}$



For B>A ; $\bar{A}B$



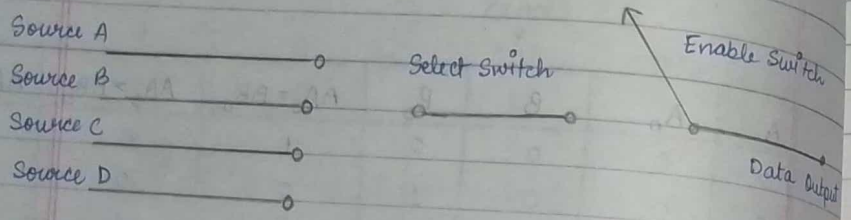
2) For 4 input :- (2 input compared to 2 output)



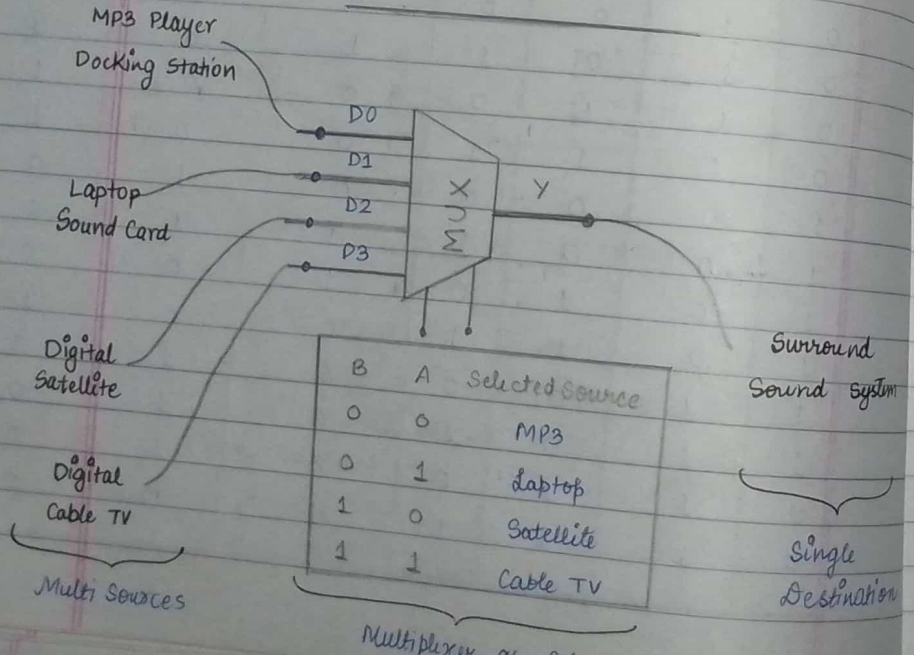
A	A_0	B	B_0	$AA_0 = BB_0$	$AA_0 > BB_0$	$AA_0 < BB$
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	1	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

Multiplexer (Selector):

- Multiplexer are special and one of the most widely used combinational circuits.
- Main requirement is out of many inputs we have to select one for e.g. telephone or train leaving the station. So, multiplexer do not perform any logical operation or comparision, it just acts as a switch or relay.



Applications of Multiplexer



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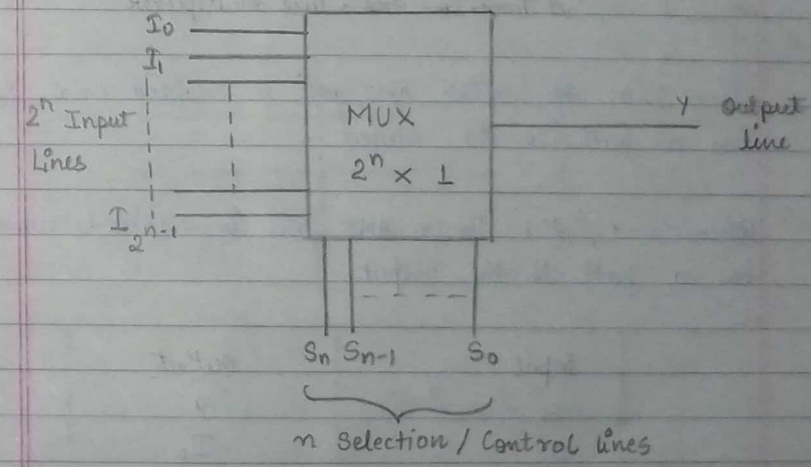
- A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line.
- A multiplexer is also called a data selector, since it selects one of many inputs and steers the binary information to the output line.
- The selection of a particular input line is controlled by a set of selection lines.
- There are 2^n input lines and n selection lines whose bit combinations determine which input is to be selected.
- No. of input line = $< 2^n$



Multiplexer

Note: Can never have two input connected to out at a time.

1119.2

Application:

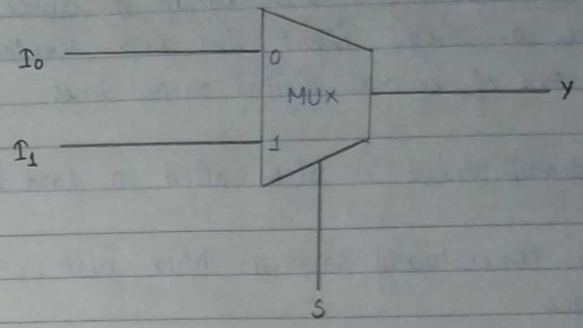
- Parallel data to serial data conversion.
- Used as data selector, as the output of a multiplexer is directed from one of various inputs.
- Used in Implementation of Boolean functions
- Used in Communication Systems, Computer Memory, Telephone Network, Transmission from the Computer System of a Satellite.

A two-to-one-line multiplexer

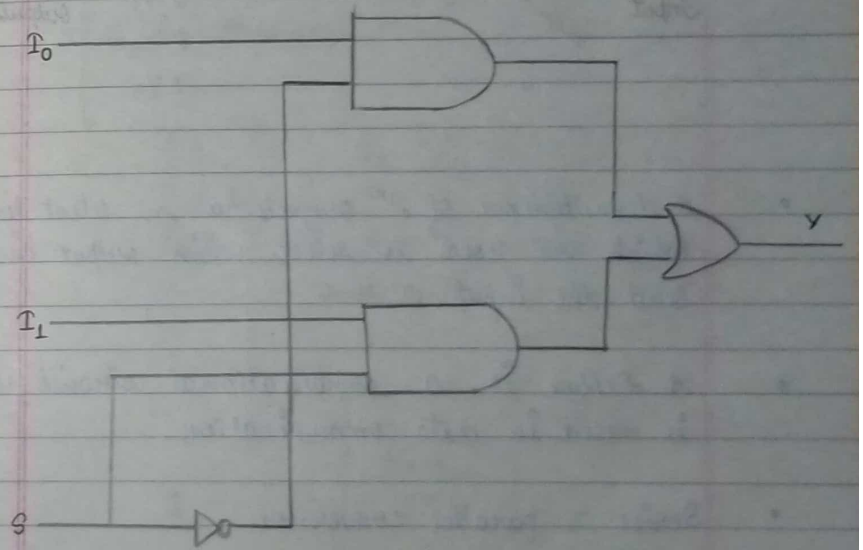
- When S=0, the upper AND gate is enabled and I_0 has a path to the output
- When S=1, the lower AND gate is enabled and I_1 has a path to the output.

Input S	output Y
0	I_0
1	I_1

Characteristic Equation : $Y = S_0'I_0 + S_0I_1$



Block Diagram

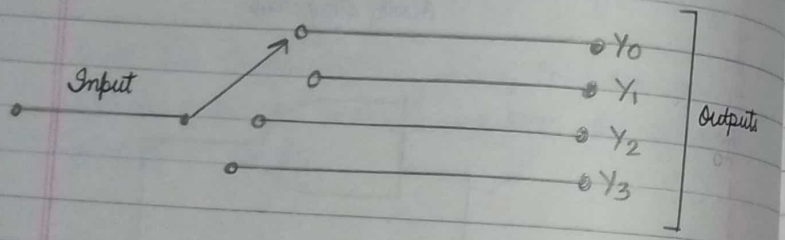


Logic Diagram

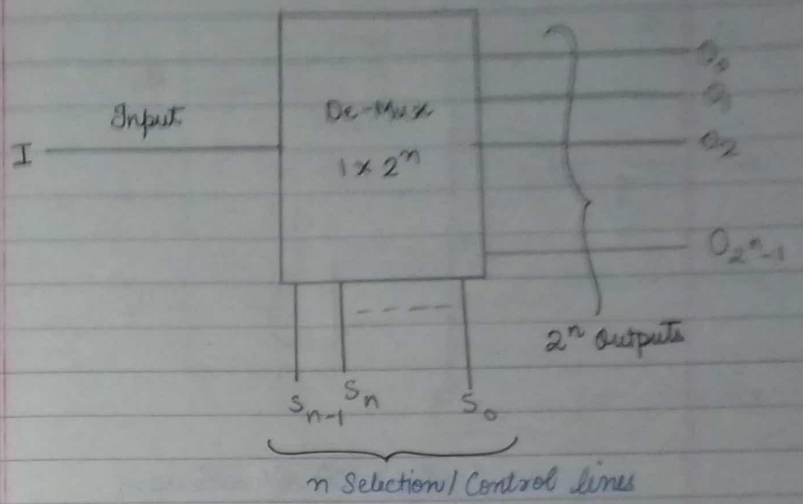
28.10.23

Demultiplexer

- A demultiplexer (or Demux) is a device that takes a single input line and routes it to one of several digital output lines.
- A demultiplexer is also called a data distributor.
- It is conceptually same as Mux just with reverse logic.



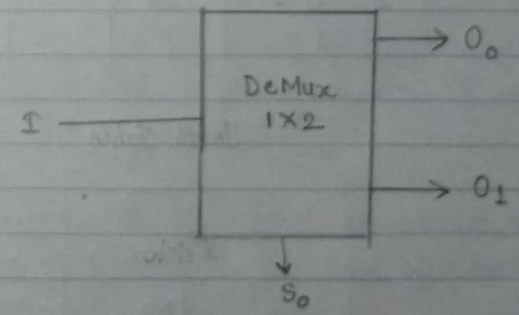
- A demultiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input.
- A DeMux is a combinational circuit, which is used in data communication.
- Series to parallel conversion.
- Demultiplexers are mainly used in Boolean function generators and decoder circuits.



1 to 2 Demultiplexer

S_0	O_1	O_0
0	0	1
1	1	0

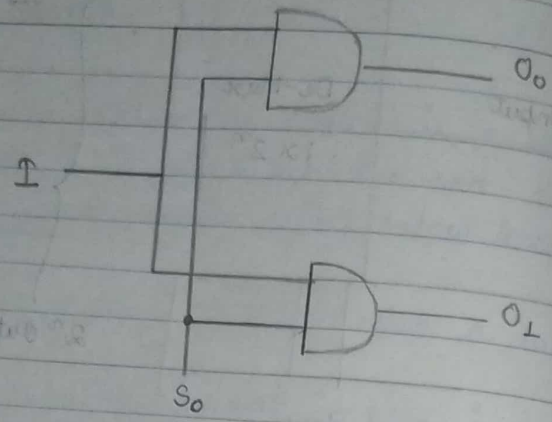
Truth Table



Block Diagram

11.9.2

Ques

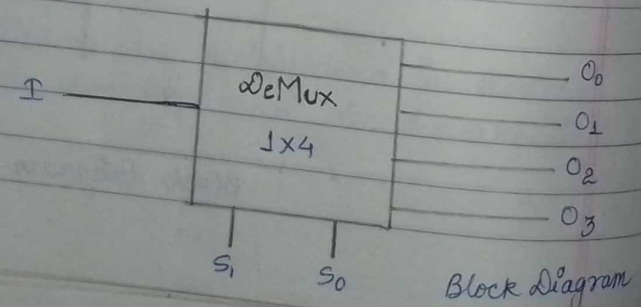


Logic Circuit Diagram

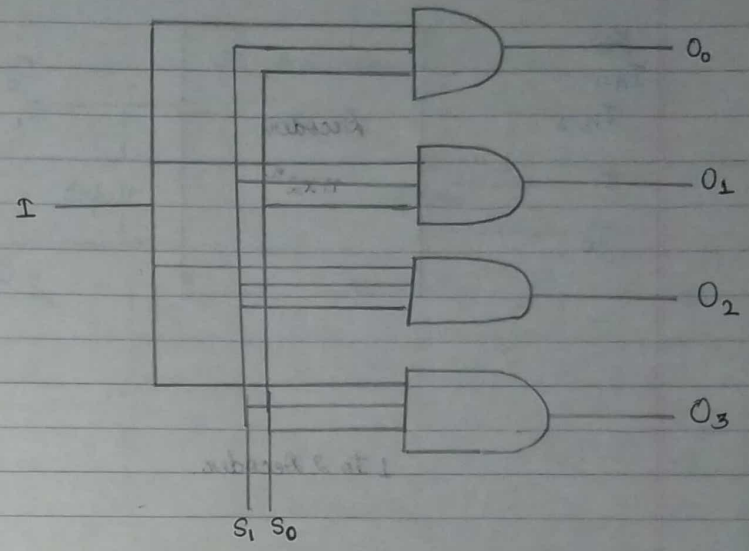
1 to 4 Multiplexer :

S_1	S_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Truth Table



Block Diagram

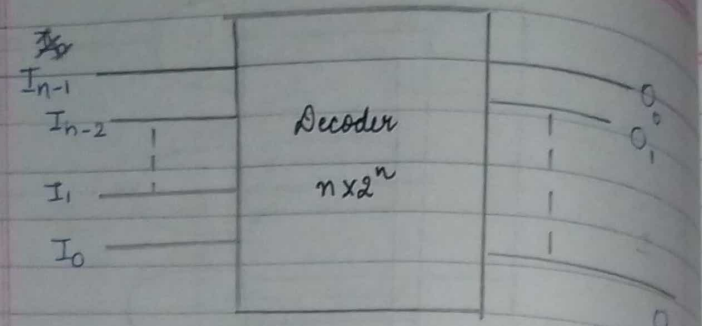


Logic Circuit Diagram

04.1.24

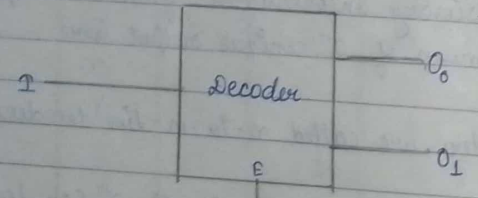
Decoder : • A decoder is a combinational circuit that decodes binary information from n input lines to a maximum of 2^n unique output lines.

- The decoders are called n-to-m-line decoders, where $m \leq 2^n$
- Their purpose is to generate the 2^n (or fewer) minterms of n input variables Each combination of inputs will assert a unique output
- If the n-bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.

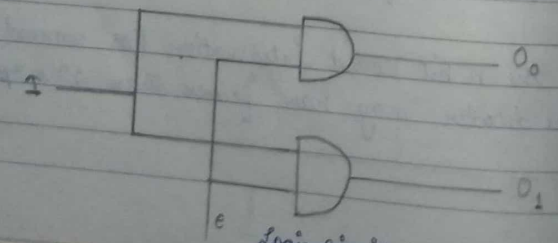


1 to 2 Decoder.

I	O_1	O_0
0	0	1
1	1	0



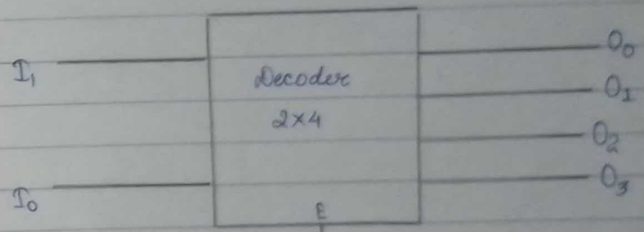
Block Diagram



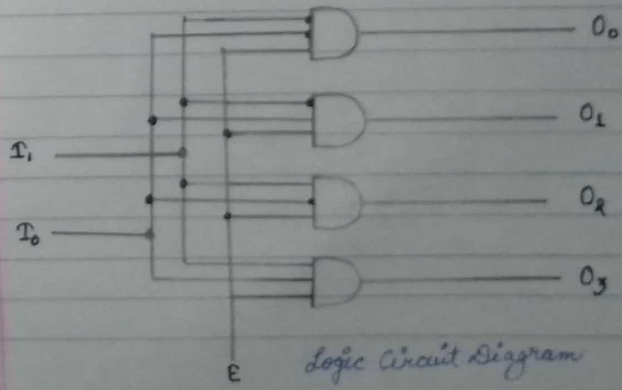
Logic Circuit Diagram

2 to 4 Decoder

Input		Output			
I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



Block Diagram



Logic Circuit Diagram