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Unit:2 (Detailed Notes)

Fixed and floating point sufousentation: They are the nuthods. Used in arithmetic and logic units to handle numerical data in digital systems.

- (1) fixed Point Representation: Numbers are supresented with a fixed number of integer and fractional bits.
 - format: For example, in a 16 bit fixed point format with. 8 integer bits and 8 fractional bils, the range might be from -128 to 127.9999
- · Arithmetic Operations: fixed-point arithmetic operations Involve simple integer arithmetic, followed by scaling to adjust for fractional parts.
 - Poros: · Simple to implement en Hardware.
 - and precision requirements -
- * Cons: · Linuted dynamic range and precision.

 · Can lead to loss of precision or overflow/ emduflow errors in calculations involving very large or very small numbers.

- Desting Point Representation: In floating point superesentations numbers are superesented as a combination of a sign bit, exponent and mantissa (fraction)
 - · Format: Typically follows the IEEE 754 Standards with diffui prucision operations like Single Precision (32 bil) or double precision (64 bits)
- Aruthmetic operations: Floating point aruthmetic Involves complex operations to handle normalization, rounding, and exponent manipulation.
- e Pros: Offers a wide dynamic range and precision, Suitable for scientific and engineering applications.
- · Allows representation of very large and very small numbers with reasonable precision.
- · Cons: More Complex to implement in Hardware compared to fixed point arithmetic
- Requires additional processing time and resources for operations like normalization and rounding

and an over many and the series (the second of the contraction of the second of the se	IEEE Standards for floating point supresentation;
	Single Precision Format (32 bits)
)	Sign bit: I bit (Represents the sign of the number, 0 for positive and 1 for negative).
2)	Exponent: 8 bits (Represents the exponent of the floating point number in blased form).
3)	Significand (Mantissa): 23 bits (Represents the foractional. Part of the floating point number.
*	Double Precision Format:
1)	Sign bit: 1 bit
2)_	Exponent: 11 bit
<u>á)</u>	Significand (Mantissa) 59 bits
	The same of the sa
	Standard features: 1) Normalized Numbers
	2) Exponent Bias
	z) Special Values
	4) Rounding Modes
Photodesia shipsendapan dala salamba	5) Avithmetic Oberations.

Booth's Algorithm: It is a multiplication algorithm that efficiently multiplies two signed binary numbers using a Sequence of addition and shifting operations. Process: a) Represent the 2 numbers in Signed binary format Divide one of the numbers ento groups of adjacent bits. Apply a series of addition & shifting operations based on the bit pattern of the other number. Advantages: Requires fewer arithmetic operations
compared to traditional methods, especially for large Suitable for hardware implementation en digital circuits due to sugular and repetitive Structure Désaduantages: · Complexity increases with the Size May require additional hardware ensources for implementation in hardware circuits.

Array Multiplier: It is a hardware Implementation of multiplication that utilizes an array of address and Shifters to perform the multiplication operation.

Process: a) Represent the 2 numbers to be multiplied in binary format.

- b) Organize the bite of one number into yours of a matrix
- c) Organize the bete of the other number into columns of the same matrix.
- d) Perform a series of partial products to obtain the final result by adding them.

Advantages: · Can handle wide input sizes.

· Provides a straightforward Pmplementation in hardware using adders & shifters.

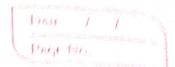
Disadvantages: Requires large numbers of adders & shifters.

Elower for large operands.

	Components of ALV Design: 1) Avithmetic Unit: Handles
	arithmetic operations -
B	consists of circuits for performing binary addition - and subtraction using carry propagate or carry -
	and subtraction, wing carry brippagate or carry -
	LEEK II WUU TERUNIOUUS.
0	Multipliers and déviders may also be liveleded en multiplication and dévision operations.
	multiplication and division oberations.
	그 나는 그 그 그 그 그 그 그 그 그는 그는 그는 그는 그는 그는 그는 그
2)	Logic Unit: · AND, OR, NOT, XOR. are performed by
	dogic Unet
0	Utilizes Logic Gatu (AND, OR, NOT) to perform oberations
	Utilizes Logic Gates (AND, OR, NOT) to perform operations on binary data.
3)	
)	Control Unit: Decodes instructions fetched from memory
	and generales control signals to coordinate the activities
	and generales control signals to coordinate the activities of ALU.
<u> </u>	
	Determines which operation to have
	instruction of code and operands.
k 1, s. (4).	THE STATE OF THE S
4)	Registers: o Holds oberande Port
	Registers: o Holds operands, Intermediate results, and operation flags during ALU operations.

Includes GPRs, used for storing data and special purpose. sugisters for storing data and special flags and control operations. Design Consideration: (1) Speed: ALU operations should be executed quickly to minimize overall processing time. Precision: ALU should provide accurate results. Flexibility: Al U design should support a wide range of operations and data types 4 Power Efficiency: Power Consumption should be energy efficient. Implementation Jechniques: 1/2 Combinational Logic: Basic operations are perforemed by combinational logic circuits.

2/2 Sequential Logic: More complex ALU designs include flip flops and state machines. Parallelism: By processing multiple operations simultaneously by using parallel adders, multipliers and pipelined execution. Hardware Accelaration: Hardware Accelarators like floating point units (FPUs) and Vector Processing



units (VPU's) maybe included to accelerate authorities

Modern Trends:

- 1) Vector Processing: ALUS optimized for Vector operations are used in Scientific Computing and Graphic procusing.
- 2) Customization: ALU duigns can be customized for specific applications and architectures.
- Heterogeneous Computing: ALUS are integrated ento heterogeneous computing systems alongside after specialized processing units like GPVs, TPVs and accelerators to liverage their respective strengs for different types of computations.