ADITYA SARIPALLI

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Have 12 years of experience in software industry across Systems Software / Firmware development, NMS/EMS (Network/Element Management Systems) and Telecom Billing.

ACADEMIC QUALIFICATION

- Bachelor of Technology (in Electronics and Communication Engineering) from Jawaharlal Nehru Technological University, Hyderabad, April 2006. Grade Achieved – 72%.

- Currently pursuing masters from International Institute of Information Technology, Hyderabad (Part Time).

PATENTS AND PUBLICATIONS

Wrote a patent titled – "PCIe Link Reset to Minimize Workload Impact", patent application "US 15/343194" – which got filed at United States Patent and Trademark Office in November 2016.

Brief Description: The core idea of this invention is to perform an abbreviated PCIe bus IPL (Initial Program Load) which restore a PCIe link to the maximum width and speed and return recoverable EEH (Enhanced Error Handling) events to device drivers attempting to perform I/O operations to devices connected by the PCIe link during the IPLs.

PROFESSIONAL EXPERIENCE

IBM India Systems Development Labs, Hyderabad **(Dec 2012 – Present)**

Designation: Senior Staff Software Engineer

Product: PHYP (Power Hypervisor)

Tools and Technologies: C/C++, Perl, I2C, PCIe 3.0/4.0, LPC (Low Pin Count), CMVC, Linux/AIX, Jenkins, DevOps, Simics, Git, GitHub, OpenBMC.

Brief Description: PHYP is the lowest layer of firmware that runs on the host processors to provide virtualization services to higher layers of software (operating systems), by virtualizing physical resources like Memory, Processors and I/O (Input/Output). Higher level functions such as system error reporting, logical partition management, and hardware error detection and recovery are also a part of the PHYP.

Individual Role:

- Understanding I2C, PCIe and LPC protocols. Developing firmware for PHB (PCIe Host Bridge), Switch, I/O Controller, Platform, I/O Expansion Drawers and SPCN (System Power Control Network).
- Involved in the firmware development of major IBM Power8 system offerings (Tuleta, Brazos, and Brazos with PCIe 3.0 I/O Expansion Drawer) and Power9 open power systems offerings (Barreleye and Habanero).
- Currently working on the firmware development of enterprise Power9 systems offerings, PCIe 4.0 I/O Expansion Drawers and CAPI (Coherent Accelerator Processor Interface).
- I am also involved in open source contribution towards OpenBMC firmware stack development for the IBM OpenPOWER systems offerings like Witherspoon.

TATA Consultancy Services Ltd, Hyderabad (Apr 2010 – Nov 2012)

Designation: Information Technology Analyst

Project #1: NetViewer

Client: Nokia Siemens Networks (NSN), Milan, Italy.

Duration: 24 months

Tools and Technologies: C/C++, Python, Subversion, TortoiseSVN, Linux, MIB Browser, SNMP (Simple Network Management Protocol), UDP, Jenkins, CppUnit, OpenHPI.

Brief Description: NetViewer is an Element Management System (EMS) used to manage the Microwave transport network elements in FCAPS (Fault, Configuration, Accounting, Performance and Security) model.

Individual Role:

- Responsible for developing plug-ins for any new network element launched by the NSN as part of SNMP plug-in development team, by analyzing MIB files, functional specifications and other technical documents of the network elements.
- Responsible for managing Fault, Performance and Security tasks of FCAPS model through the plugins.
- Travelled to NSN, Milan, Italy (May - July 2011) to work on plugin-development of the newly arrived network element FPH800 (Flexi Packet Hub 800).

Project #2: LTE Simulator

Client: Qualcomm India Private Limited

Duration: 8 months

Tools and Technologies: C/C++, Subversion, Linux, Wireshark, TCP/IP, UDP, CppUnit.

Brief Description: LTE simulator is developed against the 3GPP-36 series release-9 specifications – 36.321(MAC), 36.322(RLC), 36.323(PDCP) and 36.331(RRC). The simulator is developed for simulating the protocol stack on both UE (User Equipment eg: Mobile) and eNodeB (Evolved Node B) sides. All the features implemented in the simulator are tested using the network protocol analyzer – Wireshark.

Individual Role:

- Development of LTE - L2/L3 stack framework consisting of MAC (Medium Access Control), RLC (Radio Link Control) and PDCP (Packet Data Convergence Protocol) layers on both UE and eNodeB sides. My contribution was on implementing the RLC layer.
- Implemented data transmission and reception procedures in TM (Transparent Mode), UM (Un-Acknowledged Mode) and AM (Acknowledged Mode) modes for RLC layer.
- TM: Transmission and reception procedures between the peer RLC entities (UE & eNodeB).
- UM & AM: Segmentation and concatenation procedures on the transmission side, re-assembling and re-ordering procedures on the receiving side.

Convergys IMG India Pvt Ltd, Hyderabad (Jul 2006 – Mar 2010)

Designation: Associate Programmer / Analyst

Product: Infinys Rating and Billing (IRB)

Tools and Technologies: C/C++, Perl, Clearcase, Linux, Valgrind, Bullseye, Oracle 10g, PL/SQL Developer, Toad.

Brief Description: IRB is a convergent Rating and Billing system designed to work with a range of goods and services, in which usage is metered and events are billed. I was part of the Rating Subsystem.

Individual Role:

- Designed and developed volume processing applications like Terminated Account Deleter, Managed File Modifier, RATE Dispatch Plug-in, and Bill Post Processor.
- Travelled to Ankara, Turkey (November 2008 - January 2009) and Riyadh, Saudi Arabia (November – December 2009) for migration/upgrade activities and technical assistance of the product.

POSTER PRESENTATIONS

- Presented a poster titled, "MEX as a Next Generation IO Drawer" at the Regional Technical Exchange event conducted by IBM India Research Labs, and held at IBM Hyderabad (September 2015).
- Exhibited a poster on 'Virtualization in Power Systems' in the technical paper presentation event conducted by the IBM Systems Group, Bangalore and held at IBM Hyderabad (April 2015).

CERTIFICATIONS AND TRAINING

- Algorithms: Design and Analysis, Part 2 by Stanford University on Coursera - September 23, 2016. Grade Achieved 98%.
- Algorithms: Design and Analysis, Part 1 by Stanford University on Coursera - July 31, 2016. Grade Achieved 96%.
- Trained on PCIe 3.0 and IBM Power systems firmware development – by IBM India Systems Development Labs, Hyderabad (January 2013 - February 2013).

AWARDS AND ACHIEVEMENTS

- Received "First Patent Application" award from IBM, in November 2016.
- Received "Certificate of Excellence" for delivering RAS (Reliability, Availability and Serviceability) features in Power8 and Power9 firmware releases, from IBM Enterprise Systems Development, in April 2016.