



Gateway Classes

**Semester -III****CS IT & CS Allied Branches****BCS302- COMPUTER ORGANIZATION AND ARCHITECTURE**

UNIT-1 : Introduction

Hand Written Notes



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BCS302- COMPUTER ORGANIZATION AND ARCHITECTURE

Hand Written Notes

Unit-1

Introduction

Syllabus

Introduction: Functional units of digital system and their interconnections, buses, bus architecture, types of buses and bus arbitration. Register, bus and memory transfer. Processor organization, general registers organization, stack organization and addressing modes.



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COMPUTER ORGANIZATION AND ARCHITECTURE

UNIT 1

Difference between computer Architecture and computer Organization. [AKTU 2020-21]

COMPUTER ARCHITECTURE

- Architecture describes what the computer does.
- It deals with the high-level design issues.
- Computer Architecture deals with the functional behaviour of computer systems.
- Architecture indicates its hardware.

COMPUTER ORGANIZATION

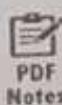
- The organization describes how computer does it.
- It deals with low-level design issues.
- Computer organization deals with a structural relationship.
- Organization indicates its performance.

FUNCTIONAL UNIT OF DIGITAL SYSTEM

[AKTU 2019-20 / 2022-23]



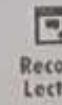
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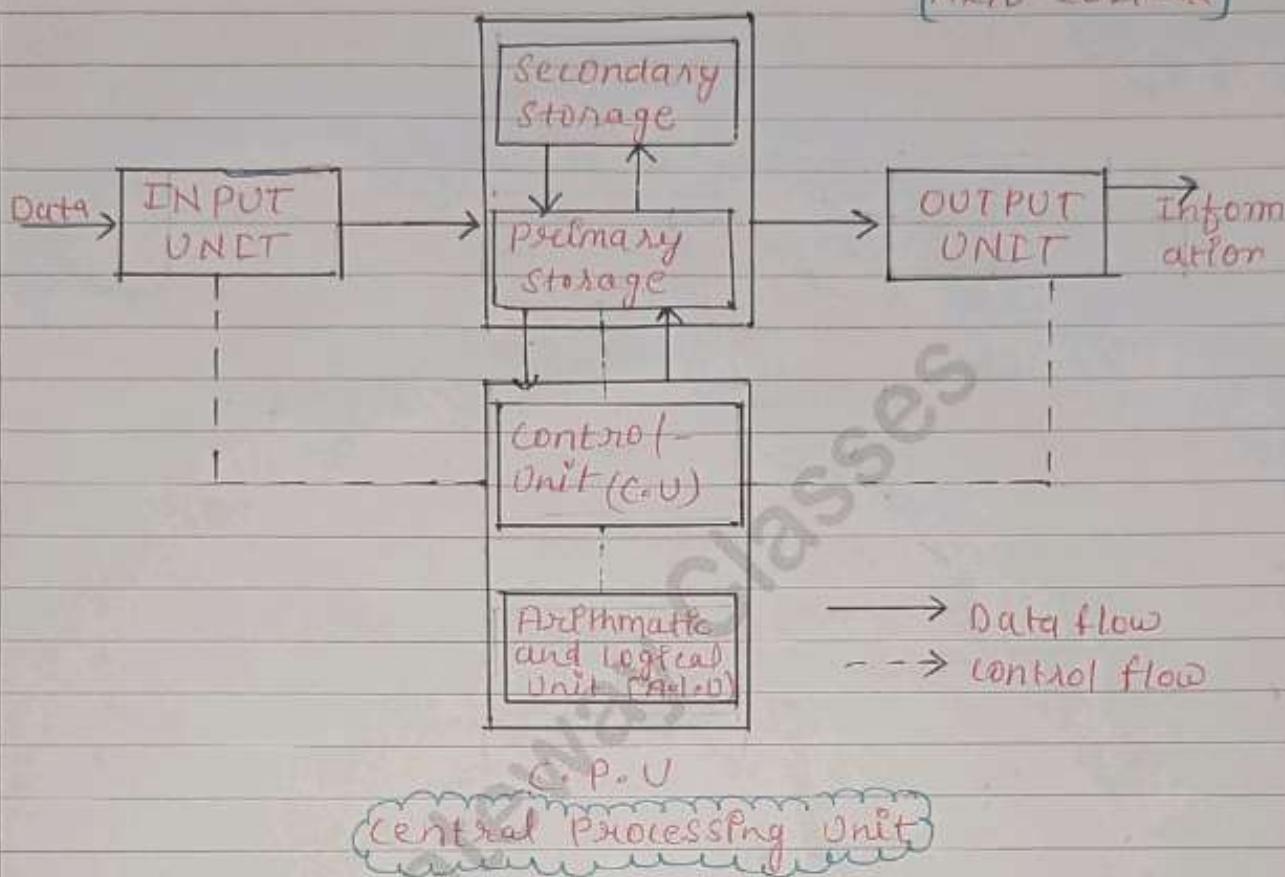
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Main structural Components of the computer system

[AKTU 2021-22]

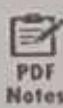


INPUT UNIT:-

- We need to first enter the data & instruction in the computer system, before any computation begins.
- This task is done by the input devices. (Keyboard, mouse, scanner, digital camera).



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computer system structural components :-

- INPUT Unit
- STORAGE Unit
- Arithmetic Logical Unit [ALU]
- control Unit [CU]
- OUTPUT Unit

OUTPUT UNIT:-

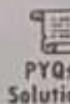
- Output unit accepts the results produced by the computer in coded form. [Low level language].
- It converts these coded results to human readable form.
- It displays the converted results to the outside world with the help of output devices [Monitors, Printers, Projectors].

STORAGE UNIT:-

- This storage unit is designed to save the initial data, the intermediate result and the final result.
 - ① Primary storage (Main memory)
 - ② Secondary storage (Auxiliary storage)



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1. Primary Storage [Main Memory]:-

- It is the computer memory that a processor or a computer accesses first or directly.
- faster access speed.
- It is of two types RAM and ROM.
- Smaller storage capacity.

1.1 RAM [Random Access Memory]

- Volatile (loses data when power is off)
- It is also known as Read/Write Memory.
- Used for temporary data storage and quick access by the CPU.
- RAM are of two types ① SRAM → Static RAM
② DRAM → Dynamic RAM

1.2 ROM Read Only Memory

- Non-Volatile (It can retain data when power is off)



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- ROM provides the necessary instructions to load the Operating System from Secondary storage into RAM during the boot process.
- ROM holds the data that doesn't need to be modified, such as system-level instructions, bootstrapping data or default settings.

TYPES OF ROM → 1. PROM
2. EEPROM
3. EEPROM

① PROM → Programmable Read Only Memory

- PROM is a Non-Volatile chip.
- It is PROM chips to write data once and can read data many times.
Once chip programmed, recorded information can't be changed.

② EPROM → Erasable Programmable Read Only Memory.

- EPROM chip can be programmed time and again by erasing the information stored earlier in it.
- Information stored in EPROM exposing the chip for some time Ultra violet light (U.V).

③ EEPROM → Electrical Erasable Programmable Read - Only Memory.

- The EEPROM is programmed and erased by special



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Electrical waves in millisecond.

- A single byte of data or entire content of device can be erased.

2. Secondary Storage

- It can retain information even when the system is off.
- It is basically used for holding the program instruction and data on which the computer is not working currently, but needs to process them later.

Central Processing Unit [CPU]

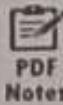
- It has two main components ALU and CU.
- The CPU is the brain of the computer.

① Arithmetic Logic Unit :- [ALU]

- the actual execution of the instructions (arithmetic or logical operations) take place over here.
- the ALU performs simple addition, subtraction, multiplication, division and logic operations such as OR and AND.



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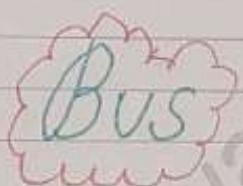
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Q. control Unit:- [CU]

- this unit controls the operations of all parts of the computer but don't carry out any actual data processing.
- It manages and co-ordinates of all the units of the system.

(Another way this question may be asked).

Explain the arrangement of CPU with memory and I/O.



What is bus? [AKTU 2017-18]

- A bus is a communication system that transfers the data between components.
- It consists of a set of parallel wires or lines that carry data, addresses.
- It enables various parts of a computer, like the CPU, memory and peripherals, to communicate with each other efficiently.



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What is System Bus?

- A bus that connects major components (CPU, memory and I/O devices) of a computer system.
- It includes the data bus, address bus and control bus which work together to manage data flow and communication throughout the system.

Why we need bus?

* communication :-

- Buses facilitate communication between the CPU, memory and peripheral devices, allowing data and instructions to be transferred efficiently.

* co-ordination :-

- they manage and coordinate the flow of data and control signals ensuring that different components of the computer work together - harmoniously.

* Scalability :-

- Buses allow for the expansion of the computer systems by connecting additional components and peripherals, such as expansion cards or external



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devices.

* Efficiency :-

- By using shared pathways (buses), multiple-components can access the system's resources without needing individual connections for each device which simplifies the design and reduces costs.

TYPES OF BUS :-

- # Data Bus
- # Address Bus
- # Control Bus

① Data Bus :-

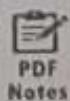
- It is used for transmitting the data or instructions from CPU to memory / I/O and vice-versa.
- It is bi-directional.

② control Bus :- (AKTU 2017-18/18-19)

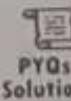
- It is used to transfer and control timing signals from one component to other component
- It is bi-directional.



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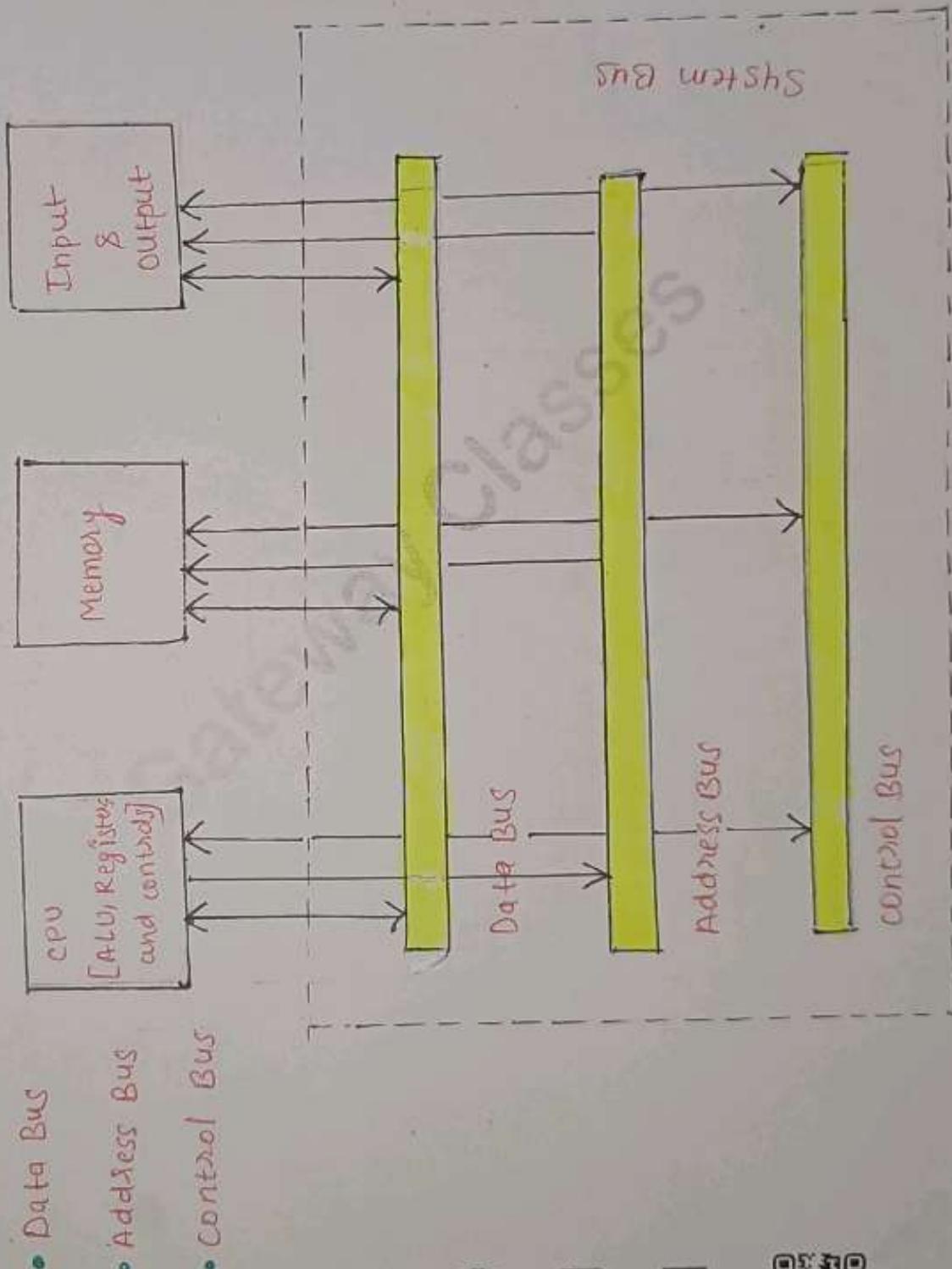
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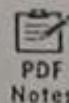
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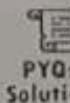
MAJOR COMPONENT OF SYSTEM BUS CAKTU 2015-16]



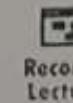
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③ Address BUS :-

- It is used to carry address from CPU to memory/ I/O devices.
- It is Uni-directional.

NOTE :- control signals are generated in the control-unit of CPU.

Memory Read :- Data from memory address location to be placed on data bus.

Memory Write :- Data from data bus to be placed on memory address location.

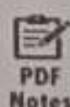
I/O Read :- Data from I/O address location to be placed on data bus.

I/O write :- Data from data bus to be placed on I/O address location.

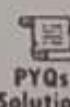
Timing Signals are used to synchronize the memory and I/O operations with a CPU clock.



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ADVANTAGES OF SYSTEM BUS

* Simplified communication :-

- It provides a standardized way for different components (CPU, memory, Peripherals) to communicate, reduce complexity.

* Cost-effective :-

- Using a common bus for data transfer reduces the need for multiple separate connections, saving on hardware costs.

* Scalability :-

- System buses can be easily expanded to support additional devices, making system upgrades simpler.

DISADVANTAGES OF SYSTEM BUS

* Bottleneck risk :-

- All data transfers share the same bus, which can lead to congestion and slow performance as the number of devices increases.



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* Limited Bandwidth:

- The bus has a finite bandwidth, restricting the speed at which data can be transferred between components.

* Shared Resources:

- Devices on the bus compete for the same resources, which can lead to delays and inefficiency in data processing.

Difference between Data Bus Width and Address-Bus width.

Data Bus Width

- The width of a data bus refers to the number of bits (electrical wires) that the bus can carry at a time.
- Each line carries 1 bit at a time. So, the number of lines in data bus determine how many bits can be transferred parallelly.

Address Bus width

- The width of address bus determines the amount of physical memory addressable by the processor.
- In other words, it determines the size of the memory that the computer can use.



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Data Bus Width

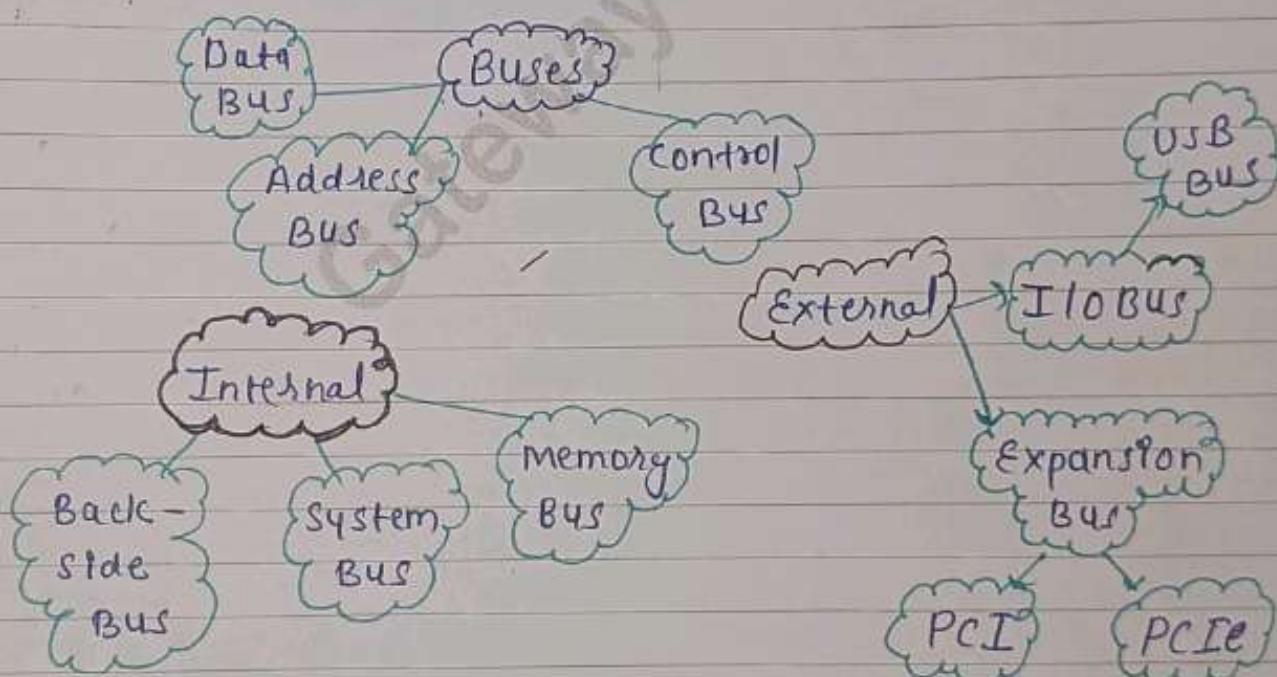
- A 32-bit bus has (32) thirty-two wires and thus can transmit 32 bits of data at a time.

Address Bus Width

- The wider is the address bus, more memory a computer will be able to use.

- A address bus that consists of 16 wires can convey $[2^{16} = 64K]$ different addresses.

Buses:-



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TYPES OF BUSES

1) INTERNAL BUS

- An Internal bus refers to the pathways within a computer that connect the internal components, such as CPU, memory (RAM) and internal storage devices.

2) EXTERNAL BUS

- It facilitates communication between the computer and external hardware such as keyboards, mice, printers and storage devices.

2.1 Input / Output (I/O) BUS:-

- Connects external devices to the computer and manages data transfer between the computer and peripherals such as USB and serial ports.

Universal Serial Bus (USB), Firewire (IEEE 1394)

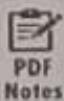
2.2 Expansion BUS:-

- Allows for the addition of extra hardware components to the computer, such as graphics cards and network-cards, through slots on the motherboard.

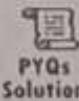
Example include PCI.



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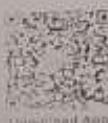


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TYPES OF BUSES

Type of Bus	Function	Direction	Components connected	Characteristics
CONTROL BUS	Transfer control signals from the CPU to manage CPU operations (e.g. Read/ write - commands, interrupt - signals).	Bi-directional	CPU, RAM, I/O devices, System - clock.	carries signals like read / write, interrupt requests and clock pulses.
Pcie Bus (older version)	connects high-speed components like graphics cards, sound cards, and network cards to the motherboard.	Unidirectional [from CPU]	CPU, GPU, sound cards, Network - cards	Pcie [Peripheral Express] offers multiple lanes for data transfer, allowing faster communication.
Memory Bus	Specifically connects the CPU and memory including RAM and Cache	Bi-directional	CPU, RAM cache	High-speed bus design to handle large volumes of data between CPU and memory.



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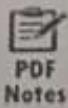
Types of BUSES

Type of Bus	Function	Direction	Components Connected	Characteristics
Back Side Bus [BSB]	connects the CPU to the level 2 [L2] cache (and sometimes L3 cache).	Bidirectional	CPU, L2 / L3, cache	Operates at a higher speed to reduce latency in accessing cache memory.
USB Bus	connects external devices like keyboards, mice, storage devices, and printers to the computer.	Bi-directional	External devices (keyboards, mice, storage).	Universal Serial Bus [USB] standardizes connections for external devices, providing both data transfer and power supply.

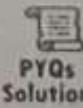


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Q Why data bus is bi-directional?

Soln

- Because it allows the CPU to both read data from and write data to memory peripherals.
- Data flows from the CPU to devices or from the devices to CPU, depending upon the operation.

Q Why control bus is bi-directional?

Soln

- The control bus is bi-directional because it carries control signals from the CPU to devices (E.g. Read/write commands) and receives signals back from devices (E.g. acknowledgments or interrupts).

Q Why Address bus is uni-directional?

Soln

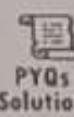
- Because it only sends memory or I/O addresses from CPU specifying where data should be read from or written to, without requiring any return signal.



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REGISTER

- A register is a small and temporary storage unit inside a computer's (CPU).
- It plays a vital role in holding data required by the CPU for immediate processing.
- It usually holds a limited amount of data ranging from 8 to 64 bits, depending on the processor architecture.

Register Transfer :- the information transformed from one register to another register.

What are advantages of using many Register ?

[AKTU-2018-19]

- When more registers are available, the CPU can store intermediate results and frequently accessed data directly in the registers instead of repeatedly reading and writing from memory.
- Having many registers allow the CPU to handle complex computations and multiple operations simultaneously.



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Different Types of Register

① Memory Data Registers (MDR) :-

- It temporarily holds data that is being transferred to or from the memory. It acts as buffer between the memory and the processor.

② Memory Address Registers (MAR) :-

- It holds the address of the location to be accessed from memory.
- MAR and MDR together facilitate the communication of the CPU and main memory.

③ Accumulator :-

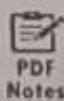
- This is the most frequently used register used to store the intermediate results of arithmetic and logical operations.

④ General Purpose Registers :-

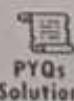
- These are numbered as R₀, R₁, R₂ --- R_{n-1}, and used to store temporary data during any ongoing operation.
- Its content can be accessed by assembly programming.



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⑤ Program counter (PC) :-

- It contains the memory address of the next instruction to be fetched.

⑥ Stack Pointer (SP) :-

- The stack pointer points to the top of the stack, which is the part of the memory used to store function calls and other operations.

⑦ Instruction Register (IR) :-

- The instruction register (IR) holds the instructions which is just about to be executed.

⑧ Flag Register (Status register or condition code)

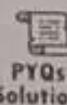
- It is a special type of register in a computer's central processing unit (CPU) used to indicate the status of the CPU or the outcome of various operations such as Zero flag, Carry flag, Sign flag, Overflow flag, Parity flag, Auxiliary Carry flag, and Interrupt Enable flag.



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* BUS ARBITRATION

(AKTU 2019-20 / 21-22 / 23-24)

- In a computer system, multiple devices such as the CPU, memory and I/O controllers, are connected to a common communication pathways, known as a Bus.
- In order to transfer data between these devices, they need to have access to the bus.
- Problem arise when multiple device try to access bus simultaneously.
- It can lead to data corruption and system instability.
- Bus arbitration is the process of resolving the conflicts that arises when multiple devices attempt to access the bus at the same time.

NOTE:-

- The device that has access to a bus at an instance is known as a Bus Master.
- The bus arbiter device who will be the current bus master.



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Why bus arbitration is needed?

- Preventing Data collisions :-

When multiple devices attempt to bus (use) simultaneously, data collisions can occur. Bus arbitration manages access to prevent these collisions.

- Fair Access :-

Ensures that all devices get a fair opportunity to access the bus, preventing any single device from monopolizing the bus.

- Efficient Resource Utilization :-

Maximizes the utilization of the bus by co-ordinating access, thereby improving overall system performance.

- Priority Management :-

Allows for prioritization of bus access, giving critical devices or high-priority tasks that preferential access to the bus.

- Conflict Resolution :-

Resolves conflicts that arise when multiple devices request access to the bus at the same time.



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- **Scalability:** Supports system expansion by managing access as more devices are added, ensuring bus can handle increased traffic.
- **Power Efficiency:** Optimizes power usage by controlling when and how device access the bus, potentially reducing power consumption.

Q How does the computer Organisation affect the performance of the computer?

- Computer Organisation affects performance through its architecture, including the CPU, memory hierarchy.
- Efficient design can reduce bottlenecks, improve processing speed, and enhance all over system throughout.
- For ex:- faster CPUs, larger caches and optimized bus architectures can significantly boost performance.

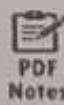
Q Discuss the Storage component of CPU.

(AKTU 2018-19)

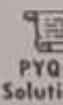
- The primary storage component of a CPU is



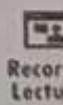
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the register.

- Registers are small, fast storage locations within the CPU used to hold data and the instructions that are currently being processed.

TYPES OF BUS ARBITRATION

There are two approaches to bus arbitration :-

- ① Centralized Bus Arbitration
- ② Distributed Bus Arbitration

(1) Centralised Bus Arbitration :-

The controller, called the bus arbiter, decides which device gets to use the bus when multiple-devices request it.

(2) Distributed Bus Arbitration :-

All devices participating in the selection of the next bus master.

Method of centralized Bus Arbitration:-

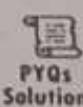
- Daisy chaining method
- Polling or Rotating Priority method.
- Fixed Priority or Independent Request Method.



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① Daisy Chaining Method:

- The same line is used for bus requests by all devices.
- The Bus controller sends out the Bus Grant signal if the bus busy line is not active.
- Beginning with the nearest device, the bus grant signal is transmitted serially through every device
- The device, who needs the system Bus, get the control of the system Bus and then Bus busy line is activated and become bus master.

Advantage:-

- simple design is an advantage
- there are fewer control lines.
- It is also simple to add new device

Disadvantage :-

- the device who is physically closest to the bus arbiter has the highest priority.
- Bus access is granted serially, which causes a propagation delay in a circuit.
- If one device stop working, the whole system might stop working too.



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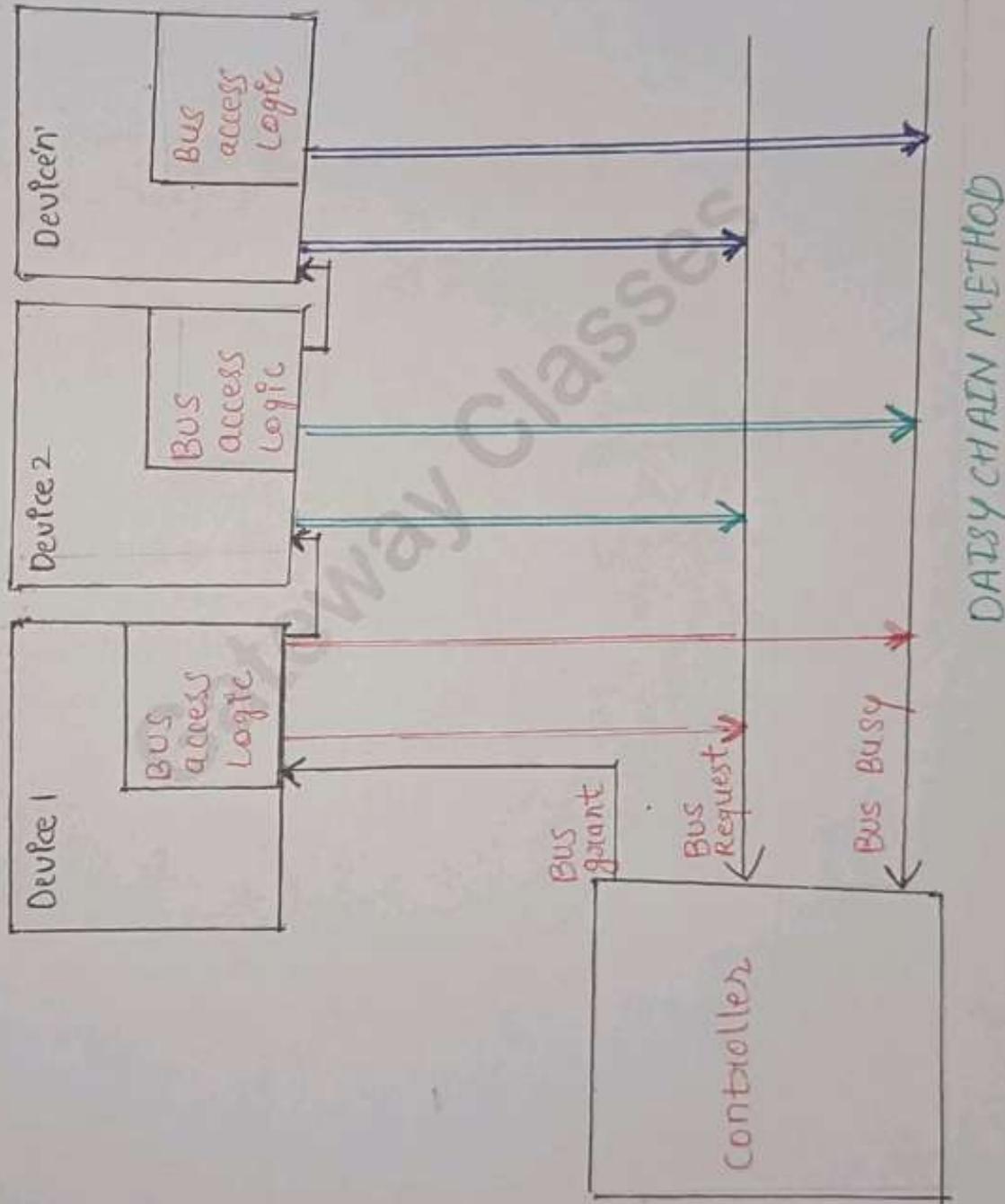
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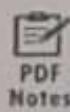
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DATA CHAINING

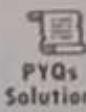


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(2)

Polling or Rotating Priority Method:-

- The same line is used for Bus request by all device in this instance. Here, a controller creates a master's binary address.
- For instance, 3 address lines are required ($2^3 = 8$) to connect 8 bus device. The controller "polls" the device in response to a bus request by transmitting a series of bus master addresses on the address lines.
- The Selected device takes control of the bus and signals that the bus is in use. (Bus busy line is activated)

Advantages:-

- This method does not favour any particular device and processor.
- The Method is also quite simple.
- If one device fails then the entire system will not stop working.

Disadvantages:-

- Adding new device is difficult as increases the number of address lines of the circuit.



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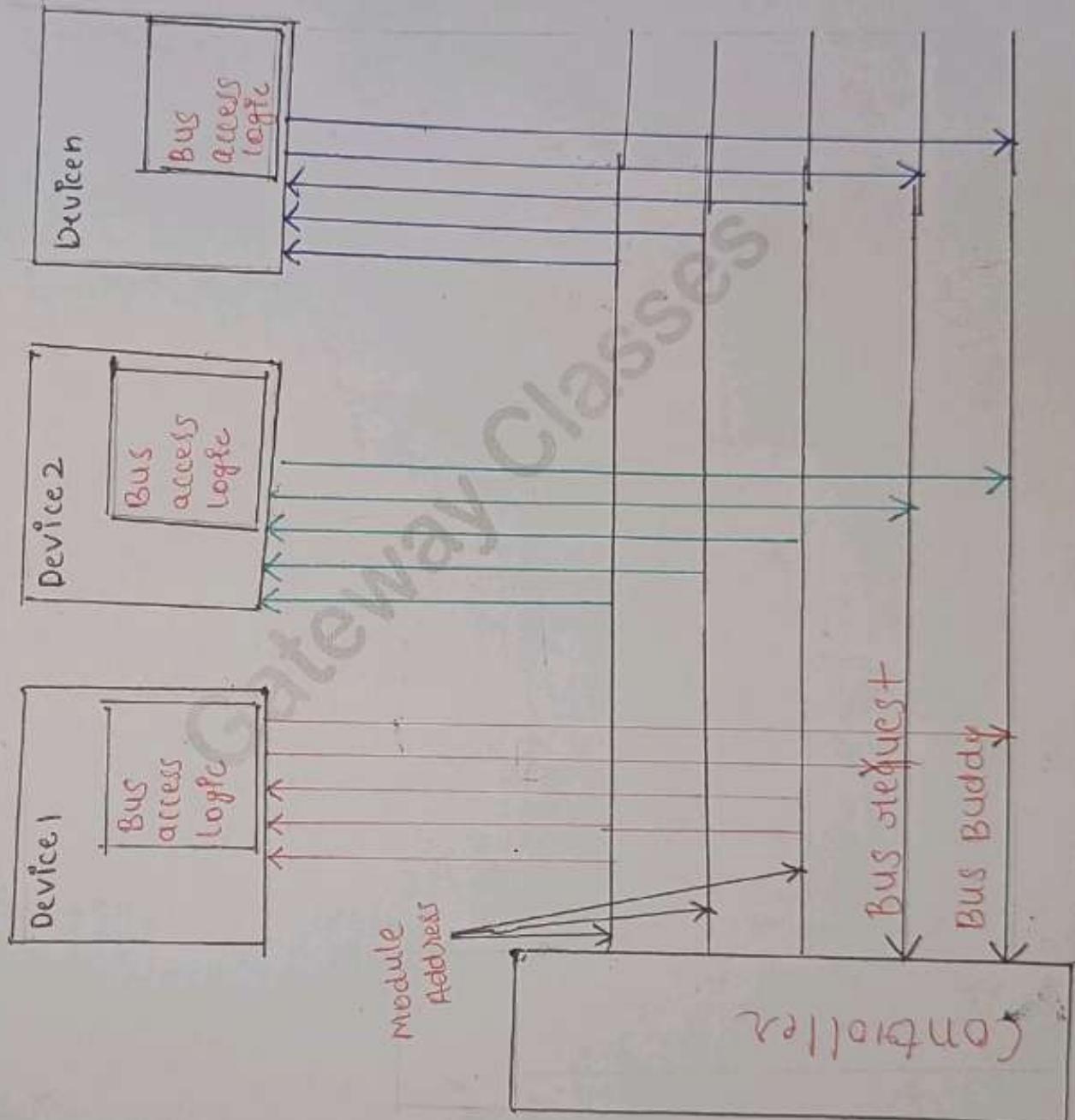
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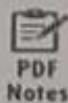
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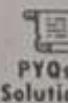
Polling or Rotating Priority Method



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fixed Priority or Independent Request Method:

- Each device has a separate Bus Request and Bus Grant here.
- By knowing which device has asked, the controller can give that device the bus.
- If multiple devices request the bus at the same time, the bus is given to the one with higher priority, as long as the bus is not already in use. [Bus busy line is not activated].
- The controller is made up of circuits that determine the order of priority using encoder and decoder logic.

Advantage:-

- This technique produces a quick response.
- The speed of Bus Arbitration is unaffected by the quantity of connected devices.

Disadvantage:-

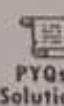
- More control lines are needed (2^n lines are needed for n devices).



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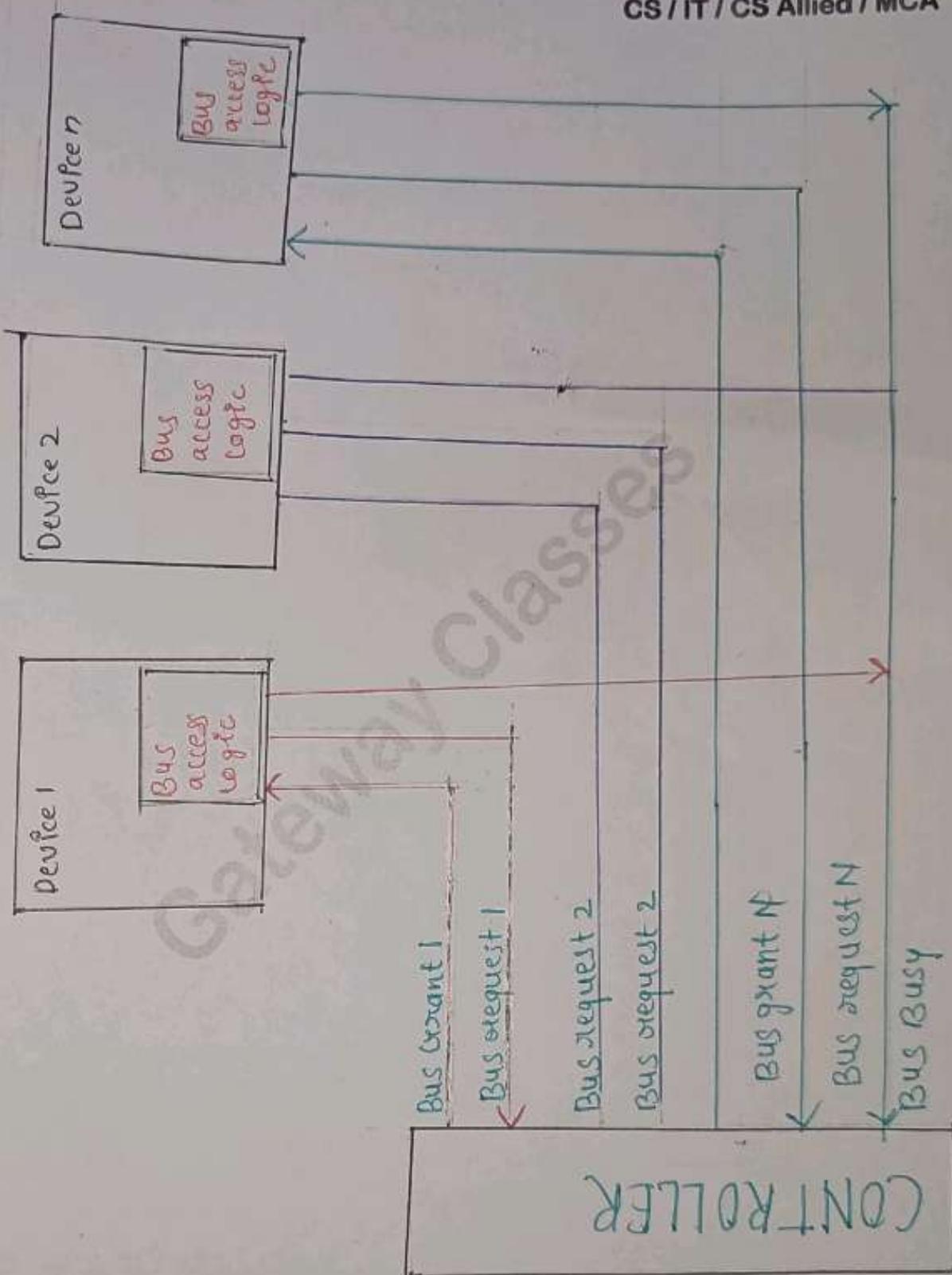
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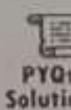
INDEPENDENT REQUESTS



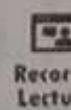
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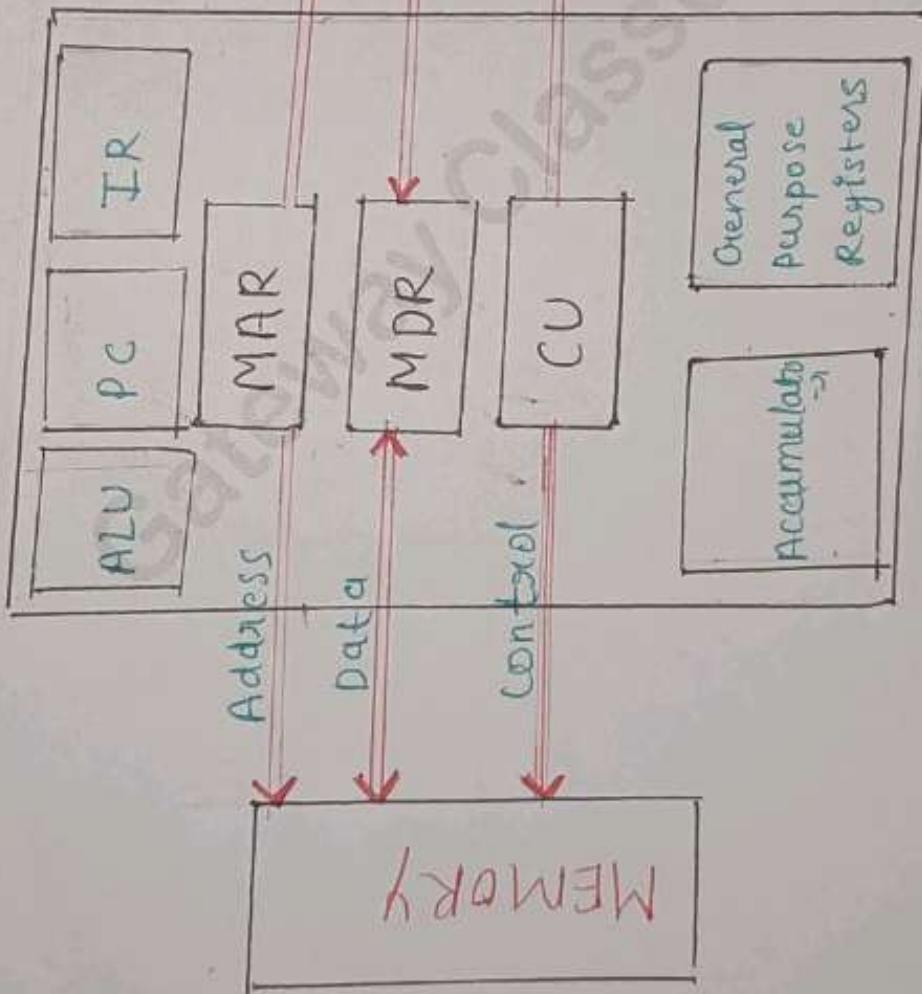
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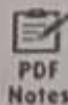
[AKTU 2016-17]

BLOCK DIAGRAM OF CPU

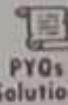
CPU



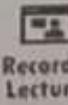
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① Memory Address Register (MAR) :-

- It holds the memory address of the data that needs to be accessed either for reading from or writing to memory.

② Memory Data Register (MDR) :-

- This is a CPU register that temporarily holds data being transferred to or from memory.
- When the CPU reads from or writes to memory, the data passes through the MDR.

③ Program Counter (PC) :-

- It is a register in the CPU that holds the address of the next instruction to be executed in a program.

④ The Instruction Register (IR) :-

- It is a CPU register that holds the current instruction being executed. After the CPU fetches an instruction from memory, it is stored in the Instruction Register [IR].



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⑤ Input - Output (I/O) Bus:-

- It is a communication pathway that connects the CPU and the memory to peripheral devices, such as keyboards, printers and storage devices or drives such as Pendrives.
- It facilitates the data transfer between the central system and these external devices.

⑥ Accumulator :-

- The Accumulator is a special register within the CPU used to store intermediate results of the arithmetic and logic operations.

⑦ I/O Interface :-

- An I/O (Input/Output) interface is a system that facilitates communication between the CPU and Peripheral devices.
- It acts as a bridge, converting data and control-signals from the CPU into a form that peripheral devices can understand and vice-versa.

⑧ General Purpose Register:-

- It is a CPU register used for storing temporary



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data and performing arithmetic or logical operations.

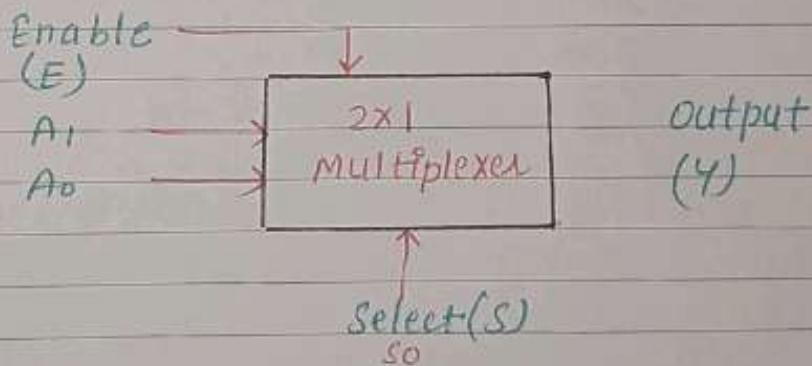
- It can hold intermediate results and data for various tasks, providing versatility in execution. Its use helps optimize processing efficiency by minimizing memory access.

Address bus, Data bus, Control bus, Control Unit, Arithmetic and Logical Unit (ALU) [Already explained]

*MUX (MDX)

- A Multiplexer is a combinational circuit that has 2^n input lines and a single output line.
- It is a multi-input and single-output combinational circuit.

2x1 Mux



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data and performing arithmetic or logical operations.

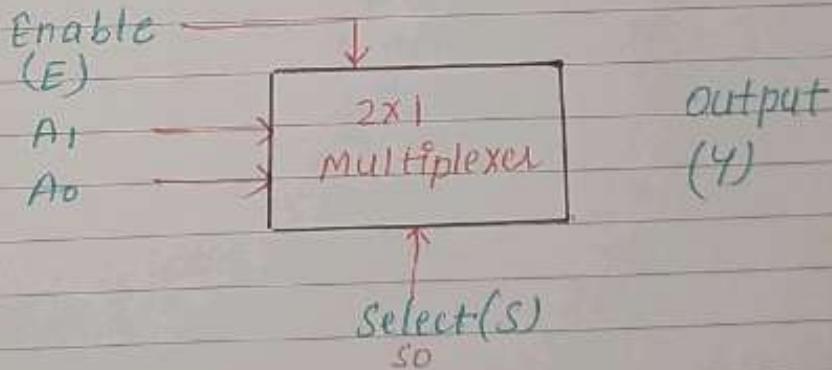
- It can hold intermediate results and data for various tasks, providing versatility in execution. Its use helps optimize processing efficiency by minimizing memory access.

Address bus, Data bus, Control bus, Control Unit, Arithmetic and Logical Unit (ALU) [Already Explained]

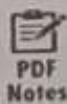
* MULTIPLEXER (MUX)

- A multiplexer is a combinational circuit that has 2^n input lines and a single output line.
- It is a multi-input and single-output combinational circuit.

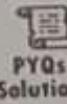
2x1 MUX



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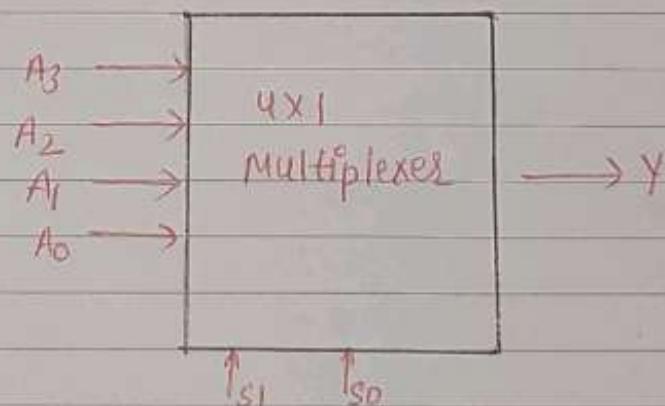
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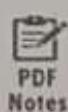
INPUTS	OUTPUTS
S0	Y
0 1	A0 A1

4x1 MUX

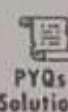
INPUTS		OUTPUT
SI	SD	Y
0	0	A0
0	1	A1
1	0	A2
1	1	A3



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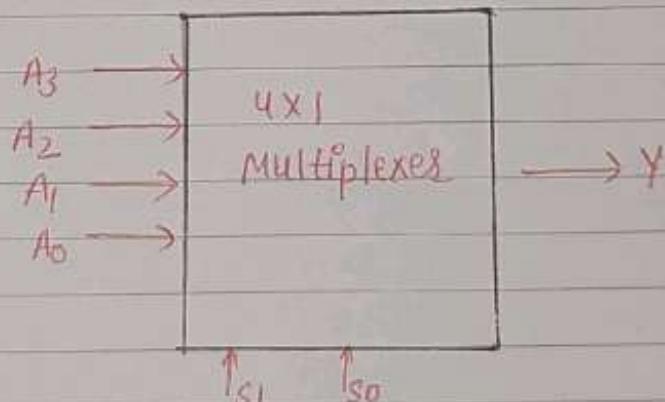
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INPUTS	OUTPUTS
S0	Y
O I	A0 A1

4x1 MUX

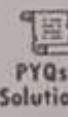
INPUTS		OUTPUT
SI	SO	Y
0	0	A0
0	1	A1
1	0	A2
1	1	A3



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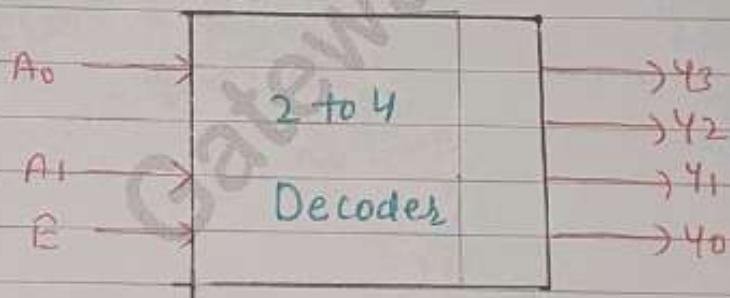
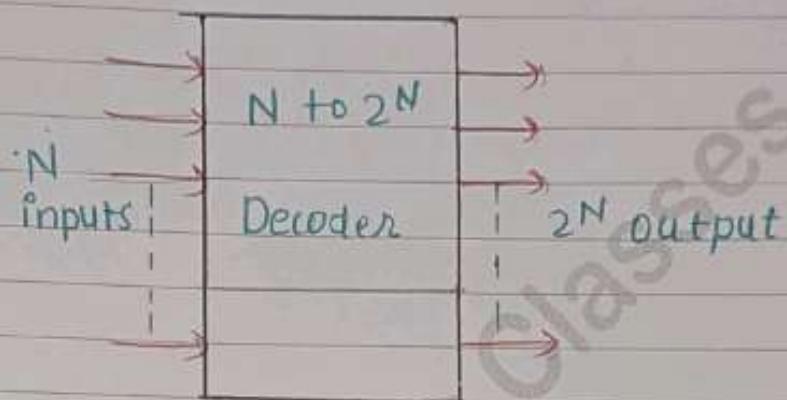
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DECODER

- The combinational circuit that changes the binary information into 2^N output lines is known as Decoders.

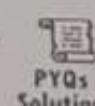
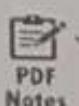


where $N=2$

$$\Rightarrow 2^2 \Rightarrow 4$$



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ENABLE	INPUTS		OUTPUTS				
E	A ₀	A ₁	Y ₃	Y ₂	Y ₁	Y ₀	
0	X	X	0	0	0	0	
1	0	0	0	0	0	1	
1	0	1	0	0	1	0	
1	1	0	0	1	0	0	
1	1	1	1	0	0	0	

Memory Transfer

OR

How memory Read and write operation performed

[AKTU 2022-23]

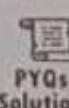
- The transfer of information from a memory unit to the user end is called a **Read Operation**.
- The transfer of new information to be stored in the memory is called a **Write Operation**.
- A memory word is designated by the letter **M**
- we must specify the address of memory word while writing the memory transfer operations.



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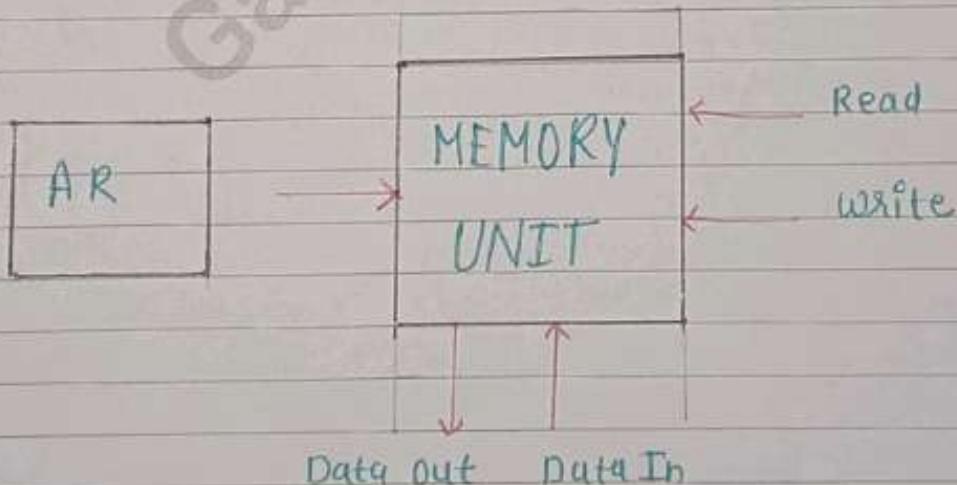
- The address register is designed by AR and the Data Register by DR.
- The address register and data register mainly used for memory transfer.

Read: $DR \leftarrow M[AR]$

- The Read statement causes a transfer of information into the Data Register [DR] from the memory word [M] selected by the address register [AR]

Write: $M[AR] \leftarrow RI$

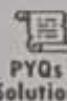
- The write statement causes a transfer of information from Register RI into the memory word [M] selected by address register [AR]



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BUS TRANSFER

The act of sending data from one component another through the bus. This can involve reading from or writing to memory, or exchanging data between devices.

There are two methods in Bus Transfer

- Bus transfer using Multiplexer
- Bus transfer through three state buffer.

BUS transfer through Multiplexer or

Common Bus System Using Multiplexers

- A digital system composed of many registers and paths must be provided to transfer information from one register to another.
- The number of wires connecting all of the registers will be excessive if separate lines are used between each register and all other registers in the system.
- A bus structure on the other hand is more efficient for transferring information between registers



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in a multi-register configuration system.

The two selection lines S_1 and S_0 are connected to the Selection inputs of all four multiplexers. The Selection lines choose the four bits of one register and transfer them into the four-line common bus.

When both of the select lines are at low logic level $S_1 S_0 = 00$, the 0 data inputs of all four multiplexers are selected and applied to the outputs that forms the bus.

This, in turn, causes the bus lines to receive the content of register A since the outputs of this register are connected to the 0 data inputs of the multiplexers.

S_1	S_0	REGISTER SELECTED
0	0	A
0	1	B
1	0	C
1	1	D

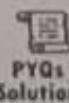
Implement the bus of 4 lines with MUX



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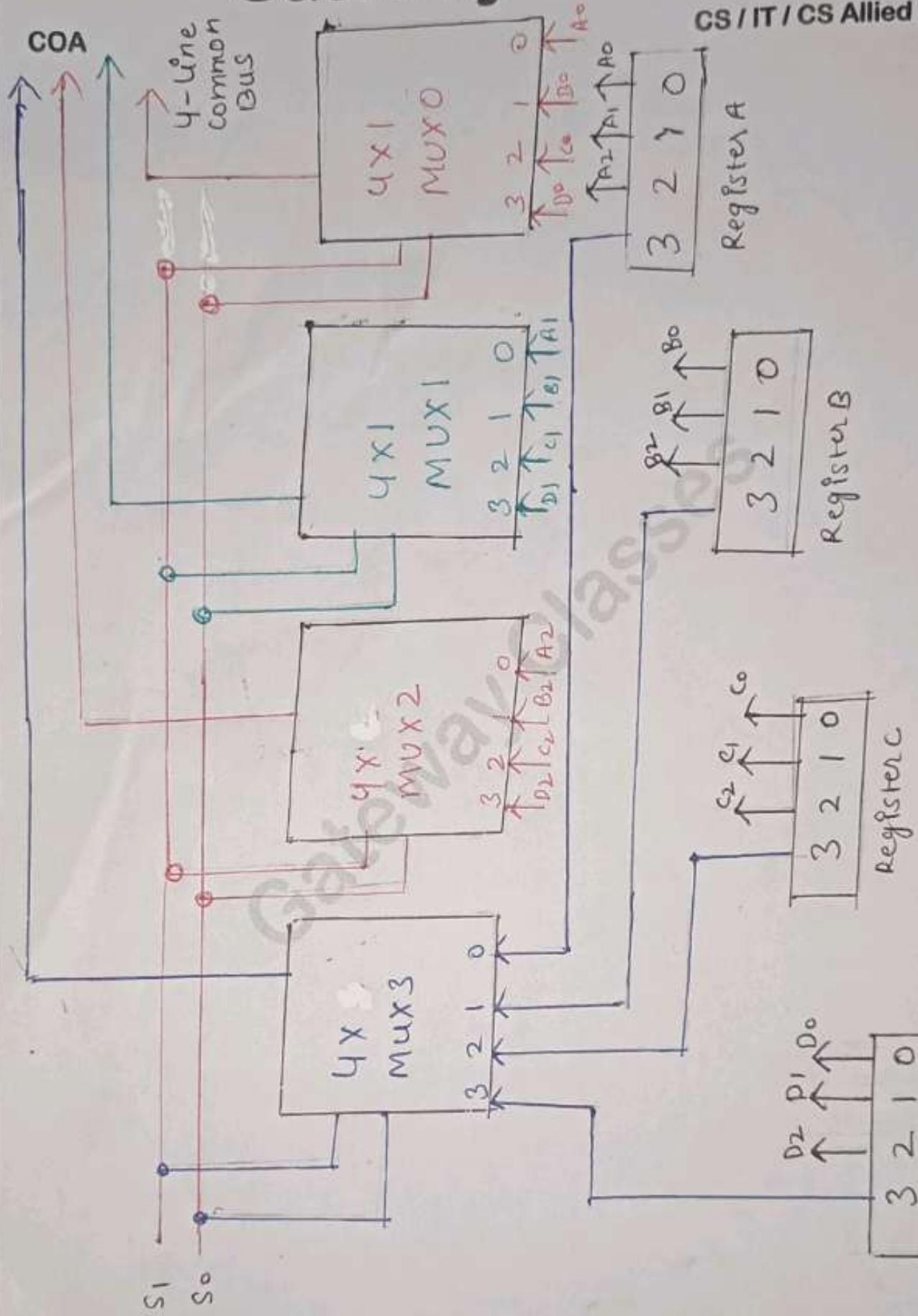
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Implementation of Bus of 4 Lines with MUX

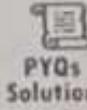
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NOTE:

- ① Number of Multiplexers needed = Number of bits in Each Register
- ② Number of inputs in each = Total number of registers.

IMPLEMENT A BUS OF 8 LINES WITH MUX

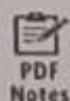
S1	S0	REGISTER SELECTED
0	0	A
0	1	B
1	0	C
1	1	D

Representation of 8 line common bus with the help of multiplexers

The use of different colour pen is for the proper understanding only.



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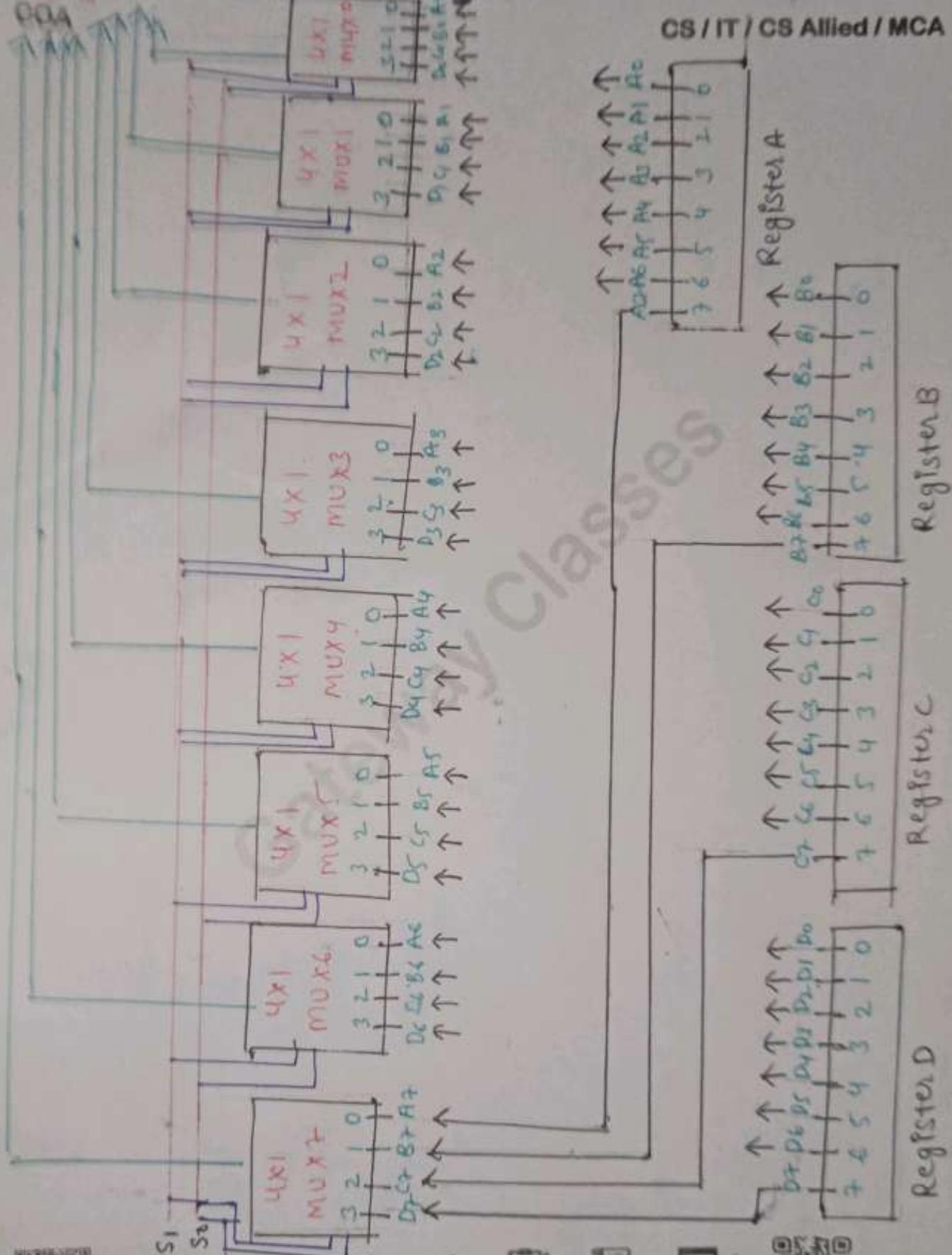


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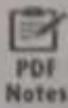


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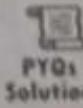
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BUS Transfer Through Three State Buffer
OR

Ques Bus transfer through three state Buffer and Decoder instead of Multiplexers

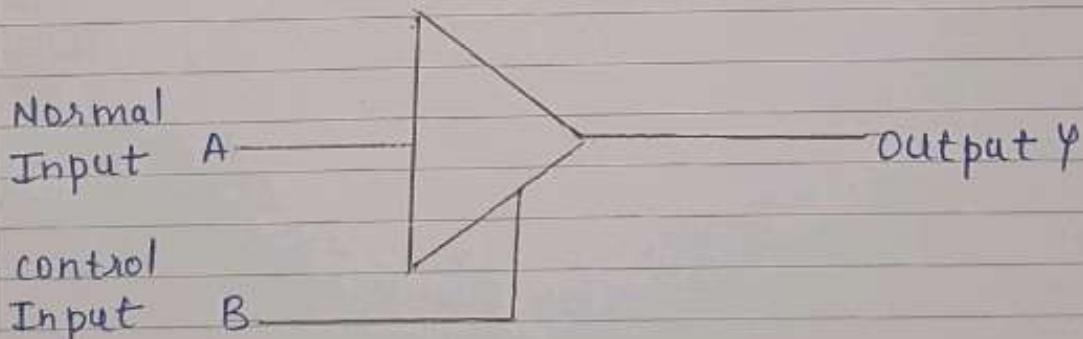
[AKTU 2020-21 / 2021-22]

- The three state gates can be considered as a digital circuit that has three states two of which are signals equivalent to logic 1 and 0 as in a conventional gate.
- The most commonly used three state gates in case of the bus system is a buffer gate.

The graphical symbol of a three-state buffer gate can be represented as -

$$Y = A \text{ IF } B=1$$

High impedance if $B=0$



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Three state gates have two inputs, normal input and control input.

- Control input determines the output of the three state gates.
- If control input is equal to 1, then the output is the normal input in the gate.
- If control input is equal to 0, then the gate goes to a high impedance state (a state in which output is disconnected).

Working :-

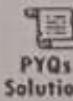
- Four three state gates are used for each bit whose outputs are connected together to form a single line of a common bus.
- Each gate has control inputs which decides whose data will be transferred to the bus line. The control input of only one gate is active at a time. The other gates are at high impedance state.
- To ensure that the control input of only single gate is active at a time, a decoder is used at this time.



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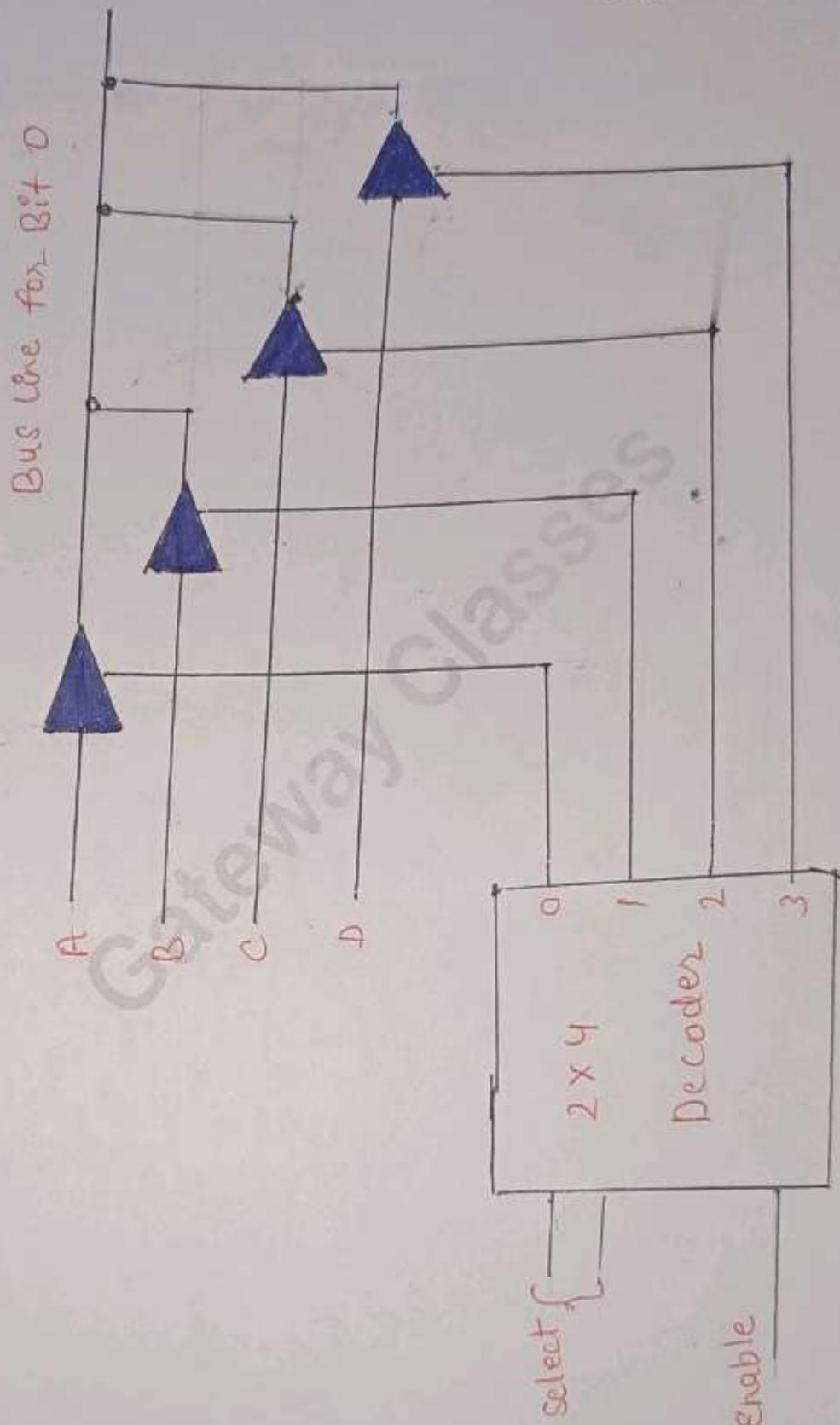


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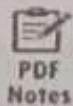


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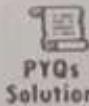
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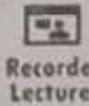
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Decoder has enable input:-

- If the enable input is 0, then the control inputs of all the gates are disabled and the bus line goes to the high impedance state.
- If the enable input is 1, then the control input of any one of the gate is active depending on the binary value of the selection variables.

Some Important Points:-

- The operation field (opcode) specifies the operation to be performed, like addition.
- Address field which contains the location of the operand i.e register or memory location.
- Mode field which specifies how operand is to be founded.

MODE	OPCODE	ADDRESS FIELD

ADDRESSING MODES

[AKTU 2022-23/2019-20]

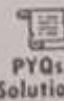
The different ways of specifying the location of an operand in an instruction.



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Types of Addressing Modes :-

- Implied / Implicit Addressing Mode.
- Stack Addressing Mode.
- Immediate Addressing Mode.
- Direct Addressing Mode.
- Indirect Addressing Mode.
- Register Direct Addressing Mode.
- Register Indirect Addressing Mode.
- Relative Addressing Mode.
- Indexed Addressing Mode.
- Base Register Addressing Mode.
- Auto-Increment Addressing mode.
- Auto-Decrement Addressing Mode.

The effective address refers to the location where the operand resides.

Significance of Addressing Mode

Addressing Mode specify how the operand of an instruction is accessed. They provide flexibility in accessing data, optimized memory usage and improve instruction efficiency.

① Implied Addressing Mode (Implicit addressing Mode)

The definition of the instruction itself specify the operands implicitly.



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Example :- complement Accumulator.

② Stack Addressing Mode :-

The Operand is contained at the top of the stack

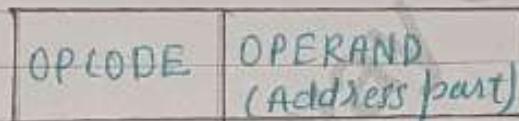
Example:- ADD

③ Immediate Addressing Mode :-

The Operand is specified in this instruction explicitly

Example:-

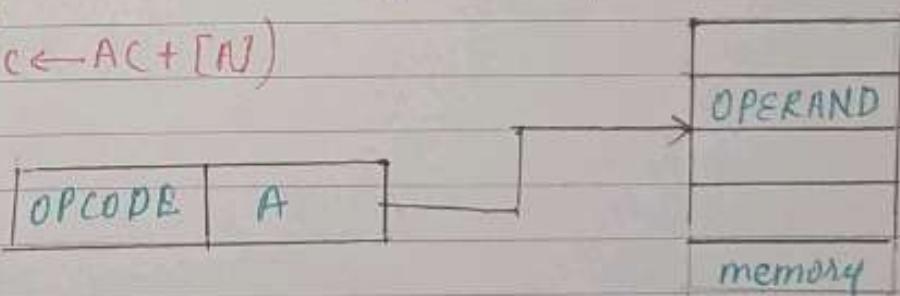
- (1) MOV R #20
- (2) ADD 10



④ Direct Addressing Mode: - (absolute addressing mode)

- The address field of the instruction contains the effective address of the Operand.
- Only One reference to memory is required to fetch the Operand.

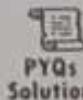
ADD A ($AC \leftarrow AC + [N]$)



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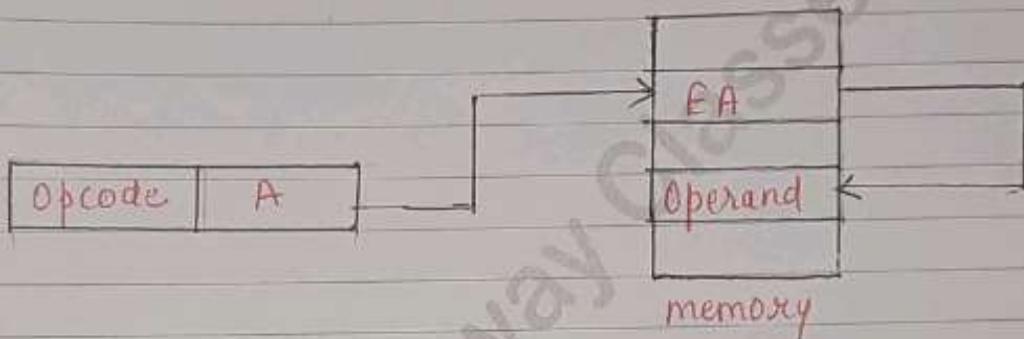
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⑤ Direct Addressing Mode :-

- The address field of the instruction specifies the address of memory location that contains the effective address of the Operand.
- Two references to Memory are required to fetch the Operand.

$$AC \leftarrow A + [A]$$



⑥ Register Direct Addressing Mode :-

- The operand is contained in the register set.
- The address field of the instruction refers to the CPU register that contains the Operand.
- No reference to memory is required to fetch the Operand during the Operation.



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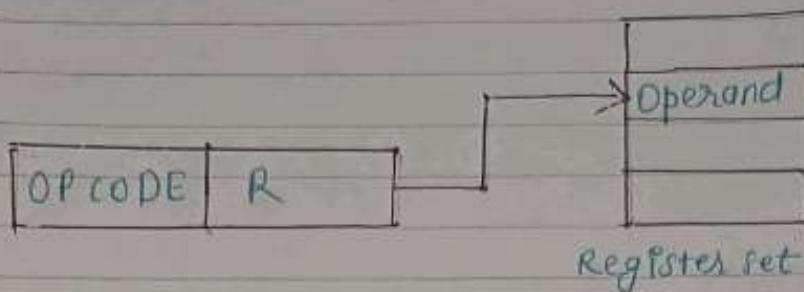


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⑦ Register Indirect Addressing Mode:-

- The address field of the instructions refer to the CPU register that contains the effective address of the Operand.
- Only one reference of memory is required to fetch the Operand.



⑧ Relative Addressing Mode:-

- Effective address of the Operand is obtained by adding the content of program counter with the address part of the instruction.



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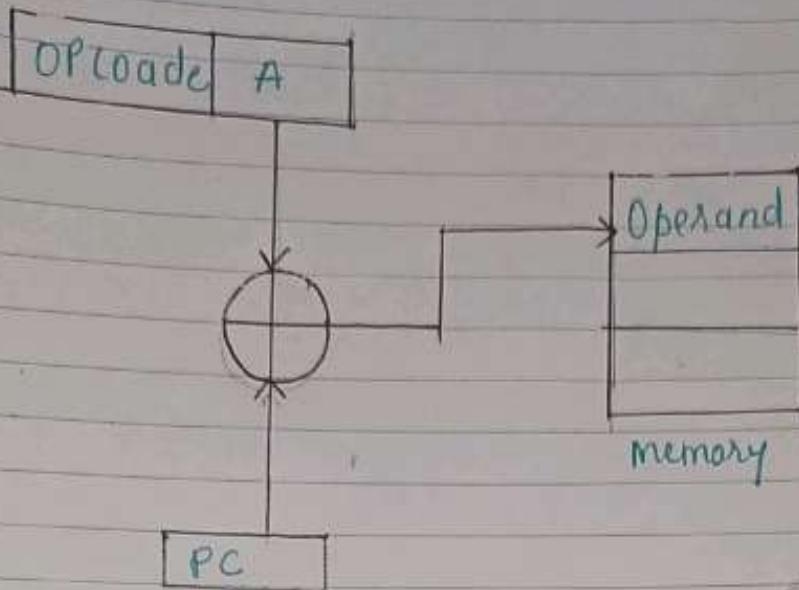


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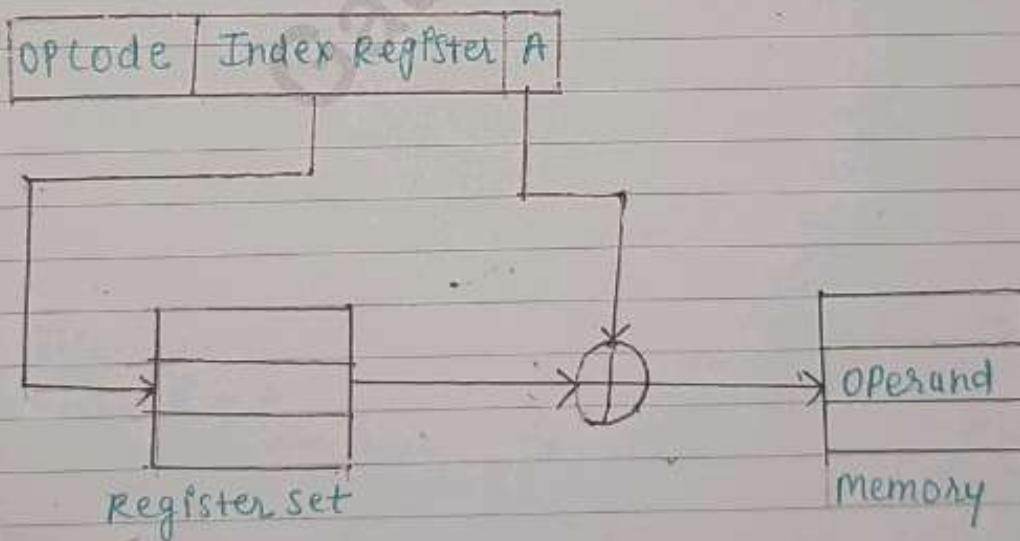
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⑨ Index Addressing Mode :-

Effective address of the Operand is obtained by adding the content of Index register with the address part of the instruction.



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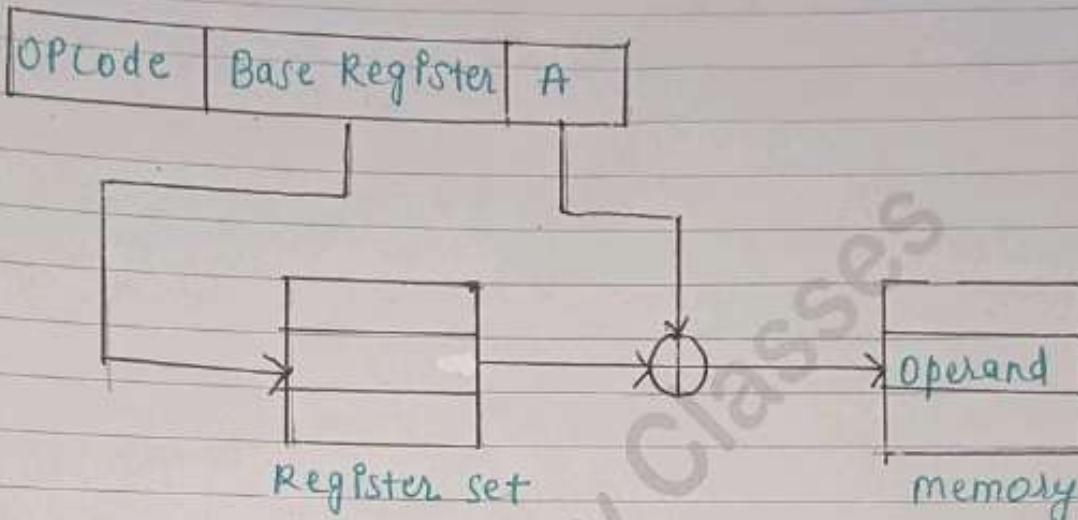
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(10)

Base Register Addressing Mode :-

Effective address of the operand is obtained by adding the content of base register with the help of addressing part of the instruction.



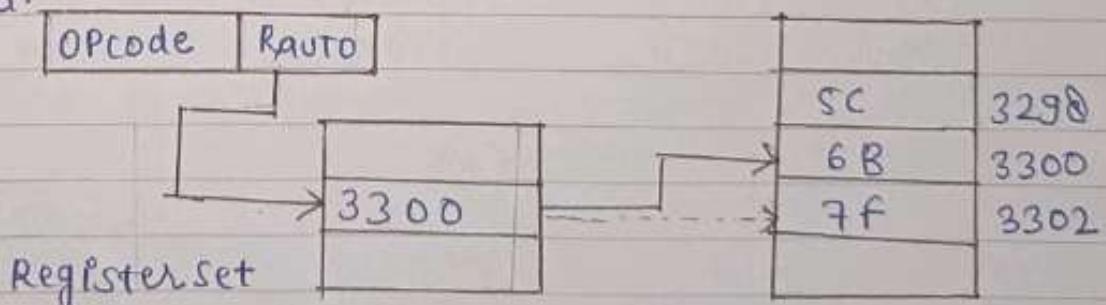
(11)

Auto-Increment Address Mode :-

This addressing mode is a special case of Register-Indirect Addressing Mode.

Effective Address of the Operand = Content of Register.

Only one reference to memory is required to fetch the Operand.



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(11) →

After accessing the Operand, the content of the Register is automatically incremented by step size 'd'

Step size 'd' depends upon the size of Operand accessed.

(12) Auto-Decrement Addressing Mode :-

The addressing mode is again a special case of Register Indirect Addressing.

Effective Address of the Operate =

content of Register - Step Size

First the content of register is decremented by step size of 'd'.

Step size 'd' depends on the size of the Operand accessed.

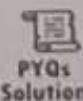
After decrementing, the Operand is read.

Only one reference to memory is required to fetch the Operand.

Representation -



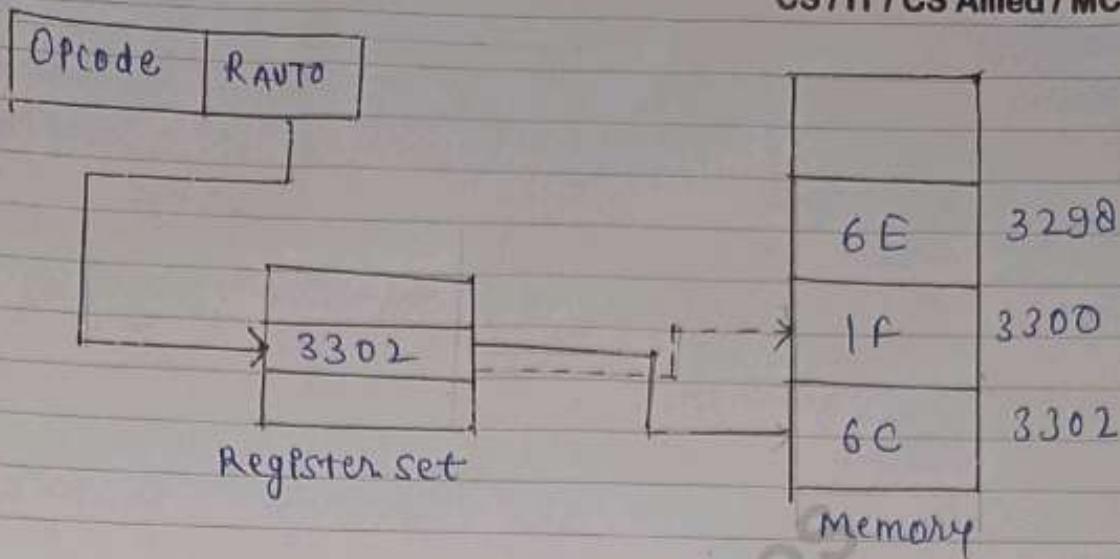
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PROCESSOR ORGANISATION

[AKTU 2023-24 / 24-25 / 19-20]

- Processor Organisation refers to the internal architecture and design of CPU, including how components like the ALU (Arithmetic Logic Unit), control unit, registers, and buses are arranged and interact to execute instructions.
- It defines the CPU's data processing capabilities and operational efficiency.

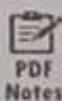
There are three type of Processors organization

① General Register Organization :-

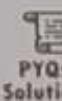
- It involves using multiple general-purpose registers



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- for data storage during instruction execution.
- It allows direct access to Operands and results, reducing memory access frequency.
- this organization enhances CPU Speed and flexibility in executing Operations.

② Stack Organization :-

- Stack organization uses a stack to store and retrieve data.
- Instructions work by automatically using the top items on the stack, so no need to specify Operands.
- This makes it simple but limit control over data access.

③ Accumulator - Based Organization :-

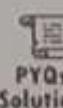
- It uses a single register, called the accumulator to hold one operand and store result's. All operation use the accumulator, making it simple but less flexible compared to the multiple - register system.
- Generally CPU has Seven general registers.



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- Register Organization show how register are Selected and how data flow between register and ALU.
- A decoder is used to select a particular register.
- the output of each register is connected to two (MUX) multiplexers to form two buses A and B.
- the Selection lines in each multiplexer select the input data for particular bus.
- The A and B buses from the two inputs of an ALU.
- The Operation Select lines decide the micro-operation to be performed by ALU.
- the result of the micro-operation is used to available at the output bus.
- the Output bus connected to the inputs of all the registers, thus by selecting a destination register it is possible to store the result in it.

Representation:-



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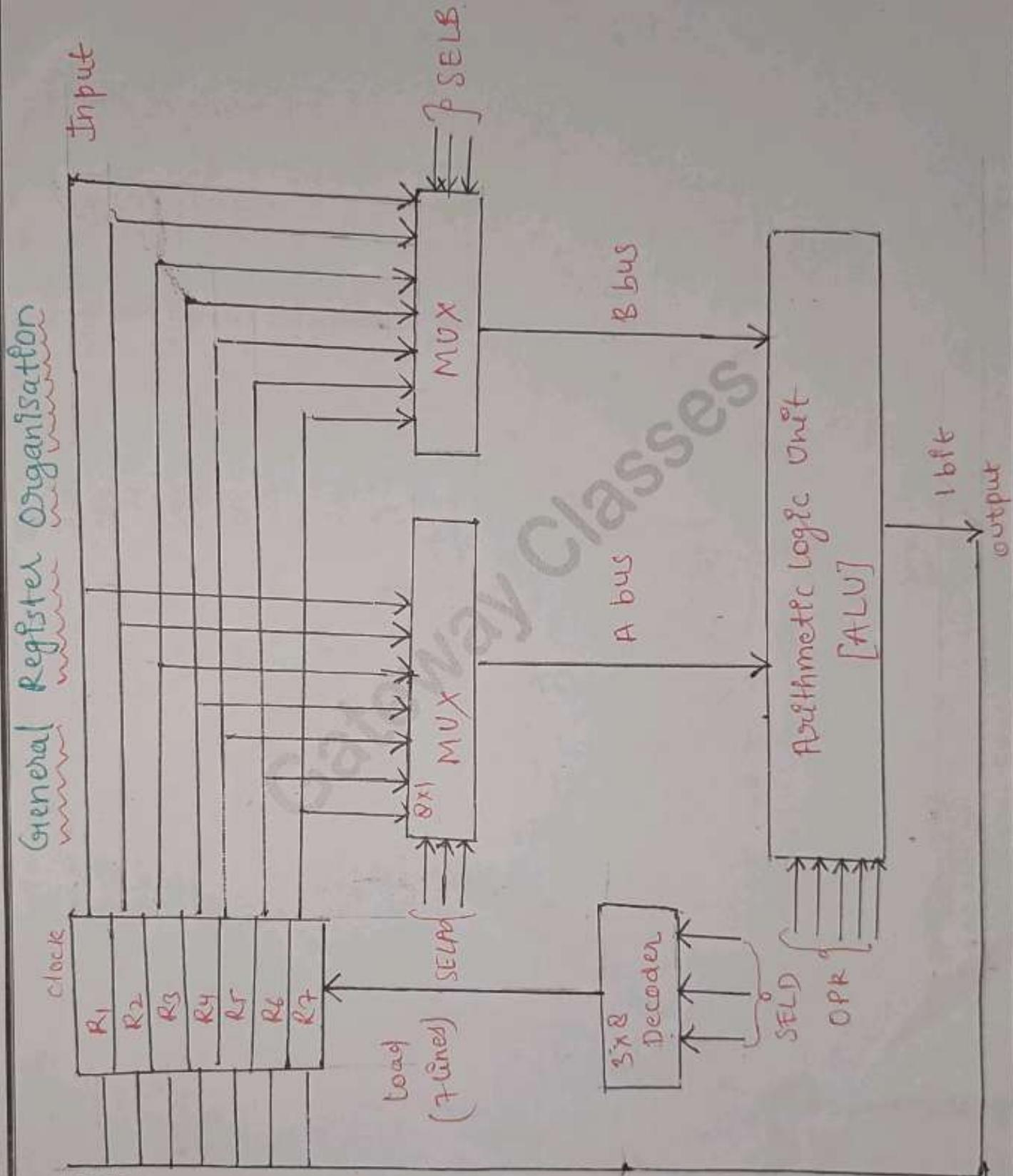


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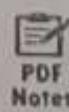
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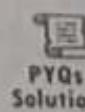
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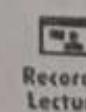
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Register and Multiplexer Input Selection Code

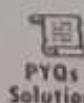
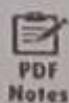
Binary Code	SEL A	SEL B	SEL D OR SEL REG
000	INPUT	INPUT	---
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

OPERATION WITH SYMBOLS

OPR Select	Operation	Symbol
00000	Transfer A	TSFA
00001	Increment A	INCA
00010	Add A+B	ADD
00101	Subtract A-B	SUB
00110	Decrement A	DECA
01000	AND A and B	AND
01010	OR A and B	OR
01100	XOR A and B	XOR
01110	Complement A	COMA
10000	Shift right A	SHRA
11000	Shift left A	SHLA



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EXAMPLE 1:-

Micro-Operation	SELA	SELB	SELD	OPR
$R_1 \leftarrow R_2 - R_3$	R_2	R_3	R_1	SUB
CONTROL WORD	010	011	001	00101

EXAMPLE 2:-

Micro-Operation	SELA	SELB	SELD	OPR
$R_7 \leftarrow R_1$	R_1	-	R_7	TSFA
CONTROL WORD	001	000	111	00000

CONTROL WORD

the combined value of a binary selection input specifies the control word.

SELA (3 BITS)	SELB (3 BITS)	SEL REG 6 ₂ OR SELD (3 BITS)	SE L OPR (5 BITS)
------------------	------------------	---	----------------------



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Micro Operation	SEL A	SEL B	SEL D	OPR
Output $\leftarrow R_2$	R_2	-	None	TSFA
CONTROL WORD	010	000	000	00000

Advantages:

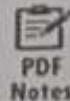
- Registers are quicker to access than memory, improving instruction execution speed.
- Multiple registers allow simultaneous operations, reducing the need to access memory frequently.
- General-purpose registers can hold data, address or intermediate results, offering greater flexibility.

Disadvantages:

- More registers require complex control logic and larger instruction sets, which can complicate CPU design.
- Additional registers increase the power usage of the processor.
- Despite multiple registers, the space is still limited, which may require careful management in complex programs.



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The function of control unit in general register organization

- The control unit (CU) is a general register organization. It is responsible for directing the operations of the CPU by controlling the flow of data between the registers, ALU (Arithmetic Logic Unit) and memory.
- It generates the necessary control signals based on the instructions fetched from memory.

① Instruction fetching :-

- The CU fetches the instruction from memory by generating the appropriate control signals.
- This instruction is then placed into the instruction register (IR).
- The control unit uses the Program Counter (PC) to keep track of the next instruction's address.
- It updates the PC after fetching each instruction.

② Instruction Decoding :-

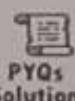
- Once the instruction is fetched, the CU decodes it to determine the operation to be performed.



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- The decoding process involves breaking down the instruction into its OPCODE (Operation code) and Operands (data or address).

③ Control Signal Generation :-

- Based on the decoded instruction, the CU generates control signals that direct various components of the CPU on what actions to take.
- These signals control data transfer between registers, instruct the ALU to perform arithmetic or logical operations, and manage data exchange between the CPU and memory.

④ Execution control :-

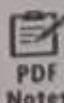
- the CU controls the execution of the instructions by coordinating the sequence of operations needed to execute the instruction.
- for example, If the instruction is an addition operation the CU will signal the ALU to perform the addition on the specified registers.

⑤ Memory and I/O control :-

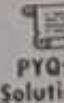
the CU manages the transfer of data between the CPU and memory, as well as input/output devices.



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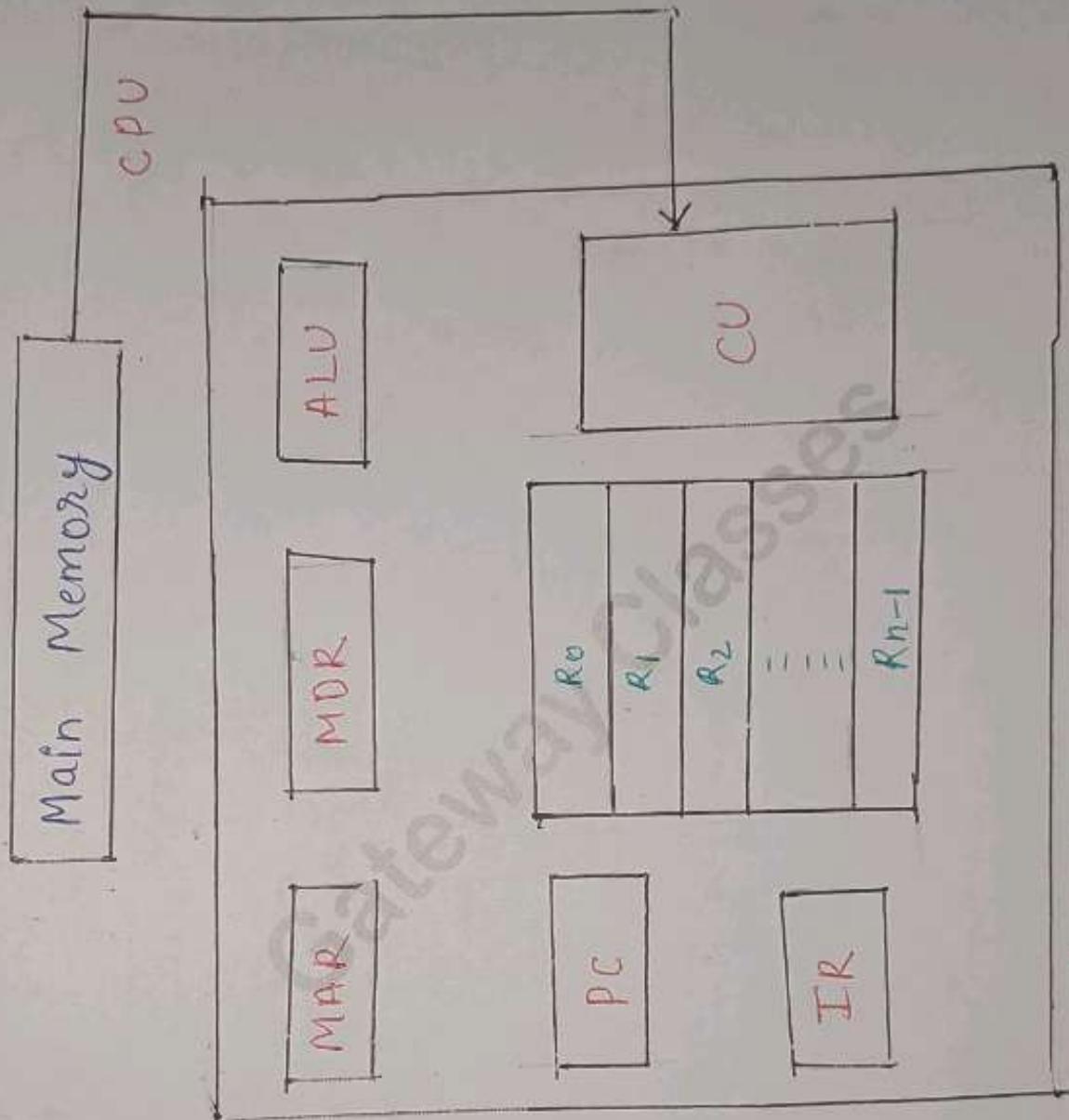


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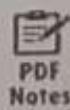
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You can also write about all Revision.



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Accumulator-Based Organization

- It is sometimes also called as Single accumulator Based organization.
- In this type of CPU organization, the accumulator register is used implicitly for processing all instructions of a program and storing the results into the accumulator.
- The instruction format that is used by this organization is the one address field. Due to this, the CPU is also known as One Address Machine.

The main points about single Accumulator based CPU organization are:

- In this CPU organization, the first ALU Operand is always stored into the Accumulator and second Operand is present either in Registers or in the Memory.
- Accumulator is the default address thus after the data manipulation the results are stored into the Accumulator.
- One address instruction is used in this type of the organization.



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Mainly two types of operation are performed in a single accumulator based CPU organization:

① Data transfer Operation :-

For example: LOAD X, STORE Y

- LOAD is a memory read operation that is data is transferred from memory to Accumulator.
- STORE is a memory write operation that data is transferred from the accumulator to memory.

② ALU Operation:-

Arithmetic operations are performed on the data.

for example: MUL X
 $AC \leftarrow AC * M[X]$

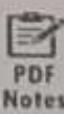
AC is the Accumulator and M[X] is the memory word located at the location X.

Advantages :-

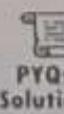
- One of the operands is always held by the accumulator register. This results in short instructions and less memory space.



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- the instruction cycle takes less time because it saves time in instruction fetching from memory.

Disadvantages :-

- When complex expressions are computed, program size increases due to the usage of many short instructions to execute it. thus memory size increases.
- As the number of instructions increases for a program, the execution time increases.

Stack Organization

[AKTU 2022-23]

The stack organization is a method of managing data in a computer system using a stack data structure.

A stack is a collection of elements with two primary operations:

Push (to add an item to the stack) and
Pop (to remove the item from the top of stack)

It follows the Last In First Out (LIFO) principle, meaning the most recently added item is the first to be removed.

The stack can be implemented using two ways:

- Register Stack
- Memory Stack.



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Implementation of register as a Stack

OR

Register Stack Organisation

64 general registers are used for stack implementation
so 6 bits are required to address 64 registers.

SP is a stack pointer (top of the stack) that stores the location address where we must push or pop any data. As SP stores the address of that location where we need push or pop data, its size will be 6 bits.

We use two flag registers named full and EMPTY

If the value of full is 1, then empty will be zero and vice versa.

If the full value is 1, then there is no more space to enter any new data.

If the Empty value is 1, then it means we can add new data in stack organised registers.

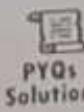
Representation of Register Stack Organisation using PUSH and POP Operation



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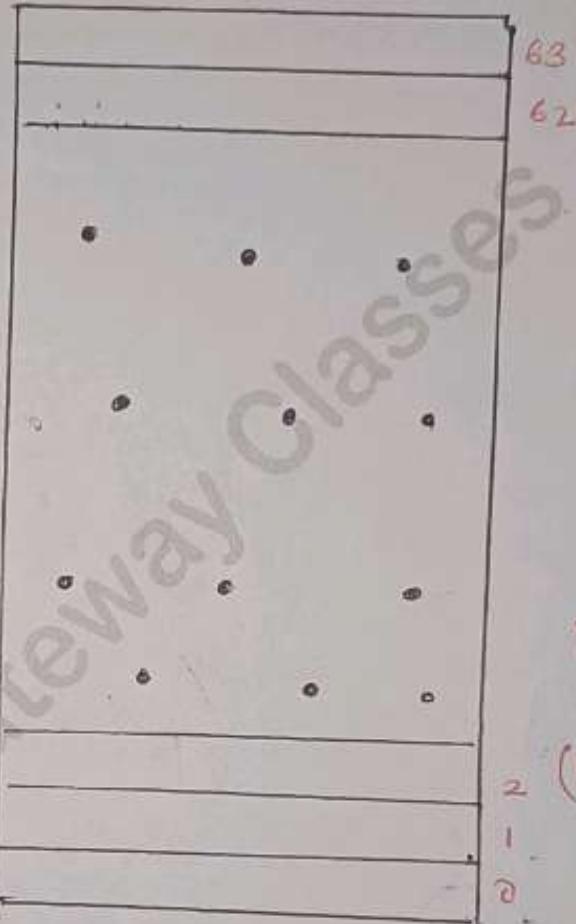
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Register Stack Organisation

full
empty



PUSH

$SP \leftarrow SP + 1$

$M[SP] \leftarrow DR$

if ($SP = 0$) then
($full \leftarrow 1$) and
($empty \leftarrow 0$)

POP

$OR \leftarrow M[SP]$

$SP \leftarrow SP - 1$

if ($SP = 0$) then

2. ($empty \leftarrow 1$) and
1. ($full \leftarrow 0$)

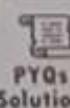
Data Register



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SP points to be a beginning value '2001'. Therefore the stack increases with decreasing addresses. The first element is saved at address 2000, the next element is saved at 1999 and the last element is saved at address 1000.

PUSH OPERATION	POP OPERATION
$SP \leftarrow SP - 1$	$DR \leftarrow K[SP]$
$K[SP] \leftarrow DR$	$SP \leftarrow SP + 1$

Difference between Memory Stack v/s Register Stack

[AKTU 2023-24 / 2021-22]

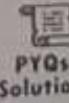
Features	Memory Stack	Register Stack
Location	Located in system RAM	Located in CPU registers
Size	Generally larger, limited by RAM	Generally smaller, limited by the number of the registers.



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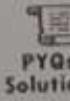
Features	Memory Stack	Register Stack
Access Time	slower access due to Memory latency	faster access due to the proximity to CPU.
Usage	Stores function calls information, location variables.	Stores temporary data during computation.
Management	Managed by OS and compiler	Managed directly by CPU.
Overflow	can lead to the stack overflow if exceeded	Overflow is typically handled by CPU or results in errors.
Access = method	Accessed via memory-addresses	Accessed via CPU registers directly.
Operations	Push and Pop operations LIFO (last in first out)	Push and Pop operations; LIFO [last in, first out].
Performance Impact	slower due to memory access delays.	faster, as registers are part of the CPU.



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Features	Memory Stack	Register Stack
Initialization	Initialized by the operating system and compiler.	Initialized by the CPU automatically during execution.
Scalability	can grow larger as long as RAM allows.	Limited by number of hardware register.
Functionality	Used for managing function calls and local variables.	Limited by the number of available CPU Used for fast access to frequently used data registers.

Question 1: The instruction is stored at location 300 with its address fields at location 301. The address field has the value 400. A processor register (R1) contains the value 200 and evaluate the effective address if the addressing mode of the instruction is

- (a) Direct
- (b) Indirect
- (c) Immediate
- (d) Register Indirect/ direct
- (e) Relative and indexed (consider R1 as Index register)
- (f) Auto increment
- (g) Auto decrement



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Solution :-

ADDRESSING MODE	EFFECTIVE ADDRESS
Implied / Implicit	-
Stack	-
Immediate	301
Direct	400
Indirect	M [400]
Register Direct	A1 [Register name]
Register Indirect	200
Relative	$\text{PC} + \text{Address} = 302 + 400$ $= 702$
Indexed	$\text{Indexed Register} + \text{Address Part} = 200 + 400 = 600$
Auto Increment	200
Auto Decrement	$200 - 1 = 199$



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Question 2: The effective address is the actual memory location where data is accessed or stored, computed by using the addressing mode of an instruction

$$PC = 200$$

$$R1 = 400$$

$$XR = 100 \text{ (INDEXED REGISTER)}$$

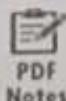
AC

ADDRESS	LOAD TO	MODE
200	AC	
201	ADDRESS = 500	
202	NEXT INSTRUCTION	
399	450	
400	700	
500	800	
600	900	
700	333	
702	325	
800	300	

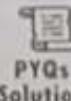
Solution :-



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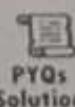
ADDRESSING MODE	EFFECTIVE ADDRESS	CONTENT OF AC / CONTENT OF EFFECTIVE ADDRESS
Immediate	201	500
Direct	500	800
Indirect	800	300
Register direct	31	400
Register Indirect	400	700
Relative	PC + Address = 20 + 500 702	325
Indexed	XR + Address = 100 + 500 = 600	900
Auto - Increment	400	700
Auto - Decrement	399	450



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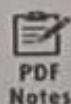
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IMPORTANT POINTS :

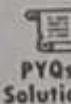
- ① Number of Multiplexer = Number of bits in a register.
- ② Number of input line = Number of Register (n)
- ③ Number of Selection Line = $\log_2 n$
- ④ Size of Multiplexer = $n \times 1$



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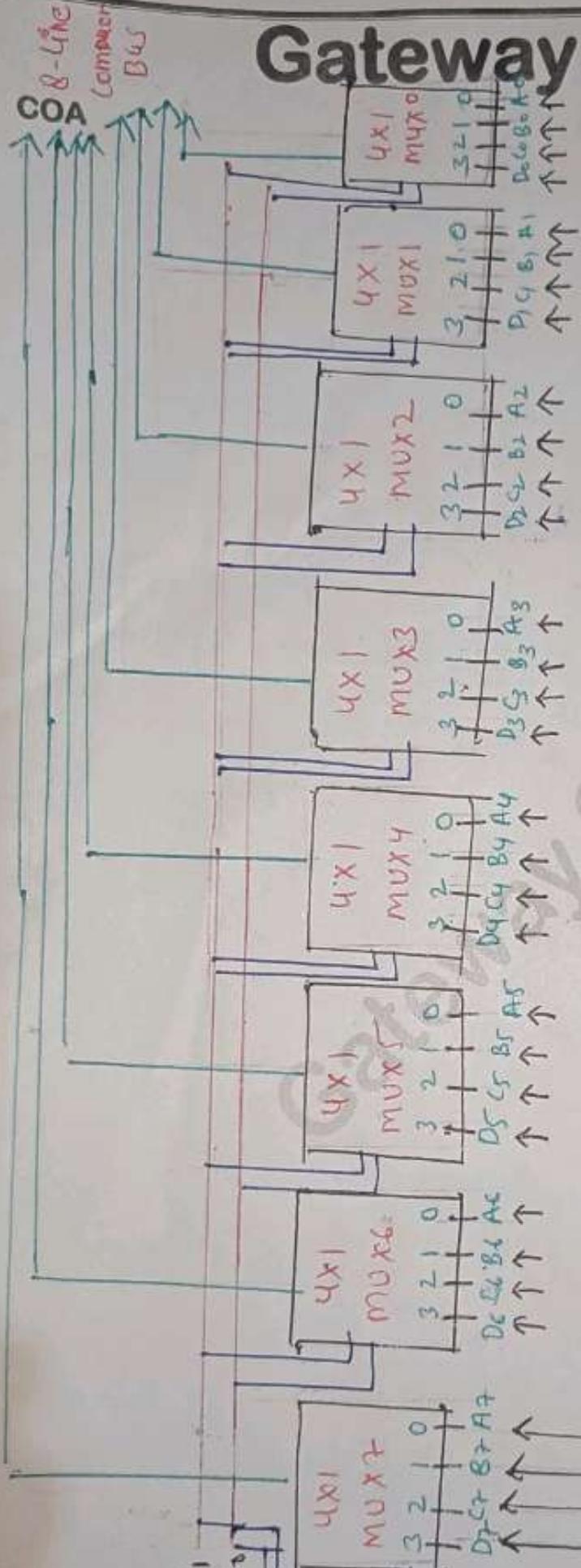


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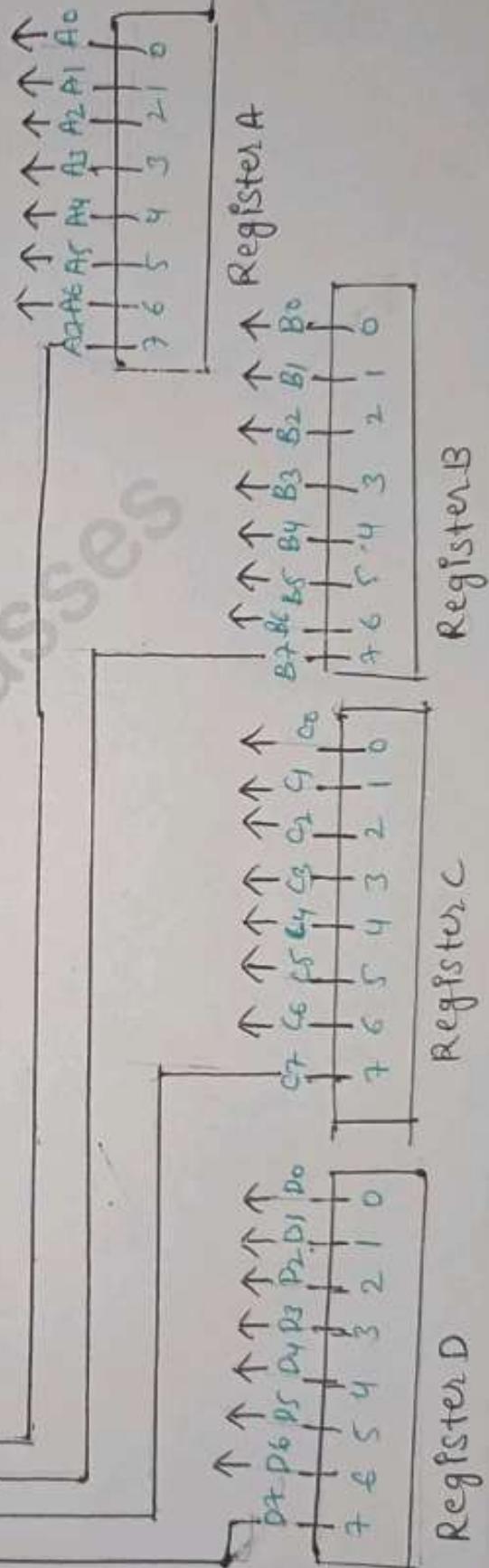


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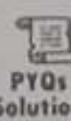
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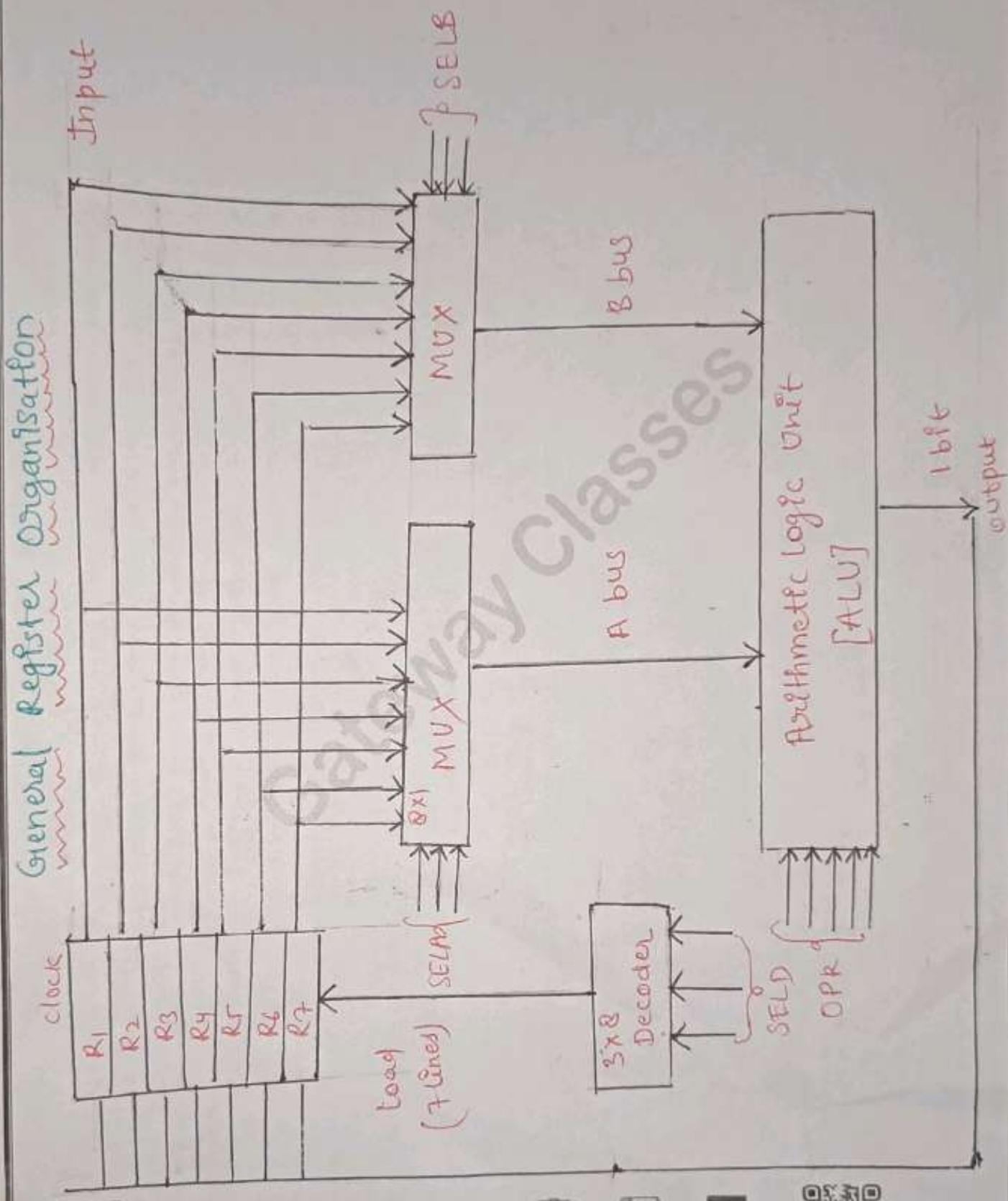


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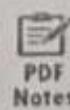
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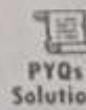
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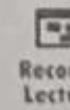
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Question 37 A bus-organized CPU has 16 register and width 32 bits in each, an ALU, and a destination decoder.

1. How many multiplexers are there in a bus what is the size of Multiplexer?
2. How many selection lines are needed for multiplexers (MUXA and MUXB).
3. How many input (select) and output line in decoder.
4. How many input and output are there in the ALU for data including input and output carrier.
5. Formulate a control word for the system assuming that ALU has 35 operations.

Solution 37 :-

(Bus A | Bus B)

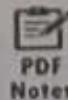
$$\text{Number of Multiplexers} = \frac{\text{Number of bits in Register}}{32} = 16$$

$$\text{Number of Input Lines} = \text{Number of Register} = 16$$

$$\begin{aligned}\text{Size of Multiplexer} &= \frac{\text{Number of Input Lines} \times 1}{16 \times 1} \\ &= 16\end{aligned}$$



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②

Number of Selection Lines = 4

BUSA BUSB
(MUX)

Input Lines in decoder = 4 (Selection Line)

Output Line decoder = 16

Input Lines in ALU = 32 bit + 32 bit + 1 bit
(from (from (input
BUSA) BusB) carriers)
= 65 bit

Output Lines in ALU = 32 bit + output (1 bit carrier)
= 33 bit.

CONTROL WORD

4 bit	4 bit	4 bit	6 bit
SELA	SELB	SELD	OPR

18 bits



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Question 4:- A bus-organised CPU has 8 registers with 16 bits in each, an ALU, destination decoder.

1. How many multiplexor are there in A bus what is the size of multiplexers?
2. How many selection lines are needed for multiplexers and decoder?
3. Formulate a control word for the system assuming that ALU has 35 Operations.

[AKTU 2018-19]

Solution 4:-

① Number of Multiplexer = Number of bits \log_2 = 16
Bus A Register

Number of Input Lines = Number Of Register = 8

Size of Multiplexer = Number of Input Lines \times 1
 8×1

② Number of Selection Line in Multiplexer and decoder = 3

③

3 bits	3 bits	3 bits	6 bits	
SEL A	SEL B	SEL C	OPR	\Rightarrow 15 bits



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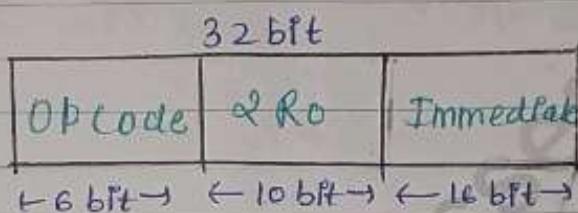
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Question 5 :- A Processor has 40 distinct instruction and 24 general purpose registers. A 32 bit instruction word has an OPCODE, two registers Operands and an immediate Operand. The number of bits available for the Immediate Operand field is?

[AKTU 2020-21]

Solution 5 :-



$$\text{Number of distinct instructions} = 40$$

$$\text{Number of bit to represent 1 instruction} = 6$$

$$\text{Number of Register} = 24$$

$$\text{Number of bits to represents 1 register} = 5$$

$$2 \text{ Register Operand} = 10 \text{ bit}$$

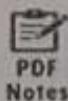
$$\text{Immediate Operand bit} = \text{Total instruction size} - (10 + 6)$$

$$= 32 - 16$$

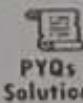
$$= 16 \text{ bits}$$



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Question

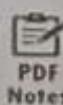
The instruction is stored at location 700 with its address fields at location 701. The address field has the value 1000. A processor register contains the value 500 and index register contains the value 300. Evaluate the effective address if the addressing mode of the instruction is
 (A) Direct (B) Indirect (C) Immediate (D) Relative (E) Register-Indirect (F) Auto Increment (G) Auto Decrement.

Solution:

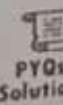
	Addressing Mode	Effective Address
700	OPcode / Mode	1000
701	Address	M[1000]
702	IR = 1000	701
703	NR = 300	PC + Address
704		702 + 1000 \Rightarrow 1702
<hr/>		
let Processor Register PC = 500 IR = 300 (Index Register) PC = 702		
Register Indirect Auto Increment Auto Decrement		
500 500 500 - 1 \Rightarrow 499		



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Question: If a two word instruction is start at a memory location 200 and its address is 500 started at location 201. If the contents at location 400 is 700, 500 is 800, 600 is 900, 702 is 325 and 800 is 300 and a processor register R has the value 400. Evaluate the effective address and contents of AC if the addressing modes are Immediate, Direct, Indirect, Register, Register Indirect, Relative and Indexed.

Solution

from the given data
load to AC

	OP Code	Mode
200		
201	Address = 500	
400	700	
500	800	
600	900	
700	325	
800	300	

Index Reg



R = 400

PC = 202



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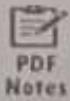
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Addressing Mode	Effective Address	Content of Ac / Content of Effective Address
Immediate	201	500
Direct	500	800
Indirect	800	300
Register	R	400
Register Indirect	400	700
Relative	Pc + Address $202 + 500 = 702$	325
Indexed Register	$400 + 500 = 900$	M [900]



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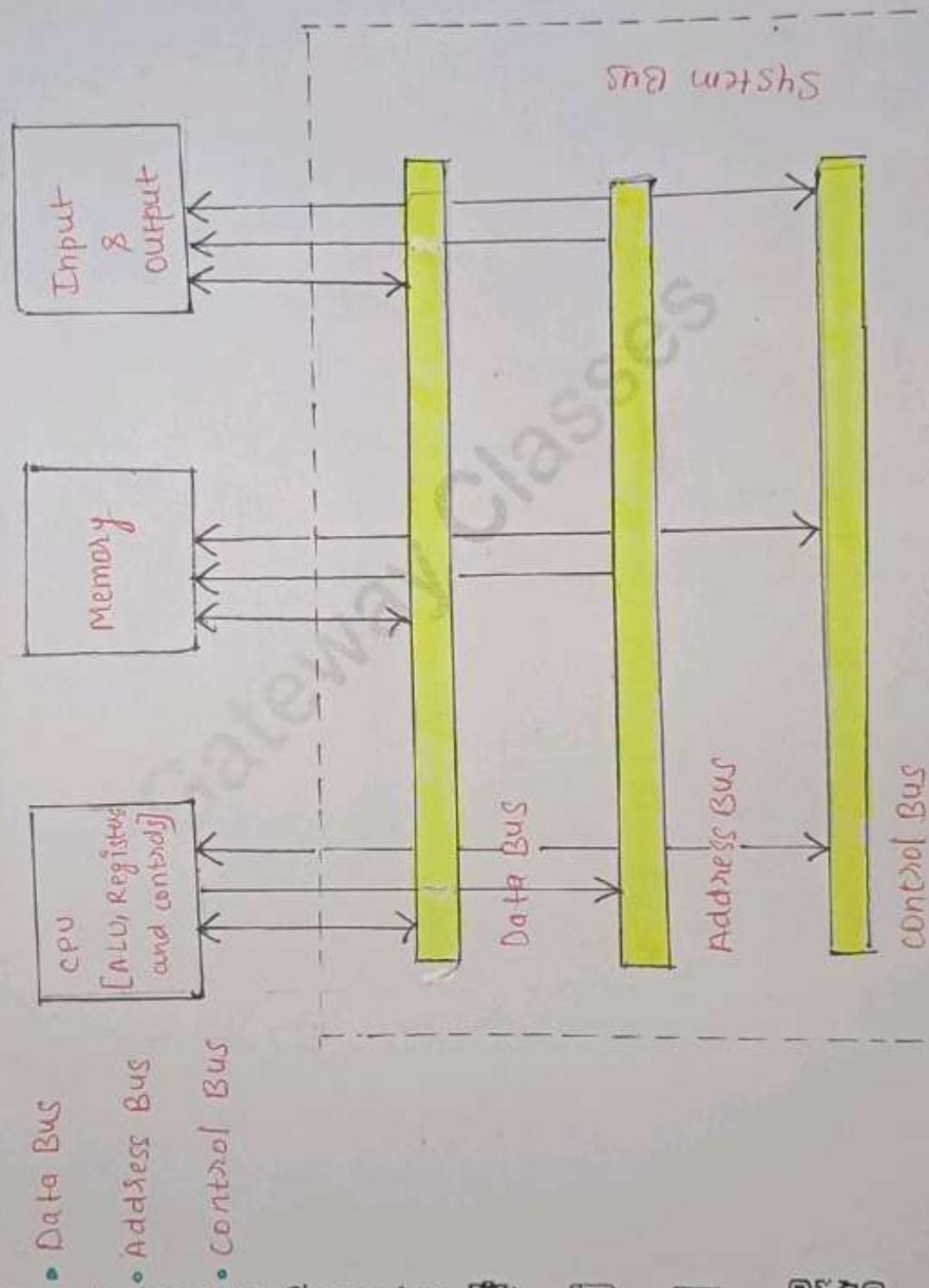
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MAJOR COMPONENT OF SYSTEM BUS (AKTU 2015-16)

MAJOR COMPONENT OF SYSTEM BUS

(AKTU 2015-16)



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Question: How operation performed by the stack evaluate

$$(A+B/C \times (D+C)-F)$$

How expression are evaluated using stack

Solution

Symbol	Stack	Postfix
((-
A	(A
+	(+	A
B	(+	AB
/	(+ /	AB
C	(+ /	ABC
*	(+ * /	ABC /
((+ * (/	ABC /
D	(+ * (/ D	ABC / D
+	(+ * (+ /	ABC / D
C	(+ * (+ / DC	ABC / DC
)	(+ * / DC +	ABC / DC +
-	(- / DC + * +	ABC / DC + * +
F	(- / DC + * + F	ABC / DC + * + F
)	(- /	ABC / DC + * + F -

Question: How operation performed by the stack Evaluate

[AKTV 2022-23]



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$$X = (5 + 6 * (8 - 2 * 3))$$

How expression are evaluated Using Stack

[2018-19]

Solution :-

Symbol	Stack	Post fix
(C	-
5	- C	5
+	C+	5
6	C+	56
*	(+*	56
((+*(56
8	(+*(C	568
-	(+*(C-	568
2	(+*(C-	5682
*	(+*(C-*	5682
3	(+*(C-*	56823
)	(+*	56823*-
)	—	56823*-*+

Short trick

$$5 + 6 * (8 - 2 * 3)$$

$$5 + 6 * (8 - 2 * 3 *)$$

$$5 + 6 * \frac{8 - 2 * 3}{*} -$$

$$5 + 6 8 2 3 * - *$$

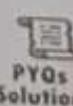
$$\boxed{5 6 8 2 3 * - * +}$$



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MULTIPLE BUS HIERARCHY

A multiple bus hierarchy in computer architecture refers to a system design where multiple buses are used to connect different components, such as CPUs, memory and I/O devices.

Need for Multiple Bus Hierarchy in Computer Architecture:

① Performance Improvement :-

A single bus architecture often becomes a bottleneck as it forces all the data transfers through one bus, leading to congestion.

② Multiple bus hierarchy allows different components (CPU, memory, I/O devices) to communicate simultaneously, reducing waiting times and improving overall system performance.

③ Parallelism :-

With multiple buses, data transfers can occur in parallel across different buses, enabling multiple operations to be carried out simultaneously.



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(4)

Scalability :

As system grow complexity (e.g., adding more CPUs, memory modules, or I/O devices) a single bus can become overwhelmed.

Multiple bus hierarchy provides scalability by distributing the load across several buses ensuring that the system can handle increased demand without significant performance degradation.

(5)

Reduced Latency :

In a single bus system, components often have to wait for the bus to become available, increasing latency.

A multiple bus hierarchy reduces this latency by allowing different buses to handle specific tasks (e.g.: a dedicated memory bus), ensuring quicker data access and the transfer of data.



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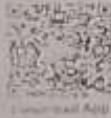
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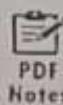
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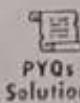
Traditional Hierarchical Bus Architecture



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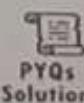
- Isolate processor to memory traffic from I/O Traffic.
- Cache - memory act as an interface to a system bus.
- Expansion bus interface it to the external devices.
- Local bus support cache memory and one more local devices.
- Cache memory attached.
- Expansion bus interface buffer data transfer between the System bus and I/O bus.
- This arrangement allows the systems to support a wide variety of I/O devices.
- So this architecture is efficient.



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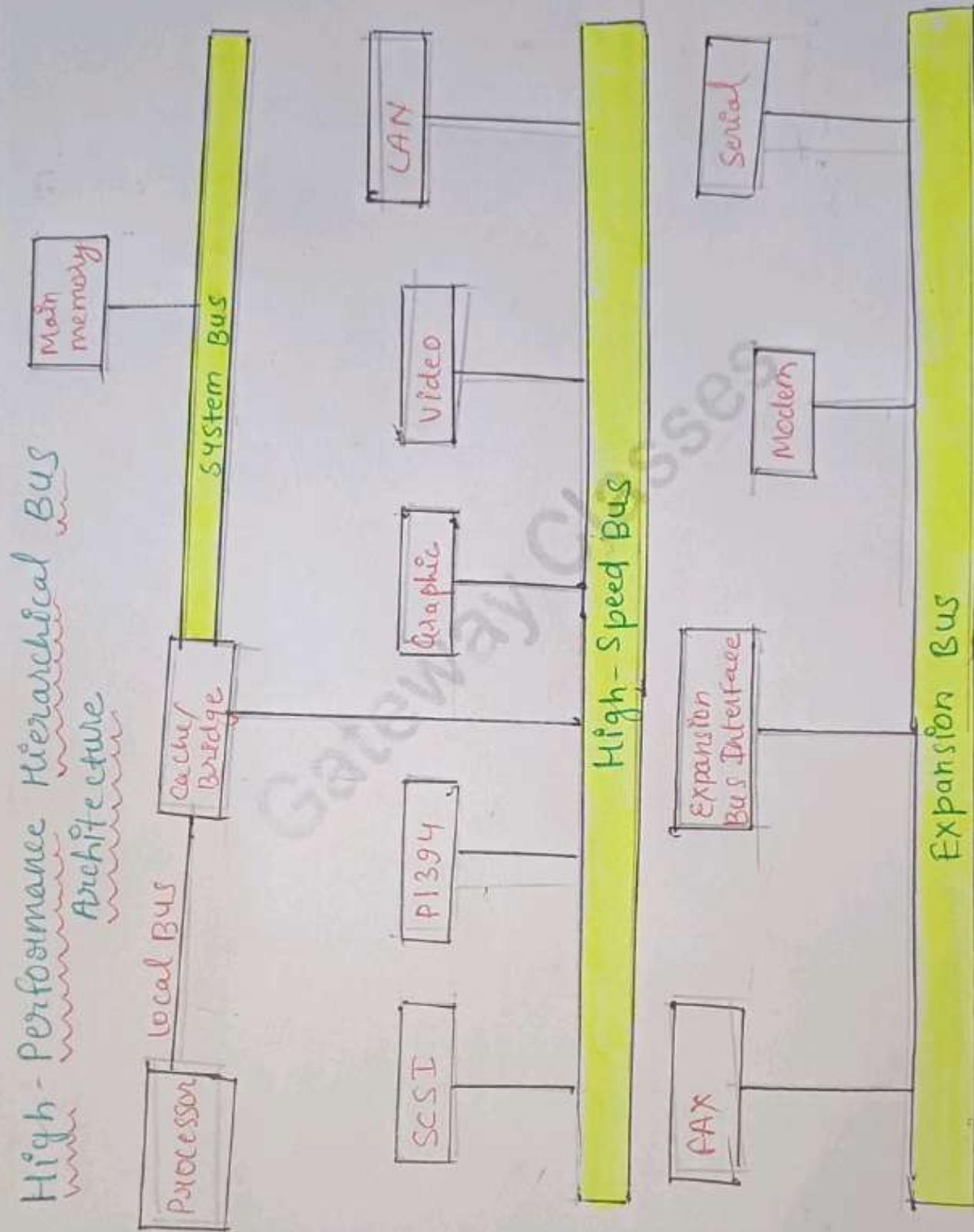


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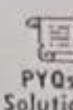


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High-Performance Hierarchical Bus Architecture

- This architecture requires a bridge between the processor's bus and the high speed bus.
- There is a local bus that connects the processor to a cache controller, which is turn is connected to a system bus that supports main memory.
- The cache controller is integrated into a bridge or buffering device, that connects to a high-speed bus. This bus supports connection to high speed LANs.



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