ELD

* combinational circuit : The output depends upon the present input (same clock cycle)

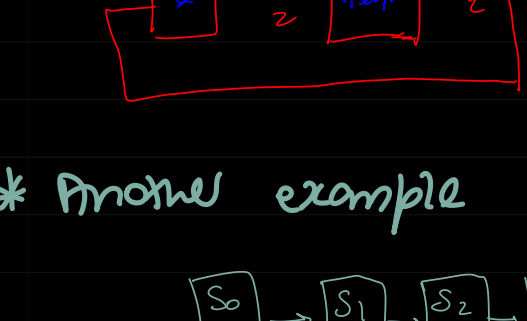
* sequential circuit : output depends upon the current input and the current state of the circuit

(you need current state of circuit, need to store state ✓, hence we use flip flops ✓; Note: we need not store current input)

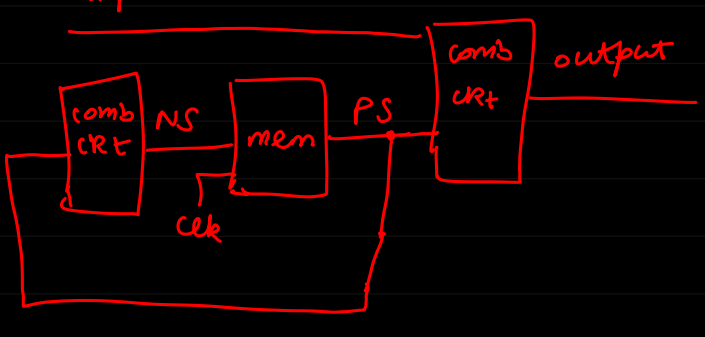
What we get → output + next state (because we go from one state to another)

⇒ Note: combinational circuits use clock as its an input as well.

* D flip flop (edge triggered) : input is stored at falling or rising edge of the clock (next state becomes current state)

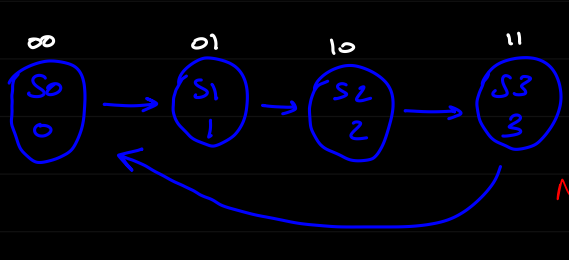


* Sequential circuit using combinational ckt



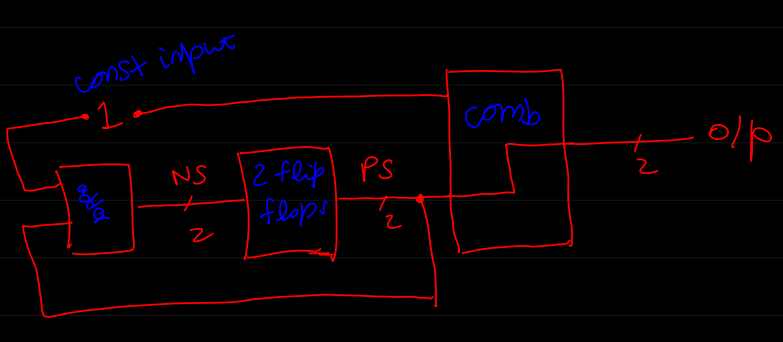
* FSM (finite state machine)

⇒ up counter

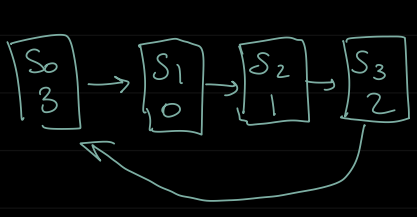


Note: if curr state = S_n, the output is n

2 bits required to store in mem

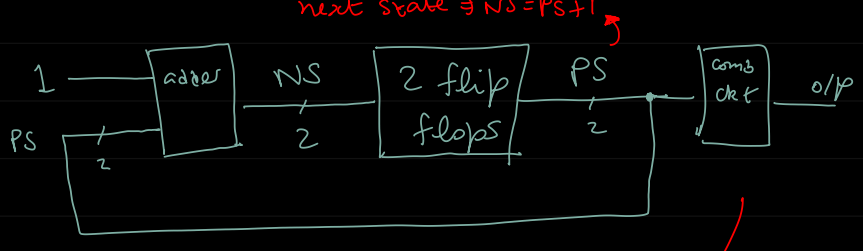


* Another example



$S_0 = 00$
$S_1 = 01$
$S_2 = 10$
$S_3 = 11$

relation btw present state & next state ⇒ NS = PS + 1



eg: if PS = S_0 (00) ⇐ Here we should use 2 not gates for the 2 bits

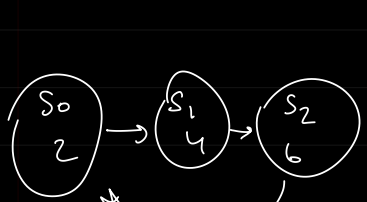
output is 3 (11)

i.e. NOT(0), NOT(0) ⇒ (11)

So, we are storing current state + processing input (using comb ckt)

* Example : 3

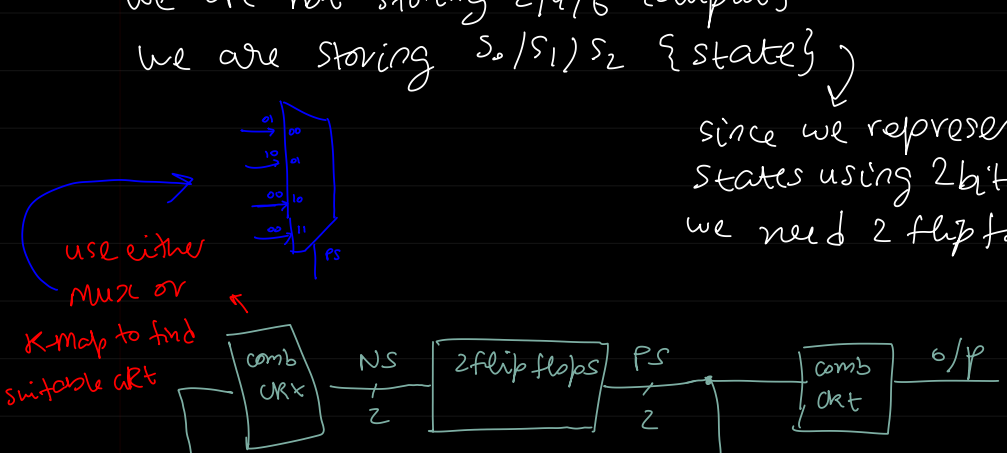
counter : 2 → 4 → 6



S_0 00
S_1 01
S_2 10

we are not storing 2/4/6 {outputs}
we are storing $S_0/S_1/S_2$ {states}

since we represent states using 2 bits, we need 2 flip flops



NOTE: no. of states is equal to no. of flip flops

* Any combinational circuit can be implemented using memory (↳ lookup table) LUT

In DC, we learnt that we can implement any comb. ckt using gates.

However implementing it using memory is more versatile since we can always change memory (i.e. it is dynamic)

Conclusion,

Combinational ckts can be implemented using...

① Pure gates
② Lookup Table

* FPGA Field Programmable Gate Array

→ Array of generic logic gates

→ Gates where logic function can be programmed

→ Programmable interconnection btw gates

→ Field : System can be programmed in the field (after fabrication)

CLB : configurable logic blocks

BUFG : global buffer
BUFR : regional "
BUFIO : input/output "

* Comb CKts on FPGA
≡ Generic FPGA Design Flow