ELD LAB 7 CLASSWORK

Aditya Gautam
2023043

Project Structure

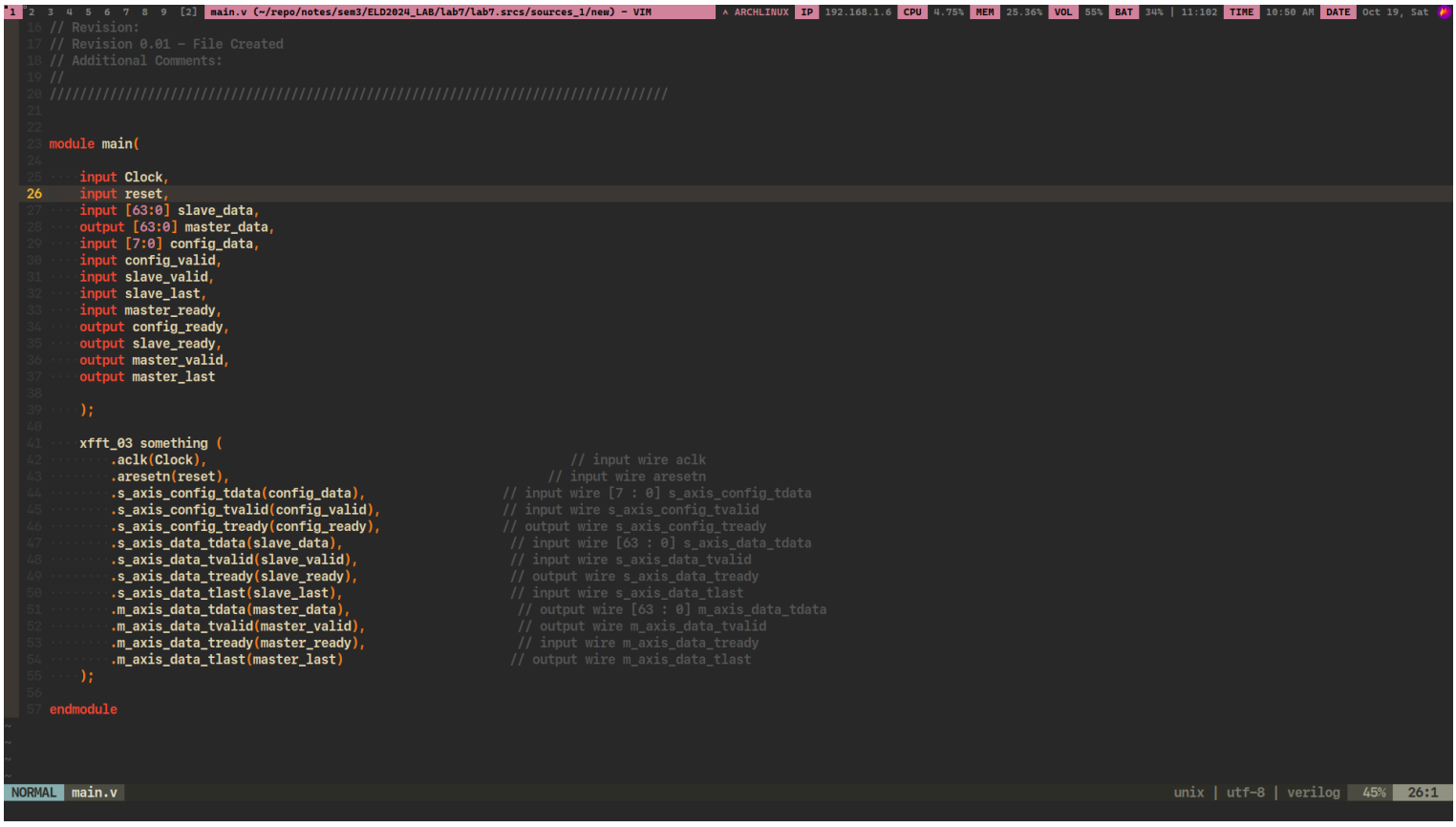
```
main.v
|__  xfft_03.xci
```

Code

- main.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/15/2024 09:38:43 AM
// Design Name:
// Module Name: main
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module main(

	input Clock,
	input reset,
	input [63:0] slave_data,
	output [63:0] master_data,
	input [7:0] config_data,
	input config_valid,
	input slave_valid,
	input slave_last,
```

```
        input master_ready,
        output config_ready,
        output slave_ready,
        output master_valid,
        output master_last

        );

        xfft_03 something (
        .aclk(Clock),                                           // input wire aclk
        .aresetn(reset),                                        // input wire aresetn
        .s_axis_config_tdata(config_data),                  // input wire [7 : 0] s_axis_config_tdata
        .s_axis_config_tvalid(config_valid),                // input wire s_axis_config_tvalid
        .s_axis_config_tready(config_ready),                // output wire s_axis_config_tready
        .s_axis_data_tdata(slave_data),                     // input wire [63 : 0] s_axis_data_tdata
        .s_axis_data_tvalid(slave_valid),                   // input wire s_axis_data_tvalid
        .s_axis_data_tready(slave_ready),                   // output wire s_axis_data_tready
        .s_axis_data_tlast(slave_last),                     // input wire s_axis_data_tlast
        .m_axis_data_tdata(master_data),                    // output wire [63 : 0] m_axis_data_tdata
        .m_axis_data_tvalid(master_valid),                  // output wire m_axis_data_tvalid
        .m_axis_data_tready(master_ready),                  // input wire m_axis_data_tready
        .m_axis_data_tlast(master_last)                     // output wire m_axis_data_tlast
        );

endmodule
```



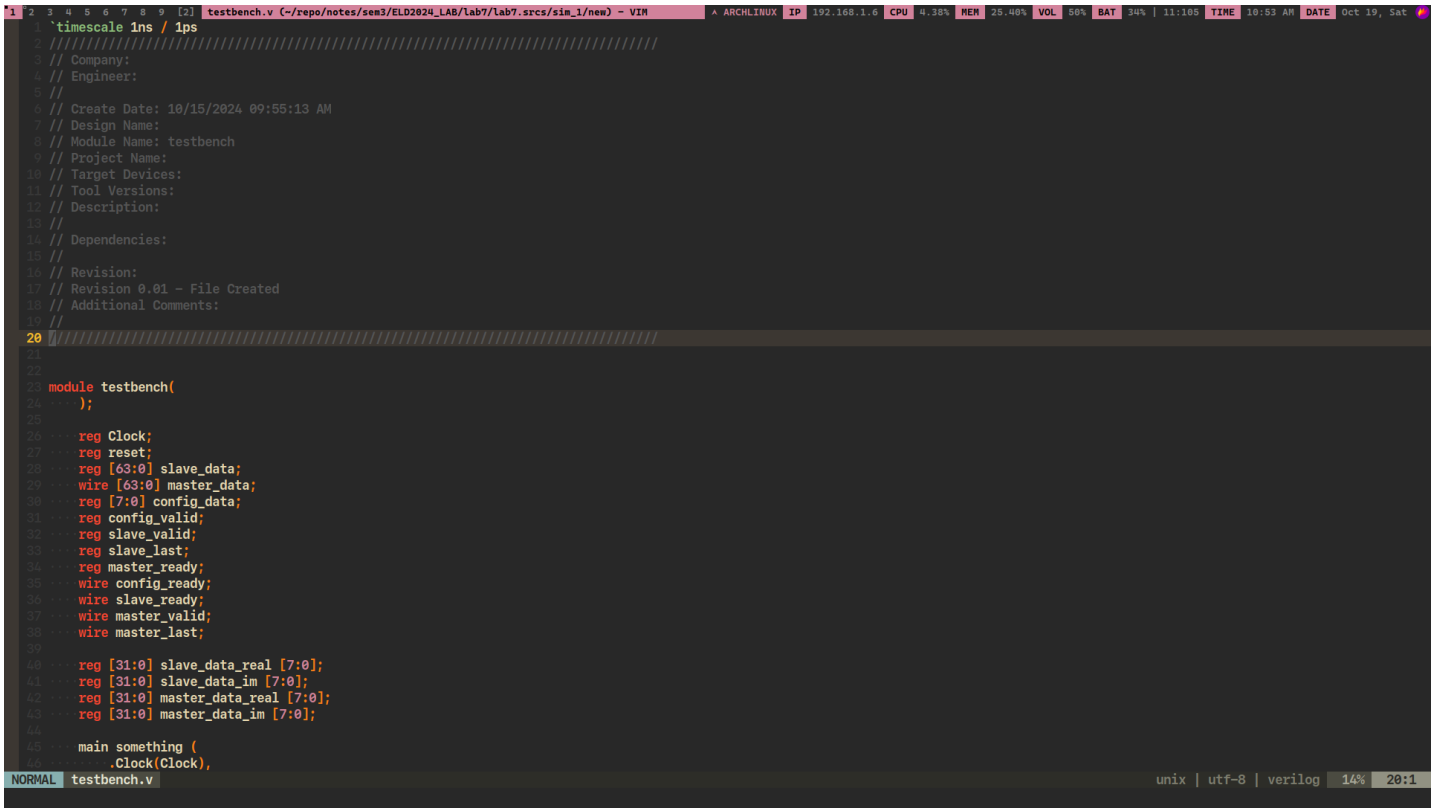
- testbench.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/15/2024 09:55:13 AM
// Design Name:
// Module Name: testbench
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module testbench(
       );

       reg Clock;
       reg reset;
       reg [63:0] slave_data;
       wire [63:0] master_data;
       reg [7:0] config_data;
       reg config_valid;
       reg slave_valid;
       reg slave_last;
       reg master_ready;
       wire config_ready;
       wire slave_ready;
       wire master_valid;
       wire master_last;

       reg [31:0] slave_data_real [7:0];
       reg [31:0] slave_data_im [7:0];
       reg [31:0] master_data_real [7:0];
       reg [31:0] master_data_im [7:0];

       main something (
       .Clock(Clock),
       .reset(reset),
       .slave_data(slave_data),
       .master_data(master_data),
       .config_data(config_data),
       .config_valid(config_valid),
       .slave_valid(slave_valid),
```

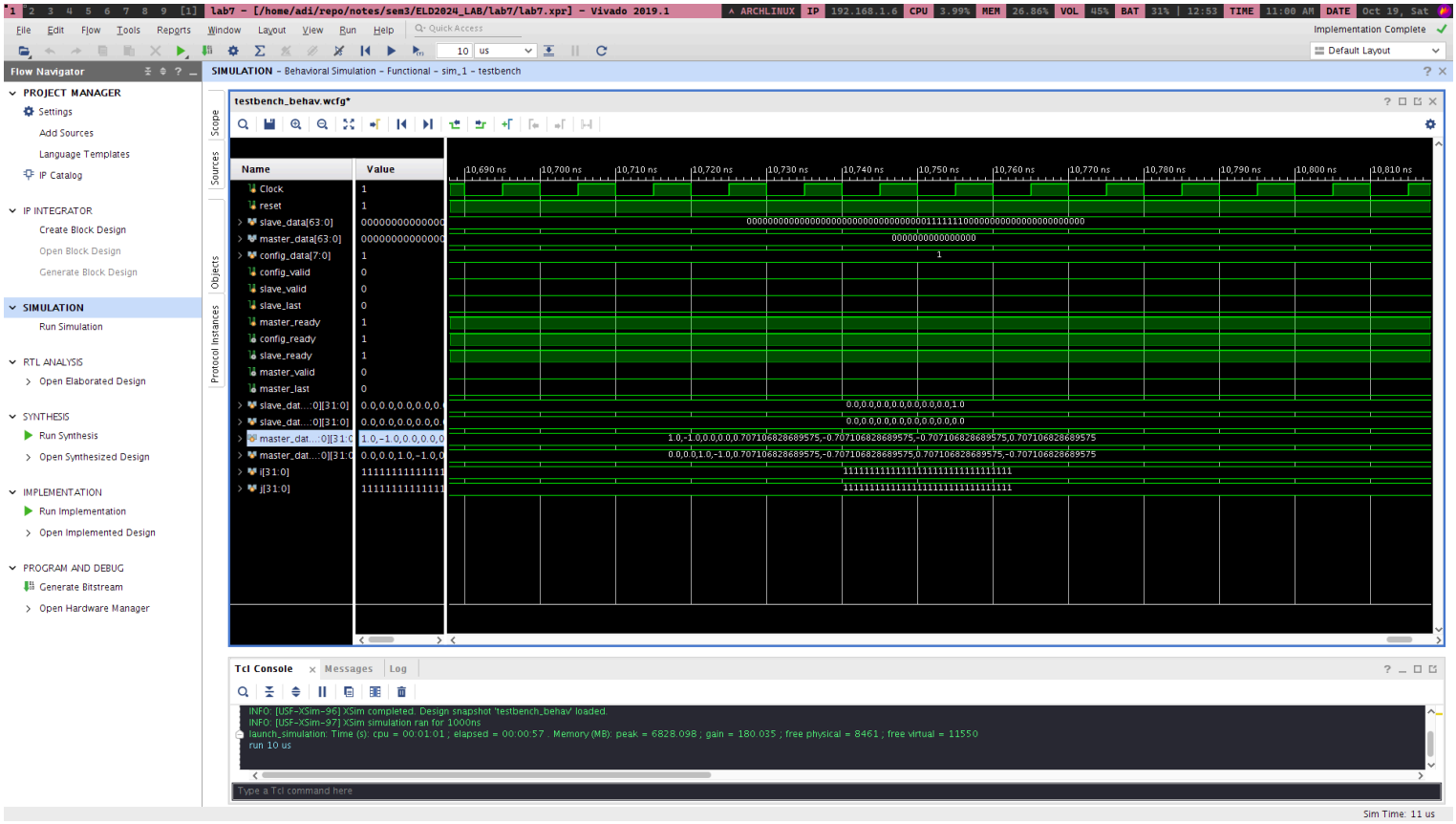
```
.slave_last(slave_last),
.master_ready(master_ready),
.config_ready(config_ready),
.slave_ready(slave_ready),
.master_valid(master_valid),
.master_last(master_last)
);

// init
initial
begin
	Clock = 0;
	reset = 0;
	config_valid = 0;
	config_data = 0;
	slave_valid = 0;
	slave_data = 0;
	slave_last = 0;
	master_ready = 1;
end

// clock
always
#5 Clock = ~Clock;

// input
initial
begin
	slave_data_real[0] = 32'h3f800000;
	slave_data_im[0] = 32'h0;
	slave_data_real[1] = 32'h0;
	slave_data_im[1] = 32'h0;
	slave_data_real[2] = 32'h0;
	slave_data_im[2] = 32'h0;
	slave_data_real[3] = 32'h0;
	slave_data_im[3] = 32'h0;
	slave_data_real[4] = 32'h0;
	slave_data_im[4] = 32'h0;
	slave_data_real[5] = 32'h0;
	slave_data_im[5] = 32'h0;
	slave_data_real[6] = 32'h0;
	slave_data_im[6] = 32'h0;
	slave_data_real[7] = 32'h0;
	slave_data_im[7] = 32'h0;
end

// config
initial
begin
	#70 reset = 1;
	config_data = 1; // forward fft not inverse
	config_valid = 1;
	while(config_ready == 0)
	#2 config_valid = 1;
```

```
        #10 config_valid = 0;
    end

    // input
    integer i,j;
    initial
    begin
        #70 for(i=7;i≥0;i=i-1) begin
        #10 if(i==0)
            slave_last = 1;
        slave_data = {slave_data_im[i],slave_data_real[i]};
        slave_valid = 1;
        while(slave_ready == 0)
            #2 slave_valid = 1;
        #10 slave_valid = 0;
        slave_last = 0;
        end
    end

    // output
    initial
    begin
        for(j=7;j≥-1;j=j-1) begin
        #5 master_ready = 1;
        wait(master_valid == 1);
        {master_data_im[j],master_data_real[j]} = master_data;
        #10 master_ready = 0;
        end
        #20 $stop;
    end
```

endmodule



OUTPUT


lab7 - [/home/adi/repo/notes/sem3/ELD2024_LAB/lab7/lab7.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Run Help
Implementation Complete
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
SIMULATION - Behavioral Simulation - Functional - sim_1 - testbench
testbench_behav.wcfg*
Scope
Sources
Objects
Protocol Instances
Name
Value
Clock
reset
slave_data[63:0]
master_data[63:0]
config_data[7:0]
config_valid
slave_valid
slave_last
master_ready
config_ready
slave_ready
master_valid
master_last
slave_dat...:0][31:0]
slave_dat...:0][31:0]
master_dat...:0][31:0]
master_dat...:0][31:0]
i[31:0]
j[31:0]
10,690 ns
10,700 ns
10,710 ns
10,720 ns
10,730 ns
10,740 ns
10,750 ns
10,760 ns
10,770 ns
10,780 ns
10,790 ns
10,800 ns
10,810 ns
Tcl Console
Messages
Log
INFO: [USF-XSim-96] XSim completed. Design snapshot 'testbench_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:01:01 ; elapsed = 00:00:57 . Memory (MB): peak = 6828.098 ; gain = 180.035 ; free physical = 8461 ; free virtual = 11550
run 10 us
Type a Tcl command here
Sim Time: 11 us