ELD LAB 4 HOMEWORK
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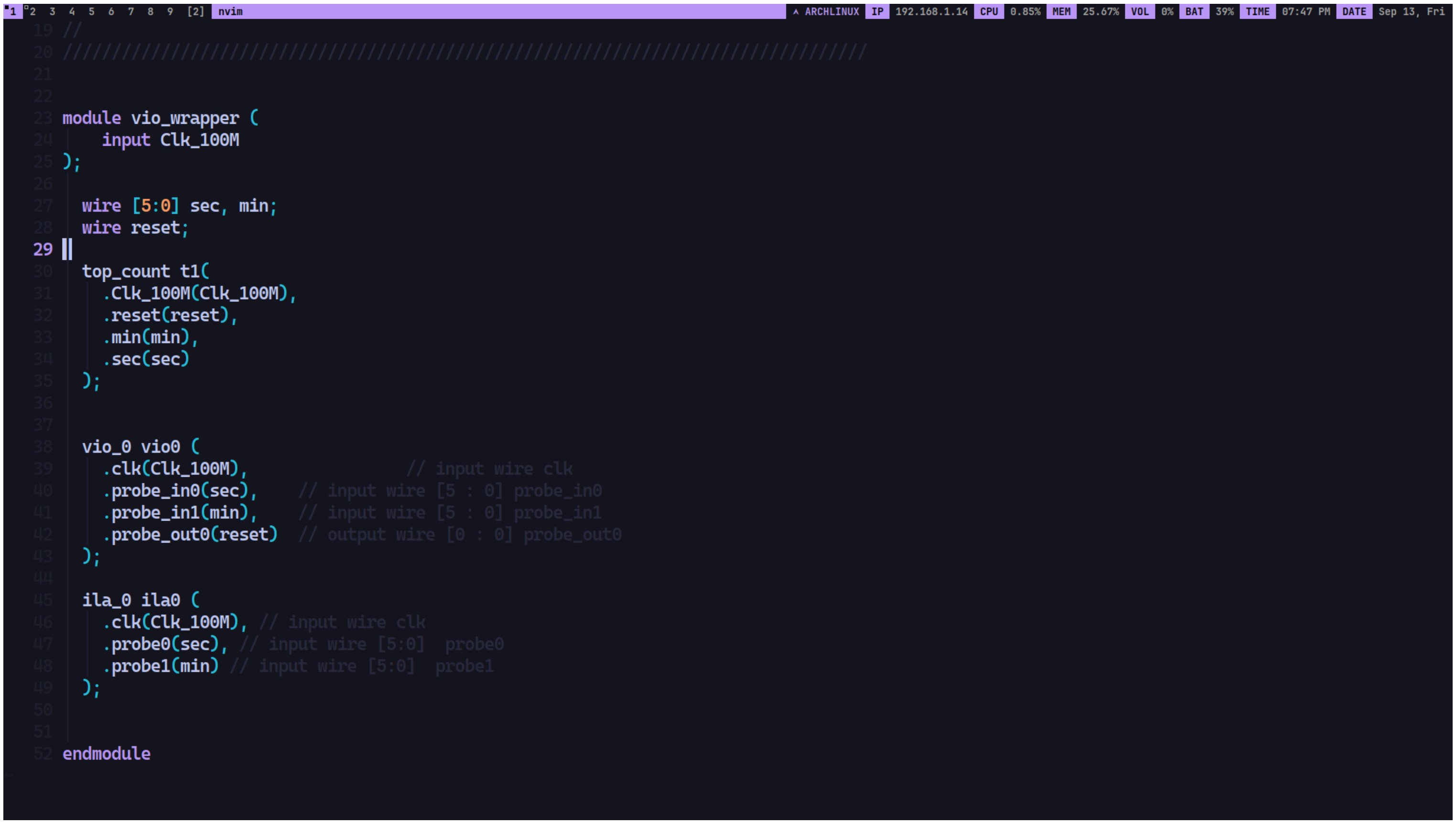
- Project Directory

```
vio_wrapper.v
|__ top_count.v
|    |__ clock_wizard_ip (cmt)
|    |__ clk_div_rtl.v
|    |__ counter_6bit.v (= digital counter)
|__ vio_ip (virtual input output)
|__ ila_ip (integrated logic analyzer)
```

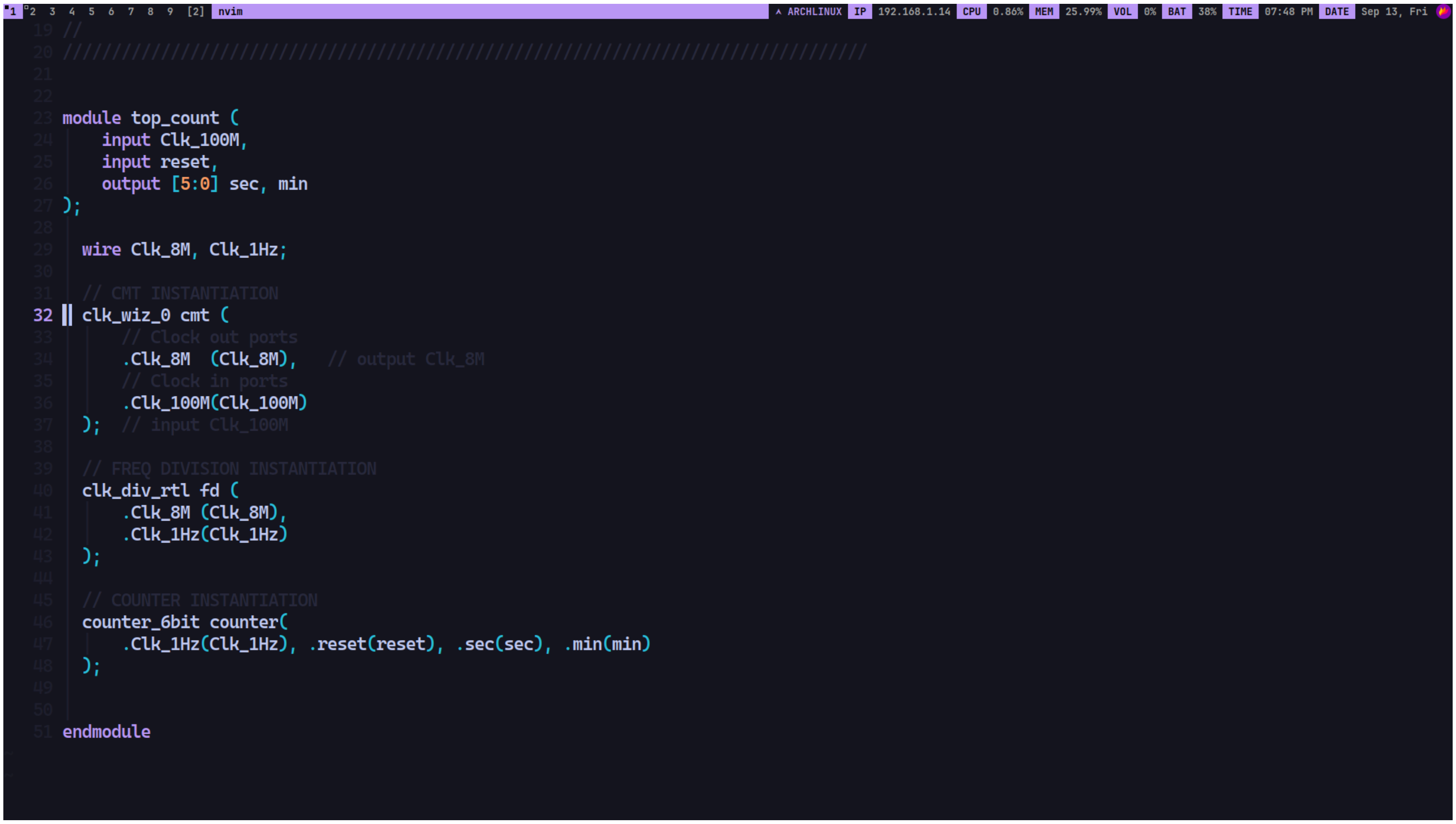
- Files

– vio_wrapper.v


1 2 3 4 5 6 7 8 9 [2] nvim
ARCHLINUX IP 192.168.1.14 CPU 0.85% MEM 25.67% VOL 0% BAT 39% TIME 07:47 PM DATE Sep 13, Fri

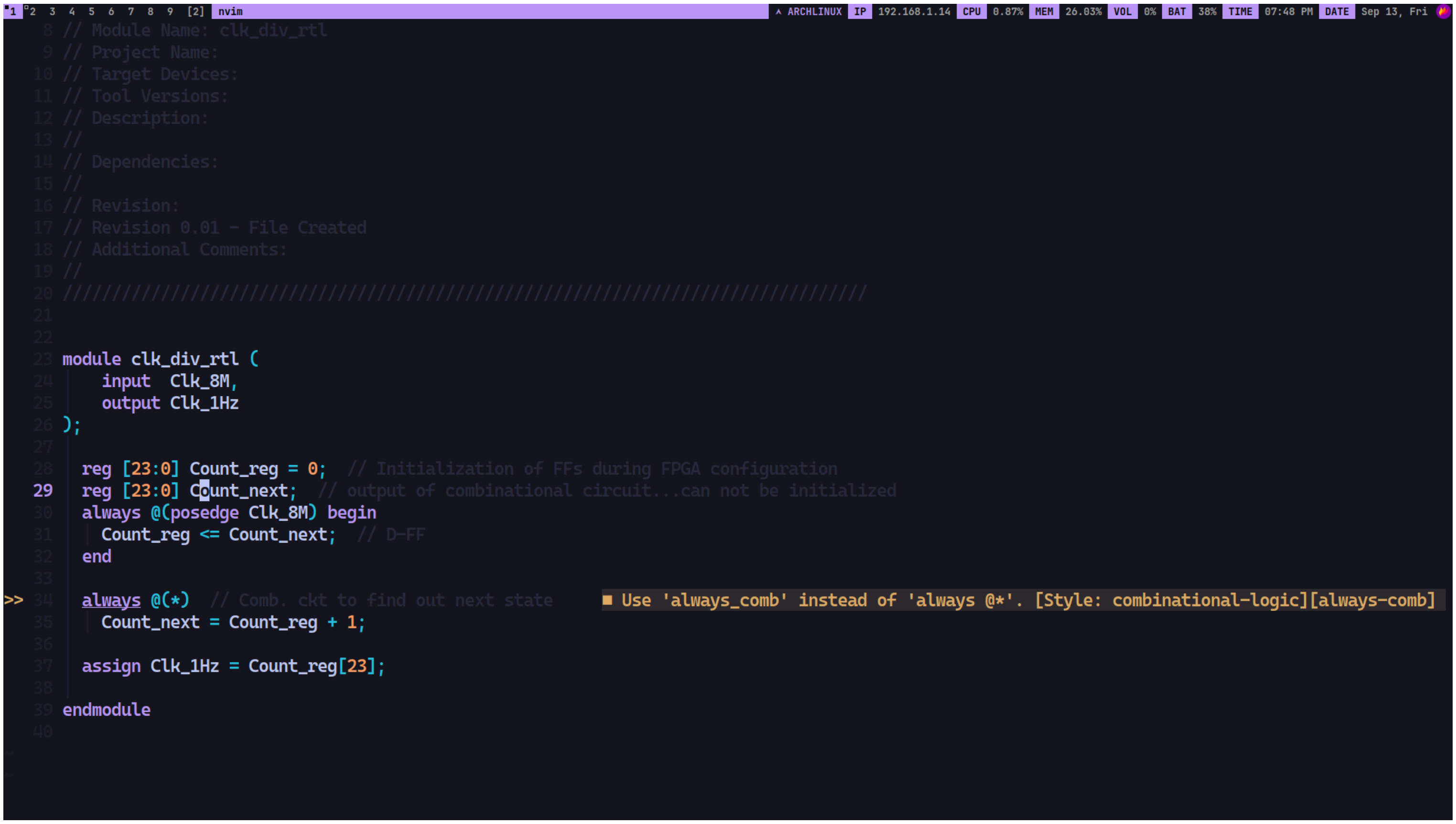
```verilog
//
/////////////////////////////////////////////////////////////////////////////////////


module vio_wrapper (
    input Clk_100M
);

  wire [5:0] sec, min;
  wire reset;

  top_count t1(
    .Clk_100M(Clk_100M),
    .reset(reset),
    .min(min),
    .sec(sec)
  );


  vio_0 vio0 (
    .clk(Clk_100M),                // input wire clk
    .probe_in0(sec),    // input wire [5 : 0] probe_in0
    .probe_in1(min),    // input wire [5 : 0] probe_in1
    .probe_out0(reset)  // output wire [0 : 0] probe_out0
  );

  ila_0 ila0 (
    .clk(Clk_100M), // input wire clk
    .probe0(sec), // input wire [5:0]  probe0
    .probe1(min) // input wire [5:0]  probe1
  );


endmodule
```

- top_count.v


1 2 3 4 5 6 7 8 9 [2] nvim
ARCHLINUX IP 192.168.1.14 CPU 0.86% MEM 25.99% VOL 0% BAT 38% TIME 07:48 PM DATE Sep 13, Fri

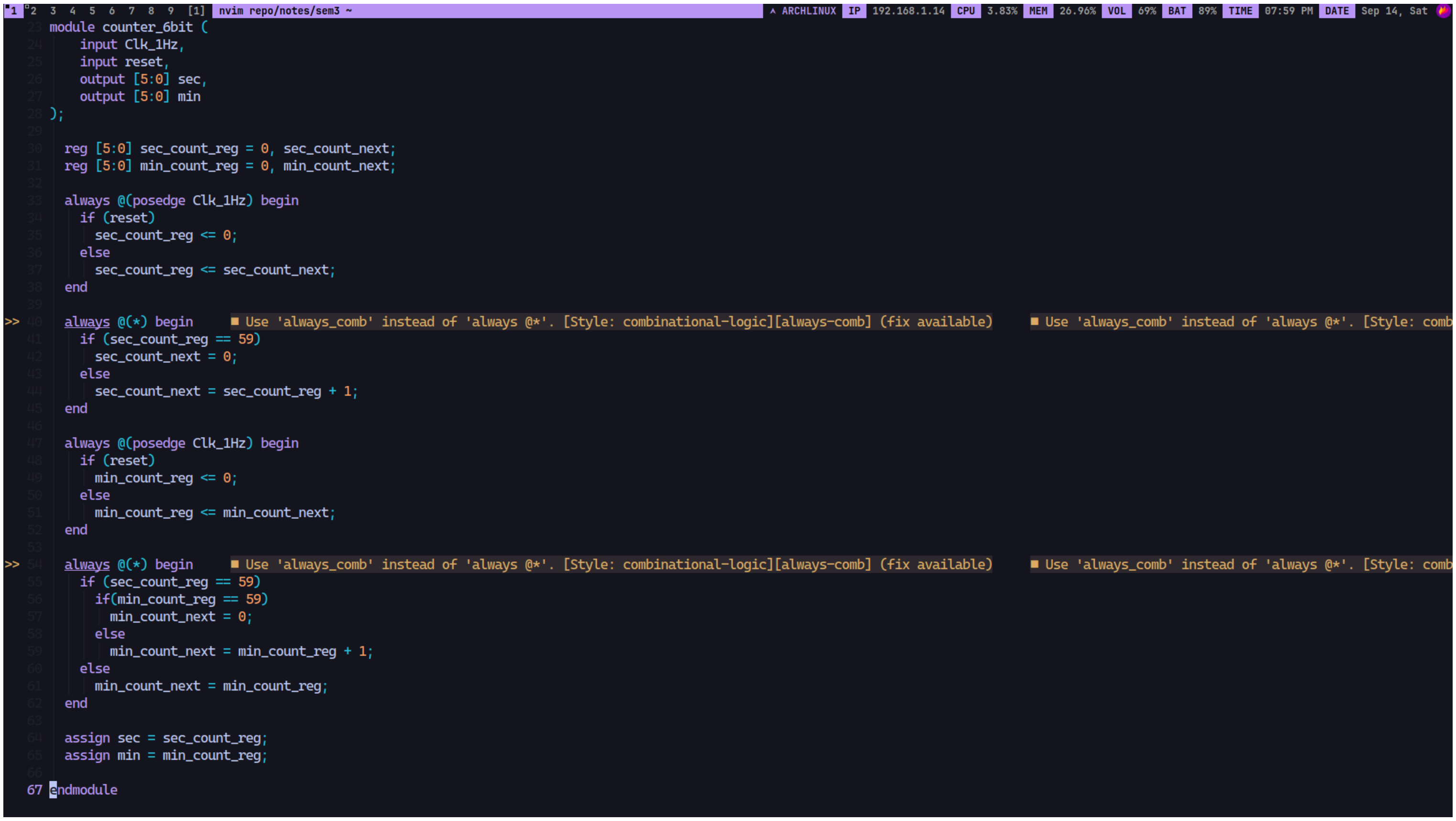
```verilog
//
//////////////////////////////////////////////////////////////////////////////////


module top_count (
    input Clk_100M,
    input reset,
    output [5:0] sec, min
);

  wire Clk_8M, Clk_1Hz;

  // CMT INSTANTIATION
  clk_wiz_0 cmt (
      // Clock out ports
      .Clk_8M  (Clk_8M),    // output Clk_8M
      // Clock in ports
      .Clk_100M(Clk_100M)
  );  // input Clk_100M

  // FREQ DIVISION INSTANTIATION
  clk_div_rtl fd (
      .Clk_8M (Clk_8M),
      .Clk_1Hz(Clk_1Hz)
  );

  // COUNTER INSTANTIATION
  counter_6bit counter(
      .Clk_1Hz(Clk_1Hz), .reset(reset), .sec(sec), .min(min)
  );


endmodule
```

- clk_div_rtl.v


1 2 3 4 5 6 7 8 9 [2] nvim
ARCHLINUX IP 192.168.1.14 CPU 0.87% MEM 26.03% VOL 0% BAT 38% TIME 07:48 PM DATE Sep 13, Fri

```verilog
// Module Name: clk_div_rtl
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module clk_div_rtl (
    input  Clk_8M,
    output Clk_1Hz
);

  reg [23:0] Count_reg = 0;  // Initialization of FFs during FPGA configuration
  reg [23:0] Count_next;  // output of combinational circuit...can not be initialized
  always @(posedge Clk_8M) begin
    Count_reg <= Count_next;  // D-FF
  end

>> always @(*)  // Comb. ckt to find out next state     ■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb]
    Count_next = Count_reg + 1;

  assign Clk_1Hz = Count_reg[23];

endmodule
```

- counter_6bit.v



```
module counter_6bit (
    input Clk_1Hz,
    input reset,
    output [5:0] sec,
    output [5:0] min
);

  reg [5:0] sec_count_reg = 0, sec_count_next;
  reg [5:0] min_count_reg = 0, min_count_next;

  always @(posedge Clk_1Hz) begin
    if (reset)
      sec_count_reg <= 0;
    else
      sec_count_reg <= sec_count_next;
  end

  always @(*) begin     ■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb] (fix available)     ■ Use 'always_comb' instead of 'always @*'. [Style: comb
    if (sec_count_reg == 59)
      sec_count_next = 0;
    else
      sec_count_next = sec_count_reg + 1;
  end

  always @(posedge Clk_1Hz) begin
    if (reset)
      min_count_reg <= 0;
    else
      min_count_reg <= min_count_next;
  end

  always @(*) begin     ■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb] (fix available)     ■ Use 'always_comb' instead of 'always @*'. [Style: comb
    if (sec_count_reg == 59)
      if(min_count_reg == 59)
        min_count_next = 0;
      else
        min_count_next = min_count_reg + 1;
    else
      min_count_next = min_count_reg;
  end

  assign sec = sec_count_reg;
  assign min = min_count_reg;

endmodule
```

- Demo Video

https://drive.google.com/file/d/1bg8vfQwtstMj4F2m2TnLNVGippfps4kJ/view?usp=sharing

(Change the video quality to highest possible since the default quality preset is very pixelated)