

Synthesis Report for 'fft_8point'

General Information

Date: Tue Dec 17 21:39:22 2024
Version: 2019.1 (Build 2552052 on Fri May 24 15:28:33 MDT 2019)
Project: ELD_project_2
Solution: solution1
Product family: zynq
Target device: xc7z020-clg484-1

Performance Estimates

- Timing (ns)

- Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.400	1.25

- Latency (clock cycles)

- Summary

Latency		Interval		Type
min	max	min	max	
221	221	221	221	none

- Detail

- Instance

Instance	Module	Latency		Interval		Type
		min	max	min	max	
grp_FFT_stages_fu_151	FFT_stages	187	187	187	187	none

- Loop

Loop Name	Latency		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- Loop 1	7	7	1	-	-	8	no
- Loop 2	24	24	3	-	-	8	no

Utilization Estimates

- Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	45	-
FIFO	-	-	-	-	-
Instance	4	20	2129	3873	0
Memory	0	-	131	9	0
Multiplexer	-	-	-	176	-
Register	-	-	22	-	-
Total	4	20	2282	4103	0
Available	280	220	106400	53200	0
Utilization (%)	1	9	2	7	0

- Detail

- Instance

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
grp_FFT_stages_fu_151	FFT_stages	4	20	2129	3873	0
Total	1	4	20	2129	3873	0

- **DSP48E**

N/A

- **Memory**

Memory	Module	BRAM_18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
FFT_rev_M_real_U	fft_8point_FFT_rev_M_real	0	64	4	0	8	32	1	256
FFT_rev_M_imag_U	fft_8point_FFT_rev_M_real	0	64	4	0	8	32	1	256
rev8_U	fft_8point_rev8	0	3	1	0	8	3	1	24
Total		3	0	131	9	0	24	67	536

- **FIFO**

N/A

- **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln35_fu_161_p2	+	0	0	12	3	1
i_fu_185_p2	+	0	0	13	4	1
icmp_ln35_fu_173_p2	icmp	0	0	9	3	2
icmp_ln4_fu_179_p2	icmp	0	0	11	4	5
Total		4	0	45	14	9

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
FFT_rev_M_imag_address0	21	4	3	12
FFT_rev_M_imag_ce0	15	3	1	3
FFT_rev_M_imag_ce1	9	2	1	2
FFT_rev_M_imag_d0	15	3	32	96
FFT_rev_M_real_address0	21	4	3	12
FFT_rev_M_real_ce0	15	3	1	3
FFT_rev_M_real_ce1	9	2	1	2
FFT_rev_M_real_d0	15	3	32	96
ap_NS_fsm	38	7	1	7
i_0_i_reg_140	9	2	4	8
phi_ln35_reg_129	9	2	3	6
Total	176	35	82	247

- **Register**

Name	FF	LUT	Bits	Const Bits
ap_CS_fsm	6	0	6	0
grp_FFT_stages_fu_151_ap_start_reg	1	0	1	0
i_0_i_reg_140	4	0	4	0
i_reg_213	4	0	4	0
phi_ln35_reg_129	3	0	3	0
zext_ln5_reg_218	4	0	64	60
Total	22	0	82	60

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
ap_clk	in	1	ap_ctrl_hs	fft_8point	return value
ap_rst	in	1	ap_ctrl_hs	fft_8point	return value
ap_start	in	1	ap_ctrl_hs	fft_8point	return value
ap_done	out	1	ap_ctrl_hs	fft_8point	return value
ap_idle	out	1	ap_ctrl_hs	fft_8point	return value
ap_ready	out	1	ap_ctrl_hs	fft_8point	return value
FFT_input_M_real_address0	out	3	ap_memory	FFT_input_M_real	array
FFT_input_M_real_ce0	out	1	ap_memory	FFT_input_M_real	array
FFT_input_M_real_q0	in	32	ap_memory	FFT_input_M_real	array

FFT_input_M_imag_address0	out	3	ap_memory	FFT_input_M_imag	array
FFT_input_M_imag_ce0	out	1	ap_memory	FFT_input_M_imag	array
FFT_input_M_imag_q0	in	32	ap_memory	FFT_input_M_imag	array
FFT_output_M_real_address0	out	3	ap_memory	FFT_output_M_real	array
FFT_output_M_real_ce0	out	1	ap_memory	FFT_output_M_real	array
FFT_output_M_real_we0	out	1	ap_memory	FFT_output_M_real	array
FFT_output_M_real_d0	out	32	ap_memory	FFT_output_M_real	array
FFT_output_M_real_address1	out	3	ap_memory	FFT_output_M_real	array
FFT_output_M_real_ce1	out	1	ap_memory	FFT_output_M_real	array
FFT_output_M_real_we1	out	1	ap_memory	FFT_output_M_real	array
FFT_output_M_real_d1	out	32	ap_memory	FFT_output_M_real	array
FFT_output_M_imag_address0	out	3	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_ce0	out	1	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_we0	out	1	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_d0	out	32	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_address1	out	3	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_ce1	out	1	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_we1	out	1	ap_memory	FFT_output_M_imag	array
FFT_output_M_imag_d1	out	32	ap_memory	FFT_output_M_imag	array
