

x should be $> 4\text{MHz}$ (CMT's constraint)

$$\frac{[\text{CMT output}]}{2^n} = [\text{intended o/p}]$$

n : size of frequency divider

to achieve: $3\text{Hz} \rightarrow$

$$100\text{MHz} \xrightarrow{\text{CMT}} x > 4\text{MHz} \xrightarrow[\text{div.}]{\text{freq.}} 3\text{Hz}$$

$$\frac{x}{2^n} = 3 \Rightarrow x = 3 \times 2^n$$

$$\text{and } x > 4\text{MHz}$$

$$\text{let } x = 6\text{MHz}$$

$$\text{then } 6 \times 10^6 = 3 \times 2^n$$

$$2 \times 10^6 = 2^n$$

$$10^6 = 2^{n-1}$$

$$\log_{10} 10^6 = (n-1) \log_{10} 2$$

$$6 = (n-1) \cdot \log_{10} 2$$

$$6 = (n-1) \cdot 0.3$$

$$n-1 = 20 \approx 21 \text{ bits}$$

vector: `reg [2:0] something = 3'b111;`

memory: `reg [2:0] else [255:0];`

a	b	a & b	a b	a && b	a b
0	1	0	1	0/F	1/T
000	000	000	000	0/F	0/F
000	001	000	001	0/F	1/T
011	001	001	011	1/T	1/T

if any of the bits of the output of bitwise operator is 1 \Rightarrow then logical operator output = 1
 else: 0 (FALSE) (TRUE)

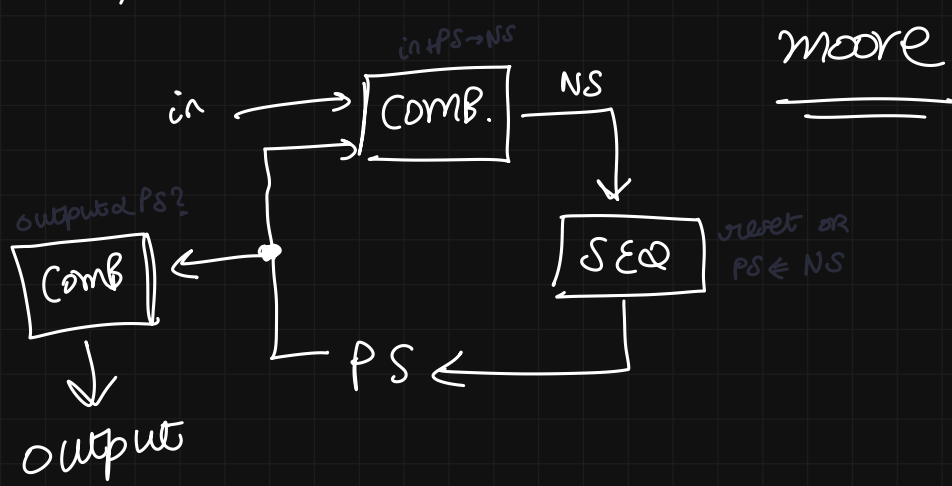
$$100\text{MHz} \xrightarrow{\text{CMT}} 8.388\text{MHz} \xrightarrow{23} 1$$

$$\frac{2}{2} \times \frac{8.388}{2^{23}} = 1$$

$$\frac{16.677}{2^{24}} = 1$$

So, 24 bits required now

in, PS, NS, output



do not initialize the output of a combinational circuit or else the tool might ignore it

(switch) case

if/else

parallel execution

serial execution

- full case: mutually exhaustive
- parallel case: mutually exclusive

note: `?: Verilog :: - : dart`

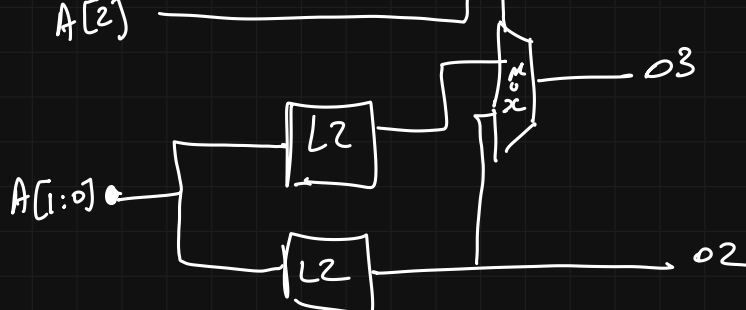
blocking \rightarrow combinational

`always@*`

non-blocking \rightarrow sequential

`always@ (posedge clk)`

values in RHS of an always block are stored at the (...) condition in case of non-blocking



1 x 3 input comb. ckt's $3 \leq 3, 1 \leq 2, 0 \leq 0$

2 x 2 input comb ckt's $3 \leq 3, 2 \leq 2, 2 \leq 2$

$f(A,B)$

$f(B,C)$

sequential = comb + memory