ELD LAB HOMEWORK - 2

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- **NOTE:** I am using Arch Linux and my date and time appear on my custom status bar (DWM window manager's default status bar) and hence it does not resemble the one on Windows
- **NOTE 2:** By doing $ cat [filename], I intend to show the contents of the file whose name is given by [filename]
- **NOTE 3:** I use neovim as my external editor instead of the inbuilt vivado text editor and hence, the screenshots I have shared of the code do not resemble the vivado UI

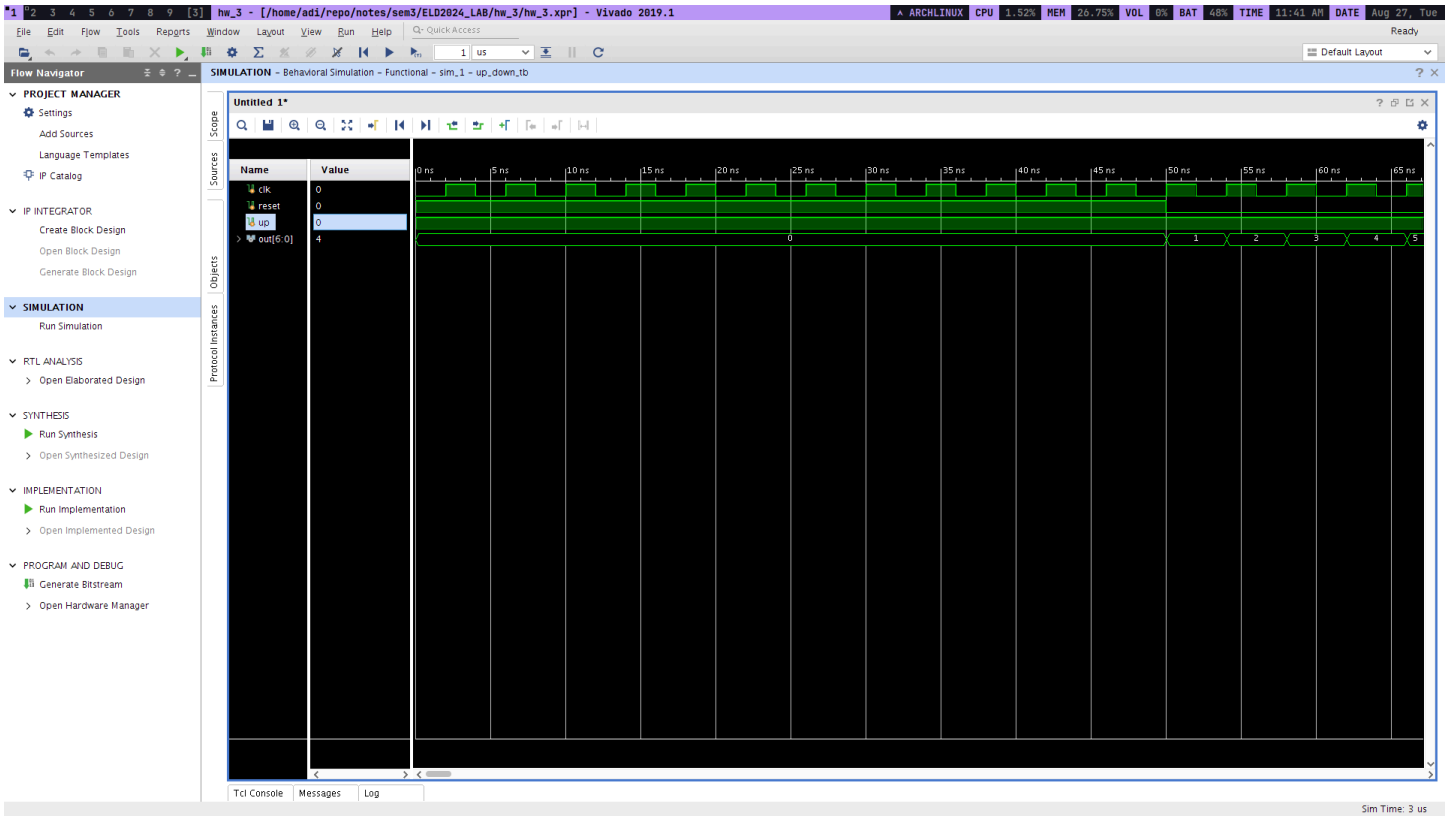
$ cat up_down_7bit.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/27/2024 10:39:09 AM
// Design Name:
// Module Name: up_down_7bit
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module up_down_7bit (
      input clk,
      input reset,
      input up,
      output [6:0] out
);

  reg [6:0] PS = 0, NS = 0;

  always @(posedge clk) begin
      if (reset) PS <= 7'd0;
      else PS <= NS;
  end

  always @(*)
  begin
      if(up==1'b1)
            if(PS == 7'd85)
                  NS = 7'd0;
            else
                  NS = PS + 7'd1;
      else if(up==1'b0)
            if(PS == 7'd0)
                  NS = 7'd85;
            else
                  NS = PS - 7'd1;
  end

  assign out = PS;

endmodule
```

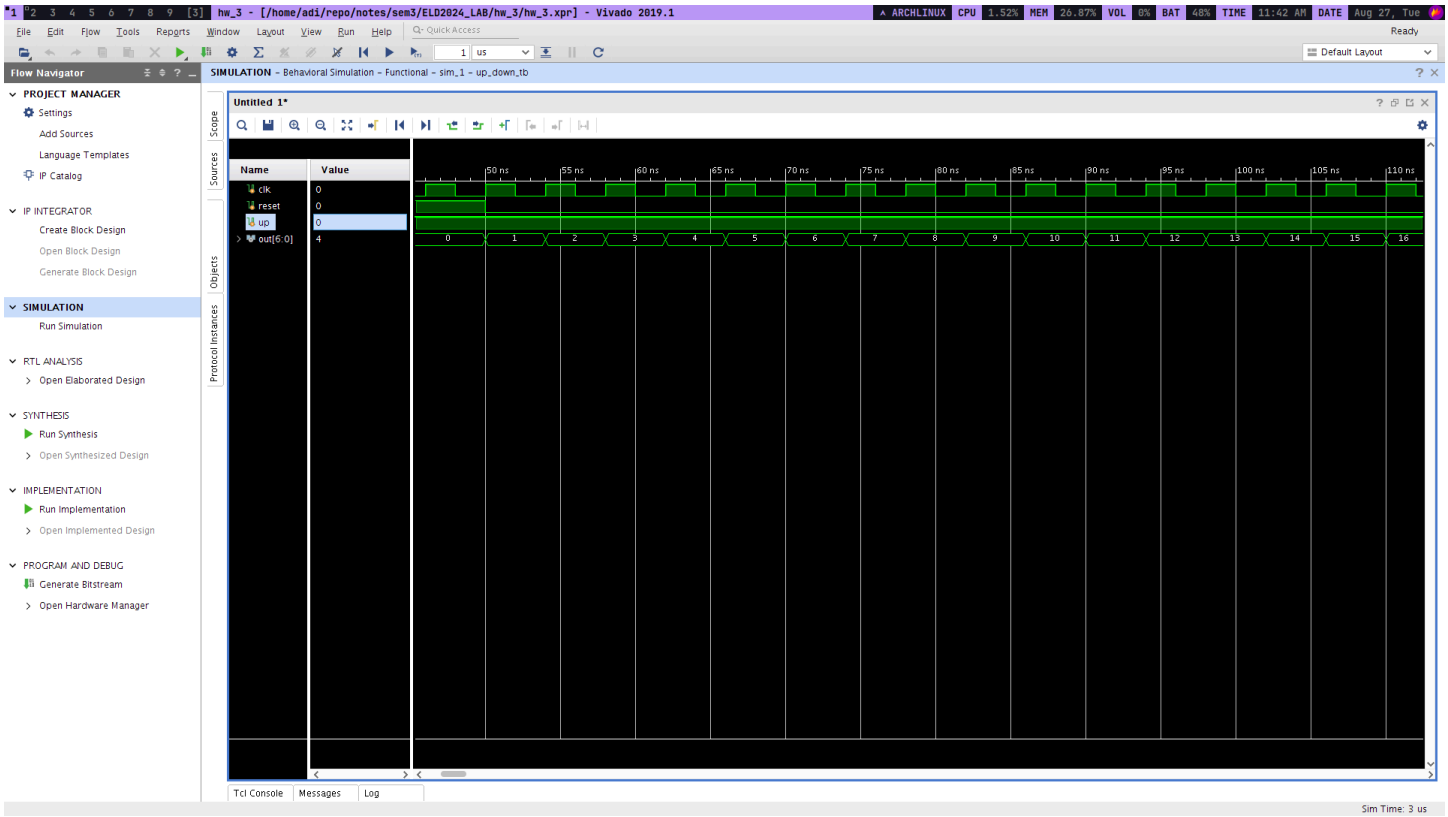
$ cat up_down_tb.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 08/27/2024 10:44:36 AM
// Design Name:
// Module Name: up_down_tb
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module up_down_tb();

  reg clk, reset, up;
  wire [6:0] out;


  up_down_7bit foo(
      .clk(clk),
      .reset(reset),
      .up(up),
      .out(out)
  );

  always
  begin
      #2 clk = ~clk;
  end

  initial
  begin
      clk = 0;
      up = 1;
      reset = 1;
      #50 reset = 0;
      #1000 up = 0;
      #2000 $stop;
  end

endmodule
```

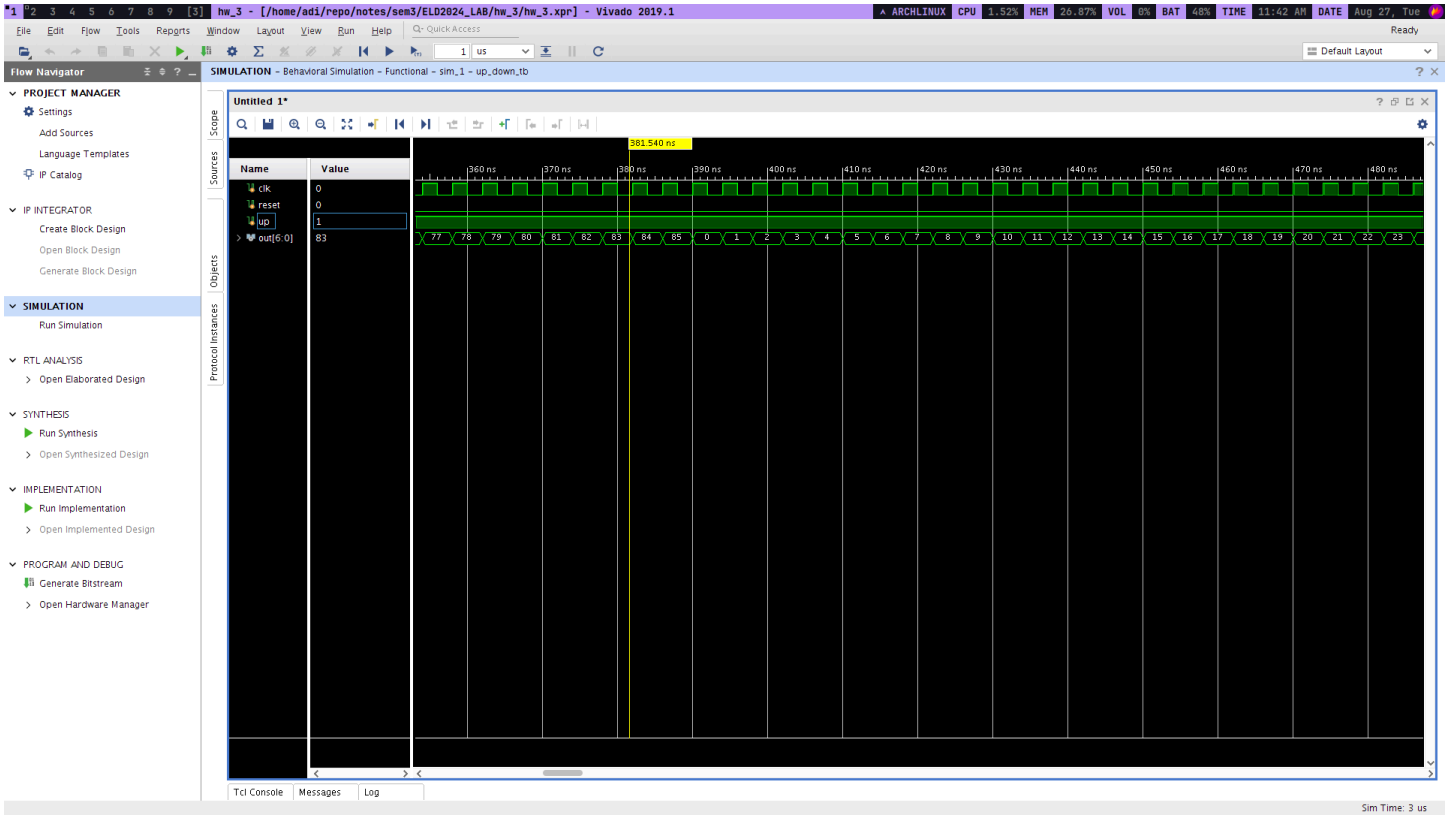
- RESET


hw_3 - [/home/adi/repo/notes/sem3/ELD2024_LAB/hw_3/hw_3.xpr] - Vivado 2019.1
SIMULATION - Behavioral Simulation - Functional - sim_1 - up_down_tb
Untitled 1*
Name
Value
clk
reset
up
out[6:0]
Tcl Console
Messages
Log
Sim Time: 3 us

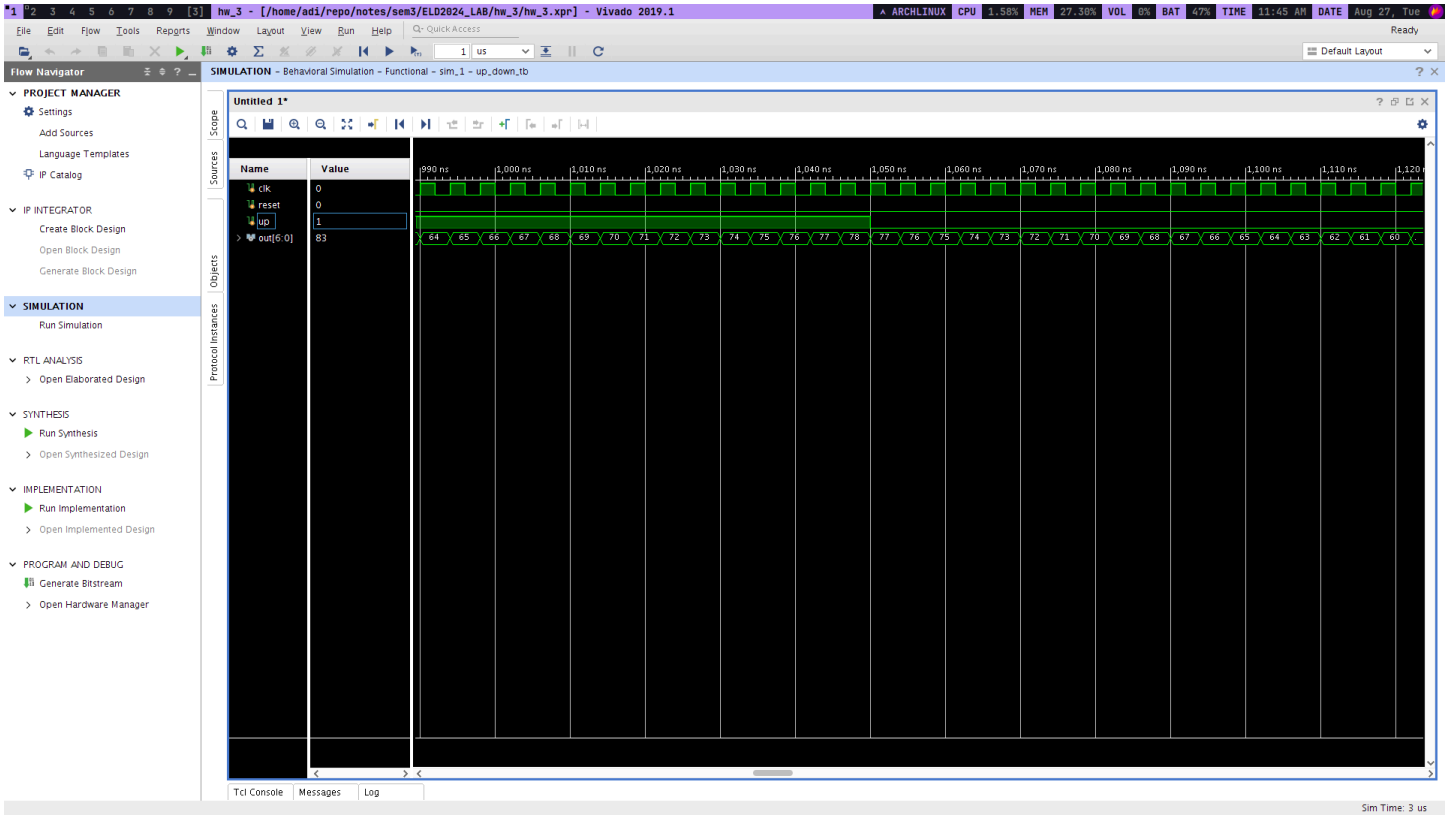
- UP


hw_3 - [/home/adi/repo/notes/sem3/ELD2024_LAB/hw_3/hw_3.xpr] - Vivado 2019.1
SIMULATION - Behavioral Simulation - Functional - sim_1 - up_down_tb
Untitled 1*
Name
Value
clk
reset
up
out[6:0]
Tcl Console
Messages
Log
Sim Time: 3 us

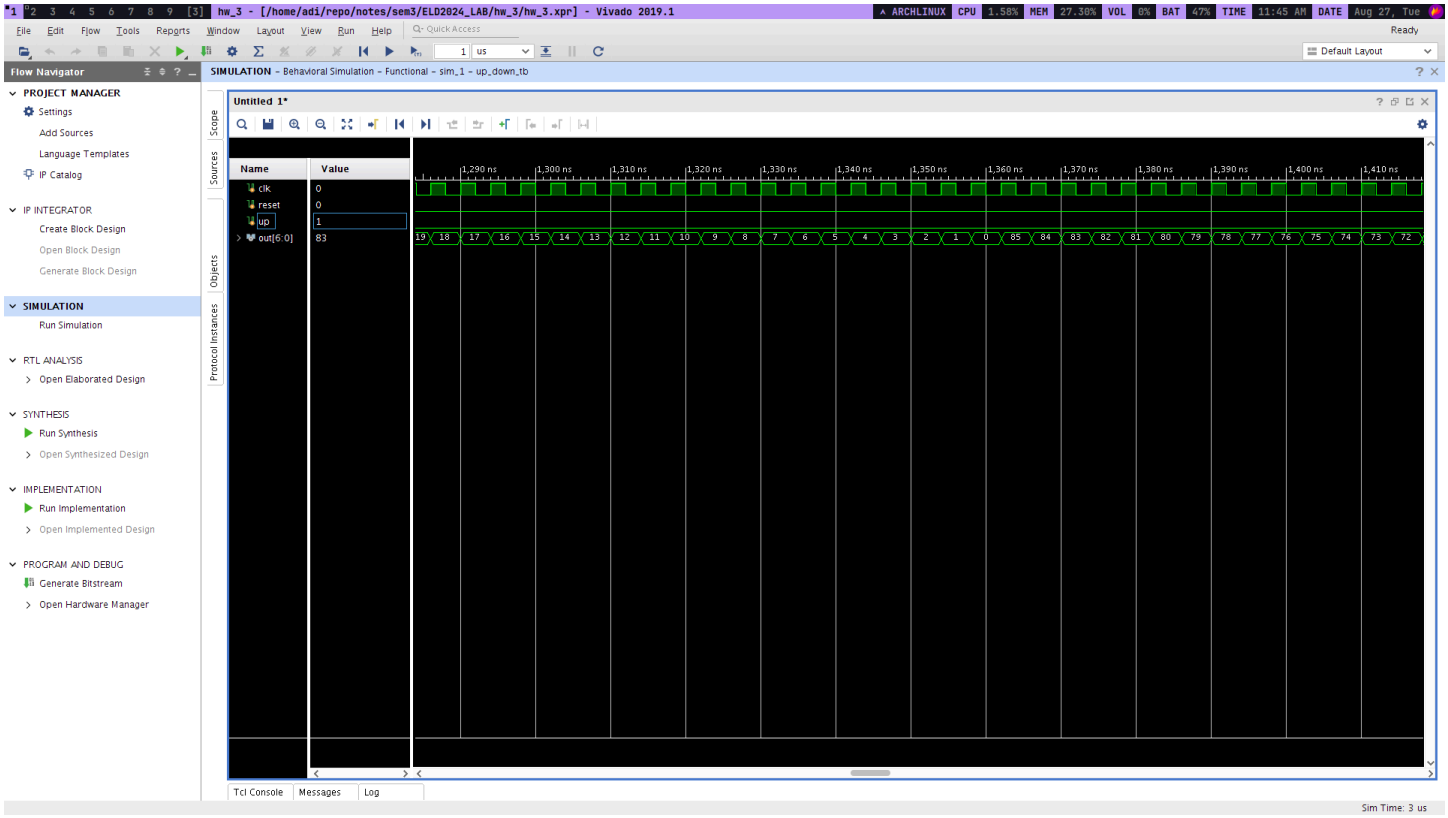
- UP (WRAPPING : 85 -> 0)



- UP to DOWN



- DOWN (WRAPPING : 0 -> 85)



- Main Source Code

```
module up_down_7bit (
    input clk,
    input reset,
    input up,
    output [6:0] out
);


  reg [6:0] PS = 0, NS = 0;

  always @(posedge clk) begin
    if (reset) PS <= 7'd0;
    else PS <= NS;
  end

  always @(*) begin     ■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb] (fix available)     ■ Use 'alway
    if(up==1'b1)
      if(PS == 7'd85)
        NS = 7'd0;
      else
        NS = PS + 7'd1;
    else if(up==1'b0)
      if(PS == 7'd0)
        NS = 7'd85;
      else
        NS = PS - 7'd1;
  end

  assign out = PS;

endmodule
```

"repo/notes/sem3/ELD2024_LAB/hw_3/hw_3.srcs/sources_1/new/up_down_7bit.v" 53L, 920B written

- Test Bench Code