

ELD LAB 7 HOMEWORK 1

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Project Structure

```
main.v
| xfft_03.xci
```

CODE

- main.v

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 10/15/2024 09:38:43 AM
// Design Name:
// Module Name: main
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module main(

    input Clock,
    input reset,
    input [63:0] slave_data,
    output [63:0] master_data,
    input [7:0] config_data,
    input config_valid,
    input slave_valid,
    input slave_last,
```

```

input master_ready,
output config_ready,
output slave_ready,
output master_valid,
output master_last

);

xfft_03 something (
    .aclk(Clock),                // input wire aclk
    .aresetn(reset),             // input wire aresetn
    .s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_config_tdata
    .s_axis_config_tvalid(config_valid), // input wire s_axis_config_tvalid
    .s_axis_config_tready(config_ready), // output wire s_axis_config_tready
    .s_axis_data_tdata(slave_data), // input wire [63 : 0] s_axis_data_tdata
    .s_axis_data_tvalid(slave_valid), // input wire s_axis_data_tvalid
    .s_axis_data_tready(slave_ready), // output wire s_axis_data_tready
    .s_axis_data_tlast(slave_last), // input wire s_axis_data_tlast
    .m_axis_data_tdata(master_data), // output wire [63 : 0] m_axis_data_tdata
    .m_axis_data_tvalid(master_valid), // output wire m_axis_data_tvalid
    .m_axis_data_tready(master_ready), // input wire m_axis_data_tready
    .m_axis_data_tlast(master_last) // output wire m_axis_data_tlast
);

```

- testbench.v

```
// timescale 1ns / 1ps  
////////////////////////////////////  
// Company:  
// Engineer:  
//  
// Create Date: 10/15/2024 09:55:13 AM  
// Design Name:  
// Module Name: testbench  
// Project Name:  
// Target Devices:  
// Tool Versions:  
// Description:  
//  
// Dependencies:  
//  
// Revision:  
// Revision 0.01 - File Created  
// Additional Comments:  
//  
////////////////////////////////////
```

```

reg reset;
reg [63:0] slave_data;
wire [63:0] master_data;
reg [7:0] config_data;
reg config_valid;
reg slave_valid;
reg slave_last;
reg master_ready;
wire config_ready;
wire slave_ready;
wire master_valid;
wire master_last;

reg [31:0] slave_data_real [31:0];
reg [31:0] slave_data_im [31:0];
reg [31:0] master_data_real [31:0];
reg [31:0] master_data_im [31:0];

main something (
.Clock(Clock),
.reset(reset),
.slave_data(slave_data),
.master_data(master_data),
.config_data(config_data),
.config_valid(config_valid),
.slave_valid(slave_valid),
.slave_last(slave_last),
.master_ready(master_ready),
.config_ready(config_ready),
.slave_ready(slave_ready),
.master_valid(master_valid),
.master_last(master_last)
);

// init
initial
begin
    Clock = 0;
    reset = 0;
    config_valid = 0;
    config_data = 0;
    slave_valid = 0;
    slave_data = 0;
    slave_last = 0;
    master_ready = 1;
end

// clock
always
#5 Clock = ~Clock;

// input
initial
begin

```

```
slave_data_real[0] = 32'h3f800000;
slave_data_im[0] = 32'h0;
slave_data_real[1] = 32'h0;
slave_data_im[1] = 32'h0;
slave_data_real[2] = 32'h0;
slave_data_im[2] = 32'h0;
slave_data_real[3] = 32'h0;
slave_data_im[3] = 32'h0;
slave_data_real[4] = 32'h0;
slave_data_im[4] = 32'h0;
slave_data_real[5] = 32'h0;
slave_data_im[5] = 32'h0;
slave_data_real[6] = 32'h0;
slave_data_im[6] = 32'h0;
slave_data_real[7] = 32'h0;
slave_data_im[7] = 32'h0;
slave_data_real[8] = 32'h0;
slave_data_im[8] = 32'h0;
slave_data_real[9] = 32'h0;
slave_data_im[9] = 32'h0;
slave_data_real[10] = 32'h0;
slave_data_im[10] = 32'h0;
slave_data_real[11] = 32'h0;
slave_data_im[11] = 32'h0;
slave_data_real[12] = 32'h0;
slave_data_im[12] = 32'h0;
slave_data_real[13] = 32'h0;
slave_data_im[13] = 32'h0;
slave_data_real[14] = 32'h0;
slave_data_im[14] = 32'h0;
slave_data_real[15] = 32'h0;
slave_data_im[15] = 32'h0;
slave_data_real[16] = 32'h0;
slave_data_im[16] = 32'h0;
slave_data_real[17] = 32'h0;
slave_data_im[17] = 32'h0;
slave_data_real[18] = 32'h0;
slave_data_im[18] = 32'h0;
slave_data_real[19] = 32'h0;
slave_data_im[19] = 32'h0;
slave_data_real[20] = 32'h0;
slave_data_im[20] = 32'h0;
slave_data_real[21] = 32'h0;
slave_data_im[21] = 32'h0;
slave_data_real[22] = 32'h0;
slave_data_im[22] = 32'h0;
slave_data_real[23] = 32'h0;
slave_data_im[23] = 32'h0;
slave_data_real[24] = 32'h0;
slave_data_im[24] = 32'h0;
slave_data_real[25] = 32'h0;
slave_data_im[25] = 32'h0;
slave_data_real[26] = 32'h0;
slave_data_im[26] = 32'h0;
```

```

    slave_data_real[27] = 32'h0;
    slave_data_im[27] = 32'h0;
    slave_data_real[28] = 32'h0;
    slave_data_im[28] = 32'h0;
    slave_data_real[29] = 32'h0;
    slave_data_im[29] = 32'h0;
    slave_data_real[30] = 32'h0;
    slave_data_im[30] = 32'h0;
    slave_data_real[31] = 32'h0;
    slave_data_im[31] = 32'h0;
    slave_data_real[32] = 32'h0;
    slave_data_im[32] = 32'h0;
end

// config
initial
begin
    #70 reset = 1;
    config_data = 1; // forward fft not inverse
    config_valid = 1;
    while(config_ready == 0)
        #2 config_valid = 1;
    #10 config_valid = 0;
end

// input
integer i,j;
initial
begin
    #70 for(i=31;i>=0;i=i-1) begin
        #10 if(i==0)
            slave_last = 1;
        slave_data = {slave_data_im[i],slave_data_real[i]};
        slave_valid = 1;
        while(slave_ready == 0)
            #2 slave_valid = 1;
        #10 slave_valid = 0;
        slave_last = 0;
    end
end

// output
initial
begin
    for(j=31;j>=0;j=j-1) begin
        #5 master_ready = 1;
        wait(master_valid == 1);
        {master_data_im[j],master_data_real[j]} = master_data;
        #10 master_ready = 0;
    end
    #20 $stop;
end

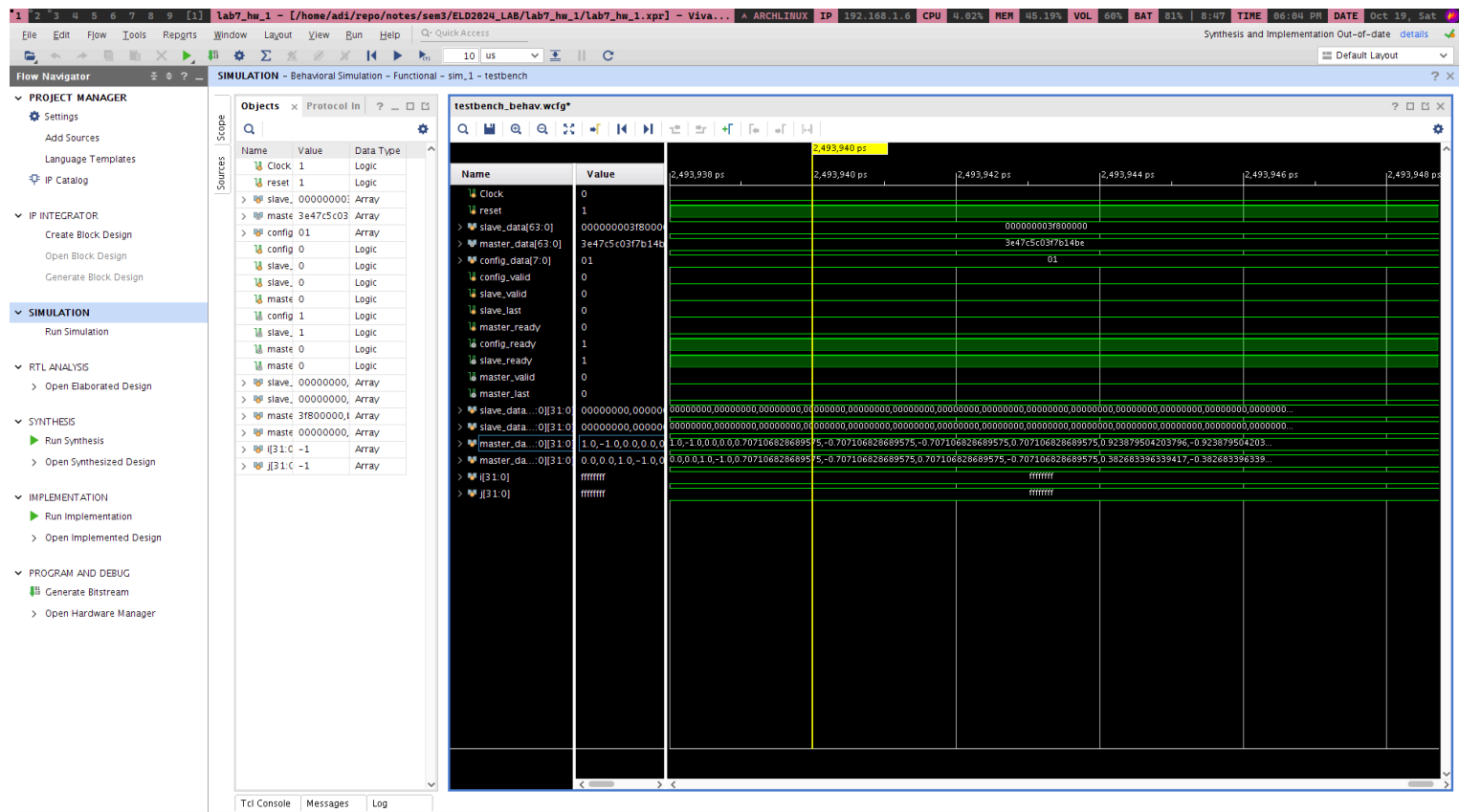
endmodule

```

```
1 2 3 4 5 6 7 8 9 [1] testbench.v (-/repo/notes/sem3/ELD2024_LAB/lab7_hw_1/lab7_hw_1.srcs/sim_1/new) - VIN A ARCHLINUX IP 192.168.1.6 CPU 4.01% MEM 44.24% VOL 60% BAT 82% | 8:43 TIME 06:02 PM DATE Oct 19, Sat
1 timescale 1ns / 1ps
2 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 10/15/2024 09:38:43 AM
7 // Design Name:
8 // Module Name: main
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////////////////////////////////////
21
22
23 module main(
24
25     input Clock,
26     input reset,
27     input [63:0] slave_data,
28     output [63:0] master_data,
29     input [7:0] config_data,
30     input config_valid,
31     input slave_valid,
32     input slave_last,
33     input master_ready,
34     output config_ready,
35     output slave_ready,
36     output master_valid,
37     output master_last
38
39 );
40
41 xfft_03 something (
42     .aclk(Clock), // input wire aclk
43     .aresetn(reset), // input wire aresetn
44     .s_axis_config_tdata(config_data), // input wire [7 : 0] s_axis_
45     .s_axis_config_tvalid(config_valid), // input wire s_axis_config_t
46     .s_axis_config_tready(config_ready), // output wire s_axis_config_
47
48 );
49
50 main.v 1% 1:1 NORMAL testbench.v unix | utf-8 | verilog 0% 1:1
189 lines yanked
```

> NOTE: Both the codes are placed in the same screenshot for convenience. You can differentiate between the splits through the filename mentioned in the status bar in the bottom as well as the module name in the code

OUTPUT



OUTPUT (REAL)

1.0, -1.0, 0.0, 0.0, 0.707106828689575, -0.707106828689575, -0.707106828689575, 0.707106828689575, 0.923879504203796, -0.923879504203796, -0.382683396339417, 0.382683396339417, 0.382683455944061, -0.382683455944061, -0.923879563808441, 0.923879563808441, 0.980785250663757, -0.980785250663757, -0.195090293884277, 0.195090293884277, 0.555570244789124, -0.555570244789124, -0.831469655036926, 0.831469655036926, 0.831469655036926, -0.831469655036926, -0.555570244789124, 0.555570244789124, 0.195090353488922, -0.195090353488922, -0.980785369873047, 0.980785369873047

OUTPUT (IMAGINARY)

0.0, 0.0, 1.0, -1.0, 0.707106828689575, -0.707106828689575, 0.707106828689575, -0.707106828689575, 0.382683396339417, -0.382683396339417, 0.923879504203796, -0.923879504203796, 0.923879504203796, -0.923879504203796, 0.382683455944061, -0.382683455944061, 0.195090293884277, -0.195090293884277, 0.980785250663757, -0.980785250663757, 0.831469655036926, -0.831469655036926, 0.555570244789124, -0.555570244789124, 0.555570244789124, -0.555570244789124, 0.831469655036926, -0.831469655036926, 0.980785369873047, -0.980785369873047, 0.195090353488922, -0.195090353488922