

# ELD Lab 9 HomeWork

Aditya Gautam

2023043

> Note: All screenshots are attached from page 2

# 1.256 Point FFT

Re-customize IP

File Edit Flow Tools Repgrts Window Layout View Help Q: Quick Access

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Block Properties

Name: xfft\_0

Parent name: design\_1

Block Design - design\_1

Diagram

Address Editor

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol

Show disabled p

Component Name: xfft\_0

Configuration Implementation

Number of Channels: 1

Transform Length: 256

Tcl Console

Messages Log Reports Design Runs

Generated Hardware Definition File: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/srcs/sources\_1/bd/design\_1/synth/design\_1.hwdef

[Sat Nov 16 21:56:32 2024] Launched design\_1\_xfft\_0\_0\_synth\_1, design\_1\_auto\_pc\_0\_synth\_1, synth\_1...

Run output will be captured here:

design\_1\_xfft\_0\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/runs/design\_1\_xfft\_0\_0\_synth\_1/runme.log

design\_1\_auto\_pc\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/runs/design\_1\_auto\_pc\_0\_synth\_1/runme.log

synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/runs/synth\_1/runme.log

[Sat Nov 16 21:56:32 2024] Launched impl\_1

Run output will be captured here: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/runs/impl\_1/runme.log

launch\_runs: Time (s): cpu = 00:00:12, elapsed = 00:00:30, Memory (MB): peak = 7571480, gain = 78578, free physical = 853, free virtual = 6592

Type a Tcl command here

Lab9\_256 - [/home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_256/lab9\_256.xpr] - Viva...

File Edit Flow Tools Repgrts Window Layout View Help Q: Quick Access

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Netlist

design\_1.wrapper

- Nets (185)
- dbg\_hub (dbg\_hub)
- design\_1\_i (design\_1)

Properties

Select an object to see properties

Project Summary

Device

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.985 ns	Worst Hold Slack (WHS): 0.026 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 40761	Total Number of Endpoints: 40745	Total Number of Endpoints: 15873

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved)

## 2.64 Point FFT

Re-customize IP

File Edit Flow Tools Repgrts Window Layout View Help Q: Quick Access

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Block Design - design\_1

Sources Design Signals Board ? - □ □ □

design\_1

- External Interfaces
- Interface Connections
- Nets
- axi\_dma\_0 (AXI Direct Memory Access 7.1)
- axi\_smc (AXI SmartConnect 1.0)
- processing\_system7\_0 (ZYNQ7 Processing System 5.5)
- ps7\_0\_axi\_periph
- rst\_ps7\_0\_100M (Processor System Reset 5.0)
- system\_ila\_0 (System ILA 1.1)
- xfft\_0 (Fast Fourier Transform 9.1)
  - M\_AXIS\_DATA
  - S\_AXIS\_CONFIG
  - S\_AXIS\_DATA

Block Properties

Name: xfft\_0

Parent name: design\_1

General Properties IP

Diagram

Address Editor

Tcl Console

Messages Log Reports Design Runs

Generated Hardware Definition File: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft/srcs/sources\_1/bd/design\_1/synth/design\_1.hwdef

[Sat Nov 16 22:12:05 2024] Launched design\_1\_vfft\_0\_0\_synth\_1, design\_1\_auto\_pc\_0\_synth\_1, synth\_1...

Run output will be captured here:

design\_1\_vfft\_0\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft/runs/design\_1\_vfft\_0\_0\_synth\_1/runme.log

design\_1\_auto\_pc\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft/runs/design\_1\_auto\_pc\_0\_synth\_1/runme.log

synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft/runs/synth\_1/runme.log

[Sat Nov 16 22:12:05 2024] Launched impl\_1

Run output will be captured here: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft/runs/impl\_1/runme.log

launch\_runs: Time (s): cpu = 00:00:13, elapsed = 00:00:32, Memory (MB): peak = 8550.246, gain = 0.000, free physical = 211, free virtual = 5274

Type a Tcl command here

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol

Component Name: xfft\_0

Show disabled

Configuration

Number of Channels: 1

Transform Length: 64

Lab9\_64fft - [/home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_64fft/lab9\_64fft.xpr] ... ARCHLINUX IP 192.168.1.9 CPU 3.78% MEM 59.61% VOL 67% BAT 56% | 10:48 TIME 10:26 PM DATE Nov 16, Sat

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic
- PROGRAM AND DEBUG

Implemented Design - xc7z0200g484-1

Sources Netlist

design\_1.wrapper

- Nets (185)
- dbg\_hub (dbg\_hub)
- design\_1\_i (design\_1)

Block Properties

Select an object to see properties

Project Summary

Device

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.945 ns	Worst Hold Slack (WHS): 0.016 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 42872	Total Number of Endpoints: 42856	Total Number of Endpoints: 17014

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved)

## 3.32 Point FFT

Re-customize IP

File Edit Flow Tools Repgrts Window Layout View Help QuickAccess

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Block Design - design\_1

Sources Design Signals Board ? - □ □ □

design\_1

- External Interfaces
- Interface Connections
- Nets
- axi\_dma\_0 (AXI Direct Memory Access 7.1)
- axi\_smc (AXI SmartConnect 1.0)
- processing\_system7\_0 (ZYNQ7 Processing System 5.5)
- ps7\_0\_axi\_periph
- rst\_ps7\_0\_100M (Processor System Reset 5.0)
- system\_lia\_0 System ILA 1.1
- xfft\_0 (Fast Fourier Transform 9.1)
- xciconstant\_0 (Constant 1.1)
- xciconstant\_1 (Constant 1.1)

Block Properties

xfft\_0

Name: xfft\_0

Parent name: design\_1

Diagram

Address Editor

Diagram

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol

Show disabled

Component Name: xfft\_0

Configuration

Number of Channels: 1

Transform Length: 32

Tcl Console

Messages Log Reports Design Runs

Generated Hardware Definition File: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft/srcs/sources\_1/bd/design\_1/synth/design\_1.hwdef

[Sat Nov 16 22:30:01 2024] Launched design\_1\_vfft\_0\_0\_synth\_1, design\_1\_auto\_pc\_0\_synth\_1, synth\_1...

Run output will be captured here:

design\_1\_vfft\_0\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft/runs/design\_1\_vfft\_0\_0\_synth\_1/runme.log

design\_1\_auto\_pc\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft/runs/design\_1\_auto\_pc\_0\_synth\_1/runme.log

synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft/runs/synth\_1/runme.log

[Sat Nov 16 22:30:01 2024] Launched impl\_1

Run output will be captured here: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft/runs/impl\_1/runme.log

launch\_runs: Time (s): cpu = 00:00:12, elapsed = 00:00:31, Memory (MB): peak = 8835453, gain = 13008, free physical = 1159, free virtual = 4964

Type a Tcl command here

Lab9\_32fft - [/home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_32fft/ab9\_32fft.xpr] ... ARCHLINUX IP 192.168.1.9 CPU 3.88% MEM 61.56% VOL 67% BAT 88% | 10:52 TIME 10:48 PM DATE Nov 16, Sat

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic
- PROGRAM AND DEBUG

Implemented Design - xc7z0200g484-1

Sources Netlist

design\_1.wrapper

- Nets (185)
- dbg\_hub (dbg\_hub)
- design\_1\_i (design\_1)

Block Properties

Select an object to see properties

Project Summary

Device

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.722 ns	Worst Hold Slack (WHS): 0.010 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 40961	Total Number of Endpoints: 40945	Total Number of Endpoints: 16155

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved)

## 4.16 Point FFT

Re-customize IP

File Edit Flow Tools Repgrts Window Layout View Help QuickAccess

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager

Block Design - design\_1

Sources Design Signals Board ? - □ □ □

design\_1

- External Interfaces
- Interface Connections
- Nets
- axi\_dma\_0 (AXI Direct Memory Access 7.1)
- axi\_smc (AXI SmartConnect 1.0)
- processing\_system7\_0 (ZYNQ7 Processing System 5.5)
- ps7\_0\_axi\_periph
- rst\_ps7\_0\_100M (Processor System Reset 5.0)
- system\_lila\_0 System ILA 1.1
- xfft\_0 (Fast Fourier Transform 9.1)
- xciconstant\_0 (Constant 1.1)
- xciconstant\_1 (Constant 1.1)

Block Properties

xfft\_0

Name: xfft\_0

Parent name: design\_1

Diagram

Address Editor

Diagram

Fast Fourier Transform (9.1)

Documentation IP Location

IP Symbol

Component Name: xfft\_0

Show disabled

Configuration

Number of Channels: 1

Transform Length: 16

Tcl Console

Messages Log Reports Design Runs

Generated Hardware Definition File: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/srcs/sources\_1/bd/design\_1/synth/design\_1.hwdef

[Sat Nov 16 22:42:19 2024] Launched design\_1\_auto\_pc\_0\_synth\_1, design\_1\_xfft\_0\_0\_synth\_1, synth\_1...

Run output will be captured here:

design\_1\_auto\_pc\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/runs/design\_1\_auto\_pc\_0\_synth\_1/runme.log

design\_1\_xfft\_0\_0\_synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/runs/design\_1\_xfft\_0\_0\_synth\_1/runme.log

synth\_1: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/runs/synth\_1/runme.log

[Sat Nov 16 22:42:19 2024] Launched impl\_1

Run output will be captured here: /home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/runs/impl\_1/runme.log

launch\_runs: Time (h) = 00:00:12, elapsed = 00:00:31, Memory (MB) peak = 9073.062, gain = 0.000, free physical = 1503, free virtual = 5066

Type a Tcl command here

Lab9\_16fft - [/home/adi/repo/notes/sem3/ELD2024\_LAB/lab9\_16fft/lab9\_16fft.xpr] ... ARCHLINUX IP 192.168.1.9 CPU 3.97% MEM 69.89% VOL 77% BAT 95% | 12:58 TIME 11:03 PM DATE Nov 16, Sat

write\_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
  - Constraints Wizard
  - Edit Timing Constraints
  - Report Timing Summary
  - Report Clock Networks
  - Report Clock Interaction
  - Report Methodology
  - Report DRC
  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic
- PROGRAM AND DEBUG

Implemented Design - xc7z0200g484-1

Sources Netlist

design\_1.wrapper

- Nets (185)
- dbg\_hub (dbg\_hub)
- design\_1\_i (design\_1)

Block Properties

Select an object to see properties

Project Summary

Device

Timing

Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.843 ns	Worst Hold Slack (WHS): 0.015 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 38521	Total Number of Endpoints: 38605	Total Number of Endpoints: 15361

All user specified timing constraints are met.

Timing Summary - impl\_1 (saved)