

ELD LAB HOMEWORK – 2

Aditya Gautam

2023043

- Note 1: I am on Arch Linux operating system, and hence the status bar does not resemble the one on Windows operating system
- Note 2: If the final Success Rate will be taken into account for grading, kindly take into consideration that I had attempted questions which were not mentioned in the question list.

MY STATS

<https://hdlbits.01xz.net/wiki/Special:VlgStats/EA35A63A256E325F>

User Stats

Problems solved: 15
Problems attempted: 15
Current rank: 34086
[Link to this page](#)

Problem	Success	Incorrect	Compile error	Simulation error	Total attempts	Success rate (%)
1. step_one	1	0	0	0	1	100%
2. zero	1	0	1	0	2	50%
3. wire	2	0	1	0	3	67%
4. wire4	2	0	0	0	2	100%
5. notgate	2	0	0	0	2	100%
6. andgate	2	0	0	0	2	100%
7. norgate	2	0	0	0	2	100%
8. xnorgate	2	1	0	0	3	67%
9. wire_def	2	1	1	0	4	50%
10. 7458	2	1	2	0	5	40%
11. exams/m2014.q4h	1	0	0	0	1	100%
12. 7420	1	1	0	0	2	50%
13. m2015.q4a	1	0	0	0	1	100%
14. m2015.q4b	1	1	0	0	2	50%
15. mux9to1v	1	4	4	0	9	11%
Attempts:	23	9	9	0	41	56%
Problems:	15				15	100%

About HDLBits

Arch Linux CPU: 3.48% MEM: 24.94% VOLUME: 72% BATTERY: 13% TIME: 10:31 PM DATE: Aug 22, Thu

Q1. Wire

```
module top_module( input in, output out );  
    assign out = in;  
endmodule
```

Lab 1 Resources × ctd.pdf × ENGINEERING CIR × (1) Lecture 05: P × Java Data Type × Lab 1 Homework × Project Ideas × Lecture 06: Part 1 × Untitled document × Wire - HDLBits × (75) WhatsApp × + ×

← → ↻ https://hdlbits.01xz.net/wiki/Wire

top_module

Stuff outside your module The module you're designing now Stuff outside your module

In addition to continuous assignments, Verilog has three other assignment types that are used in procedural blocks, two of which are synthesizable. We won't be using them until we start using procedural blocks.

Expected solution length: Around 1 line.

Module Declaration

```
module top_module( input in, output out );
```

[Hint](#)

Write your solution here

Last success: 8/20/2024, 9:49:21 PM [Load](#)

```
1 module top_module( input in, output out );  
2     assign out = in;  
3 endmodule  
4
```

[Submit](#) [Submit \(new window\)](#)

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Solution

[Show solution](#)

1 2 3 4 5 6 7 8 9 10 | wire - HDLBits - LibreWolf

ARCHLINUX CPU 2.55% MEM 6.70% VOLUME 77% BATTERY 90% TIME 01:19 PM DATE Aug 22, Thu

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← → ↻ https://hdlbits.01xz.net/wiki/Wire

Solution

[Show solution](#)

wire — Compile and simulate

Running Quartus synthesis. [Show Quartus messages](#).
Running ModelSim simulation. [Show ModelSim messages](#).

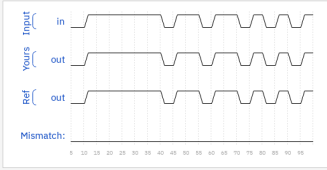
Status: Success!

You have solved 15 problems. [See my progress](#).

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).

Output should follow input

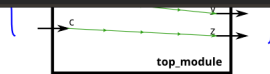
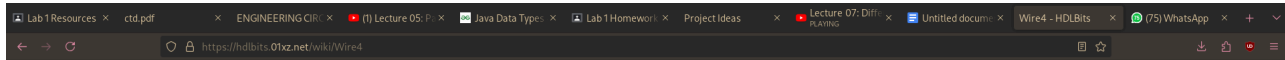


1 2 3 4 5 6 7 8 9 10 | wire - HDLBits - LibreWolf

ARCHLINUX CPU 2.55% MEM 6.70% VOLUME 77% BATTERY 90% TIME 01:19 PM DATE Aug 22, Thu

Q2. Wire4

```
module top_module(  
    input a,b,c,  
    output w,x,y,z );  
    assign w = a;  
    assign x = b;  
    assign y = b;  
    assign z = c;  
endmodule
```



Expected solution length: Around 4 lines.

Module Declaration

```
module top_module(  
    input a,b,c,  
    output w,x,y,z );
```

[Hint](#)

Write your solution here

Last success: 8/20/2024, 9:51:18 PM [Load](#)

```
1 module top_module(  
2     input a,b,c,  
3     output w,x,y,z );  
4  
5     assign w = a;  
6     assign x = b;  
7     assign y = b;  
8     assign z = c;  
9  
10    endmodule  
11
```

[Submit](#)

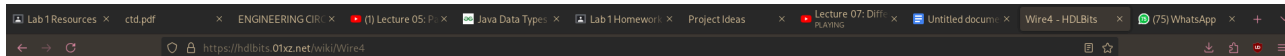
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Solution

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1 2 3 4 5 6 7 8 9 Wire4 - HDLBits - LibreWolf ARCHLINUX CPU 2.69% MEM 20.80% VOLUME 77% BATTERY 86% TIME 01:27 PM DATE Aug 22, Thu



wire4 — Compile and simulate

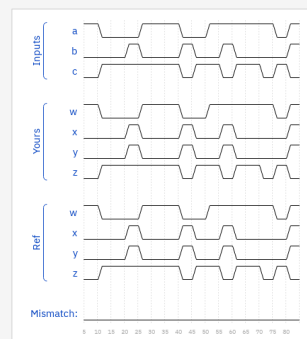
Running Quartus synthesis: [Show Quartus messages](#).
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Timing diagrams for selected test cases

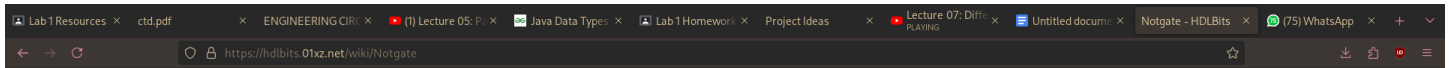
These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The 'Mismatch' trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).



1 2 3 4 5 6 7 8 9 Wire4 - HDLBits - LibreWolf ARCHLINUX CPU 2.69% MEM 20.55% VOLUME 77% BATTERY 86% TIME 01:27 PM DATE Aug 22, Thu

Q3. Notgate

```
module top_module( input in, output out );  
    assign out = ~in;  
endmodule
```



Module Declaration

```
module top_module( input in, output out );
```

[Hint](#)

Write your solution here

Last success: 8/20/2024, 9:52:16 PM [Load](#)

```
1 module top_module( input in, output out );  
2     assign out = ~in;  
3 endmodule  
4
```

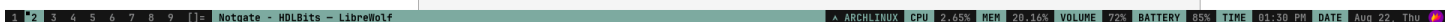
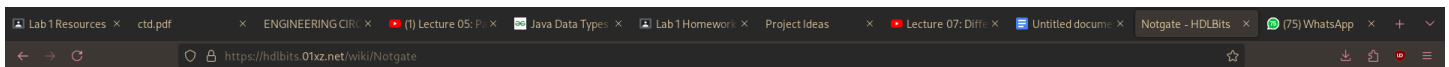
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Solution

[Show solution](#)



Q4. Andgate

```
module top_module(  
    input a,  
    input b,  
    output out );  
    assign out = a & b;  
endmodule
```

Lab 1 Resourcesctd.pdfENGINEERING CIR...Lecture 05: P...Java Data Types...Lab 1 Homework...Project IdeasLecture 07: Diff...Untitled docum...Andgate - HDLBits(75) WhatsApp

←→↻https://hdlbits.01xz.net/wiki/Andgate

top_module

Expected solution length: Around 1 line.

Module Declaration

```
module top_module(  
    input a,  
    input b,  
    output out );
```

Hint

Write your solution here

Last success: 8/20/2024, 9:52:40 PMLoad

```
1 module top_module(  
2     input a,  
3     input b,  
4     output out );  
5     assign out = a & b;  
6 endmodule  
7
```

SubmitSubmit (new window)

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←notgatePreviousNextnorgate→

...step_onezerowirewire4notgateandgate-norgate-norgate-wire_dec7458-vector0-vector1-vector2-vec

This page was last modified on 23 September 2018, at 15:05.

123456789[]Andgate - HDLBits - LibreWolfARCHLINUXCPU 2.62%MEM 20.25%VOLUME 6%BATTERY 85%TIME 01:31 PMDATE Aug 22, Thu

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←→↻https://hdlbits.01xz.net/wiki/Andgate

andgate — Compile and simulate

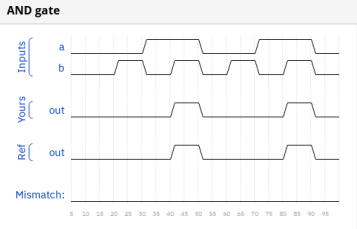
Running Quartus synthesis. [Show Quartus messages...](#)
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Status: Success!

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The 'Mismatch' trace shows which cycles your outputs don't match the reference outputs (o = correct, 1 = incorrect).



Q5. Norgate

```
module top_module(  
    input a,  
    input b,  
    output out );  
    assign out = ~(a|b);  
endmodule
```

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https://hdlbits.01xz.net/wiki/Norgate

top_module

Expected solution length: Around 1 line.

Module Declaration

```
module top_module(  
    input a,  
    input b,  
    output out );
```

Hint

Write your solution here

Last success: 8/20/2024, 9:53:16 PMLoad

```
1 module top_module(  
2     input a,  
3     input b,  
4     output out );  
5     assign out = ~(a|b);  
6 endmodule  
7
```

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← andgatePreviousNext xnorgate →

•• step_one • zero • wire • wire4 • notgate • andgate • **norgate** • xnorgate • wire_dec • 7458 • vector0 • vector1 • vector2 • vectorgates • 1

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About HDLBits

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norgate — Compile and simulate

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Running ModelSim simulation: [Show Modelsim messages...](#)

Status: Success!

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).

NOR gate

Inputs

a

b

Your's

out

Ref

out

Mismatch:

Q6. Xnorgate

```
module top_module(  
    input a,  
    input b,  
    output out );  
    assign out = ~a&~b | a&b;  
endmodule
```

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top_module

Expected solution length: Around 1 line.

Module Declaration

```
module top_module(  
    input a,  
    input b,  
    output out );
```

Hint...

Write your solution here

Last success: 8/20/2024, 9:55:34 PMLoad

```
1 module top_module(  
2     input a,  
3     input b,  
4     output out );  
5     assign out = ~a&b | a&b;  
6 endmodule  
7
```

SubmitSubmit (new window)

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←xnorgatePreviousNextwire_decl→

step_onezerowirewire4xnorgateandgatexnorgatewire_decl7458vector0vector1vector2vectorgates4ve

This page was last modified on 15 October 2016, at 03:19.

About HDLBits

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xnorgate — Compile and simulate

Running Quartus synthesis: [Show Quartus messages...](#)
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Status: Success!

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).

XNOR gate

Inputs

a

b

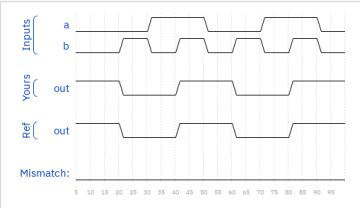
Your's

out

Ref

out

Mismatch:



Q7. Wire_decl

```
`default_nettype none
module top_module(
    input a,
    input b,
    input c,
    input d,
    output out,
    output out_n );
wire P, Q;
assign P = a&b;
assign Q = c&d;
assign out = P|Q;
assign out_n = ~P&~Q;
endmodule
```

Lab1 Resources × ctd.pdf × ENGINEERING CIR × (1) Lecture 05: F × Java Data Type × Lab1 Homework × Project Ideas × Lecture 07: Diff × Untitled docum × Wire decl - HDLBits × (75) WhatsApp × +

https://hdlbits.01xz.net/wiki/Wire_decl

Expected solution length: Around 5 lines.

Module Declaration

```
`default_nettype none
module top_module(
    input a,
    input b,
    input c,
    input d,
    output out,
    output out_n );
```

Write your solution here

Last success: 8/20/2024, 10:10:09 PM Load

```
1 `default_nettype none
2 module top_module(
3     input a,
4     input b,
5     input c,
6     input d,
7     output out,
8     output out_n );
9
10 wire P, Q;
11 assign P = a&b;
12 assign Q = c&d;
13 assign out = P|Q;
14 assign out_n = ~P&~Q;
15
16 endmodule
17
```

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wire_decl — Compile and simulate

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Status: Success!

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Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The 'Mismatch' trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).

Exhaustive test



wire_decl - HDLBits - LibreWolf

ARCH LINUX CPU 2.52% MEM 24.62% VOLUME 47% BATTERY 63% TIME 11:35 AM DATE Aug 22, Thu

Q8. 7458

```
module top_module (  
    input p1a, p1b, p1c, p1d, p1e, p1f,  
    output p1y,  
    input p2a, p2b, p2c, p2d,  
    output p2y );  
    wire P, Q, R, S;  
    assign P = p2a & p2b;  
    assign Q = p2c & p2d;  
    assign p2y = P | Q;  
    assign R = p1a & p1b & p1c;  
    assign S = p1d & p1e & p1f;  
    assign p1y = R | S;  
endmodule
```

Module Declaration

```
module top_module (  
    input p1a, p1b, p1c, p1d, p1e, p1f,  
    output p1y,  
    input p2a, p2b, p2c, p2d,  
    output p2y );
```

Hint...

Write your solution here

Last success: 8/20/2024 10:15:11 PM [Load](#)

```
1 module top_module (  
2     input p1a, p1b, p1c, p1d, p1e, p1f,  
3     output p1y,  
4     input p2a, p2b, p2c, p2d,  
5     output p2y );  
6  
7     wire P, Q, R, S;  
8  
9     assign P = p2a & p2b;  
10    assign Q = p2c & p2d;  
11    assign p2y = P | Q;  
12  
13    assign R = p1a & p1b & p1c;  
14    assign S = p1d & p1e & p1f;  
15    assign p1y = R | S;  
16  
17 endmodule
```

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7458 — Compile and simulate

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Status: Success!

You have solved 15 problems. [See my progress](#).

Timing diagrams for selected test cases

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Inputs: p1a, p1b, p1c, p1d, p1e, p1f, p2a, p2b, p2c, p2d

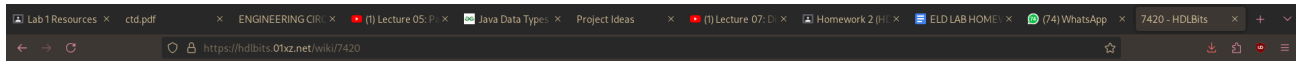
Your: p1y, p2y

Ref: p1y, p2y

Mismatch:

Q9. 7420

```
module top_module (  
    input p1a, p1b, p1c, p1d,  
    output p1y,  
    input p2a, p2b, p2c, p2d,  
    output p2y );  
    wire P,R;  
    assign P = p1a & p1b & p1c & p1d;  
    assign R = p2a & p2b & p2c & p2d;  
    assign p1y = ~P;  
    assign p2y = ~R;  
endmodule
```



Expected solution length: Around 2 lines.

Module Declaration

```
module top_module (  
    input p1a, p1b, p1c, p1d,  
    output p1y,  
    input p2a, p2b, p2c, p2d,  
    output p2y );
```

[Hint](#)

Write your solution here

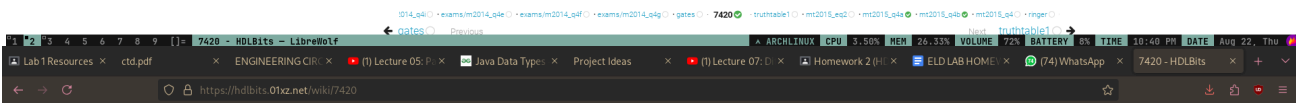
Last success: 8/20/2024, 10:20:52 PM [Load](#)

```
1 module top_module (  
2     input p1a, p1b, p1c, p1d,  
3     output p1y,  
4     input p2a, p2b, p2c, p2d,  
5     output p2y );  
6  
7     wire P,R;  
8  
9     assign P = p1a & p1b & p1c & p1d;  
10    assign R = p2a & p2b & p2c & p2d;  
11    assign p1y = ~P;  
12    assign p2y = ~R;  
13  
14 endmodule  
15
```

[Submit](#)

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7420 — Compile and simulate

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Running ModelSim simulation. [Show Modelsim messages...](#)

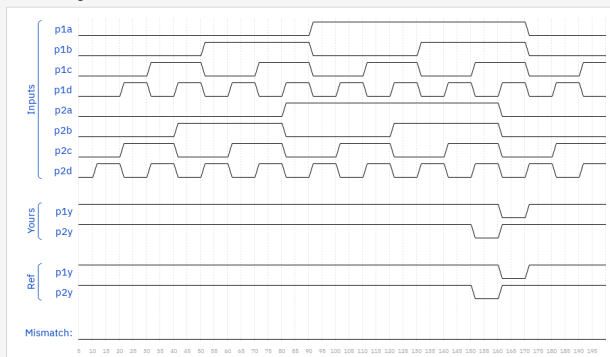
Status: Success!

You have solved 15 problems. [See my progress...](#)

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 - correct, 1 - incorrect).

Two NAND gates



Q10. mt2015_q4a

```
module top_module (input x, input y, output z);  
    wire P;  
    assign P = x^y;  
    assign z = P & x;  
endmodule
```

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https://hdlbits.01xz.net/wiki/Mt2015_q4a

Search

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Combinational Logic

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Wire

QND

NOR

Another gate

Two gates

More logic gates

7420 chip

Truth tables

Two-bit equality

Simple circuit A

Simple circuit B

Combine circuits A and B

Ring or vibrate?

Thermostat

3-bit population count

Gates and vectors

Even longer vectors

Multiplexers

Arithmetic Circuits

Karnaugh Map to Circuit

Sequential Logic

Building Larger Circuits

Verification: Reading Simulations

Verification: Writing Testbenches

CS450

Mt2015 q4a

mt2015_eq2Previous

Nextmt2015_q4b

Taken from 2015 midterm question 4

Module A is supposed to implement the function $z = (x^y) \& x$. Implement this module.

Module Declaration

module top_module (input x, input y, output z);

Write your solution here

Last success: 8/20/2024, 10:24:21 PM

Load

1 module top_module (input x, input y, output z);
2 wire P;
3 assign P = x^y;
4 assign z = P & x;
5 endmodule
6

SubmitSubmit (new window)

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1014_q4fexams/m2014_q4gates7420truthtable1mt2015_eq2mt2015_q4amt2015_q4bmt2015_q4ringthermostatpopcount3gatesvgi

mt2015_eq2Previous

Nextmt2015_q4b

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mt2015_q4a — Compile and simulate

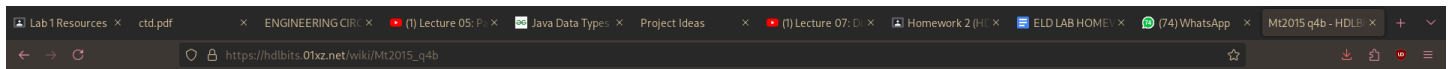
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Running ModelSim simulation. [Show Modelsim messages...](#)

Status: Success!

You have solved 15 problems. [See my progress...](#)

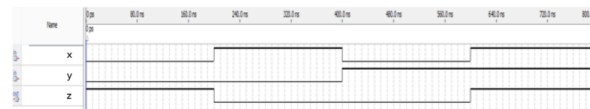
Q11. mt2015_q4b

```
module top_module ( input x, input y, output z );  
    wire P,R;  
    assign P = ~x & ~y;  
    assign R = x & y;  
    assign z = P | R;  
endmodule
```



- ☐ GND
- ☐ NOR
- ☐ Another gate
- ☐ Two gates
- ☐ More logic gates
- ☒ 7420 chip
- ☐ Truth tables
- ☐ Two-bit equality
- ☒ Simple circuit A
- ☒ Simple circuit B
- ☐ Combine circuits A and B
- ☐ Ring or vibrate?
- ☐ Thermostat
- ☐ 8-bit population count
- ☐ Gates and vectors
- ☐ Even longer vectors
- ▶ Multiplexers
- ▶ Arithmetic Circuits
- ▶ Karnaugh Map to Circuit
- ▶ Sequential Logic
- ▶ Building Larger Circuits
- ▶ Verification: Reading Simulations
- ▶ Verification: Writing Testbenches
- ▶ CS450

Circuit B can be described by the following simulation waveform:



Implement this circuit.

Module Declaration

```
module top_module ( input x, input y, output z );
```

Write your solution here

Last success: 8/20/2024, 10:27:37 PM

Load

```
1 module top_module ( input x, input y, output z );  
2     wire P,R;  
3     assign P = ~x & ~y;  
4     assign R = x & y;  
5     assign z = P | R;  
6 endmodule  
7
```

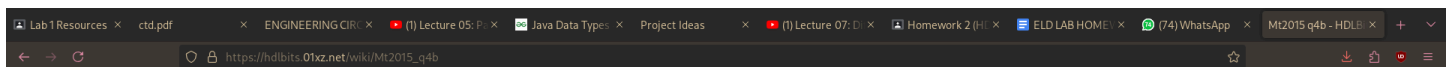
Submit

Submit (new window)

Upload a source file...

Solution

Show solution



mt2015_q4b — Compile and simulate

Running Quartus synthesis: [Show Quartus messages...](#)

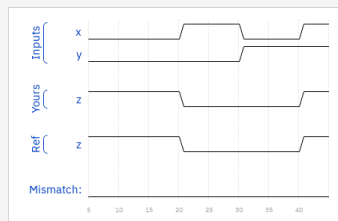
Running ModelSim simulation: [Show Modelsim messages...](#)

Status: Success!

You have solved 15 problems. [See my progress...](#)

Timing diagrams for selected test cases

These are timing diagrams from some of the test cases we used. They may help you debug your circuit. The diagrams show inputs to the circuit, outputs from your circuit, and the expected reference outputs. The "Mismatch" trace shows which cycles your outputs don't match the reference outputs (0 = correct, 1 = incorrect).



Q12. mux9to1v

```
module top_module(  
    input [15:0] a, b, c, d, e, f, g, h, i,  
    input [3:0] sel,  
    output [15:0] out );  
  
    always @(*) begin  
        if(sel == 4'b0000)  
            out = a;  
        else if(sel == 4'b0001)  
            out = b;  
        else if(sel == 4'b0010)  
            out = c;  
        else if(sel == 4'b0011)  
            out = d;  
        else if(sel == 4'b0100)  
            out = e;  
        else if(sel == 4'b0101)  
            out = f;  
        else if(sel == 4'b0110)  
            out = g;  
        else if(sel == 4'b0111)  
            out = h;  
        else if(sel == 4'b1000)  
            out = i;  
        else  
            out = {16{1'b1}};  
        end  
    end  
  
endmodule
```

