ELD LAB:3
HOMEWORK
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- **OBJECTIVE:** Recreate the previous homework in which we had to make an up/down counter which counts from 0 to 85 or vice versa in order to make it work with the hardware (zedboard/zybo)

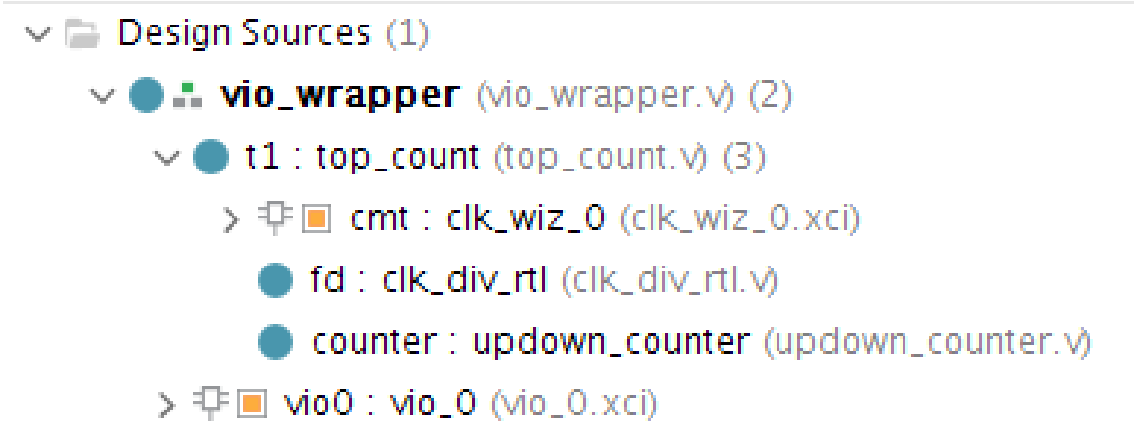
- **CHANGES MADE IN THE LAB CODE IN ORDER TO ACHIEVE THE OBJECTIVE**

1) Switched the counter_8bit.v file to updown_counter.v
2) Added “up” as a single bit input to top_count.v, updown_counter.v and as a single bit wire in vio_wrapper.v
3) Changed the dimension of “Count” from [7:0] (8 bits) to [6:0] (7 bits) in all files
4) Added “up” in all updown_counter and top_count module instantiation
5) In vio ip, added “up” as another output probe

- **IMP NOTE:** Do not add another “,” when assigning named arguments during initialization of a module since that will result in an error which is not verbose enough to be understood as a simple “,” issue

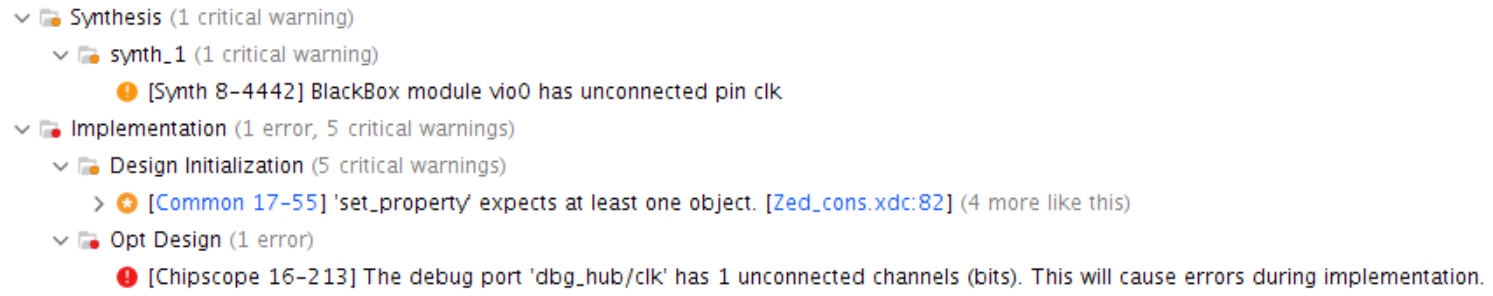
- **PROJECT DIRECTORY**

```
Lab3_hw
|__ vio_wrapper.v
    |__ top_count.v
    |    |__ clk_wiz_0.xci (clocking wizard IP)
    |    |__ clk_div_rtl.v
    |    |__ updown_counter.v
    |__ vio_0.xci (VIO IP)
```



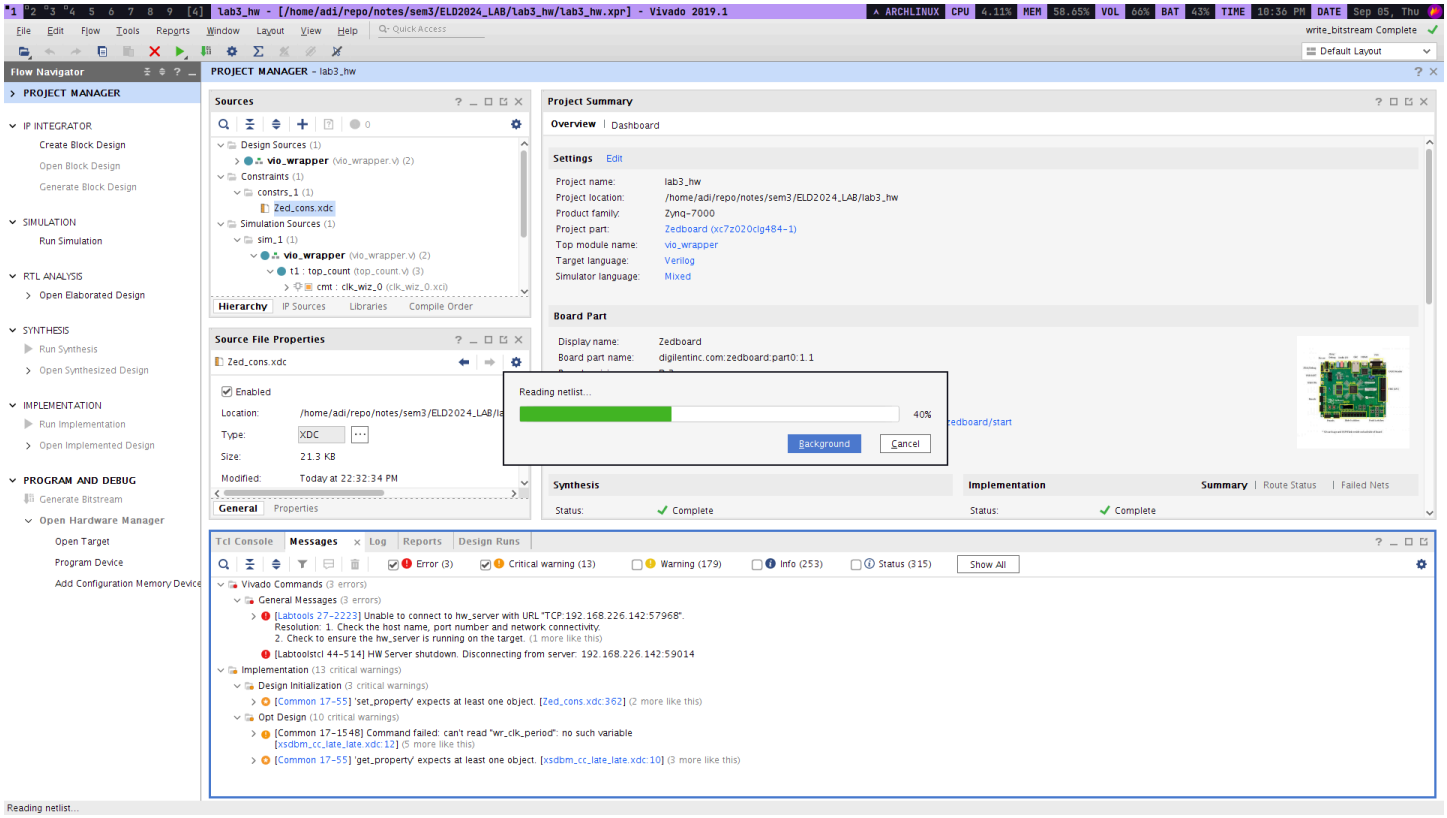
LOGS:

- As of 05/09/24 ⇒ 10:30PM, I am facing an error when running synthesis / generating bitstream

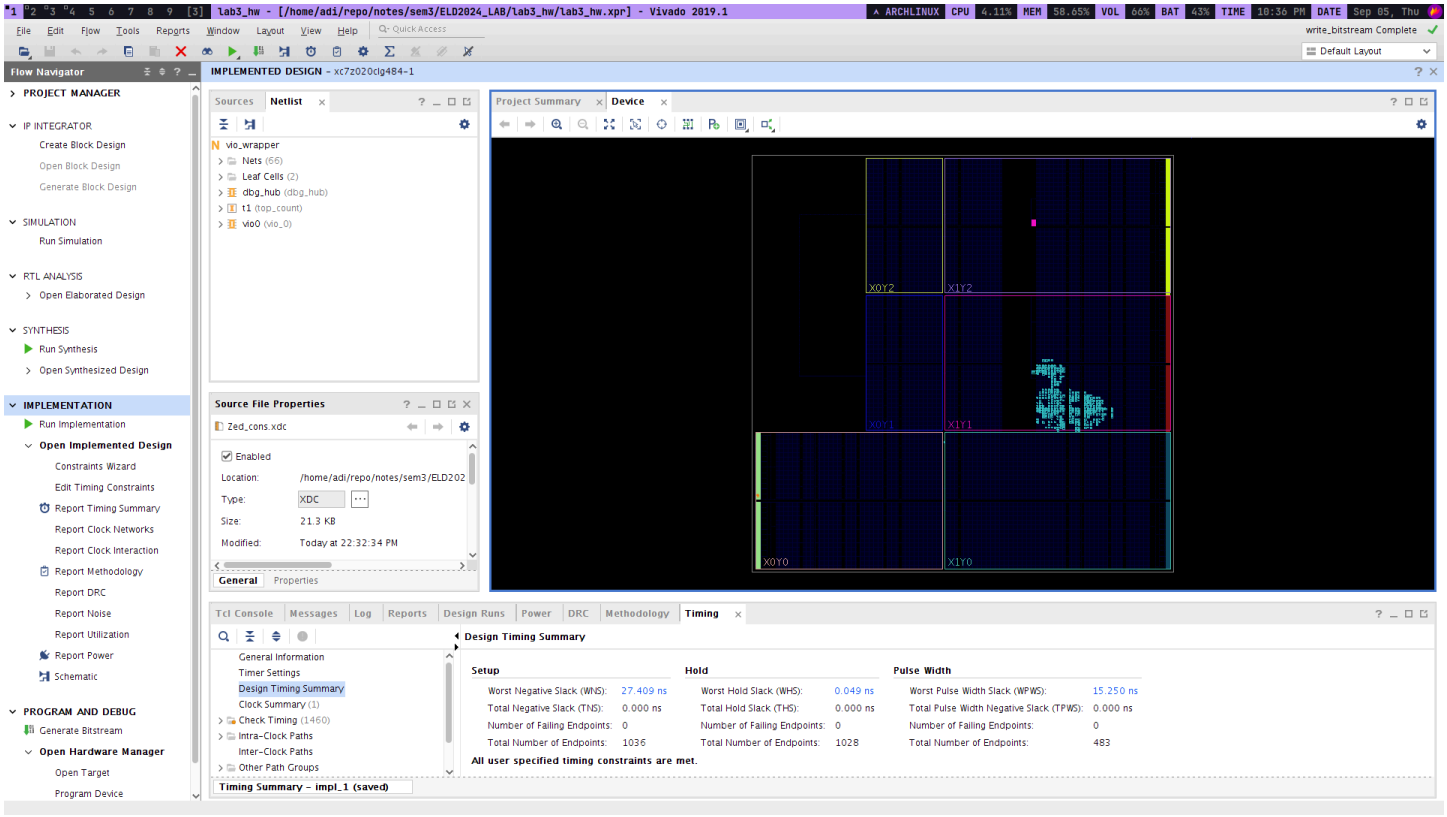


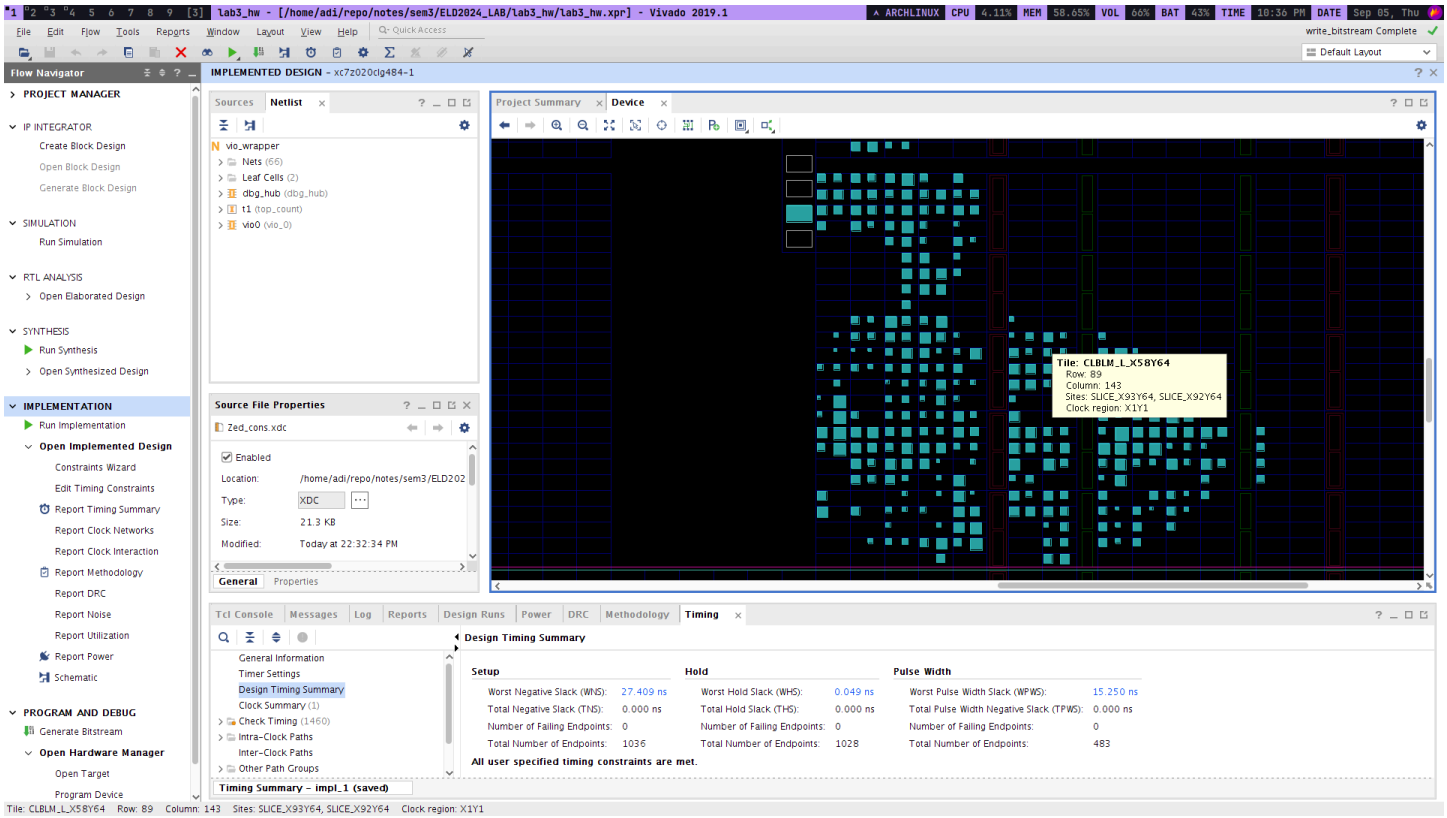
- Reason for the error: The clock label inside the constraint file was not matching with the one set in the project

- Bit stream generated

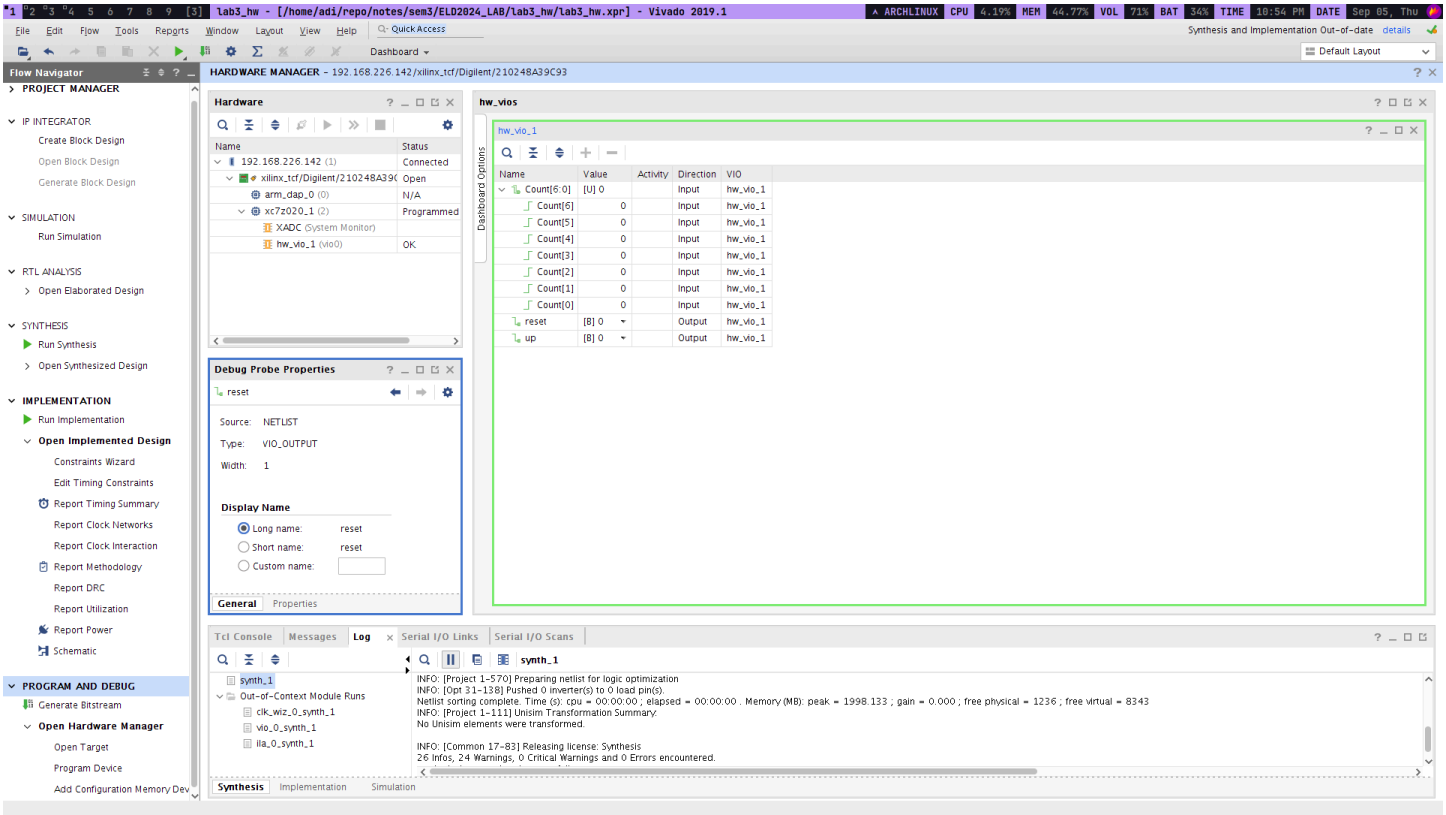


- Hardware implementation

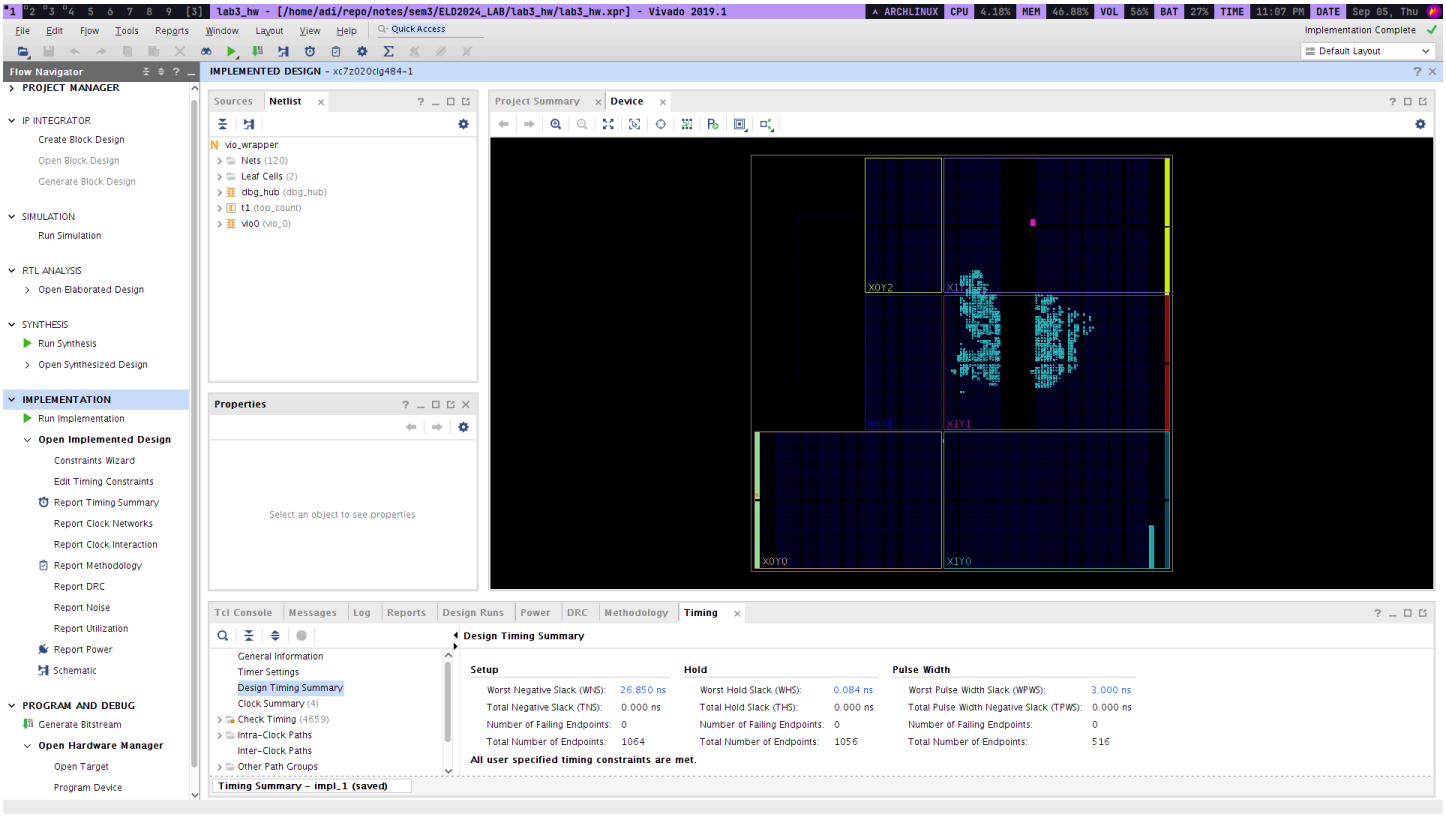




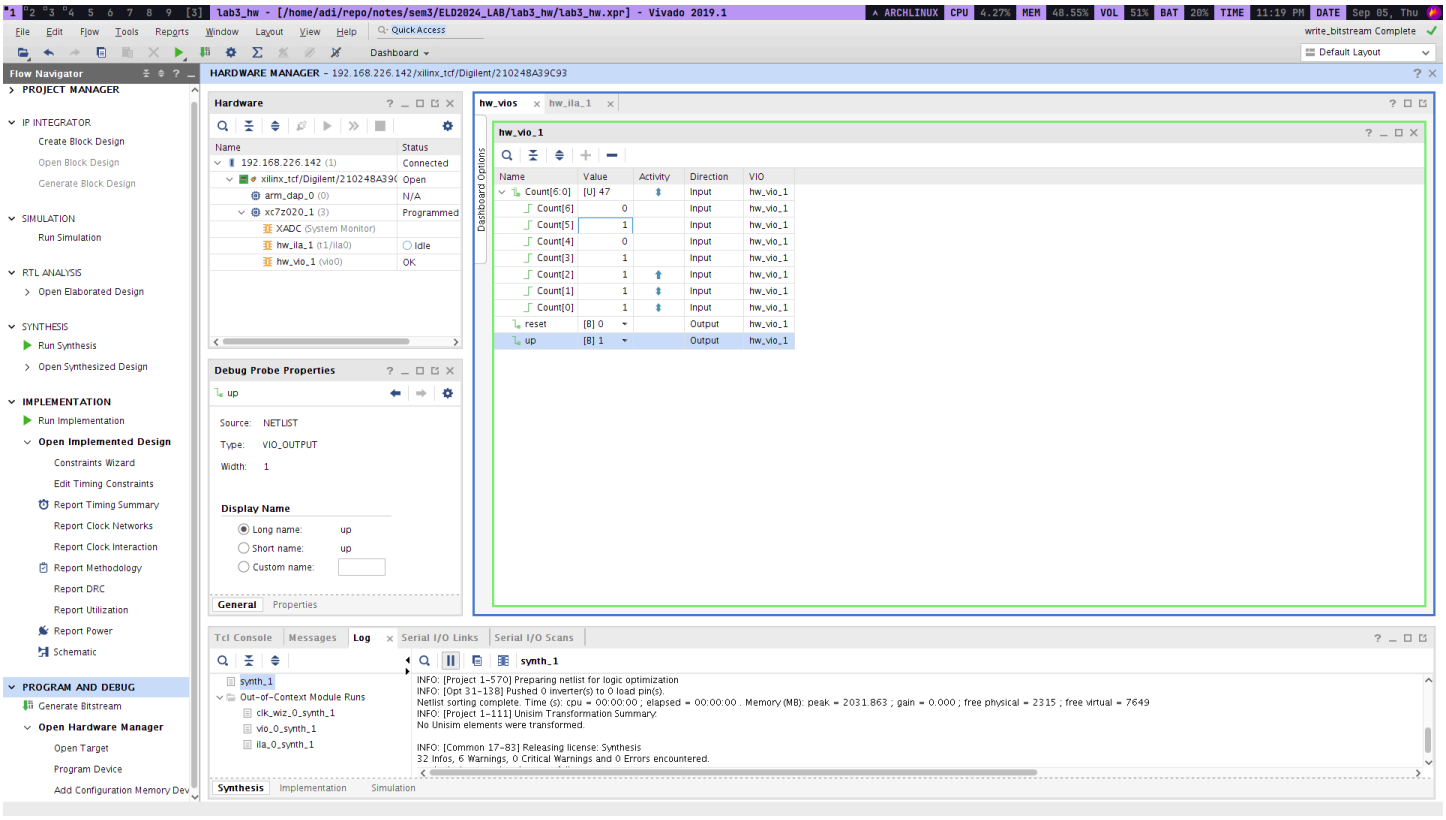
- LOG: As of this moment (10:37PM), I am able to generate the bitstream and see the hardware implementation, however my counter value does not seem to change when going to the “Program Device” tab under “Open Hardware Manager”. So, to be in sync with the lab youtube video, I am going to add another IP ⇒ ILA (Integrated Logic Analyzer) to my project to observe if that makes any difference.
- LOG_2 (11:02PM) ⇒ Adding the ILA IP made it so that I don't have to manually add all the ports myself when programming the board, but my Count output is still showing as 0 and not changing. I believe there might be a problem with my code logic.

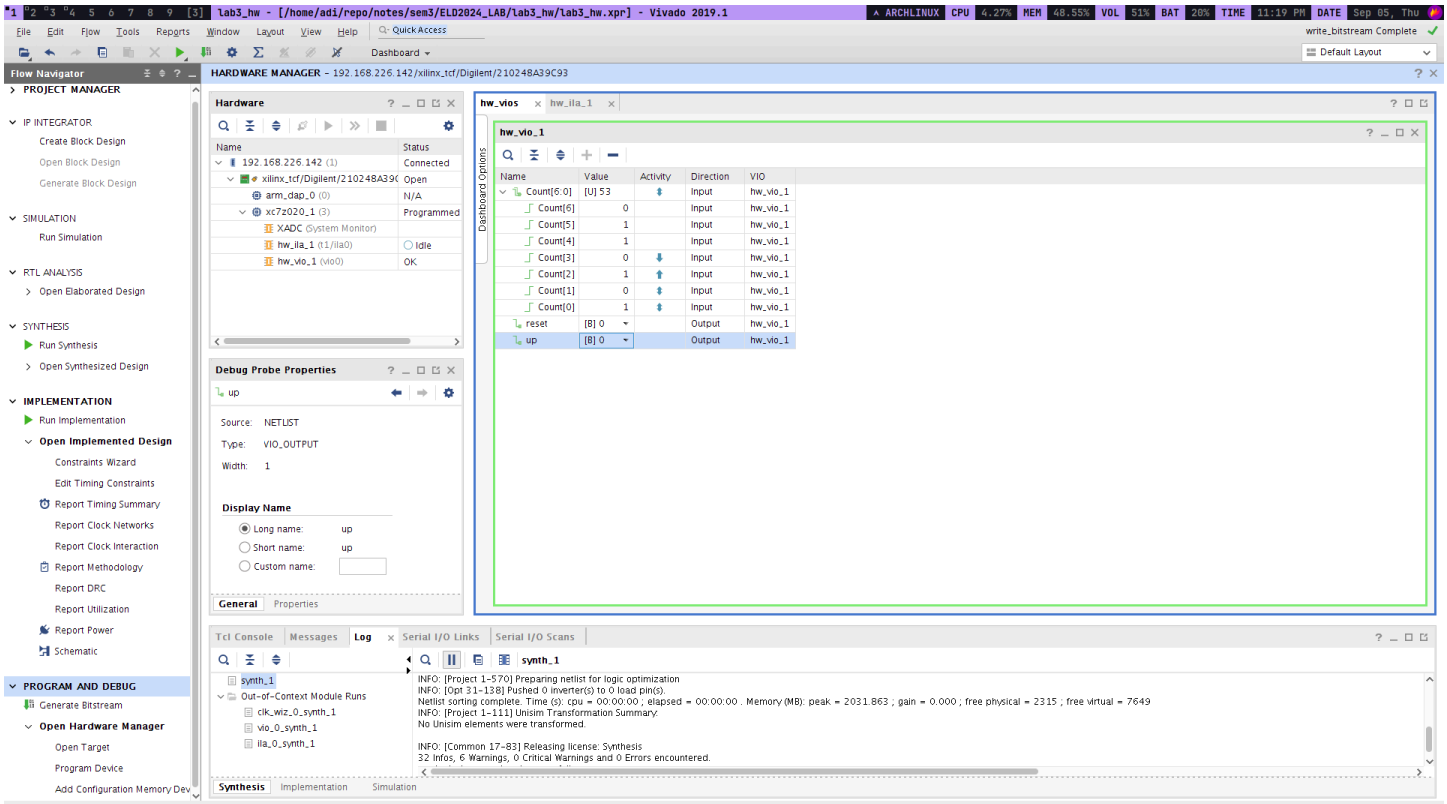


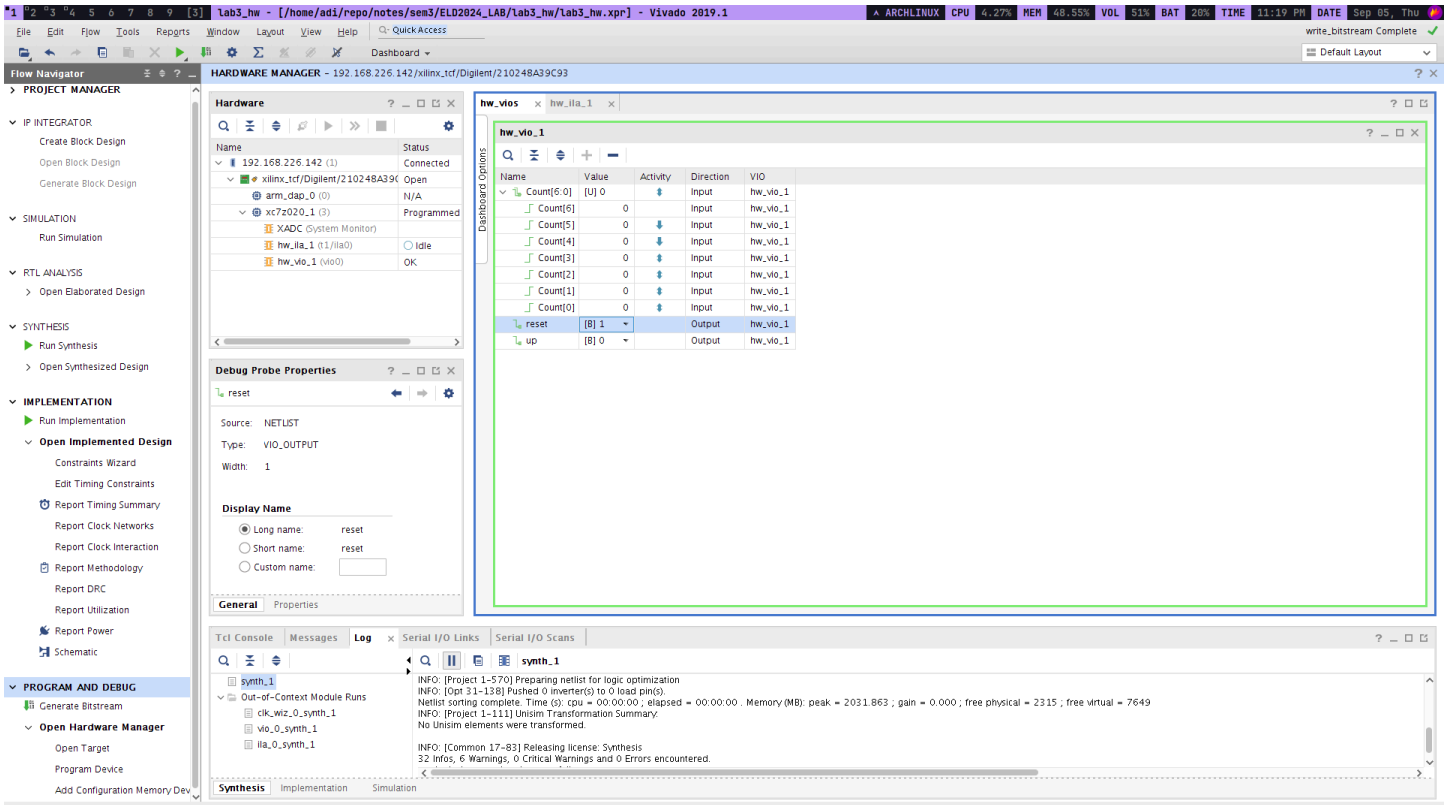
- Synthesis and Implementation done again


lab3_hw - [/home/adi/repo/notes/sem3/ELD2024_LAB/lab3_hw/lab3_hw.xpr] - Vivado 2019.1
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
PROJECT MANAGER
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
IMPLEMENTED DESIGN - xc7z020clg484-1
Sources
Netlist
vio_wrapper
Nets (120)
Leaf Cells (2)
dbg_hub (dbg_hub)
t1 (top_count)
vio0 (vio_0)
Properties
Select an object to see properties
Project Summary
Device
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Tcl Console
Messages
Log
Reports
Design Runs
Power
DRC
Methodology
Timing
General Information
Timer Settings
Design Timing Summary
Clock Summary (4)
Check Timing (4659)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
Timing Summary - impl_1 (saved)
Design Timing Summary
Setup
Worst Negative Slack (WNS): 26.850 ns
Total Negative Slack (TNS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1064
Hold
Worst Hold Slack (WHS): 0.084 ns
Total Hold Slack (THS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 1056
Pulse Width
Worst Pulse Width Slack (WPWS): 3.000 ns
Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0
Total Number of Endpoints: 516
All user specified timing constraints are met.

- **FINAL WORKING HOMEWORK (11:19PM, 05/09/24)**
    - Reason for not working earlier: I had assigned the output of “present state” variable to a variable “count” (with a small “c”) instead of the intended output, i.e. “Count” (with a big “C”)
    - How did I find out the issue: The console showed a warning message where it said that the variable Count is not connected to anything and alongside further inspection of the updown_counter.v file, I was able to find out the error.





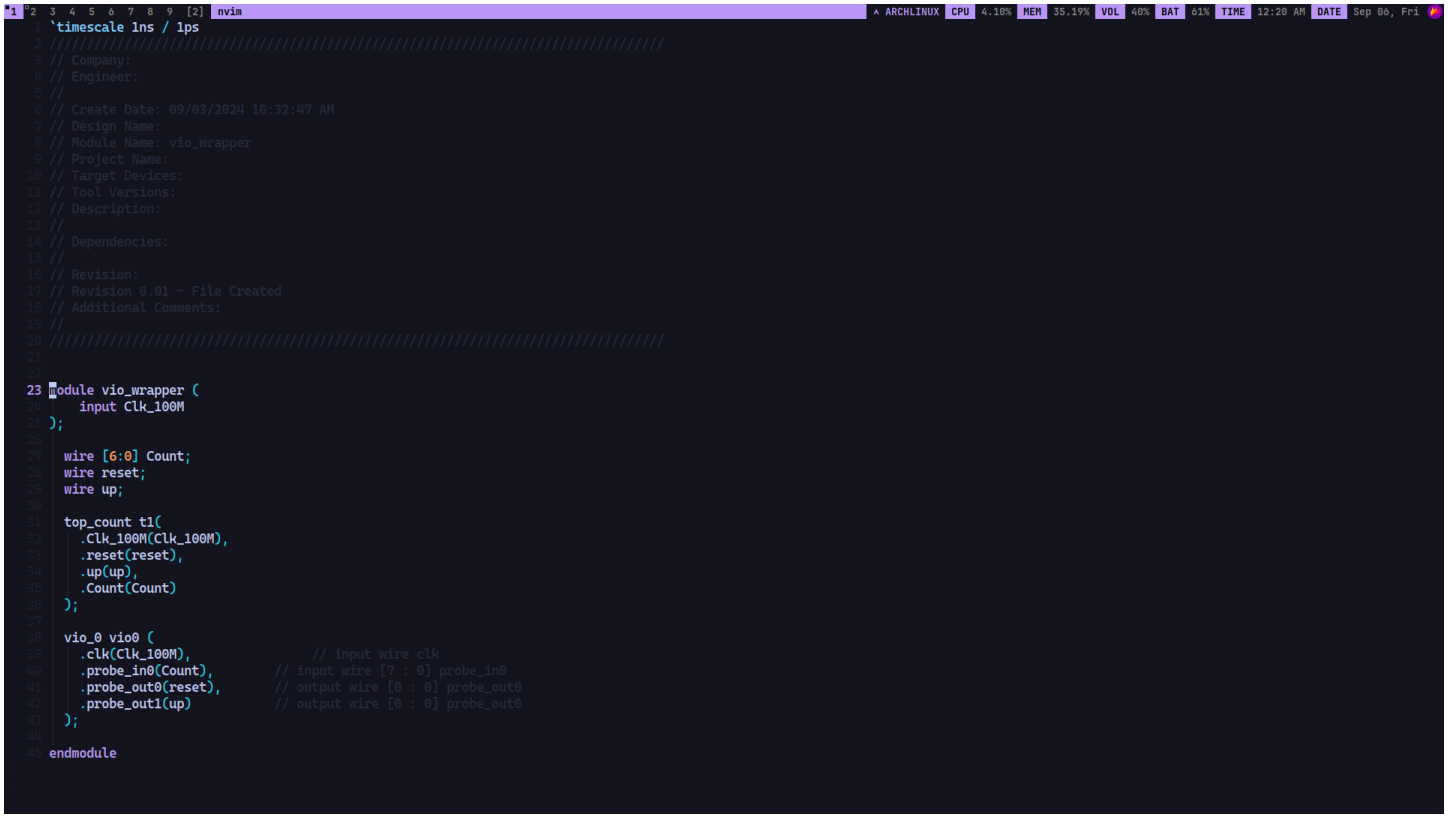


- Video recording of the working demo of the homework: https://drive.google.com/file/d/1n9O1FppWEjhuTghJk0mdoFBsIHKjiL68/view?usp=sharing

CODE

- vio_wrapper.v

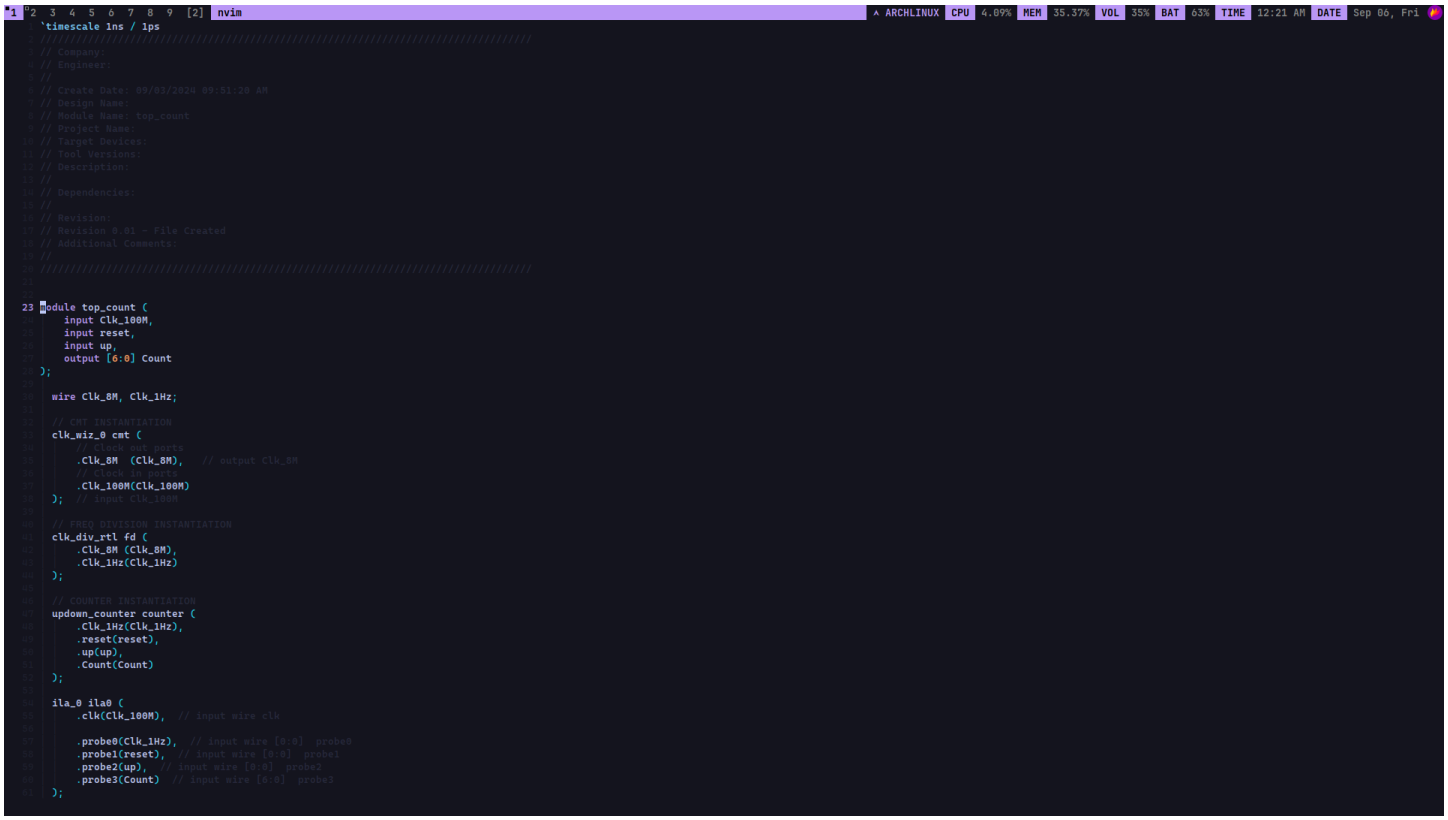
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/03/2024 10:32:47 AM
// Design Name:
// Module Name: vio_wrapper
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module vio_wrapper (
       input Clk_100M
);

  wire [6:0] Count;
  wire reset;
  wire up;

  top_count t1(
       .Clk_100M(Clk_100M),
       .reset(reset),
       .up(up),
       .Count(Count)
  );

  vio_0 vio0 (
       .clk(Clk_100M),                // input wire clk
       .probe_in0(Count),     // input wire [7 : 0] probe_in0
       .probe_out0(reset),    // output wire [0 : 0] probe_out0
       .probe_out1(up)        // output wire [0 : 0] probe_out0
  );

endmodule
```



- top_count.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/03/2024 09:51:20 AM
// Design Name:
// Module Name: top_count
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module top_count (
        input Clk_100M,
        input reset,
        input up,
        output [6:0] Count
);

  wire Clk_8M, Clk_1Hz;

  // CMT INSTANTIATION
  clk_wiz_0 cmt (
```

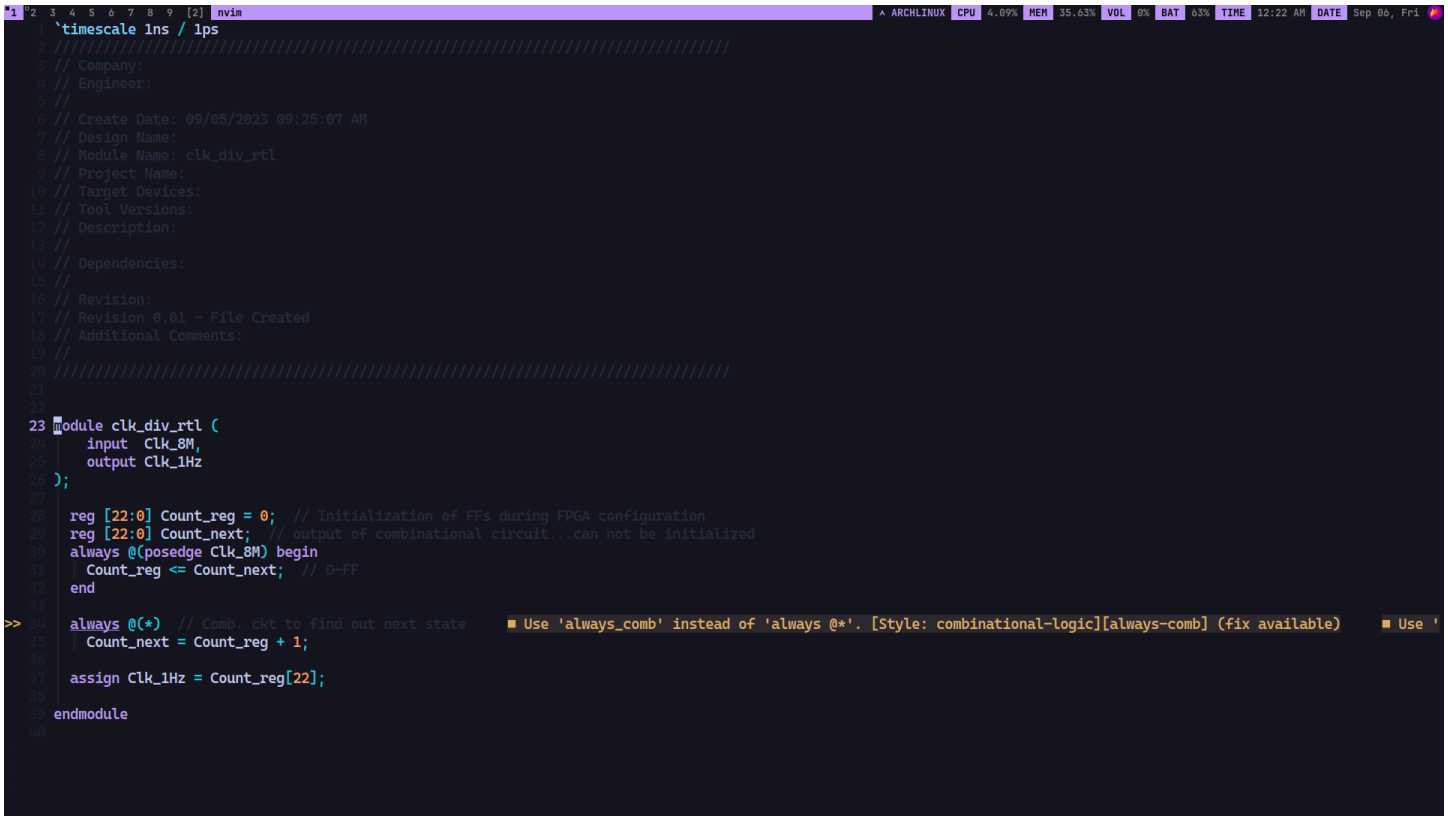
```
        // Clock out ports
        .Clk_8M  (Clk_8M),   // output Clk_8M
        // Clock in ports
        .Clk_100M(Clk_100M)
    );  // input Clk_100M

    // FREQ DIVISION INSTANTIATION
    clk_div_rtl fd (
        .Clk_8M (Clk_8M),
        .Clk_1Hz(Clk_1Hz)
    );

    // COUNTER INSTANTIATION
    updown_counter counter (
        .Clk_1Hz(Clk_1Hz),
        .reset(reset),
        .up(up),
        .Count(Count)
    );

    ila_0 ila0 (
        .clk(Clk_100M),  // input wire clk

        .probe0(Clk_1Hz),  // input wire [0:0]  probe0
        .probe1(reset),  // input wire [0:0]  probe1
        .probe2(up),  // input wire [0:0]  probe2
        .probe3(Count)  // input wire [6:0]  probe3
    );

endmodule
```



- clk_div_rtl.v

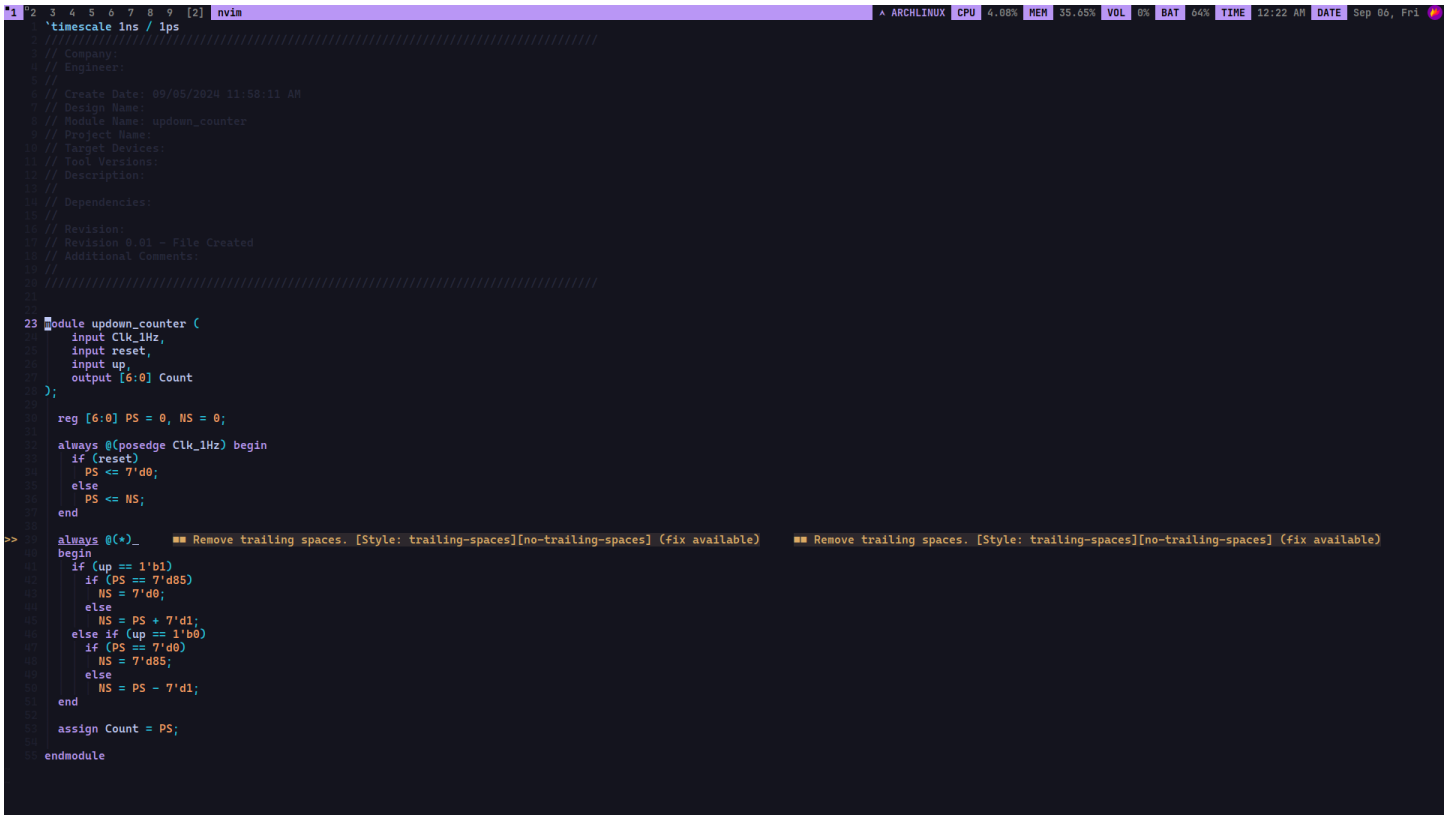
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
```

```
// Engineer:
//
// Create Date: 09/05/2023 09:25:07 AM
// Design Name:
// Module Name: clk_div_rtl
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module clk_div_rtl (
        input  Clk_8M,
        output Clk_1Hz
);

  reg [22:0] Count_reg = 0;  // Initialization of FFs during FPGA configuration
  reg [22:0] Count_next;  // output of combinational circuit...can not be initialized
  always @(posedge Clk_8M) begin
        Count_reg <= Count_next;  // D-FF
  end

  always @(*)  // Comb. ckt to find out next state
        Count_next = Count_reg + 1;

  assign Clk_1Hz = Count_reg[22];

endmodule
```



- updown_counter.v

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/05/2024 11:58:11 AM
// Design Name:
// Module Name: updown_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module updown_counter (
        input Clk_1Hz,
        input reset,
        input up,
        output [6:0] Count
);

  reg [6:0] PS = 0, NS = 0;

  always @(posedge Clk_1Hz) begin
        if (reset)
        PS <= 7'd0;
        else
        PS <= NS;
  end

  always @(*)
  begin
        if (up == 1'b1)
        if (PS == 7'd85)
        NS = 7'd0;
        else
        NS = PS + 7'd1;
        else if (up == 1'b0)
        if (PS == 7'd0)
        NS = 7'd85;
        else
        NS = PS - 7'd1;
  end

  assign Count = PS;

endmodule
```


1 2 3 4 5 6 7 8 9 [2] nvim
^ ARCHLINUX CPU 4.08% MEM 35.65% VOL 0% BAT 64% TIME 12:22 AM DATE Sep 06, Fri
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 09/05/2024 11:58:11 AM
// Design Name:
// Module Name: updown_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module updown_counter (
input Clk_1Hz,
input reset,
input up,
output [6:0] Count
);
reg [6:0] PS = 0, NS = 0;
always @(posedge Clk_1Hz) begin
if (reset)
PS <= 7'd0;
else
PS <= NS;
end
always @(*)_
Remove trailing spaces. [Style: trailing-spaces][no-trailing-spaces] (fix available)
Remove trailing spaces. [Style: trailing-spaces][no-trailing-spaces] (fix available)
begin
if (up == 1'b1)
if (PS == 7'd85)
NS = 7'd0;
else
NS = PS + 7'd1;
else if (up == 1'b0)
if (PS == 7'd0)
NS = 7'd85;
else
NS = PS - 7'd1;
end
assign Count = PS;
endmodule