

ELD LAB:3
HOMEWORK
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- **OBJECTIVE:** Recreate the previous homework in which we had to make an up/down counter which counts from 0 to 85 or vice versa in order to make it work with the hardware (zedboard/zybo)

- **CHANGES MADE IN THE LAB CODE IN ORDER TO ACHIEVE THE OBJECTIVE**
 - 1) Switched the counter_8bit.v file to updown_counter.v
 - 2) Added "up" as a single bit input to top_count.v, updown_counter.v and as a single bit wire in vio_wrapper.v
 - 3) Changed the dimension of "Count" from [7:0] (8 bits) to [6:0] (7 bits) in all files
 - 4) Added "up" in all updown_counter and top_count module instantiation
 - 5) In vio ip, added "up" as another output probe

- **IMP NOTE:** Do not add another "," when assigning named arguments during initialization of a module since that will result in an error which is not verbose enough to be understood as a simple "," issue

- PROJECT DIRECTORY

Lab3_hw

```
|__ vio_wrapper.v
    |__ top_count.v
        |__ clk_wiz_0.xci (clocking wizard IP)
        |__ clk_div_rtl.v
        |__ updown_counter.v
    |__ vio_0.xci (VIO IP)
```

▼  Design Sources (1)

▼ ●  **vio_wrapper** (vio_wrapper.v) (2)

▼ ● t1 : top_count (top_count.v) (3)

>   cmt : clk_wiz_0 (clk_wiz_0.xci)

● fd : clk_div_rtl (clk_div_rtl.v)

● counter : updown_counter (updown_counter.v)

>   vio0 : vio_0 (vio_0.xci)

LOGS:

- As of 05/09/24 ⇒ 10:30PM, I am facing an error when running synthesis / generating bitstream

- ✓ Synthesis (1 critical warning)
 - ✓ synth_1 (1 critical warning)
 - [Synth 8-4442] BlackBox module vio0 has unconnected pin clk
- ✓ Implementation (1 error, 5 critical warnings)
 - ✓ Design Initialization (5 critical warnings)
 - > [Common 17-55] 'set_property' expects at least one object. [Zed_cons.xdc:82] (4 more like this)
 - ✓ Opt Design (1 error)
 - [Chipscope 16-213] The debug port 'dbg_hub/clk' has 1 unconnected channels (bits). This will cause errors during implementation.

- Reason for the error: The clock label inside the constraint file was not matching with the one set in the project

- Bit stream generated

The screenshot displays the Vivado IDE interface for a project named 'lab3_hw'. The 'Sources' pane on the left shows the project hierarchy, including 'Design Sources', 'Constraints', and 'Simulation Sources'. The 'Source File Properties' pane for 'Zed_cons.xdc' shows it is enabled and located at '/home/ad1/repo/notes/sem3/ELD2024_LAB/lab3_hw'. The 'Tcl Console' pane at the bottom shows messages, including a warning about 'set_property' and a critical error about 'set_property' expecting at least one object. The 'Messages' pane shows a list of errors and warnings, including the same 'set_property' error. The 'Implementation' status is 'Complete'.

- Hardware implementation

The screenshot displays the Vivado 2019.1 IDE interface for a hardware implementation project named 'lab3_hw'. The top status bar indicates the project is on ARCHLINUX with CPU at 4.11%, MEM at 58.65%, VOL at 66%, BAT at 43%, and TIME at 10:36 PM on Sep 05, Thu. The main workspace is divided into several panes:

- Project Manager:** Shows the project hierarchy with 'vto_wrapper' as the top-level entity, containing 'Nets (66)', 'Leaf Cells (2)', 'dbg_hub (dbg_hub)', 't1 (top_count)', and 'vto0 (vto_0)'.
- Source File Properties:** Displays properties for 'Zed_cons.xdc', including its location, type (XDC), size (21.3 KB), and modification time (Today at 22:32:34 PM).
- Device:** Shows a grid-based representation of the device layout with labels like X0Y2, X1Y2, X0Y1, X1Y1, X0Y0, and X1Y0.
- Design Timing Summary:** Provides a detailed overview of timing constraints and their status.

The **Design Timing Summary** pane is expanded, showing the following data:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	27.409 ns	Worst Hold Slack (WHS):	0.049 ns	Worst Pulse Width Slack (WPWS):	15.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

This screenshot shows the same Vivado 2019.1 interface as the previous one, but with a different view of the device layout. The **Device** pane now displays a grid-based representation of the device layout with a yellow callout box highlighting a specific tile:

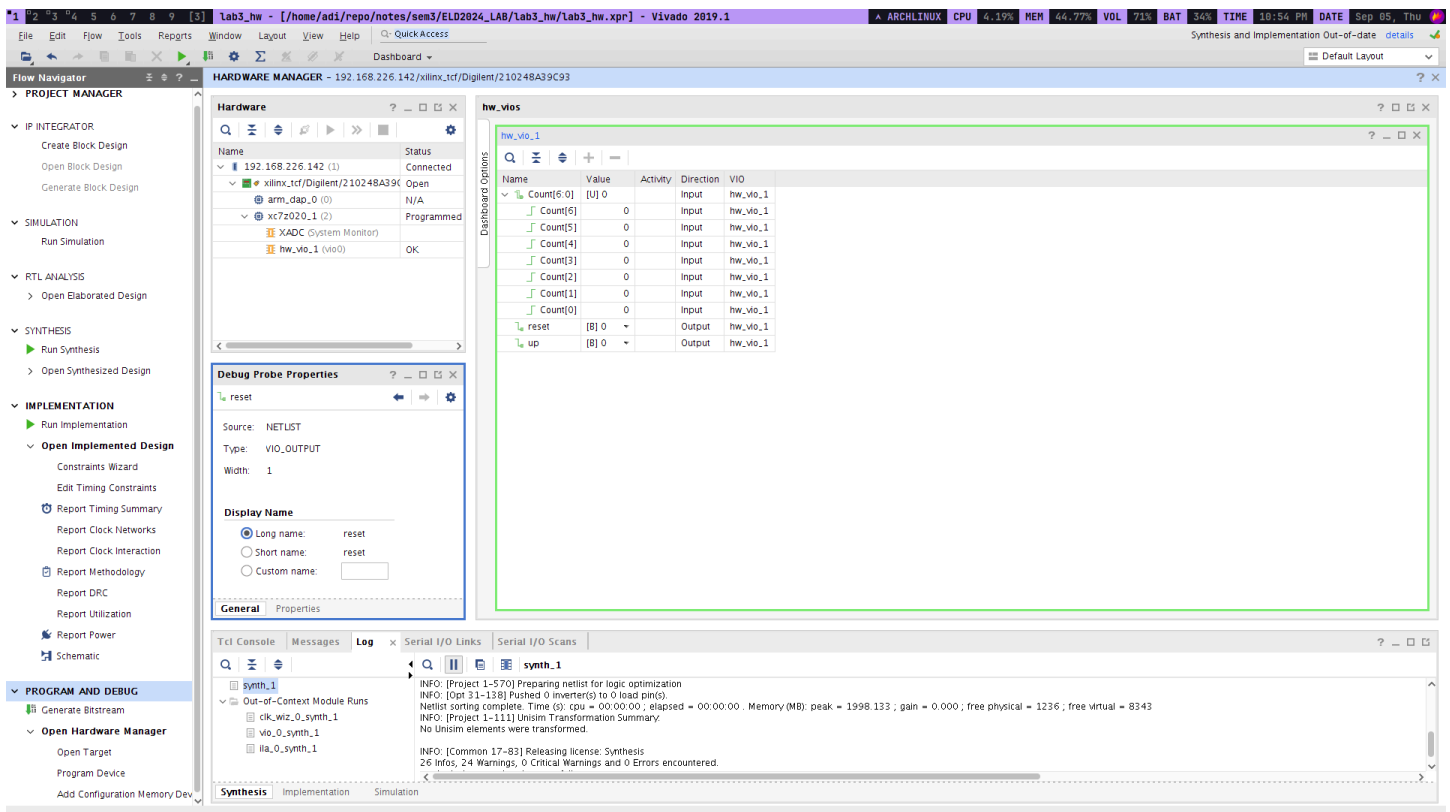
Tile: CLBML_X58Y64
Row: 89
Column: 143
Sites: SLICE_X93Y64, SLICE_X92Y64
Clock region: X1Y1

The **Design Timing Summary** pane remains expanded, showing the same timing data as before:

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	27.409 ns	Worst Hold Slack (WHS):	0.049 ns	Worst Pulse Width Slack (WPWS):	15.250 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1036	Total Number of Endpoints:	1028	Total Number of Endpoints:	483

All user specified timing constraints are met.

- LOG: As of this moment (10:37PM), I am able to generate the bitstream and see the hardware implementation, however my counter value does not seem to change when going to the "Program Device" tab under "Open Hardware Manager". So, to be in sync with the lab youtube video, I am going to add another IP \Rightarrow ILA (Integrated Logic Analyzer) to my project to observe if that makes any difference.
- LOG_2 (11:02PM) \Rightarrow Adding the ILA IP made it so that I don't have to manually add all the ports myself when programming the board, but my Count output is still showing as 0 and not changing. I believe there might be a problem with my code logic.



- Synthesis and Implementation done again

123456789[3]lab3_hw - [/home/adi/repo/notes/sem3/ELB2024_LAB/lab3_hw/lab3_hw.xpr] - Vivado 2019.1ARCHLINUXCPU 4.10%MEM 46.88%VOL 96%BAT 27%TIME 11:07 PMDATE Sep 05, Thu

FileEditFlowToolsReportsWindowLayoutViewHelpQuick Access

Flow Navigator

PROJECT MANAGER

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Open Elaborated Design

SYNTHESIS

- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION

- Run Implementation
- Open Implemented Design
 - Constraints Wizard
 - Edit Timing Constraints
 - Report Timing Summary
 - Report Clock Networks
 - Report Clock Interaction
 - Report Methodology
 - Report DRC
 - Report Noise
 - Report Utilization
 - Report Power
 - Schematic

PROGRAM AND DEBUG

- Generate Bitstream
- Open Hardware Manager
 - Open Target
 - Program Device

SourcesNetlist

- Wdg_wrapper
 - Nets (120)
 - Leaf Cells (2)
 - dbg_hub (dbg_hub)
 - t1_top_count
 - w00 (w0_0)

Properties

Select an object to see properties

Project SummaryDevice

Tcl ConsoleMessagesLogReportsDesign RunsPowerDRCMethodologyTiming

Design Timing Summary

General Information

Timer Settings

- Design Timing Summary
- Clock Summary (4)
- Check Timing (4559)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups

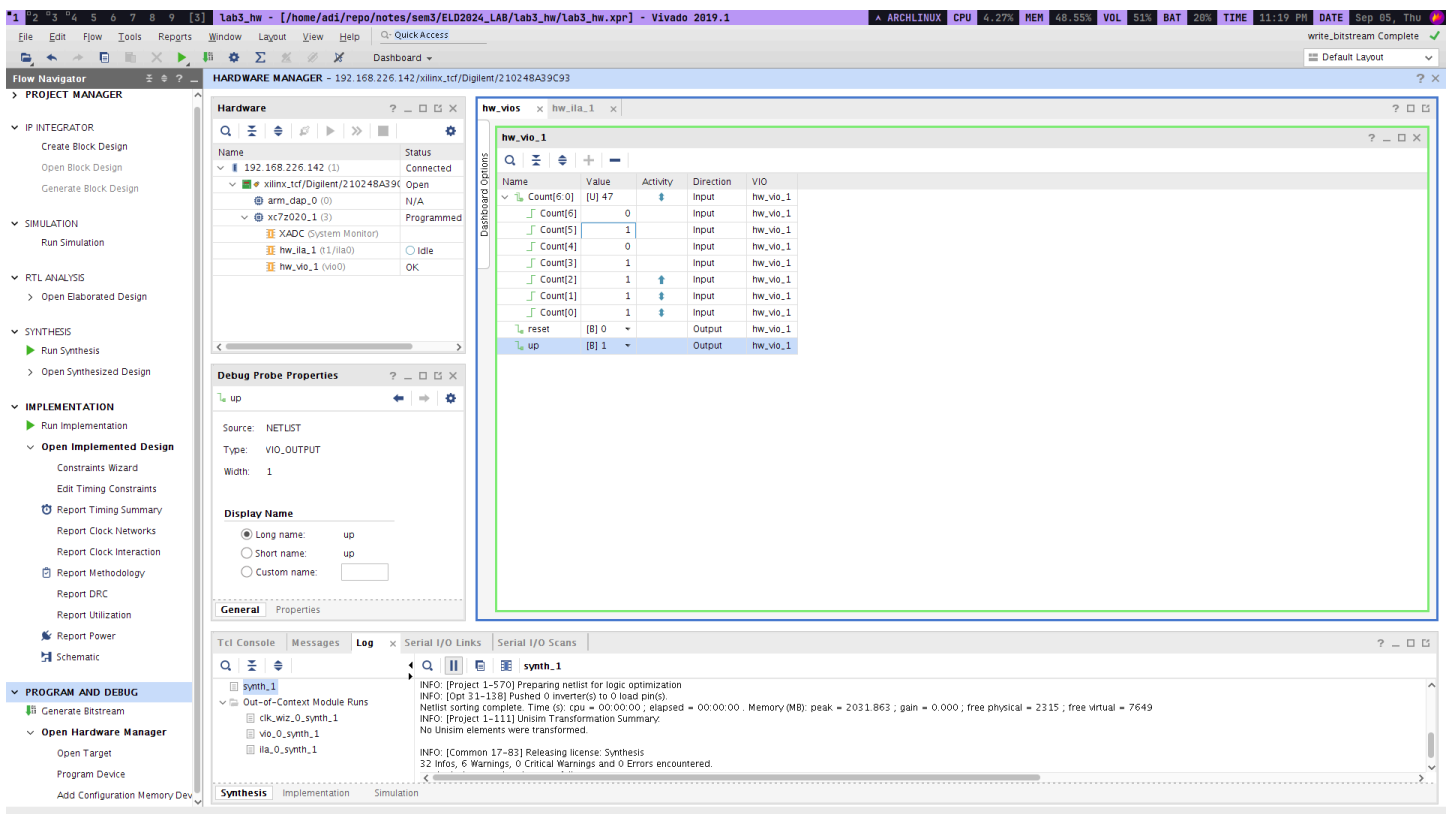
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 26.850 ns	Worst Hold Slack (WHS): 0.084 ns	Worst Pulse Width Slack (WPWS): 3.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 1054	Total Number of Endpoints: 1056	Total Number of Endpoints: 516

All user specified timing constraints are met.

Timing Summary - Impl_1 (saved)

- FINAL WORKING HOMEWORK (11:19PM, 05/09/24)

- Reason for not working earlier: I had assigned the output of "present state" variable to a variable "count" (with a small "c") instead of the intended output, i.e. "Count" (with a big "C")
- How did I find out the issue: The console showed a warning message where it said that the variable Count is not connected to anything and alongside further inspection of the updown_counter.v file, I was able to find out the error.



The screenshot shows the Vivado 2019.1 interface. The left sidebar contains the Project Manager and Implementation sections. The main window is divided into several panes:

- Hardware Manager:** Displays a list of hardware components. The 'up' signal is selected, and its properties are shown in the 'Debug Probe Properties' pane. The 'Display Name' is set to 'up'.
- hw_vios:** A table showing the status of various signals. The 'up' signal is highlighted in blue.
- Debug Probe Properties:** Shows the source as 'NETLIST', type as 'VIO_OUTPUT', and width as '1'. The 'Display Name' is set to 'up'.
- Tcl Console:** Displays the output of the 'synth_1' command, showing synthesis progress and completion status.

The screenshot shows the Vivado 2019.1 interface. The left sidebar contains the Project Manager and Implementation sections. The main window is divided into several panes:

- Hardware Manager:** Displays a list of hardware components. The 'reset' signal is selected, and its properties are shown in the 'Debug Probe Properties' pane. The 'Display Name' is set to 'reset'.
- hw_vios:** A table showing the status of various signals. The 'reset' signal is highlighted in blue.
- Debug Probe Properties:** Shows the source as 'NETLIST', type as 'VIO_OUTPUT', and width as '1'. The 'Display Name' is set to 'reset'.
- Tcl Console:** Displays the output of the 'synth_1' command, showing synthesis progress and completion status.

- Video recording of the working demo of the homework:
<https://drive.google.com/file/d/1n901FppWEjhuTghJk0mdoFBsIHKjiL68/view?usp=sharing>

CODE

- vio_wrapper.v

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/03/2024 10:32:47 AM
// Design Name:
// Module Name: vio_wrapper
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////

module vio_wrapper (
    input Clk_100M
);

    wire [6:0] Count;
    wire reset;
    wire up;

    top_count t1(
        .Clk_100M(Clk_100M),
        .reset(reset),
        .up(up),
        .Count(Count)
    );

    vio_0 vio0 (
        .clk(Clk_100M),                // input wire clk
        .probe_in0(Count),             // input wire [7 : 0] probe_in0
        .probe_out0(reset),            // output wire [0 : 0] probe_out0
        .probe_out1(up)                // output wire [0 : 0] probe_out0
    );

endmodule
```

```
1 2 3 4 5 6 7 8 9 [2] nvim ARCHLINUX CPU 4.10% MEM 35.19% VOL 40% BAT 61% TIME 12:20 AM DATE Sep 06, Fri
2 `timescale 1ns / 1ps
3 //////////////////////////////////////
4 // Company:
5 // Engineer:
6 //
7 // Create Date: 09/03/2024 10:32:47 AM
8 // Design Name:
9 // Module Name: vio_wrapper
10 // Project Name:
11 // Target Devices:
12 // Tool Versions:
13 // Description:
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////
21
22
23 module vio_wrapper (
24     input CLK_100M
25 );
26
27 wire [6:0] Count;
28 wire reset;
29 wire up;
30
31 top_count t1(
32     .clk_100M(Clk_100M),
33     .reset(reset),
34     .up(up),
35     .Count(Count)
36 );
37
38 vio_0 vio0 (
39     .clk(Clk_100M),           // input wire clk
40     .probe_in0(Count),       // input wire [7 : 0] probe_in0
41     .probe_out0(reset),      // output wire [0 : 0] probe_out0
42     .probe_out1(up)          // output wire [0 : 0] probe_out0
43 );
44
45 endmodule
```

- top_count.v

```
`timescale 1ns / 1ps
////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/03/2024 09:51:20 AM
// Design Name:
// Module Name: top_count
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////

module top_count (
    input Clk_100M,
    input reset,
    input up,
    output [6:0] Count
);

wire Clk_8M, Clk_1Hz;

// CMT INSTANTIATION
clk_wiz_0 cmt (
```



```
// Engineer:
//
// Create Date: 09/05/2023 09:25:07 AM
// Design Name:
// Module Name: clk_div_rtl
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////

module clk_div_rtl (
    input Clk_8M,
    output Clk_1Hz
);

    reg [22:0] Count_reg = 0; // Initialization of FFs during FPGA configuration
    reg [22:0] Count_next; // output of combinational circuit...can not be initialized
    always @(posedge Clk_8M) begin
        Count_reg <= Count_next; // D-FF
    end

    always @(*) // Comb. ckt to find out next state
        Count_next = Count_reg + 1;

    assign Clk_1Hz = Count_reg[22];

endmodule
```

```
1 2 3 4 5 6 7 8 9 [2] nvim
1 `timescale 1ns / 1ps
2 //////////////////////////////////////
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 09/05/2023 09:25:07 AM
7 // Design Name:
8 // Module Name: clk_div_rtl
9 // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////
21
22
23 module clk_div_rtl (
24     input Clk_8M,
25     output Clk_1Hz
26 );
27
28     reg [22:0] Count_reg = 0; // Initialization of FFs during FPGA configuration
29     reg [22:0] Count_next; // output of combinational circuit...can not be initialized
30     always @(posedge Clk_8M) begin
31         Count_reg <= Count_next; // D-FF
32     end
33
34     always @(*) // Comb. ckt to find out next state
35         Count_next = Count_reg + 1;
36
37     assign Clk_1Hz = Count_reg[22];
38
39 endmodule
40
```

■ ARCHLINUX CPU 4.09% MEM 35.63% VOL 0% BAT 63% TIME 12:22 AM DATE Sep 06, Fri

■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb] (fix available) ■ Use 'always_comb' instead of 'always @*'. [Style: combinational-logic][always-comb] (fix available)

- updown_counter.v

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 09/05/2024 11:58:11 AM
// Design Name:
// Module Name: updown_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////

module updown_counter (
    input Clk_1Hz,
    input reset,
    input up,
    output [6:0] Count
);

    reg [6:0] PS = 0, NS = 0;

    always @(posedge Clk_1Hz) begin
        if (reset)
            PS ≤ 7'd0;
        else
            PS ≤ NS;
    end

    always @(*)
    begin
        if (up == 1'b1)
            if (PS == 7'd85)
                NS = 7'd0;
            else
                NS = PS + 7'd1;
        else if (up == 1'b0)
            if (PS == 7'd0)
                NS = 7'd85;
            else
                NS = PS - 7'd1;
    end

    assign Count = PS;

endmodule
```

```

1 2 3 4 5 6 7 8 9 [2] nvim
timescale 1ns / 1ps
// Company:
// Engineer:
//
// Create Date: 09/05/2024 11:58:11 AM
// Design Name:
// Module Name: updown_counter
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
23 module updown_counter (
    input Clk_1Hz,
    input reset,
    input up,
    output [6:0] Count
);
    reg [6:0] PS = 0, NS = 0;

    always @(posedge Clk_1Hz) begin
        if (reset)
            PS <= 7'd0;
        else
            PS <= NS;
        end

    always @(*)_    == Remove trailing spaces. [Style: trailing-spaces][no-trailing-spaces] (fix available)    == Remove trailing spaces. [Style: trailing-spaces][no-trailing-spaces] (fix available)
    begin
        if (up == 1'b1)
            if (PS == 7'd85)
                NS = 7'd0;
            else
                NS = PS + 7'd1;
        else if (up == 1'b0)
            if (PS == 7'd0)
                NS = 7'd85;
            else
                NS = PS - 7'd1;
        end

        assign Count = PS;
    endmodule

```