#Lecture

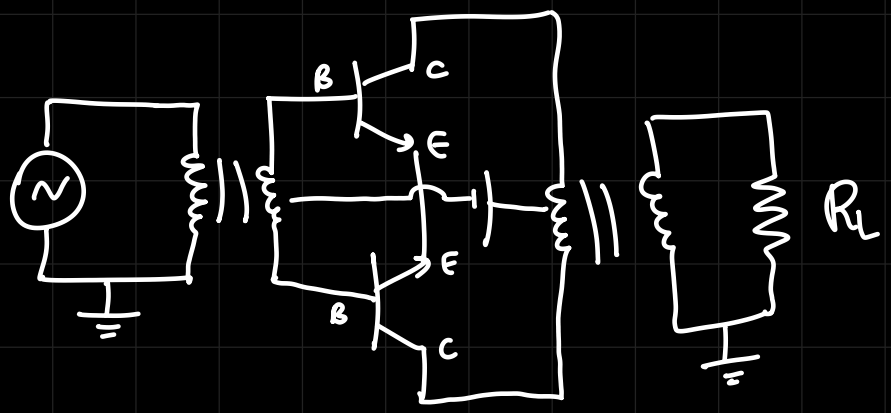
→ Class B Power amplifier

TRANSFORMER COUPLED PUSH PULL Amp

→ It consists of 2 identical transformers and 2 identical transistors Q_1 and Q_2

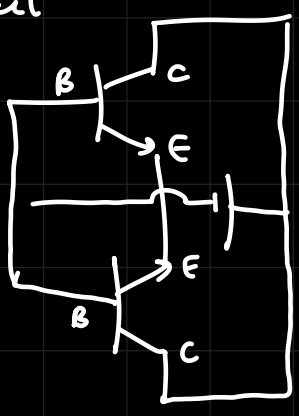
→ Q_1 → NPN , Q_2 → PNP

→ The secondary winding of the 1st transformer and the primary winding of the 2nd transformer is center tap.



DL → $X_L = 0$ for both short circuit

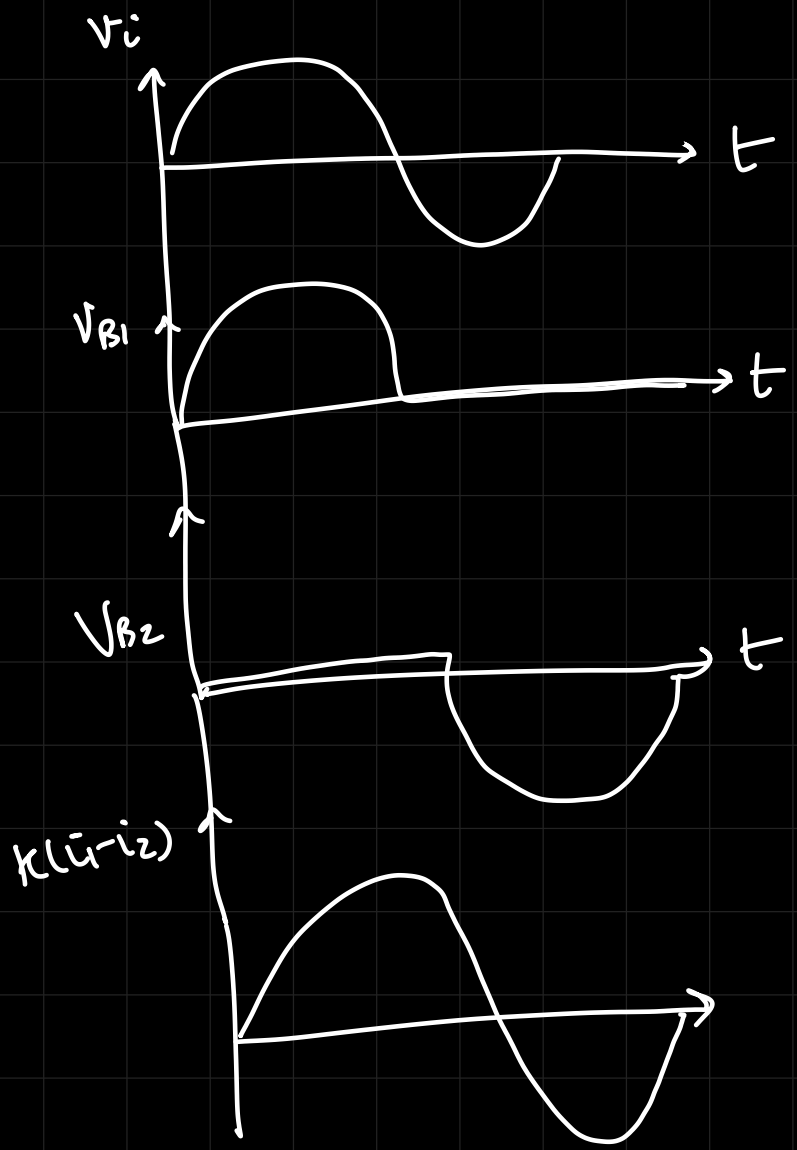
$$V_{BE_1} - V_{B2} = 0$$



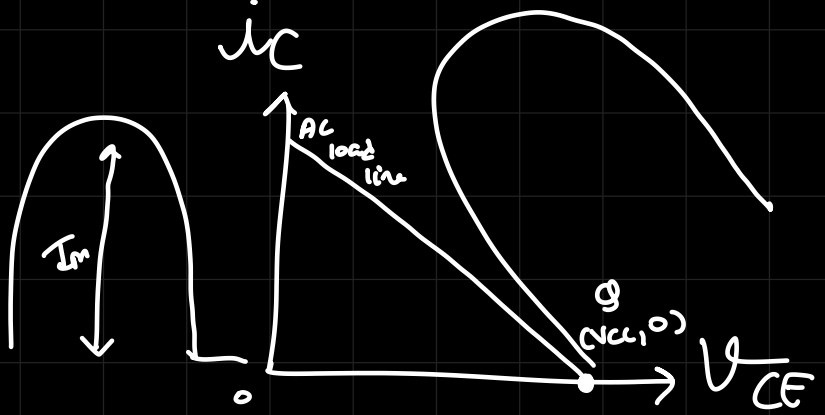
two transistors are used to obtain sinusoidal output. for each transistor, the base terminal are shorted & the emitter act DC as shown in the eqn. Therefore, both the transistors remain off / cutoff when no AC input.

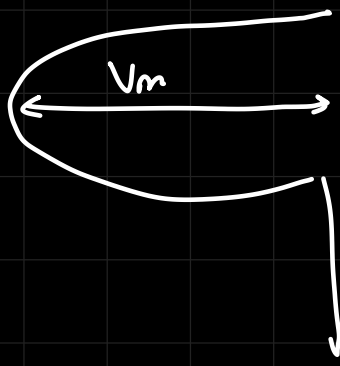
when AC input is applied at the Base 1, 2

$V_{in} \Rightarrow$



Note: DC and AC load line similar as class A transformer coupled amplifier but in class B amplifier operating point will be at extreme end point of the load line.





conduction angle → 180°

$$\eta\% = \frac{P_{ac}}{P_{dc}} \times 100\%$$

$$P_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_{cc} - 0}{\sqrt{2}} \times \frac{I_m - 0}{\sqrt{2}}$$

$$= \frac{V_{cc} \times I_m}{2}$$

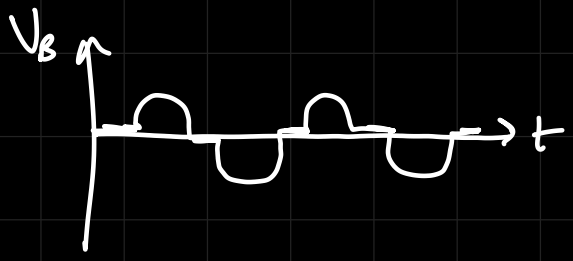
$$P_{dc} = V_{DC} I_{DC}$$

$$I_{avg} = I_{DC} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$$

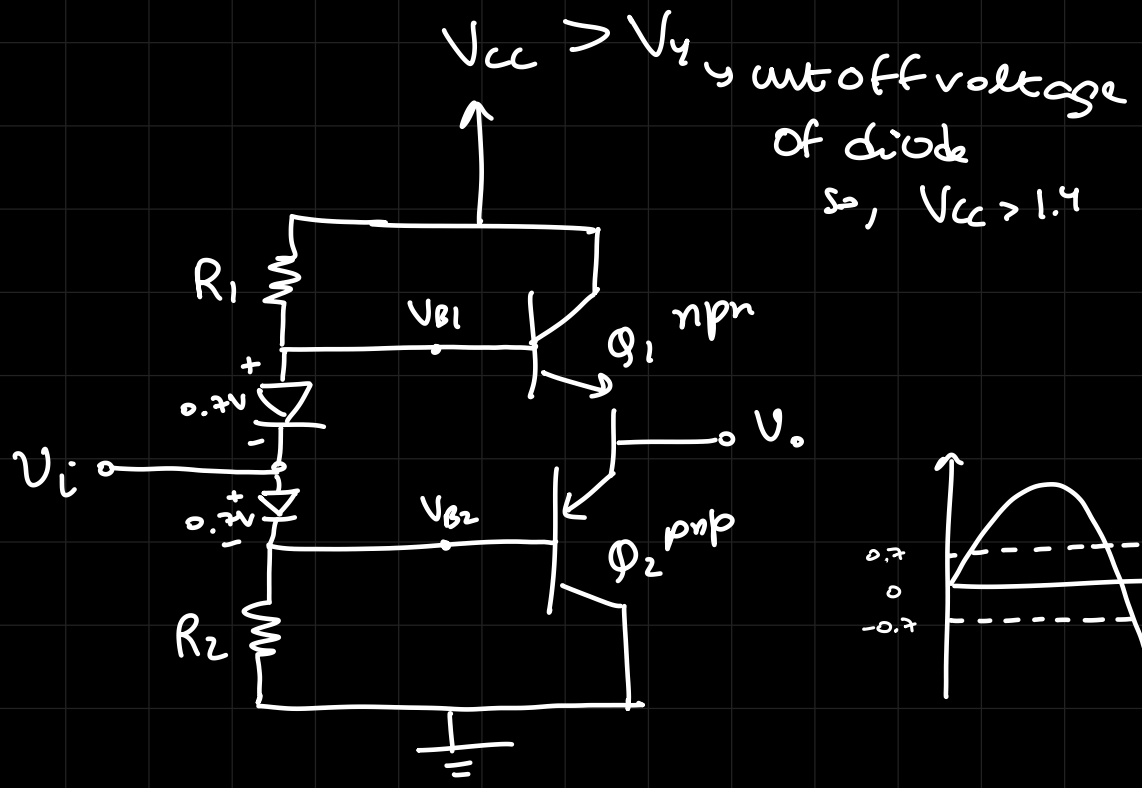
$$\eta\% = \frac{1}{2} \frac{V_{cc} \times I_m}{V_{cc} \times \frac{2I_m}{\pi}} = \frac{\pi}{4} \times 100 = 78.5\%$$

ideal case

DRAWBACK of class B Amplifier is
CROSS OVER DISTORTION
which is over come by class AB amplifier



CLASS AB amplifier

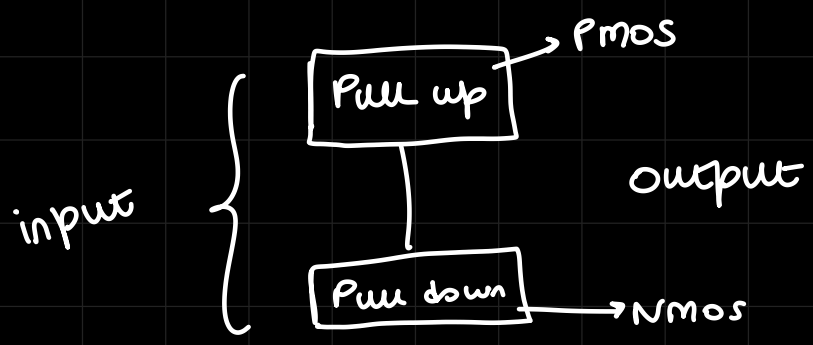


CLASS C Amplifier

Will be discussed in Friday's TUT

CMOSFET

complementary MOSFET

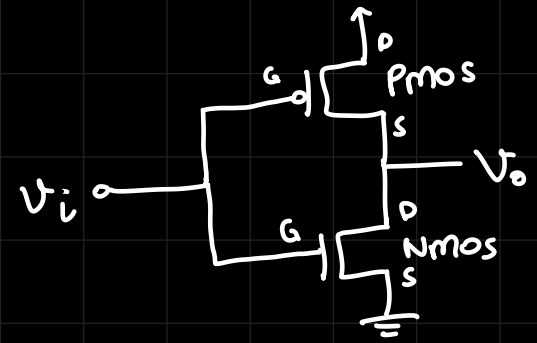


$$\lim_{x \to 8} \frac{1}{x-8} = \infty$$

$$\lim_{x \to 5} \frac{1}{x-5} = \sqcup\!\cap$$

from fig 12.14

With circle → PMOS
W/o circle → NMOS
} no need for arrow



INVERTER

≡ NOT Gate

Shunt operation

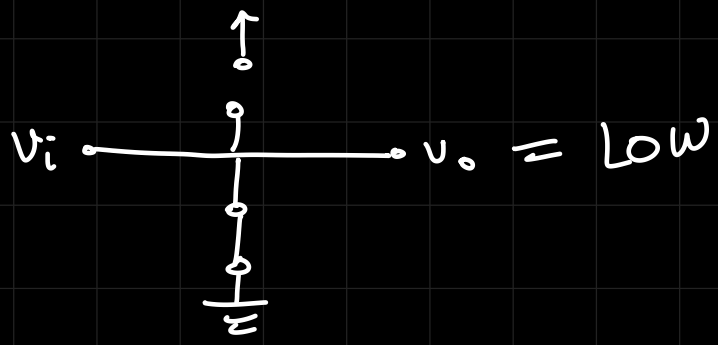
$V_i = V_{max}$

for P channel : PMOS → V_{GS} : negative $V_{GS} < -V_{th}$

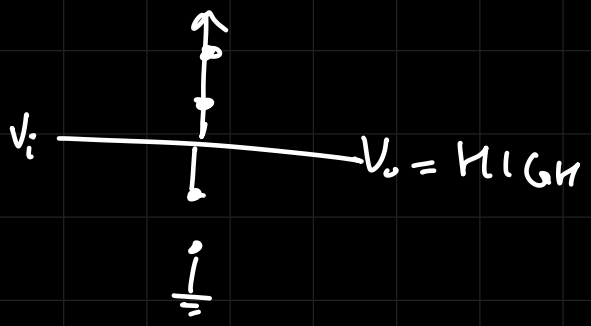
n channel : NMOS → V_{GS} : positive $V_{GS} > V_{th}$

for V_i = HIGH

M_1 → OFF, M_2 → ON



for V_i = LOW →

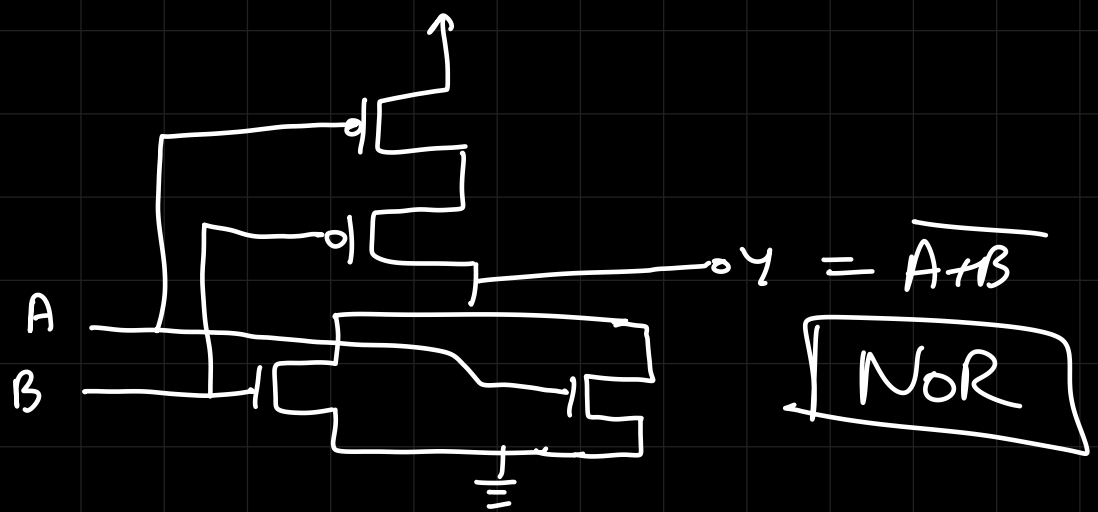


OR gate

parallel

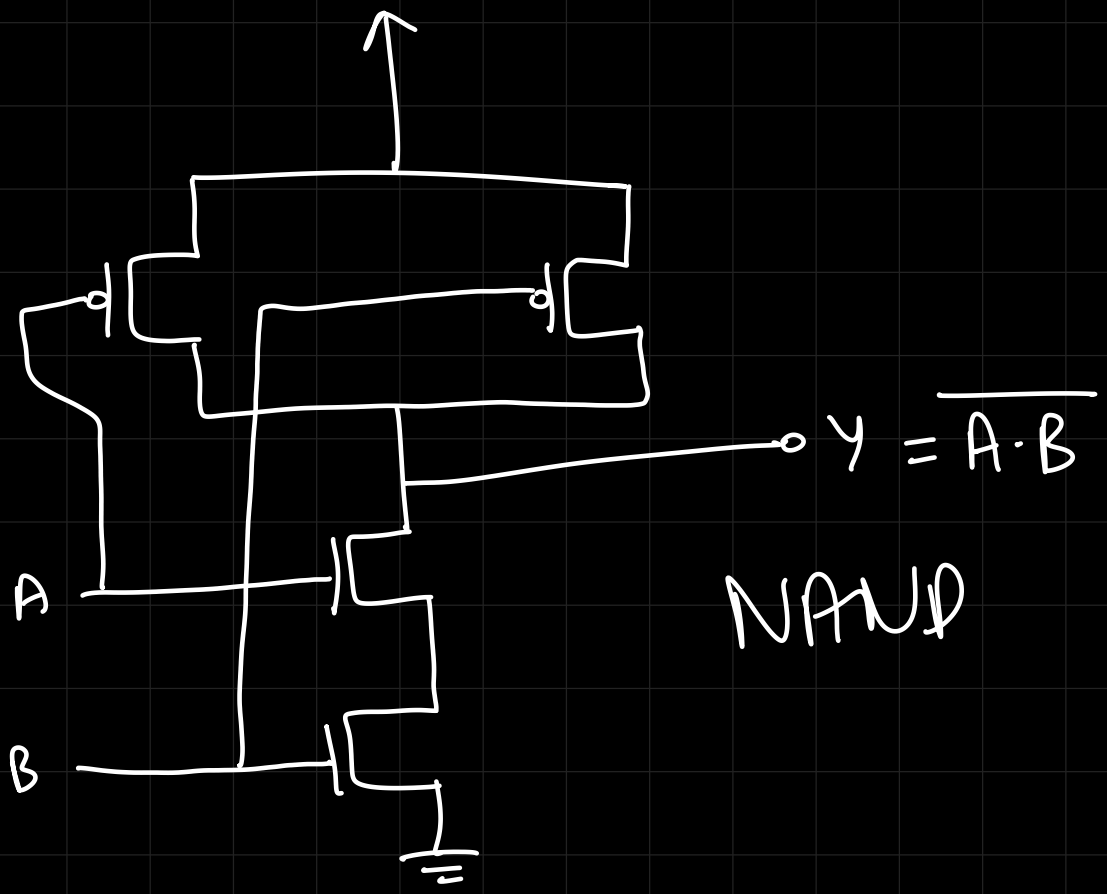
if pull down : parallel

↳ pull up : series



AND Gate

series



NAND