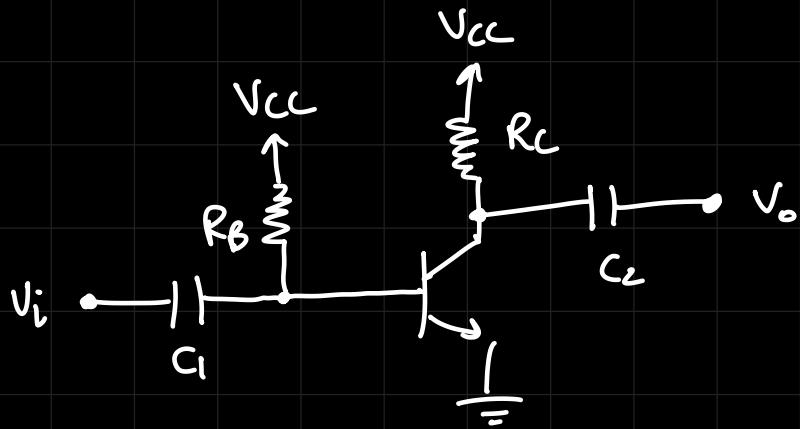


Fixed Bias



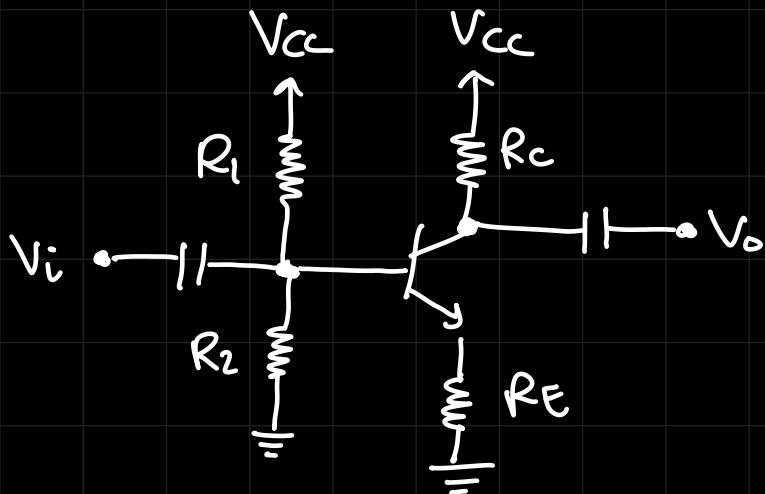
DC analysis for Q point

- ↳ Open Ckt all capacitors
- ↳ BE & CE loop
- ↳ common emitter config

Any variation in β will impact
in I_C and hence will shift the Q point.
Therefore this amplifier bias is not ideal

* For multiple devices where fixed bias Ckt
may be a subsystem (i.e. we may have
multiple values of β), we may set
different Q point which will result in
the transistor being in indeterminate mode.
We need standardized values.

Voltage Divider Bias



A dc bias voltage
can be created using R_1, R_2
 I_B can also be adjusted

Simplified using Thvenin's equivalent

$$-V_{Th} + I_B R_{Th} + V_{BE} + I_E R_E = 0$$

$$I_E = (\beta + 1) I_B$$

$$I_B (R_{Th} + R_E(\beta + 1)) = V_{Th} - V_{BE}$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + R_E(\beta + 1)}$$

$$I_C = \beta I_B = \frac{\beta(V_{Th} - V_{BE})}{R_{Th} + R_E(\beta + 1)}$$

due to variation in β , we have variation in I_C in the numerator but also a feedback pulling the value down in the denominator.

$$I_E = (\beta + 1) I_B = \frac{V_{Th} - V_{BE}}{R_E + R_{Th}} \quad \left. \begin{array}{l} \text{we want} \\ \textcircled{1} V_{Th} \gg V_{BE} \text{ to} \\ \text{not have any} \\ \text{small signal variation} \end{array} \right\}$$

CE loop, $-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$

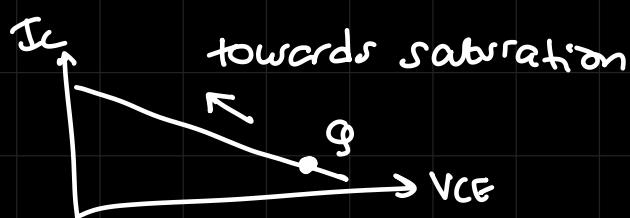
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

assuming $I_C \approx I_E$

Since I_C is stabilized, V_{CE} will be stabilized as well.

We also want \rightarrow $\textcircled{2} R_E \gg \underline{R_{Th}}$ to make β invariant

$$V_{Th} \uparrow \rightarrow I_E \uparrow \rightarrow I_C \uparrow \rightarrow V_{CE} \downarrow$$



but if $V_{Th} \downarrow$, $I_F \downarrow$, $I_C \downarrow$, $V_{CE} \uparrow$



∴ we need to maintain V_{Th} such that transistor remains in active mode

Rule of thumb →

$$V_{Th} = \frac{1}{3} V_{CC}$$

$$V_{CB} = \frac{1}{3} V_{CC} \quad (\text{or } V_{BE})$$

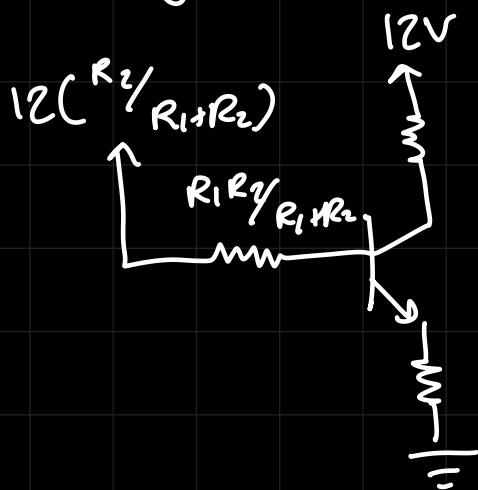
$$I_C R_L = \frac{1}{3} V_{CC}$$



$$I_1 / I_2 = (0.1 - 1) \times I_F$$

$$Q) \quad I_E = 1\text{mA} \quad V_{CC} = 12V$$

$$\beta = 100$$



$\frac{1}{3}V_{CC}$ for R_C ; $\frac{1}{3}V_{CC}$ for R_2 ; must $\leq \frac{1}{3}$ for possible negative signal swing

As per rule of thumb \rightarrow

$$V_B = \frac{1}{3}V_{CC} = 4V$$

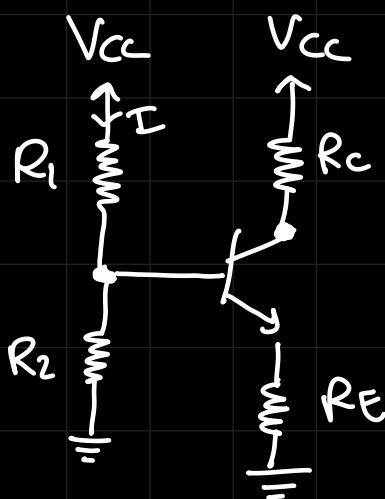
$$V_C = \frac{2}{3}V_{CC} = 8V$$

$$V_E = V_B - V_{BE} = 3.3V$$

$$R_E = \frac{V_E}{I_E} = 3.3K\Omega$$

assume, $I_B \approx 0 \rightarrow I = \frac{V_{CC}}{R_1+R_2} \rightarrow I$ can be $[I_E, 0.1I_E]$

$$\text{Case 1: } I = 0.1 \text{ mA} = 0.1 \text{ mA} = \frac{12}{R_1 + R_2} \rightarrow R_1 + R_2 = 12 \times 10^4 \quad (1)$$



$$V_B = \frac{V_{CC} \times R_1}{R_1 + R_2}$$

$$V_B = \frac{12 \times R_1}{(12 \times 10^4)}$$

$$4 \times 10^4 = R_1 \rightarrow R_1 = 40 \text{ k}\Omega$$

$$R_2 = 80 \text{ k}\Omega$$

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{\beta + 1}}, \quad R_B = \frac{320\text{k}}{12\text{k}} \Rightarrow \frac{80}{3} \text{ }\Omega$$

$$I_E = \frac{\frac{1 \times 40\text{k}}{10\text{k}} - 0.7}{R_E + \frac{320\text{k}}{12\text{k}}} = \frac{3.3}{R_E + \frac{80}{303}}$$

$$I_E = 0.92 \text{ mA} \approx 0.93 \text{ mA}$$

Now reduce R_E by $\frac{R_B}{10}$

$$R_E' = R_E - \frac{R_B}{10} = 3.3k - 0.267k = 3.031k\Omega$$

$$I_E' = \frac{9 - 0.7}{3.031k + \frac{80}{20^3}} \approx 1.0018 \text{ mA}$$

Case 2 : $I = I_E = 1 \text{ mA}$

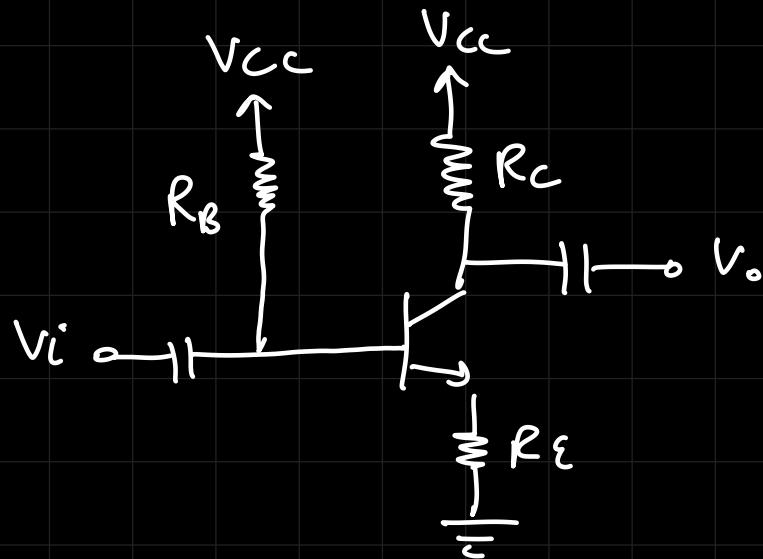
$$\frac{V_{CE}}{R_1 + R_2} = 1 \text{ mA}$$

$$R_1 + R_2 = 12k\Omega$$

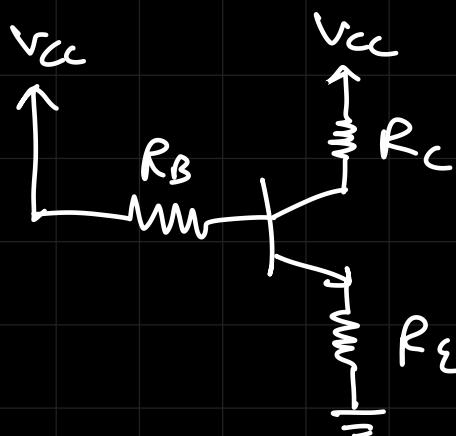
$$\left(\frac{R_2}{R_1 + R_2} \right) V_{CC} = 4V \Rightarrow R_2 = 4k\Omega$$
$$R_1 = 8k\Omega$$

$$I_E = \frac{3.3}{3.3 + \left(\frac{8}{3}\right)/10} = 0.992 \text{ mA} \approx 1 \text{ mA}$$

Emitter stabilized circuit



DC analysis



$$-V_{cc} + I_B R_B + V_{BE} + I_E R_E = 0$$

$$I_B = \frac{I_E}{(\beta+1)}$$

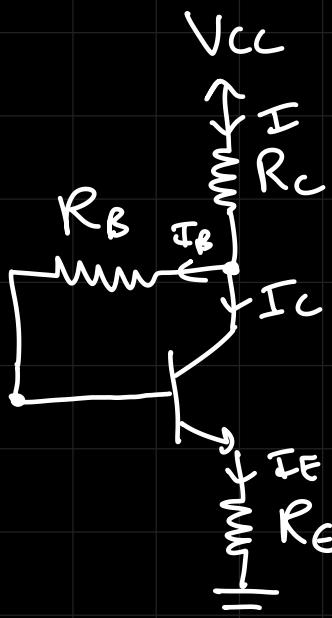
$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_E}$$

$$I_E = \frac{\beta (V_{cc} - V_{BE})}{R_B + (\beta+1) R_E}$$

Note: we have control/feedback unlike fixed bias

$$V_{CE} = V_{cc} - I_E R_C - I_F R_E$$

DC bias with voltage feedback



$$-V_{CC} + IR_C + I_B R_B + V_{BE} + I_E R_E = 0$$

Assuming $I_B \ll I_C$

$$-V_{CC} + I_C R_C + I_B R_B + V_{BE} + I_E R_E = 0$$

$$-V_{CC} + I_B (\beta R_C + R_B + (\beta + 1) R_E) + V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{\beta R_C + R_B + (\beta + 1) R_E}$$

Assuming $I_C \approx I_E$

$$\text{So, } I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta (R_C + R_E)}$$

$$I_C = \beta I_B = \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_C + R_E}$$

much better &

robust as compared to emitter stabilized bias
| What is the tradeoff? |

CE: V out \Rightarrow out of phase by 180°

CR: V amp - in phase

CC; buffers cmp

Input resistance of CE amplifier
is very high $\rightarrow R_{in} \uparrow$

$$R_{in} = R_{in} = \frac{\beta}{g_m} \rightarrow g_m \downarrow$$

$$A_v = \frac{V_o}{V_i} = -g_m(R_c \parallel R_L) \left(\frac{R_{in}}{R_{in} + R_{sig}} \right)$$

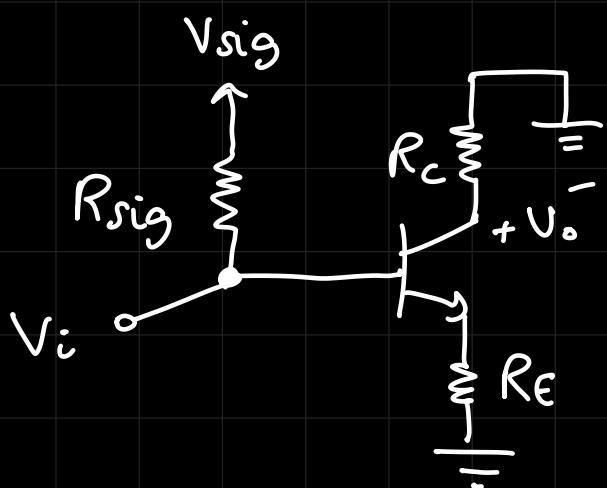
$$G_v = \frac{V_o}{V_{sig}}$$

\downarrow

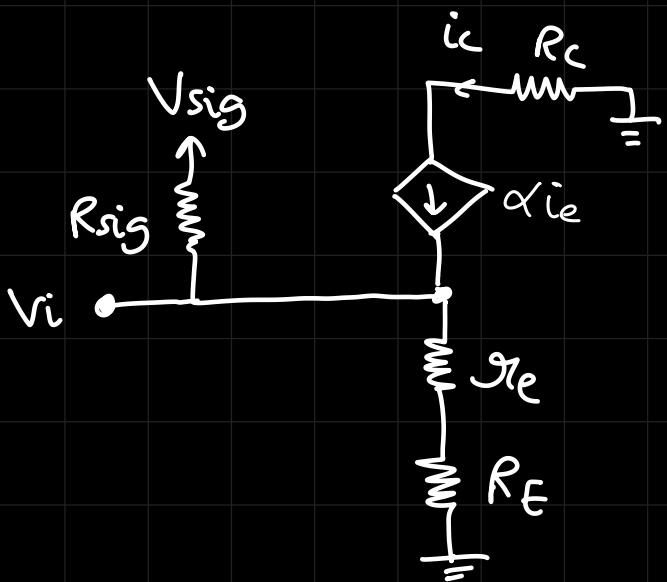
$g_m \downarrow \rightarrow A_v \downarrow$

Emitter follower circuit (modified CE)

\rightarrow helps to achieve high



T model of this circuit → (AC equivalent)



$$R_{in} = \frac{V_i}{i_b} \rightarrow V_i = i_e(r_e + R_E)$$

$$i_e = (\beta + 1) i_b$$

$$R_{in} = (\beta + 1)(r_e + R_E)$$

$$R_{in} (\text{in CE w/o } R_E) = r_\pi = (\beta + 1) r_e$$

$$\frac{R_{in} (\text{CE with } R_E)}{R_{in} (\text{CE w/o } R_E)} = \frac{r_e + R_E}{r_e} = 1 + \frac{R_E}{r_e}$$

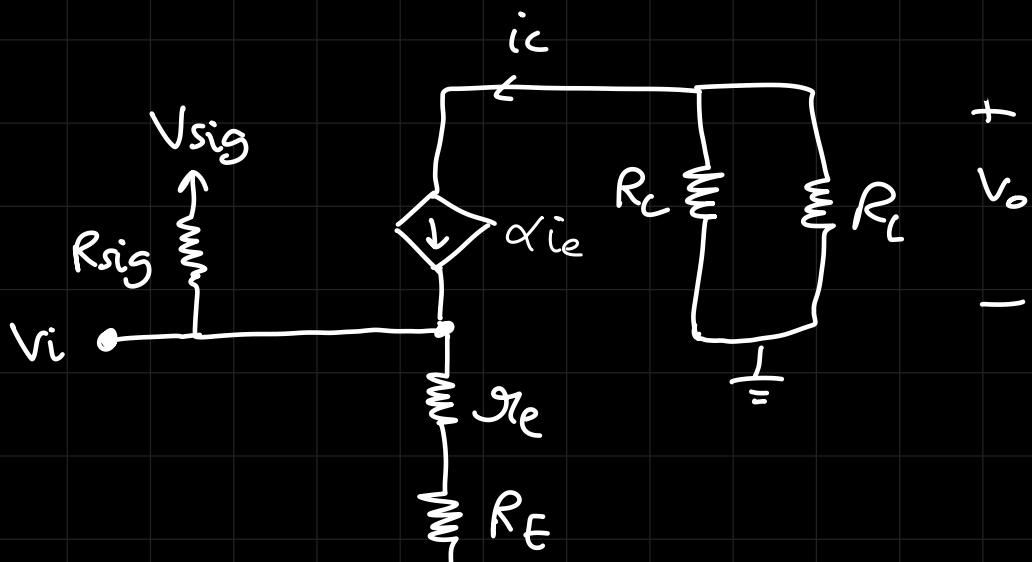
$$V_o = -i_c R_C = -\alpha i_e R_C$$

$$V_i = i_e (r_e + R_e)$$

$$A_{V_o} = \frac{V_o}{V_i} = \frac{-\alpha R_C}{r_e + R_e}$$

Open Circuit Voltage Gain

now with $R_L = ?$



$$A_V = \frac{V_o}{V_i}$$

$$V_o = -i_c (R_C \parallel R_L) = -\alpha i_e (R_C \parallel R_L)$$

$$V_i = i_e (r_e + R_e)$$

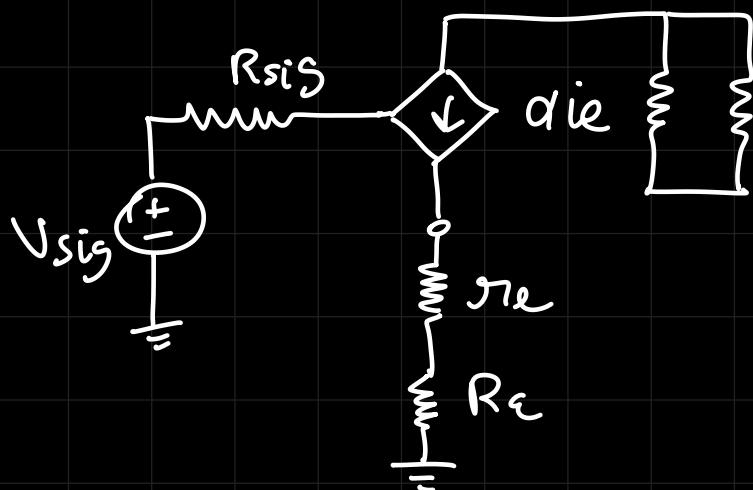
$$A_V = \frac{-\alpha (R_C \parallel R_L)}{r_e + R_e}$$

$$\text{in the OC gain } \rightarrow A_{v_o} = -\frac{\alpha R_C}{g_{re} + R_E}$$

$$= -\frac{\alpha}{g_{re}} \left(\frac{R_C}{1 + \frac{R_E}{g_{re}}} \right) = -\frac{\alpha g_m R_C}{1 + g_m R_E}$$

Input impedance depends on your input signal swing

Condition: $R_{in} \gg R_{sig}$



$$G_V = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}}$$

$$G_V = \frac{-\alpha_{die} (R_C || R_L)}{i_e (g_{re} + R_E)} \times \frac{V_i}{V_{sig}} = \frac{-\alpha (R_C || R_L)}{g_{re} + R_E + R_{sig}}$$

$$V_i = V_{sig} \times \frac{g_{re} + R_E}{g_{re} + R_E + R_{sig}}$$

$$\text{Other way} \rightarrow V_{sig} = V_i + i_B R_{sig}$$

$$V_{sig} = i_e (R_e + g_e) + i_B R_{sig}$$

$$= i_B ((\beta + 1) (R_e + g_e) + R_{sig})$$

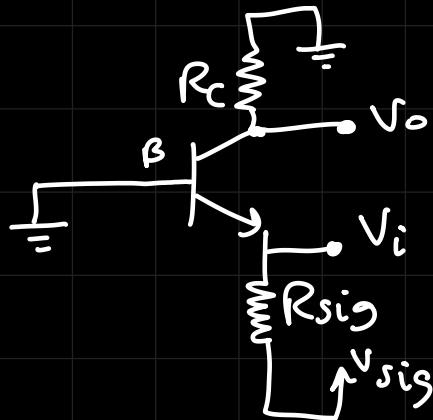
$$\frac{V_i}{V_{sig}} = \frac{(\beta + 1) (R_e + g_e)}{(\beta + 1) (R_e + g_e) + R_{sig}}$$

- ① R_{in} is much higher than standard CE
- ② A_v reduces
- ③ G_v is more tolerant to β variations

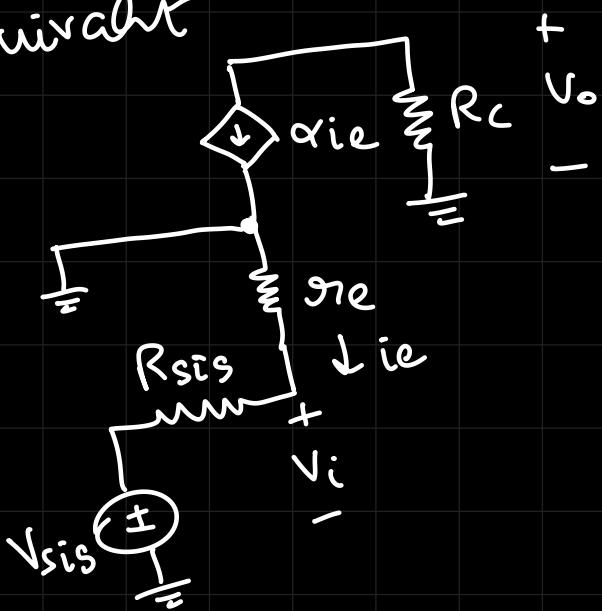
> Note: CE amp : phase out of 180° w.r.t V_o

CB amp : some phase
i.e. gain true

Common Base Configuration



AC equivalent



$$\alpha \approx 1 \rightarrow R_{in} = g_m = \frac{1}{g_m}$$

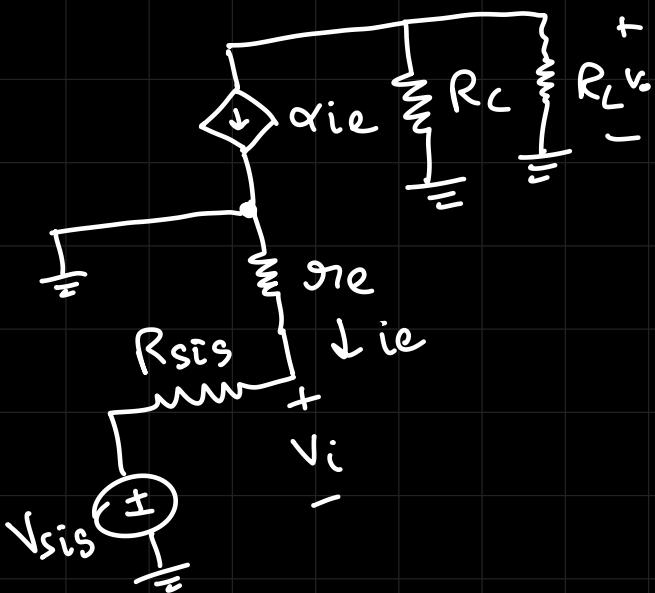
$$A_{vo} = \frac{v_o}{v_i} = -\frac{\alpha i_e (R_c)}{-i_e g_m} = \frac{\alpha R_c}{g_m} = \underline{\underline{g_m R_c}}$$

Some phase gain

but Load R

$$A_V = \frac{-\alpha_{ie} (R_C || R_L)}{-i_e g_{re}}$$

$$= g_m (R_C || R_L)$$



$$G_V = \frac{V_o}{V_{sig}} = \frac{-\alpha_{ie} (R_C || R_L)}{V_{sig}}$$

$$V_o^- = V_{sig} \times \frac{g_{re}}{g_{re} + R_{sig}}$$

$$G_V = \frac{\alpha (R_C || R_L)}{g_{re} + R_{sig}} \quad \checkmark$$

TRADEOFF:

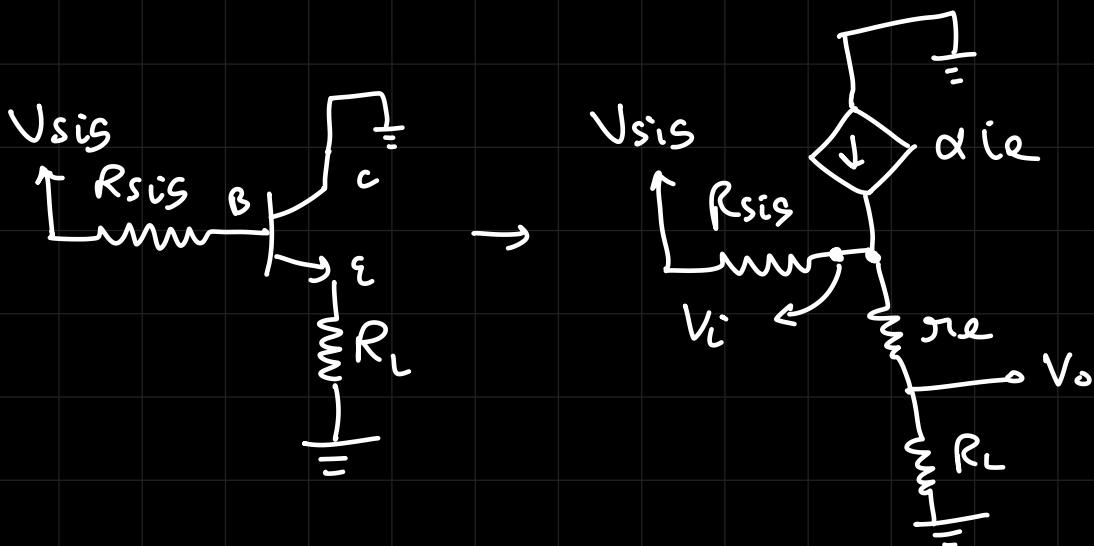
$+v_L \rightarrow$ output follows input phase

$-v_L \rightarrow R_{in}$ smaller than CE amp

because $R_{in} = g_{re}$ here but $R_{in} = g_{mT}$
these and $g_{re} \ll g_{mT}$

Common collector config

buffer amp \rightarrow

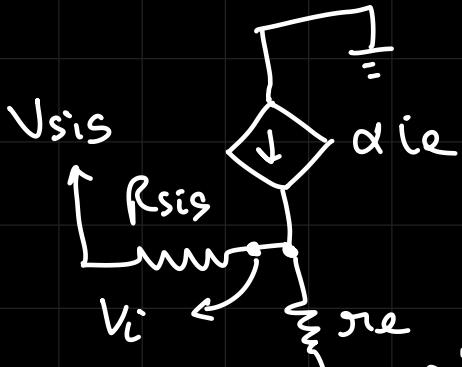


$$R_{in} = \frac{V_i}{i_B} = \frac{V_i(\beta+1)}{i_e} = (g_{re} + R_L)(\beta+1)$$

$$A_v = \frac{V_o}{V_i} = \frac{i_e R_L}{i_e (g_{re} + R_L)} = \frac{R_L}{g_{re} + R_L}$$

$$A_{v_o} = \frac{V_o}{V_i} \rightarrow \text{remove } R_L$$

$$= \frac{i_e r_e}{i_e r_e} = \boxed{1}$$



or mathematically $\rightarrow R_L = \infty$

$$A_{v_o} = \frac{1}{1 + g_{re}/R_L} \underset{\approx}{=} \frac{1}{2}$$

$$G_V = \frac{V_o}{V_{sig}} = \frac{V_o}{V_i} \times \frac{V_i}{V_{sig}} = \frac{R_L}{r_e + R_L} \times \frac{i_e(r_e + R_L)}{V_{sig}}$$

$$V_i = V_{sig} \times \frac{(r_e + R_L)(\beta + 1)}{(\beta + 1)(r_e + R_L) + R_{sig}}$$

$$V_{sig} = \frac{i_e(r_e + R_L)}{r_e + R_L + R_{sig}} \times \frac{r_e + R_L + R_{sig}}{r_e + R_L}$$

$$G_V = \frac{(\beta + 1) R_L}{(\beta + 1)(R_L + r_e) + R_{sig}} \simeq \text{comes down to almost unity } (\sim 0.9 - 1)$$

$(\beta + 1) R_L$ is the main scaling factor and if $(\beta + 1) R_L$ becomes much much greater than $R_{sig} \rightarrow G_V \simeq 1$

Used when source resistance is very high

MOSFET

Lec-12 18/03/25



metal oxide semiconductor field effect transistor

4 terminal

↳ Gate

→ Drain

→ Source

→ Body

NMOS MOSFET

↳ S and D

are heavily doped

n type

↳ p type substrate
(body)

NFET → NMOS

PFET → PMOS

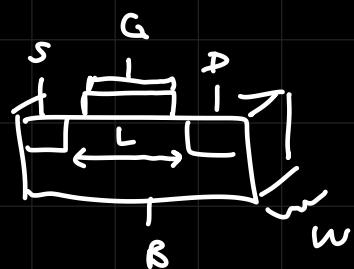
Gate: metal / p-crystalline

2 regions: p type substrate and S, D n⁺ type doped

SiO₂: gate oxide

Channel length: L

Width: W

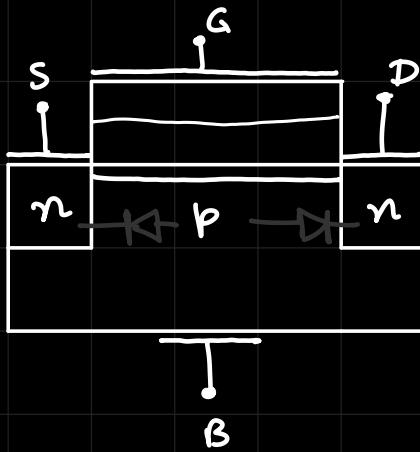


L : 0.1 - 3 mm

| 8 nm

W : 0.2 - 100 mm

0.2 - 100 nm



at equilibrium, no current flows between S and D

for inducing a channel btw S and D

a positive voltage is applied at Gate terminal : V_{GS}

but still no current flows unless there is a potential difference between S and D

Inversion Layer

for NMOS \rightarrow free e^- due to p type substrate

$V_{GS} > V_T$: threshold voltage for current flow btw S and D

$V_{GS} \uparrow \rightarrow$ inversion layer width \uparrow

$$\text{overdrive voltage} : V_o = V_{GS} - V_T$$

enhancement type mosfet

① Cutoff mode :

$$0 < V_{GS} < V_T$$

$$\approx 0.2 - 0.5V$$

$$\text{assumption: } V_{SB} = 0$$

② $0 < V_{GS}, \quad V_{GS} > V_T, \quad V_{DS} = 0$

enhancement type mosfet

no current flow

channel created

③ $0 < V_{GS}, \quad V_{GS} > V_T, \quad 0 < V_{DS} < (V_{GS} - V_T)$

I_D current from $D \rightarrow S$ flows

\leftarrow proportional to V_{DS}

$$I_D \propto V_{DS}$$

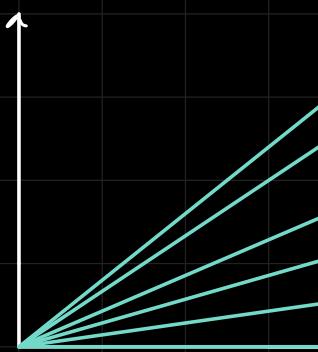
drain current

Voltage controlled resistance

triode mode / linear mode

because of SiO_2 gate oxide $\rightarrow I_G = 0$

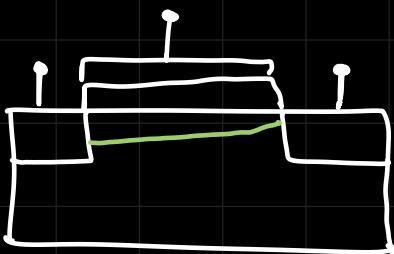
$$R_D = \frac{V_{DS}}{I_D}$$



Characteristic

for small $V_{DS} \rightarrow V_{DS} < V_{GS} - V_T$
triode mode / linear mode
 $I_D = 0$

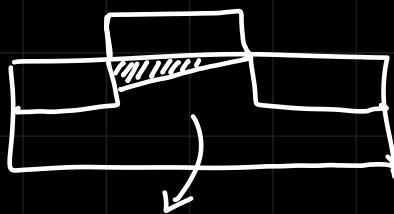
but for $V_{DS} > V_{GS} - V_T$
the Gate will attract free e^-
alongside Drain
 $I_D \neq 0$



The channel/
inversion layer's
width tapers

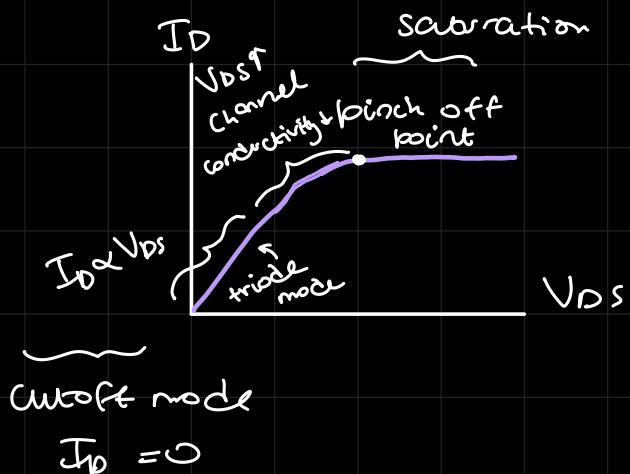
At very high V_{DS} ,
 I_D becomes constant

pinch off point situation



pinch off region

no more increase in I_D with V_{DS}



$$V_{GS} - V_T < 0$$

$V_C(x)$: Channel voltage wrt source
at position x

effective voltage inducing the channel
at $x \rightarrow V_{GS} - V_T - V_C(x)$
 $\underbrace{V_0}_{}$

net charge within narrow dx strip:

$$Q = CV \quad \text{fm}^{-2}$$
$$dq = -C_{ox}(Wdx) (\underbrace{V_{GS} - V_T - V_c(x)}_{\substack{\text{Fara} \\ \text{net potential}}})$$

\downarrow

e⁻ charge
(NMOS)

net capacitance

\bar{E} by V_{DS} is in $-x$ direction

$$\bar{E}(x) = -\frac{dV_c(x)}{dx}$$

net mobility constant : μ_n
of charge carriers

$$\text{Velocity } \left(\frac{dx}{dt} \right) = \mu_n E(x)$$

$$-\frac{dq}{dt} = \left(\frac{dq}{dx} \right) \times \left(\frac{dx}{dt} \right)$$

$$I_D(x) = W C_{ox} [V_{GS} - V_T - V_c(x)] \mu_n \frac{dV}{dx}$$

at a point x

for the entire channel \rightarrow integrate from $0 \rightarrow L$

$$\int_0^L I_d dx = \int_{V=0}^{V=V_{DS}} W C_{ox} [V_{GS} - V_T - V_C(x)] \mu_n \frac{dV_C(x)}{dx} dx$$

$$I_D \cdot L = \mu_n \cdot C_{ox} \cdot W \left([V_{GS} - V_T] V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

→ At pinch off $\rightarrow V_{DS} = V_{GS} - V_T$

$$I_{D_{max}} = \frac{1}{2} \mu_n \cdot C_{ox} \cdot \frac{W}{L} [V_{GS} - V_T]^2$$

→ for triode mode: $V_{DS} \lll$

$$\text{So, } I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} [(V_{GS} - V_T) V_{DS}]$$

$I_D \propto V_{DS}$ V_{DS}^2 term goes away

Ref → Sedra Smith 5th edition
not 7th edition

for small V_{DS} , we see a linear
relation btw I_D and V_{DS}

Saturation mode: $V_{DS} \geq V_{GS} - V_T$
 $V_{GS} \geq V_T$

MOSFET \equiv Voltage controlled
current source

AND
Voltage controlled
resistance

Lecture → Tut



DC $\rightarrow \omega = 0$

$$X_C = \frac{1}{\omega C} = \infty \text{ OC}$$

AC $\rightarrow \omega \ggg$

$$X_C = \frac{1}{\omega C} = 0 \text{ SC}$$

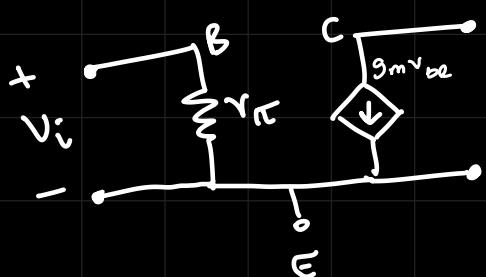
All the params bias Base, Collector and emitter current by using DC analysis

Also, the Y point of the transistor calculated by DC Analysis

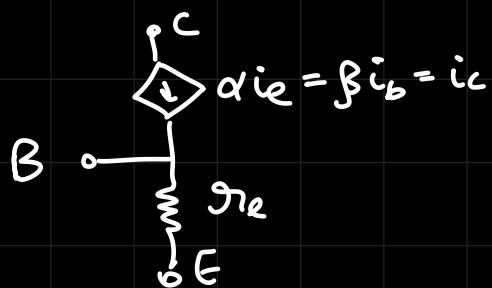
The input impedance, output impedance and the gain of the BJT calculated by AC analysis

We have 2imp methods to solve the BJT under AC analysis

(a) Π model



(b) T model



if early effect voltage gives
then consider g_o

in π model

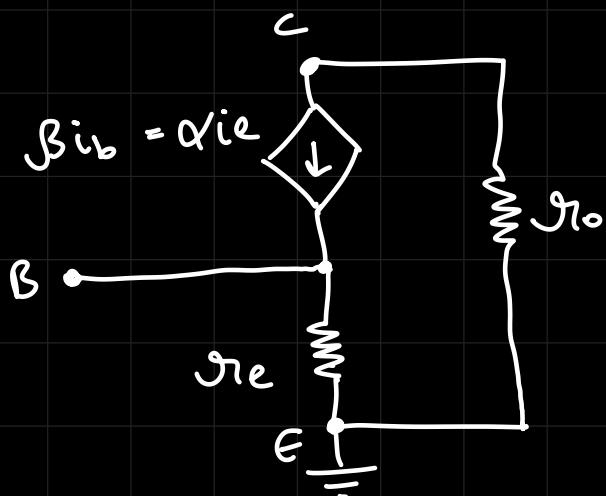
$$g_{\pi} = (\beta + 1) g_e$$

$$g_{\pi} \approx \beta g_e$$

$$g_e = \frac{V_T}{I_E}$$

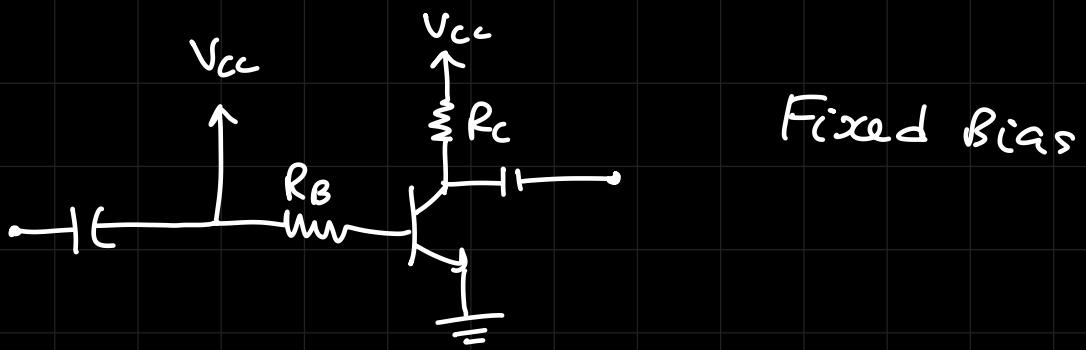
↑ Thermal voltage

$$V_T = 25/26 \text{ mV}$$



(g) for a given BJT configuration, determine the Z_{in} , Z_{out} , A_v

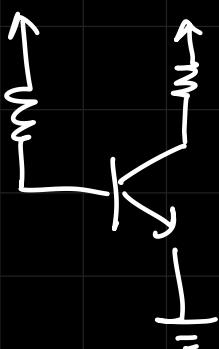
Note: we only use π model if there is a capacitor



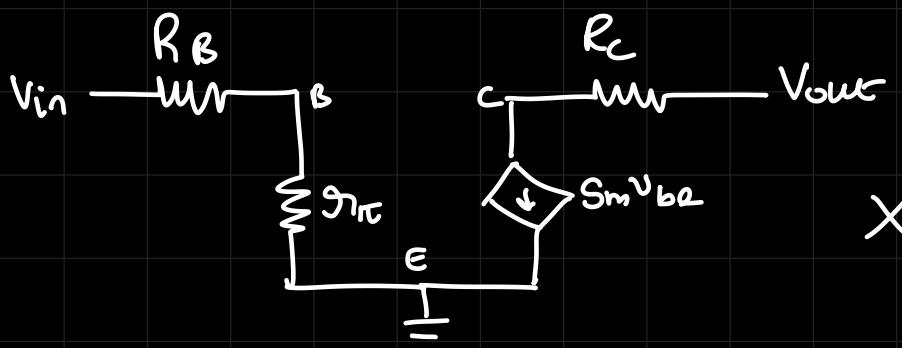
DC analysis

$I_C = \beta I_B + (\beta + 1) I_{CBO}$

↓
leakage current



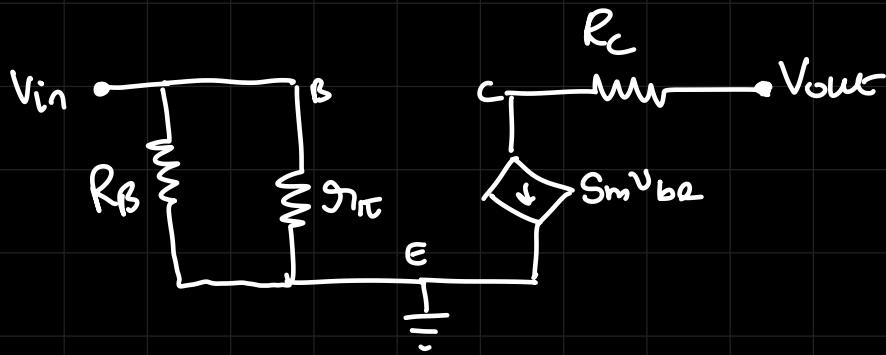
no R_C so, we use π model



$$V_{out} = -g_m v_{be} R_c$$

$$v_{be} = \frac{g_m v_{in}}{g_m + R_b} v_{in}$$

$$\frac{V_{out}}{V_{in}} = -\frac{I_C}{Y_T} \times \frac{Y_T / I_B}{Y_T / I_B + R_B}$$



$$V_{out} = -S_m V_{be} \cdot R_C$$

$$V_{BEI} = \left(\frac{g_{m\pi}}{g_{m\pi} + R_B} \right) V_{in}$$

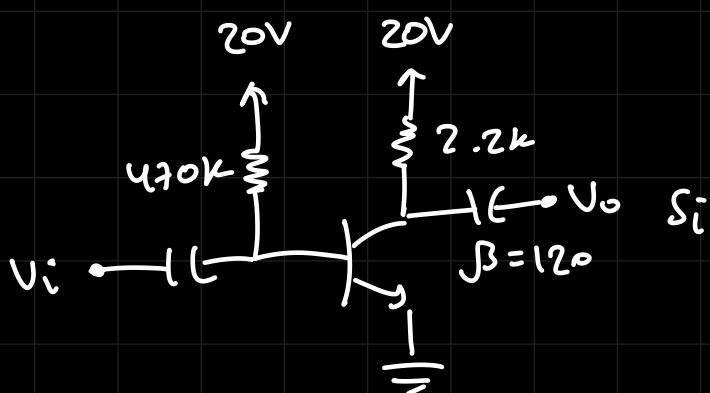
$$\frac{V_{out}}{V_{in}} = -S_m R_C \left(\frac{g_{m\pi}}{g_{m\pi} + R_B} \right)$$

$$Z_{in} = g_{m\pi} \parallel R_B$$

$$Z_{out} = R_C$$

if r_o given $\rightarrow Z_{out} = R_C \parallel r_o$

Q) calculate Z_{in} , Z_{out} , A_v , Q point



$$-20 + 470k(I_B) + 0.7 = 0$$

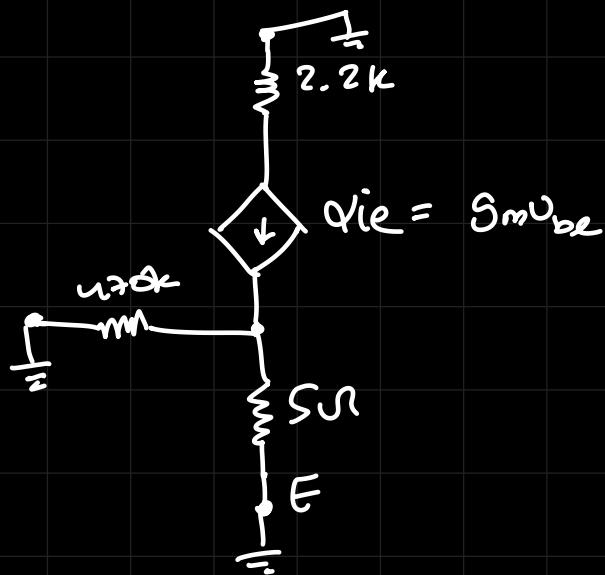
$$I_B = 19.3 / 470k = 41 \mu A$$

$$I_C = 4.92 \text{ mA} , I_E = 4.96 \text{ mA}$$

$$-20 + 2.2(4.92) + V_{CE} = 0$$

$$V_{CE} = 20 - 10.824 = 9.176 \text{ V}$$

$$r_L = \frac{V_T}{I_C} - \frac{25 \text{ m}}{4.96 \text{ mA}} = \sim 5 \text{ k}\Omega$$



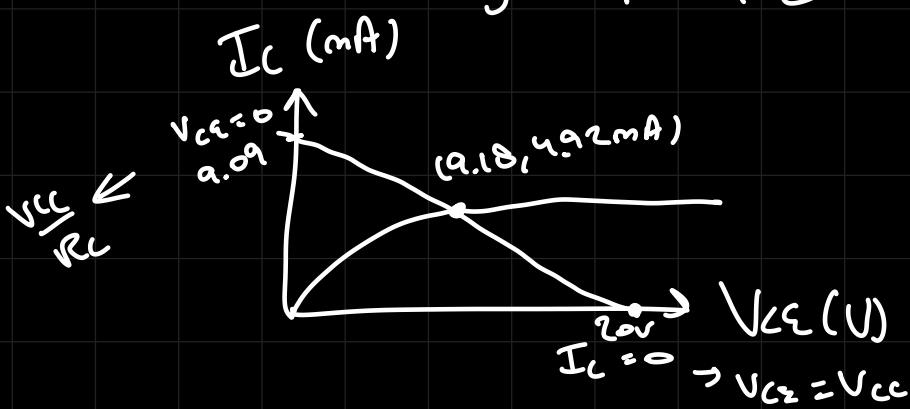
X

$\emptyset (9.18 \text{ V}, 4.92 \text{ mA})$

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{1}{R_C} V_{CC}$$

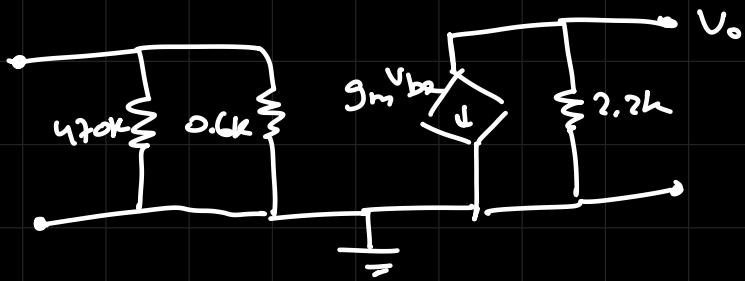
$$y = mx + c$$



AC analysis → DC remove

C → SC

π model



$$\gamma_{\pi} = \frac{V_T}{I_B} = \frac{2S}{4I_1} K = 0.6K$$

$$V_o = - \frac{2.2K}{s} V_{be}$$

$$V_{be} = V_{in} \left(\frac{470K}{470K + 0.6K} \right)$$

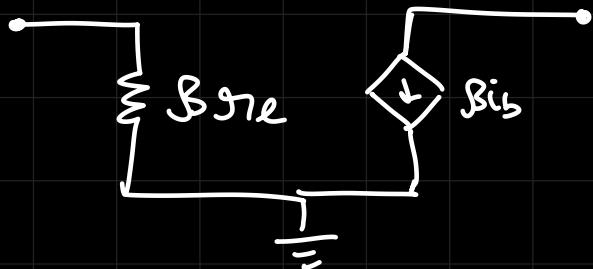
$$\frac{V_o}{V_{in}} =$$

$$V_o = - \beta i_b R_C$$

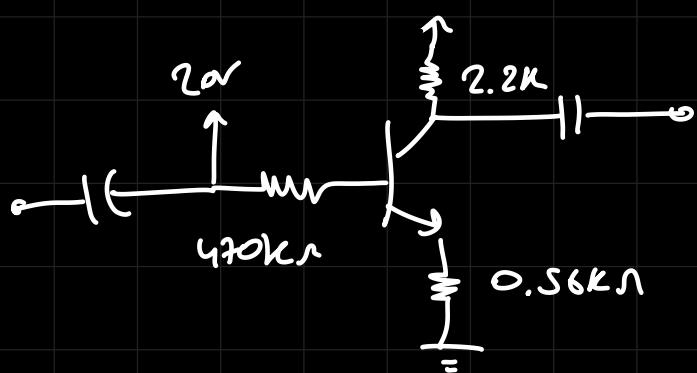
$$i_b = \frac{V_i}{\beta r_e}$$

$$\Delta V = - \frac{\beta}{\beta r_e} R_C = - \frac{R_C}{r_e} = - 470 V_N$$

repeat all the param in the above numerical considering $\beta_0 = 50 \text{ K}\Omega$
 (early effect impedance)



g) find Z_{in}, Z_{out}, A_v



$$-20 + 470k(I_B) + 0.7 + 560I_E = 0$$

If Re exists $\rightarrow T$ model
 else π model

$$-20 + 470k(I_B) + 0.7 + 560I_E = 0$$

$$I_B(470k + 67.76\Omega) = 19.3$$

$$I_B = 35.8 \mu A$$

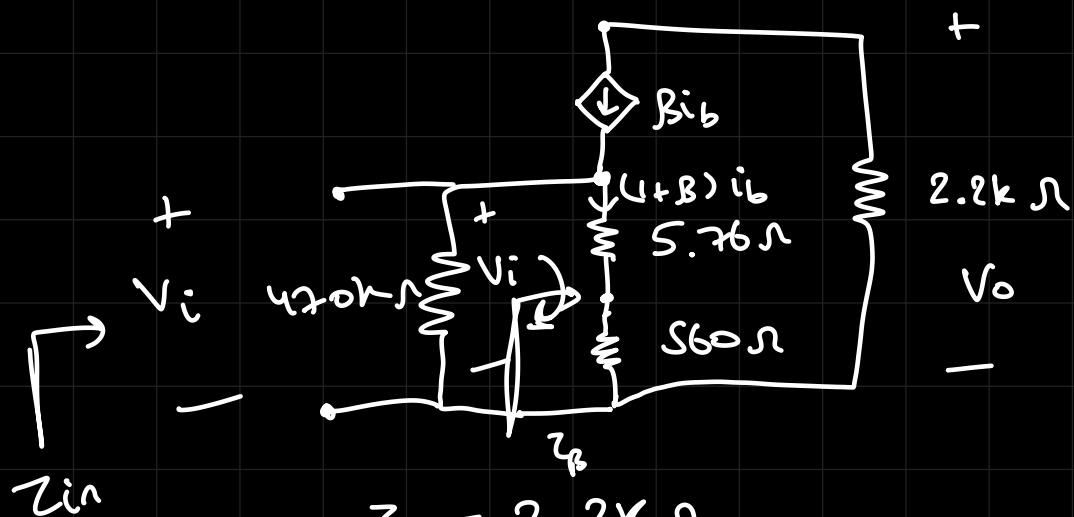
$$I_E = 4.34 mA$$

$$I_C = 4.296 mA$$

$$-20 + 9.45 + V_{CE} + 2.43 = 0$$

$$V_{CE} = 8.12 V$$

$$r_e = \frac{V_T}{I_E} = \frac{25}{4.34} = 5.76 \Omega$$



$$Z_o = 2.2 k\Omega$$

$$Z_{in} = 470k \parallel 565.76 \Omega$$

$$= \frac{470 \times 565}{470 + 565} = 564.32 \Omega$$

$$kVL \rightarrow -V_i + (1+\beta) i_b (R_e + r_e) = 0$$

$$\Rightarrow V_i = (1+\beta) i_b (R_e + r_e)$$

$$Z_b = \frac{V_i}{i_b} = (1+\beta) (R_e + r_e)$$

$$= (12)(565.76) = 68.45 k\Omega$$

$$Z_{in} = R_B \parallel Z_B = 59.7 k\Omega$$

$$V_i = (1+\beta) i_b (R_e + r_e)$$

$$V_o = -i_c R_c$$

$$= -\beta i_b R_c$$

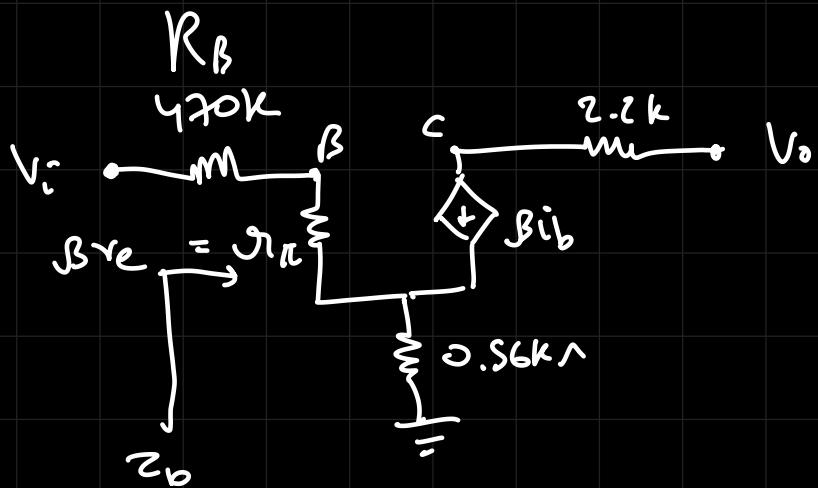
$$= -\beta R_c \left(\frac{V_i}{(1+\beta)(R_e + r_e)} \right)$$

Assume $\beta \approx \beta_{rl}$

$$Av = \frac{-R_c}{R_e + r_e} = \frac{-2.2k}{565.76} = -3.8 v_{in}$$

(g) now do with π model

$$r_{\pi} = \frac{V_T}{I_B} = \frac{25}{35.8 \mu} = 700 \Omega$$



$$V_o = -\beta i_b \cdot R_C$$

$$\times \left\{ i_b = \frac{V_i}{\beta r_e + 0.56k} \right\} \quad V_i = i_b \beta r_e + (1+\beta) R_E i_b$$

$$\left. \begin{aligned} \frac{V_o}{V_i} &= -\frac{\beta R_C}{\beta r_e + 0.56k} \\ &= \frac{-2.2k(120)}{5.76(120) + 560} \\ &= -\frac{264}{1.25} = -211.2 \end{aligned} \right\}$$

$$V_i = i_b (r_e + R_E) \beta \Rightarrow \beta \approx 1 + \beta$$

$$\frac{V_o}{V_i} = \frac{-R_C}{r_e + R_E} = -3.8 \text{ V/V} \quad \text{Same ✓}$$

$$Z_b = \frac{V_i}{i_b} = (r_s + R_E) \beta$$
$$= 6787 \text{ k}\Omega$$

$$Z_{in} = R_B || Z_b = 59.32 \text{ k}\Omega$$

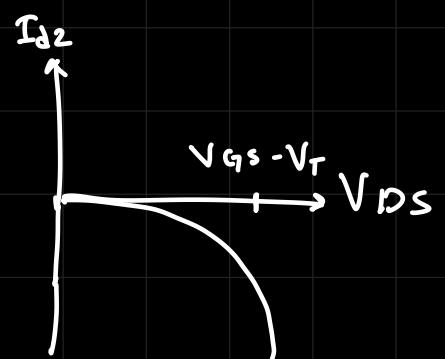
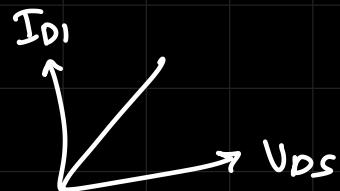
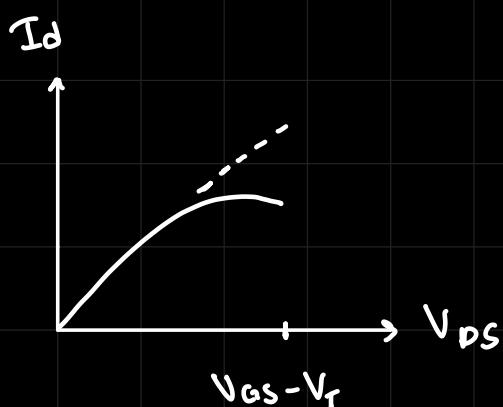
$$Z_o = R_C$$

$V_{DS} \uparrow \rightarrow$ Channel conducts $\rightarrow I_D \uparrow$ linearly
 as $V_{DS} \gg \rightarrow$ Channel conductivity $\downarrow \rightarrow I_d \downarrow$

$$I_D = I_{D1} + I_{D2}$$

$$I_{D1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$I_{D2} = -\frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{DS}^2$$



for small V_{DS} , $I_D \approx I_{D1} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$

$$R_{DS} = \frac{V_{DS}}{I_{D1}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

This approximation works for $|I_{d1}| \gg |I_{D2}|$

which happens when $(V_{GS} - V_T) \gg \frac{1}{2} V_{DS}$

> Triode Region

$$R_{DS} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)} \quad \text{for } V_{DS} \ll 2(V_{GS} - V_T)$$

In a MOSFET in saturation I_D and V_{DS} are independent X



wrong assumption because the resistance into Drain $\rightarrow \infty$

(const current)

→ pinch off region moves towards SRC terminal

→ for $V_{DS} \gg V_{DS, \text{sat}}$, the net additional potential $\propto \frac{1}{V_{DS}}$ reflected in the depletion region (E field)

$$I_D \text{ sat} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

(old)

new $I_D \text{ sat} = ?$ assuming channel length modulation



$$L \rightarrow (L - \Delta L)$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{(L - \Delta L)} (V_{GS} - V_T)^2$$

$$= \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \times \left(1 - \frac{\Delta L}{L}\right)^{-1} (V_{GS} - V_T)^2$$

$\rightarrow \frac{\Delta L}{L} \ll 1$

binomial expansion

$$(1+x)^{-1} = 1 - x + \frac{x^2}{2!} + \dots$$

Since $x = -\frac{\Delta L}{L}$ and $x^2 \ll \dots$,

neglecting terms after order = 1

$$(1+x)^{-1} = 1 - x \quad (\text{approx})$$

$$i_D = \mu_n C_{ox} \frac{W}{L} \times \left(1 + \frac{\Delta L}{L} \right) (V_{GS} - V_T)^2$$

$$\Delta L \propto V_{DS}$$

$$\Delta L = \lambda' V_{DS}$$

↳ processed parameter

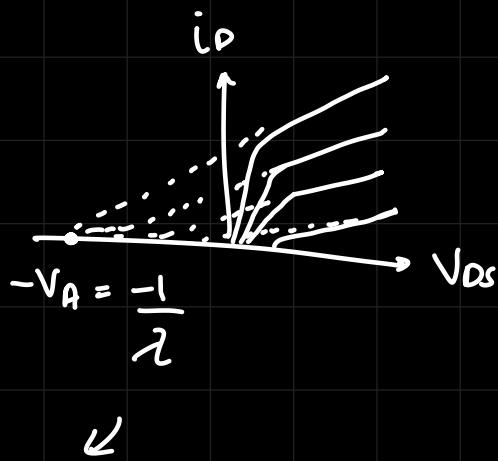
$$\text{Let } \lambda = \frac{\lambda'}{L}$$

$$\frac{\Delta L}{L} = \lambda V_{DS}$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (1 + \lambda V_{DS}) (V_{GS} - V_T)^2$$

now, we observe that $i_D \propto V_{DS}$

Similar situation as early effect in BJT



$$i_D = 0$$

$$1 + 2V_{DS} = 0$$

$$2V_{DS} = -1$$

$$V_{DS} = \frac{-1}{2}$$

$$V_A = \frac{1}{\lambda}$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + 2V_{DS})$$

$$\left[\frac{\partial i_D}{\partial V_{DS}} \right]^{-1} = g_{ro} \quad (\text{resistance})$$

$$= \underbrace{\left(\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 \lambda \right)^{-1}}_{g_{ro}}$$

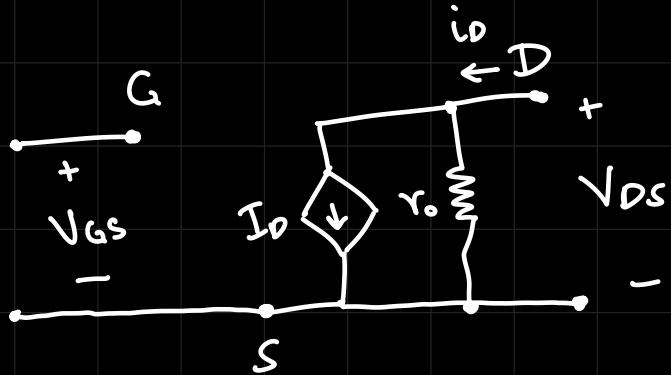
$I_{D \text{ previous}}^{\text{sat}}$

$$g_{ro} = \left(2 I_{D \text{ previous}}^{\text{sat}} \right)^{-1}$$

$$g_{ro} = \frac{V_A}{I_{D \text{ previous}}^{\text{sat}}}$$

DC model

Note: $I_{GS} = 0 \because \text{insulator (Mo)}$



Similar to IC
model of BJT

$$g_{ro} = \frac{V_A}{I_D}$$

$$i_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$I_D = \frac{i_D}{1 + \lambda V_{DS}}$$

$$g_D = \frac{V_A}{I_D} = \frac{V_A}{i_D} \times (1 + \lambda V_{DS}) = \frac{V_A}{i_D} (1 + \frac{V_{DS}}{V_A})$$

PMOS

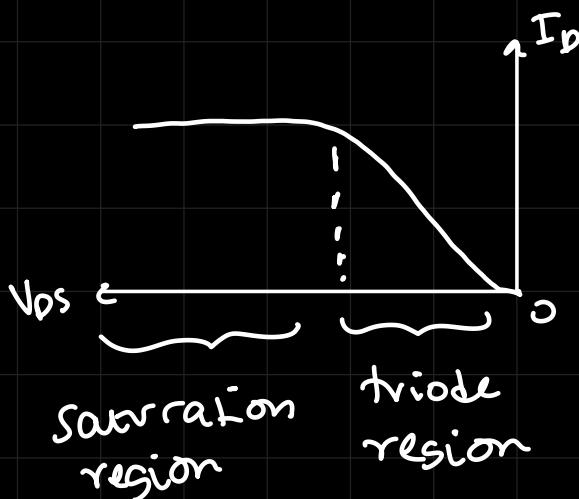
↳ n type substrate

↳ -ve V_{GS} to attract holes

majority carrier ↘

↳ I_D from S → D

because e⁻ : D → S



DC Analysis (5 steps)

① ASSUME

② ENFORCE (Id equations, $I_G = 0$, V_{DS} ? V_{GS} ?)

for Triode region:

$$I_d = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) (V_{DS} - V_{DS}^2)$$

for saturation region:

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

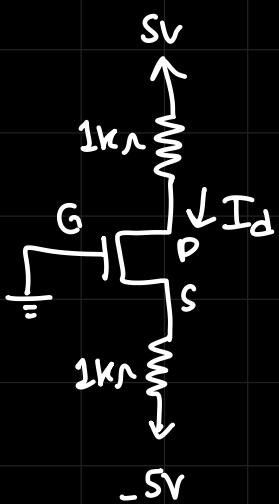
③ CHECK

cutoff: $V_{GS} < V_T$

triode: $V_{DS} < V_{GS} - V_T$ and $V_{GS} > V_T$

saturation: $V_{DS} \gg V_{GS} - V_T$ and $V_{GS} > V_T$

Eg: assume region of operation



↪ saturation

neglecting early effect

$$I_d = \frac{1}{2} \mu_n C_{ox} (V_{GS} - V_T)^2$$

Given = 0.4mA/v² and $V_T = 2V$

$$I_D = 0.4 (V_{GS} - 2)^2 \quad \text{--- ①}$$

$$0 - V_{GS} - 1K(I_D) = -5$$

$$5 - V_{GS} - 1K I_D = 0$$

$$V_{GS} = 5 - 1000 I_D \rightarrow I_D = \frac{5 - V_{GS}}{10^3} \quad \textcircled{1}$$

$$I_D = 0.4(3 - 1000 I_D)^2$$

$$I_D = 0.4(9 + 10^6 I_D^2 - 6000 I_D)$$

$$-5 + 1K I_D + V_{DS} + 1K I_D = +5$$

$$V_{DS} = 10 - (2 \times 10^3 I_D) \quad \textcircled{3}$$

$$\frac{5 - V_{GS}}{10^3} = 0.4(V_{GS}^2 + 4 - 4V_{GS})$$

$$5 - V_{GS} = 400(V_{GS}^2 + 4 - 4V_{GS})$$

$$I_d = 1.24mA$$

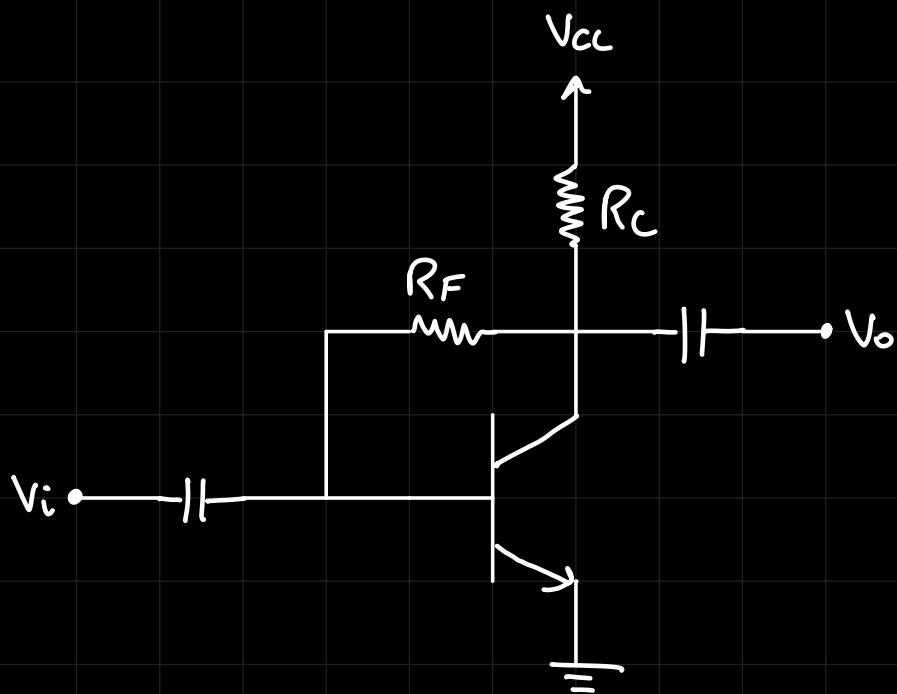
$$3.76V = V_{GS}$$

$$V_{DS} = 7.52V$$

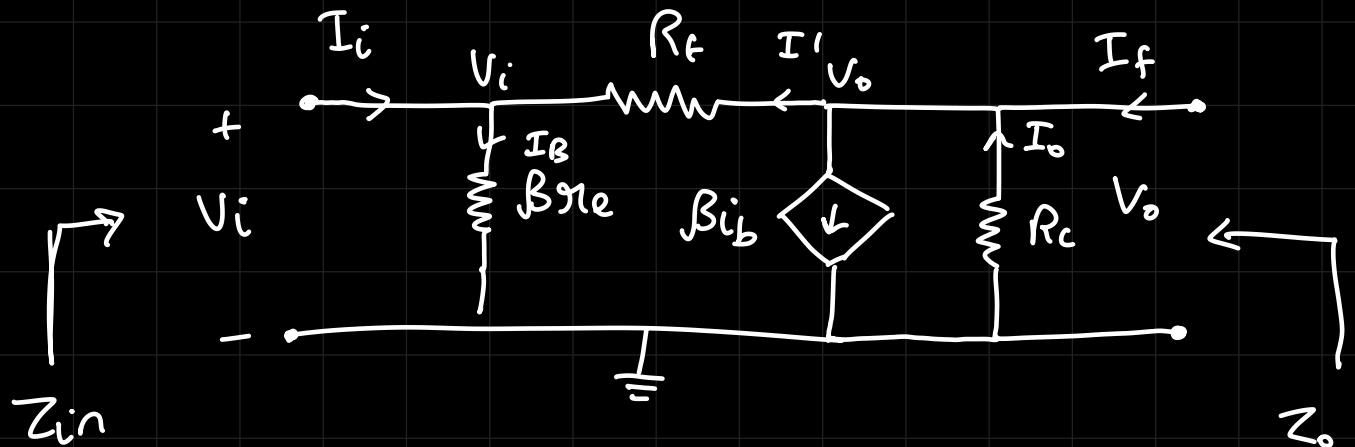
for sat $\rightarrow V_{DS} \gg V_{GS} - V_T$ and $V_{GS} > V_T$

Verified ✓

* AC Analysis of feedback biasing



$R_F = 0 \rightarrow \pi$ model



$$V_o = -I_o R_c$$

$$I_o = \beta I_B + I'$$

$$\text{assume } I' \ll \beta I_B \rightarrow I_o = \beta I_B$$

$$V_o = -\beta I_B R_c$$

$$I_B = \frac{V_i}{\beta r_e}$$

$$\boxed{\frac{V_o}{V_i} = -\frac{R_c}{r_e}}$$

Quiz 2: 4 questions

2 x AC analysis BJT

1 x AC MOSFET

1 x DC MOSFET

$$\begin{aligned} I' &= \frac{V_o - V_i}{R_f} = \frac{V_o}{R_f} - \frac{V_i}{R_f} \\ &= -\frac{V_i \cdot R_c}{r_e R_f} - \frac{V_i}{R_f} \end{aligned}$$

$$V_o = -\beta I_B R_c$$

$$I_i + I' = I_B$$

$$I_B - I_i = \frac{V_o}{R_f} - \frac{V_i}{R_f}$$

$$I_B - I_i = -\frac{\beta I_B R_c}{R_f} - \frac{V_i}{R_f}$$

$$I_b - I_i = \frac{-\beta V_i R_c}{\beta r_e R_f} - \frac{V_i}{R_f}$$

$$I_b - I_i = \frac{-V_i(R_c + r_e)}{r_e R_f}$$

$$I_b = \frac{V_i}{\beta r_e}$$

$$\frac{V_i}{\beta r_e} + \frac{V_i(R_c + r_e)}{r_e R_f} = I_i$$

$$\frac{1}{\beta r_e} + \frac{R_c + r_e}{r_e R_f} = \frac{1}{Z_{in}}$$

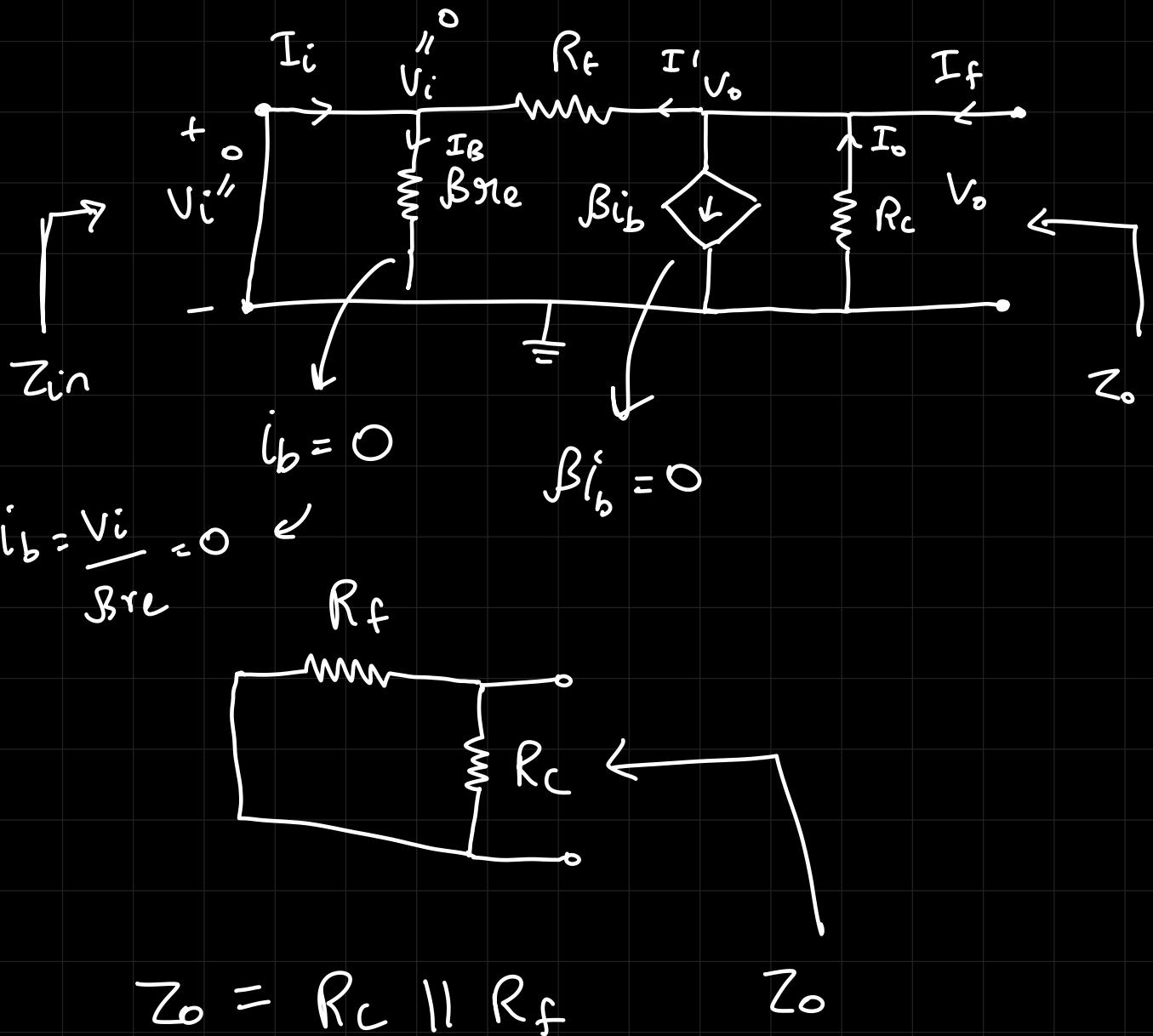
$$\frac{\beta r_e + r_e R_f}{r_e R_f + \beta r_e (R_c + r_e)} = Z_{in}$$

$$\frac{\beta + R_f}{\beta (R_c + r_e) + R_f} = Z_{in}$$

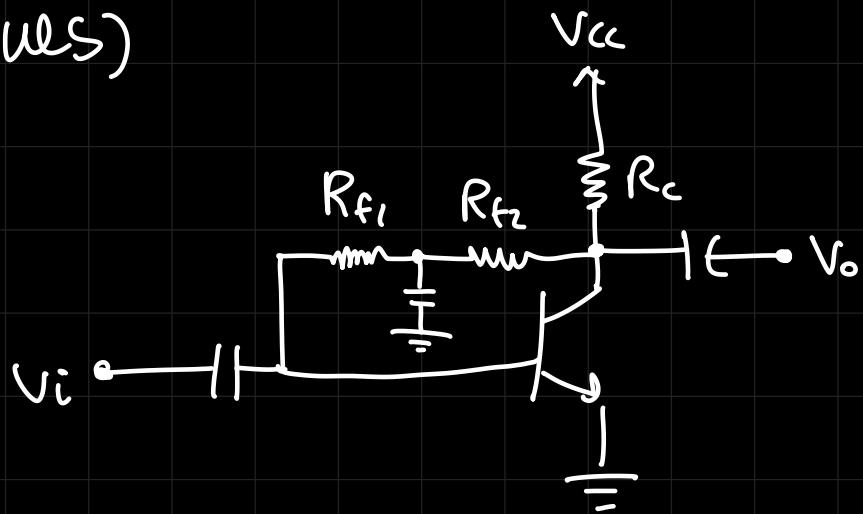
$$Z_{in} = \frac{1}{\frac{1}{R_f} + \left(\frac{1}{\beta r_e} + \frac{R_c}{r_e R_f} \right)}$$

$$Z_0 = \frac{V_o}{I_f}$$

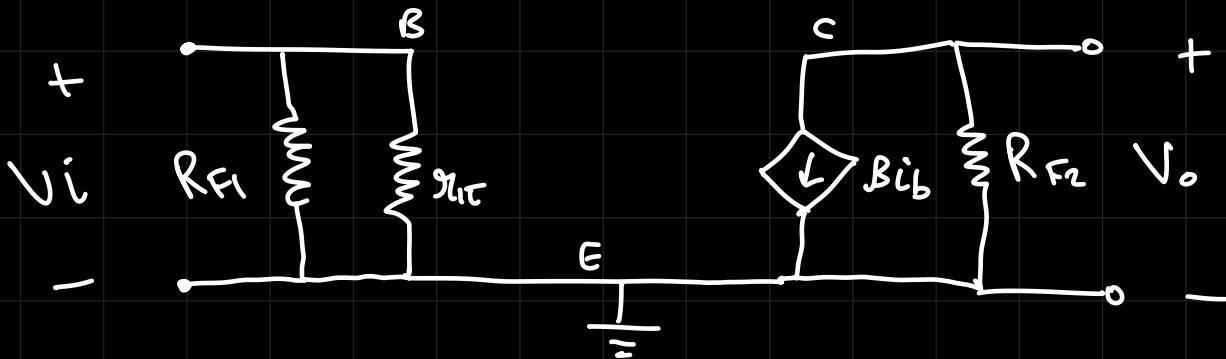
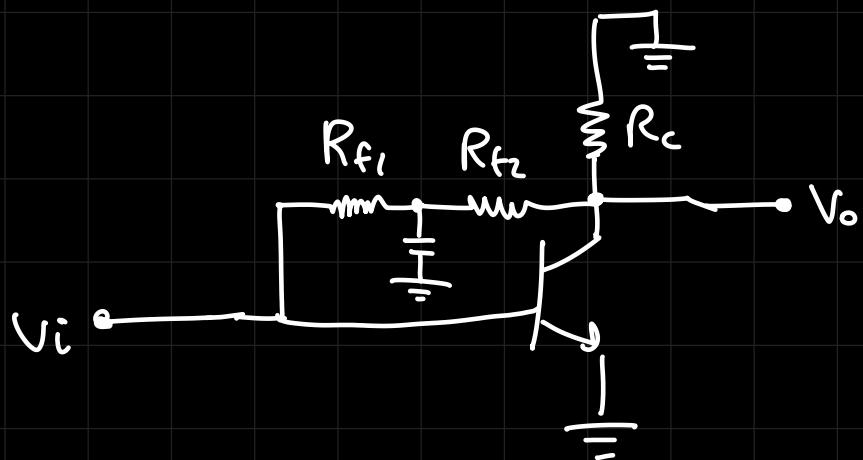
like 2port network problems,
remove input V



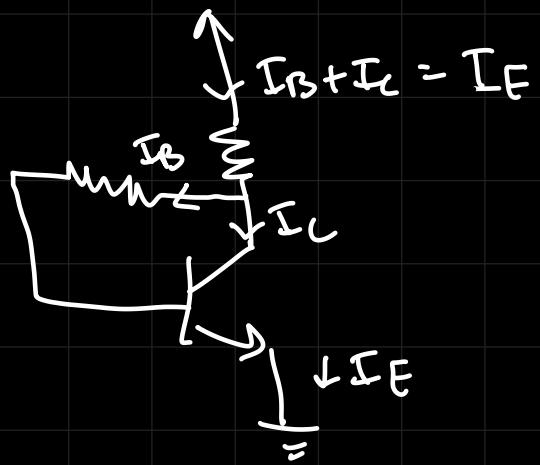
gues)



$A_C \rightarrow$

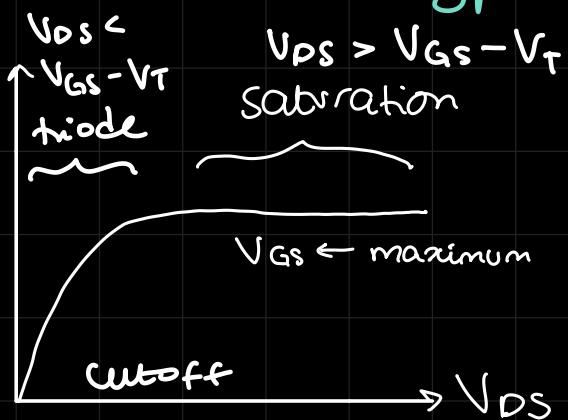


called "feedback" because
we are getting I_E in Collector
and Emitter side



MOSFET (numerical)

enhancement type



NMOS: \approx parallel plate capacitor
(principle)

Saturation mode: $V_{DS} > V_{GS} - V_T$

$$I_D = \frac{1}{2} \mu_n C_{ox} \times \frac{W}{L} \times [V_{GS} - V_T]^2$$

↓ ↓
 oxide capacitance
 e- mobility
 $\left(\frac{m^2}{V \text{ sec}} \right)$

Triode mode: $V_{DS} < V_{GS} - V_T$

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \times \left(V_{DS} - \frac{1}{2} V_{DS}^2 \right)$$

Cutoff mode : $V_{GS} < V_T$

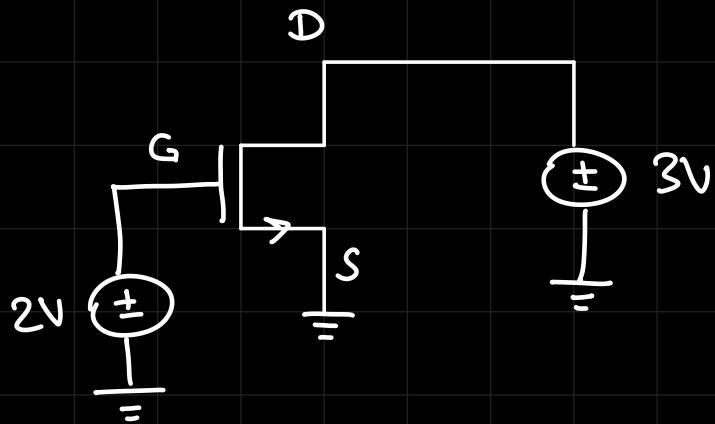
$$I_d = 0$$

→ for the given circuit shown,

$$V_T = 0.6V$$

find the region of operation

$$\begin{aligned} V_T &= +ve \rightarrow n \text{ channel} \\ &= -ve \rightarrow p \text{ channel} \end{aligned}$$



$$-2 + V_{GS} = 0$$

$$V_{GS} = 2V$$

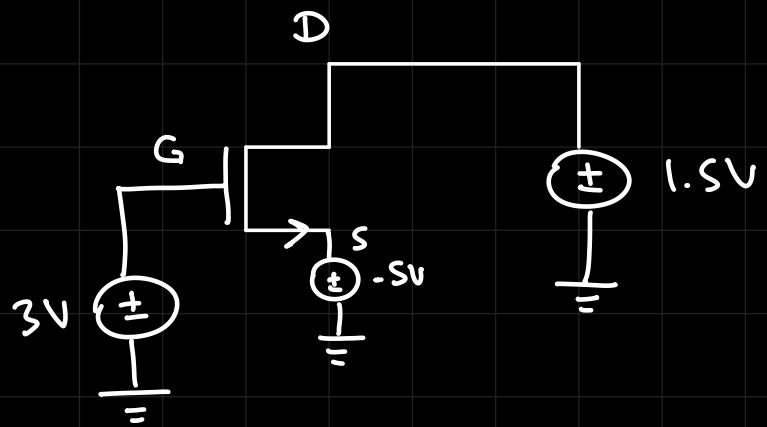
$$-3 + V_{DS} = 0$$

$$V_{DS} = 3V$$

$$V_{DS} = 3V > V_{GS} - V_T = 1.3V$$

Saturation

g) determine mode of operation



$$-3 + V_{GS} + 0.5 = 0$$

$$V_{GS} = 2.5 \text{ V}$$

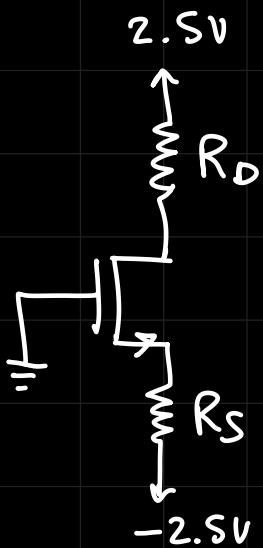
$$-1.5 + V_{DS} + 0.5 = 0$$

$$V_{DS} = 1 \text{ V}$$

$$V_{DS} = 1 \text{ V} < V_{GS} = 2.5 - 0.6 = 1.9 \text{ V}$$

Triode mode

(g)



Calculate R_D and R_S

$$\text{given : } V_T = 1V$$

$$m_n C_{ox} = 60 \mu A V^{-2}$$

$$\frac{w}{L} = \frac{120 \mu m}{3 \mu m} = 40$$

$$I_D = 0.3mA$$

$$V_D = 0.4V$$

$$V_{GS} - 2.5 + R_S I_S = 0$$

$$V_{GS} + R_S I_S = 2.5$$

$$-2.5 + R_D I_D + V_D + R_S I_S - 2.5 = 0$$

assume sat

$$0.3 \times 10^{-3} = 60 \times 10^{-6} \times 40 (V_{GS} - V_T)^2$$

$$R_D = \frac{2.5 - V_D}{I_D} \kappa = \frac{2.5 - 0.4}{0.3} \kappa = \frac{2.1}{0.3} \kappa = 7 \kappa$$

$$V_{DS} = V_D - V_S$$

$$V_{GS} = V_G - V_S$$

note: $V_G = 0$

$$V_D = 0.4V \text{ (given)}$$

$$V_{DS}$$

$$V_{GS} - V_T$$



$$V_T = 1V$$

$$V_{GS} - V_T = -V_S - 1$$

$$V_{DS} = 0.4 - V_S$$

$V_{DS} > V_{GS} - V_T \rightarrow \text{SATURATION mode}$

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

10^{-1}

$$\cancel{0.6 \times 10^{-3}} = 6.2 \times \cancel{10^{-6}} \times 4.2 \times (V_{GS} - V_T)^2$$

$$0.2S = (V_{GS} - V_T)^2$$

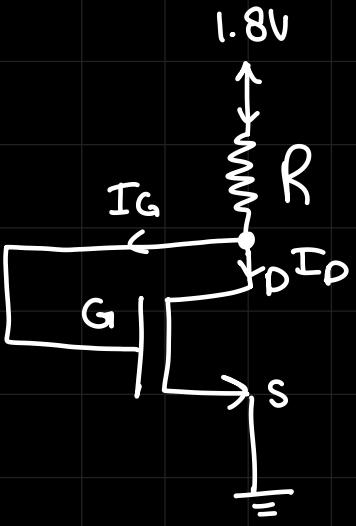
$$V_{GS} - V_T = 0.5V$$

$$V_{GS} = 1.5V \rightarrow V_{GS} = V_G - V_S \Rightarrow V_S = -1.5V$$

\overline{I}_0

$$R_s = \frac{V_S - (-2.5)}{I_S} = \frac{V_S + 2.5}{I_D} = \frac{1}{0.3} k\Omega = 3.33 k\Omega$$

g)



given:

$$V_D = 0.7V$$

$$V_m = 0.5V$$

$$M_n(\omega) = 0.4m$$

$$\frac{w}{l} = 4$$

$$R = \frac{1.8 - 0.7}{I_D (\approx I_S)}$$

$$V_D = 0.7V, V_S = 0V, V_G = 0.7V \text{ (shorted)}$$

$$V_{DS} > V_{GS} - V_T$$

saturation

$$\text{because } V_S = 0 \text{ so } V_D, V_G - V_T \\ 0.7 > 0.7 - 0.5$$

$$I_d = \frac{1}{2} \times 0.4 \times 10^{-3} \times 4 \times (V_G - V_T)^2$$

$$= 0.8 \times 10^{-3} \times 0.04$$

$$= \underline{32 \mu A}$$

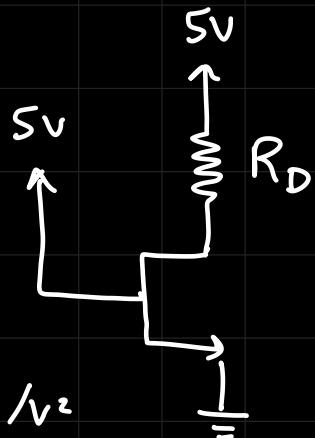
$$R = \frac{1.8 - 0.7}{32} M\Omega = \frac{1.1}{32} = \underline{34 k\Omega}$$

Q3

$$V_D = 0.1V$$

$$V_T = 1V$$

$$\mu n C_{ox} \frac{w}{L} = 1mA/V^2$$



$$-S + I_D R_D + V_{DS} = 0$$

$$V_{GS} = 5V$$

$$V_G = 5V$$

$$V_{GS} - V_T = 4V$$

$$V_{DS} = 0.1$$

triode mode

$$I_D = 10^{-3} \times 4 \times \left(0.1 - \frac{1}{2}(0.01)\right)$$

$$= 10^{-3} \times 4 \times 10^{-1} - 5 \times 10^{-3}$$

$$= 10^{-4} \times 4 - 5 \times 10^{-3}$$

$$\Rightarrow (4 - 5) \times 10^{-4}$$

\Rightarrow

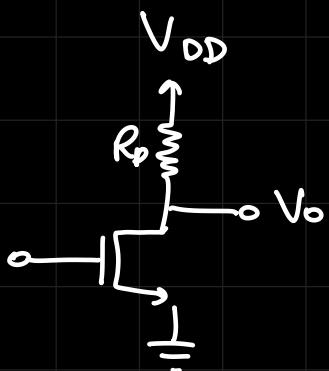
tentative date for simulation \rightarrow 15th April
project deadline: before endsem

MOSFET AC analysis (small signal operation)

Mosfet = Amplifier

only in saturation region

so that linear
amplification is
achieved



$$V_o = V_{DD} - I_D R_D$$

$$i_D R_D = V_{DD} - V_o = V_{DD} - V_{DS}$$

$$i_D = \frac{V_{DD}}{R_D} - \frac{V_{DS}}{R_D}$$

CASE 1 $\rightarrow i_D = 0$

$$\hookrightarrow V_{DS} = V_{DD}$$

CUTOFF

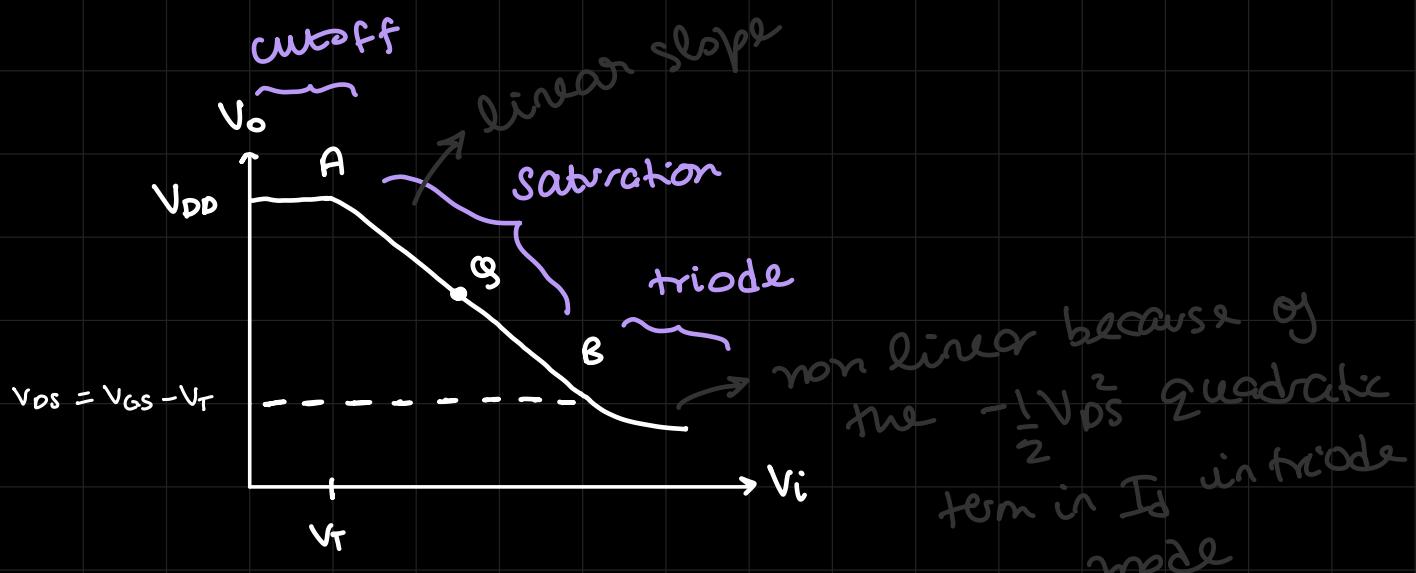
$$(V_i < V_T)$$

no channel induced

Case 2 \rightarrow Saturation : $V_{DS} > V_{GS} - V_T$

$V_i \uparrow \rightarrow V_{GS} \uparrow \rightarrow i_D \uparrow \rightarrow V_{DS} \downarrow$ until
 $V_{DS} = V_{GS} - V_T$

$$i_D = \frac{V_{DD} - V_{DS}}{R_o}$$



gain = $-ve$

(Q/P $\rightarrow 180^\circ$ out of phase)

$$V_{GS} = V_{GS} - V_{GS}$$

$$v_{nk} = DC + AC$$

$$i_D = \underbrace{\frac{1}{2} k_n (V_{GS} - V_T)^2}_{DC} + \underbrace{k_n (V_S - V_T) v_{GS}}_{\text{linear}} + \underbrace{\frac{1}{2} k_n v_{GS}^2}_{\text{non linear}}$$

$$v_{GS} \ll 2(V_{GS} - V_T)$$

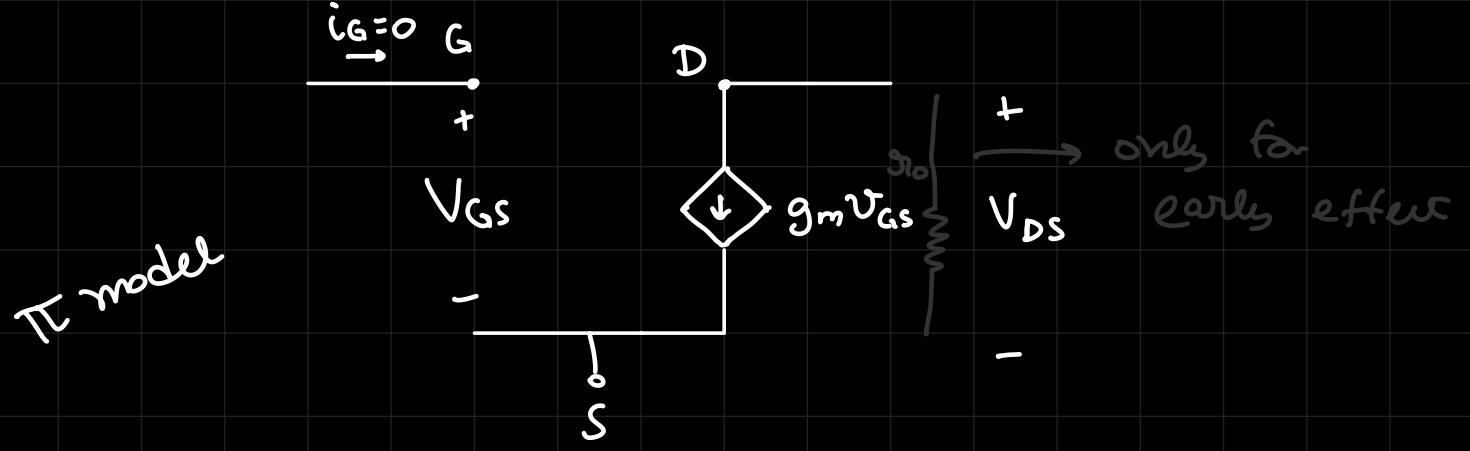
$$g_m = \frac{i_d}{v_{GS}} = k_n (V_{GS} - V_T)$$

$$g_m = \left. \frac{\partial i_d}{\partial V_{GS}} \right|_{V_{GS} = V_{GS}}$$

$$A_V = \frac{v_d}{v_{GS}} = -g_m R_D$$

for saturation \rightarrow

$$V_{GS} - V_T < V_D < V_{DD}$$



early effect impedance ~

$$i_D = K(V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$r_o = \frac{1}{\lambda K (V_{GS} - V_T)^2}$$

$$r_o = \left[\frac{\partial i_D}{\partial V_{GS}} \Bigg|_{V_{GS} = V_{GS}} \right]^{-1}$$

$$r_o = (K(V_{GS} - V_T)^2 \lambda)^{-1}$$

SMALL SIGNAL OPERATION

① DC Analysis

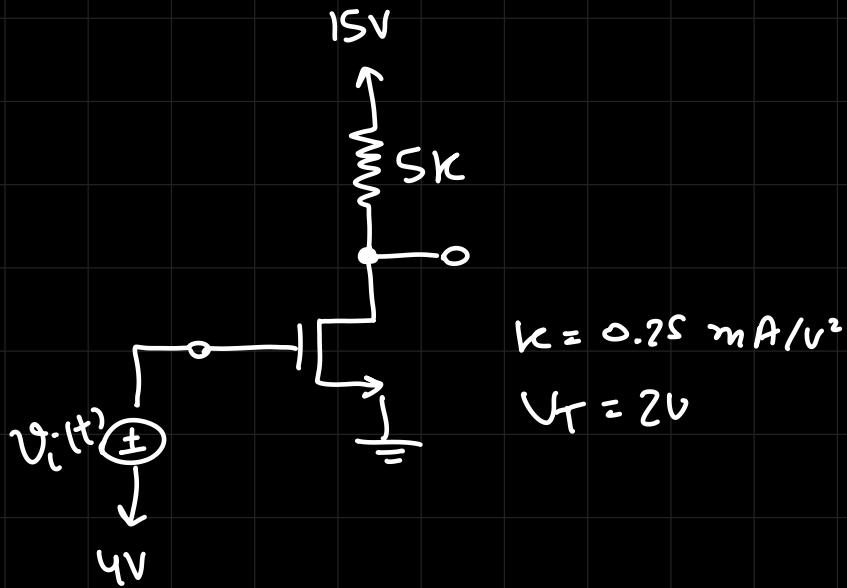
$$g_m = 2k(V_{GS} - V_T)$$

$$r_o = \frac{1}{2k(V_{GS} - V_T)^2}$$

② AC analysis

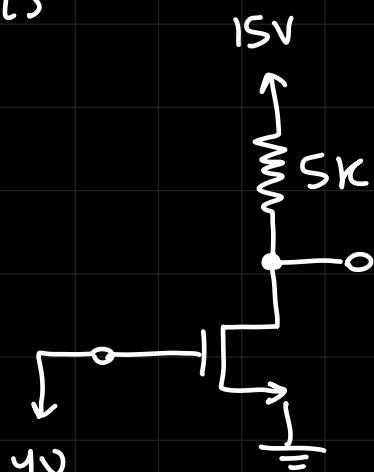
gain

g)



① DC Analysis

$$V_{GS} = 4\text{V}$$



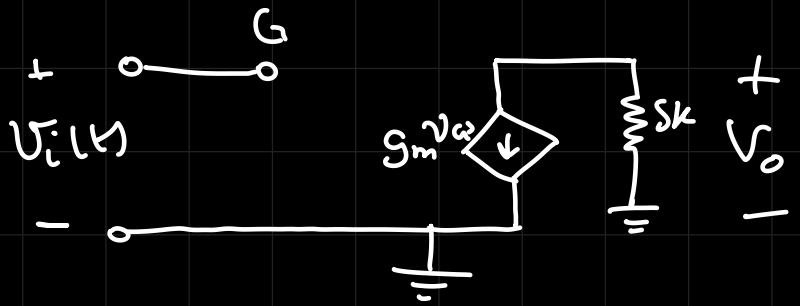
$$i_D = \mu_n C_o \frac{W}{L} (V_{GS} - V_T)^2 \quad \text{Assuming SAT}$$

$$= .25 \times 10^{-3} \times (4 - 2)^2$$

$$= 1\text{mA}$$

params

$$\left\{ \begin{array}{l} g_m = 2k(V_{GS} - V_T) = 1\text{mA/V}^{-1} \\ r_o = \infty \quad (\text{not considering early effect}) \end{array} \right.$$



$$V_o = -G_m V_{GS}(S_k)$$

$$= -G_m V_i(S_k)$$

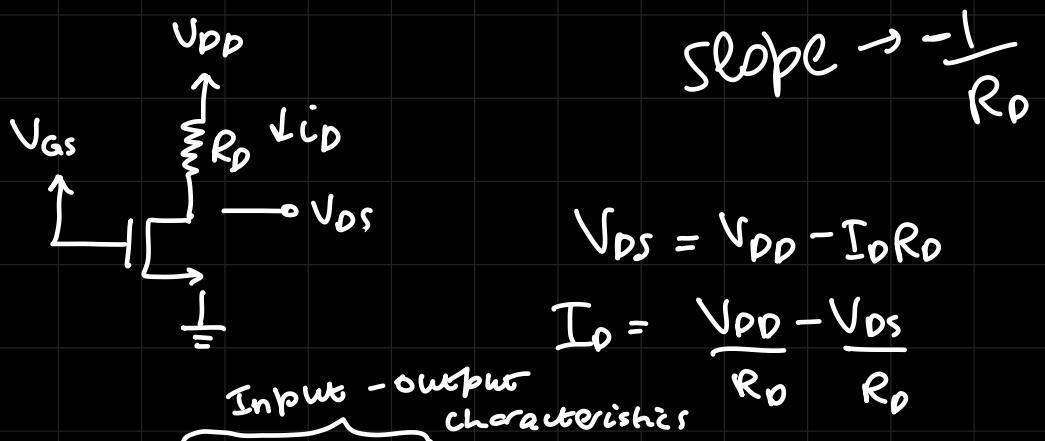
$$\text{Gain : } A_v = \frac{V_o}{V_i} = -G_m(S_k) = \underline{\underline{-5}}$$

MOSFET Amplifier Biasing

→ Establish I_D through biasing

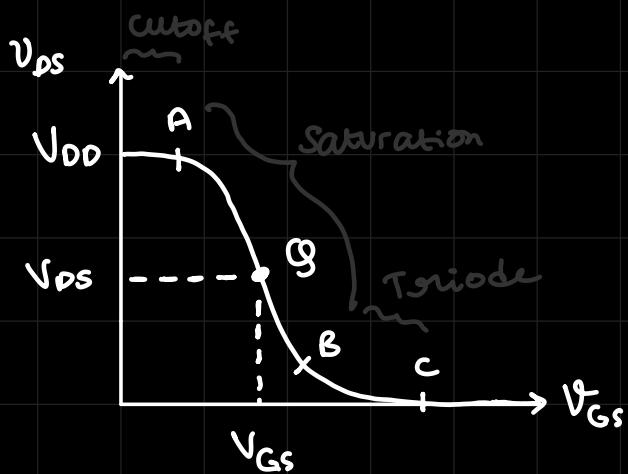
↳ DC operating point for
a given V_{GS}

so that the op-amp provides adequate gain
and undistorted output swing for input transitions

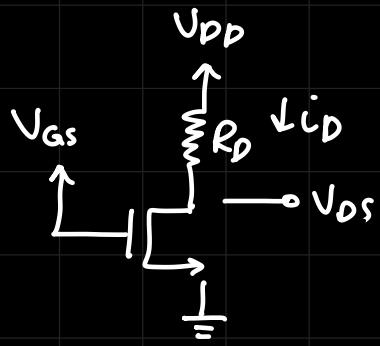


Q point in Voltage Transfer characteristics,
(V_{DS} , V_{GS})

Q point in $I_D - V_{GS}$ curve $\rightarrow (I_D, V_{DS})$

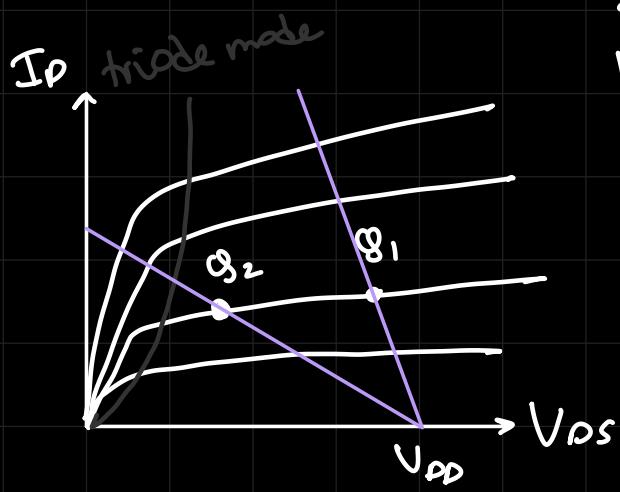


if Q was further down,
towards B, the output
will have non linear
distortions because the
Amp goes into triode
mode. (when input
signal swing is high)



What value of R_D to choose?

- ① suppose we choose $R_D = R_{D2}$
so that the we enter Q point at Q_2 for V_{GS}

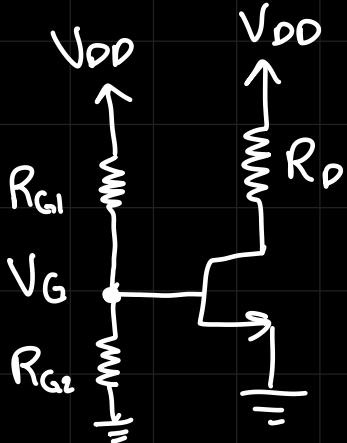


but negative transients of the input signal might make the comp go into triode mode (not ideal)

for Q point = Q_1 ,
we are very close to V_{DD} and
the amplifier might go to cutoff mode
for large -ve transients of input signal
(distorted output)

We need R_D to be such that Q point is between the above 2 extreme points

R_D should be such that for a given V_{GS} the Q point is well within the saturation point



① Since $I_G = 0$ always we can keep higher values of R_{G1} and R_{G2} and hence high input impedance so it helps us capture the entire info in the input signal

② R_{G1} and R_{G2} should be high but keep in mind $V_G > V_T$ for saturation.

$$\text{also } V_D > V_G - V_T$$

③ If I fix the value of V_G , my circuit is still not stable to variations in device parameters or temperature variation

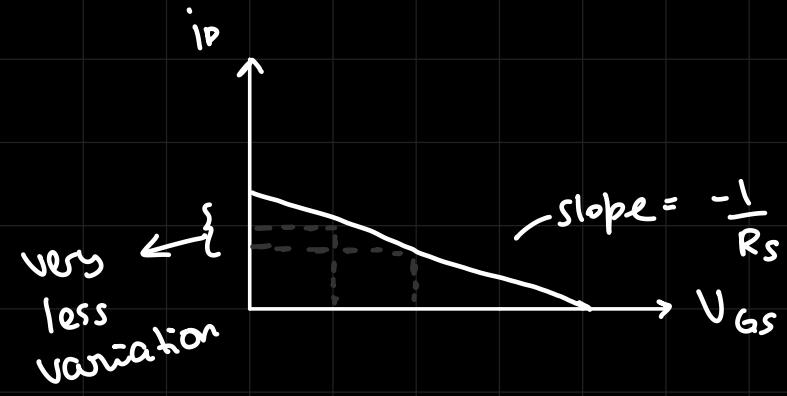
→ We need a feedback mechanism and for this, an R_s resistance is placed at the source

$$\text{if } i_D \uparrow \rightarrow V_G = V_{GS} + I_D R_s$$

$$\downarrow \\ V_{GS} \downarrow \\ V_G = V_G - I_D R_s$$

$$\hookrightarrow i_D \downarrow$$

$$\text{if } i_D \downarrow \rightarrow V_{GS} \uparrow \rightarrow i_D \uparrow \quad (\text{feedback})$$

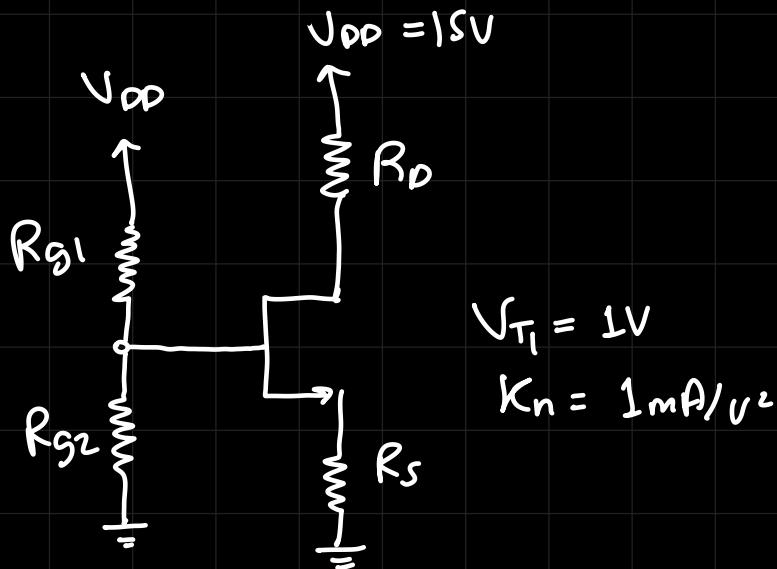


Slope should be lower $\rightarrow R_s$ should be \uparrow
but not $\rightarrow \infty$

Summary :

- ① R_D : should be high provided the cutoff region is avoided
- ② R_{G1}, R_{G2} : should be high such that MOSFET operates in the saturation region
- ③ R_s : should also be very high to avoid fluctuations in I_D

eg 3



Q) calculate the charge in I_D if mos is charged with device with some K_n but different $V_{T2} = 1.5V$

Rule of thumb: We choose the R_D and R_s voltage drop as $\frac{1}{3}$ rd of the supply voltage

$$V_D = V_{DD} - \frac{V_{DD}}{3} = 15 - 5 = 10V$$

$$V_S = V_{DD} - \frac{V_{DD}}{3} - \frac{V_{DD}}{3} = 5V$$

$$\text{Saturation} \rightarrow I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2$$

$$1 = (V_{GS} - 1)^2$$

$$V_{GS} = 2V$$

$$V_G = V_{GS} + V_S = 7V$$

$$V_{DS} = SV \quad V_{GS} - V_T = 1V$$

$$V_{DS} > V_{GS} - V_T \quad \checkmark$$

$$V_G = \frac{R_2}{R_1 + R_2} \times IS$$

$$\gamma R_1 + \gamma R_2 = IS R_2$$

$$\gamma R_1 = 8 R_2$$

if i assume $R_1 = 8m\Omega \rightarrow R_2 = 7m\Omega$

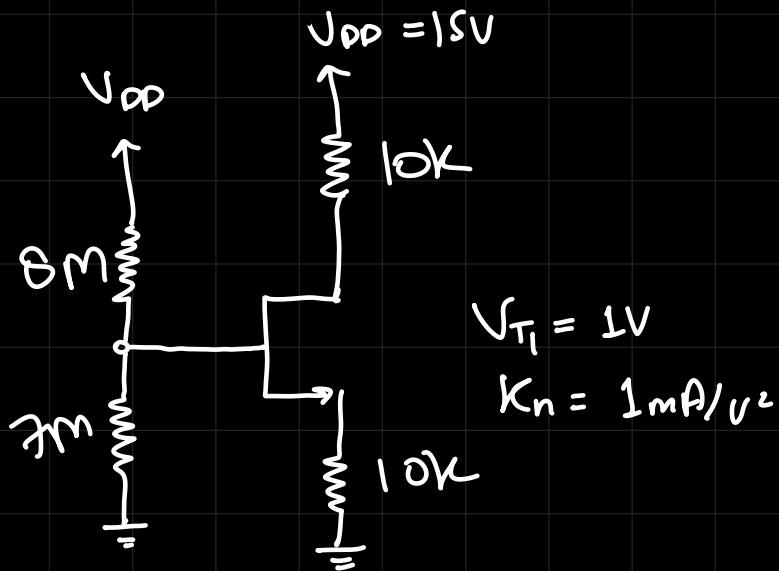
$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5}{0.5m} = 10k\Omega$$

$$R_S = \frac{V_S}{I_D} = \frac{5}{0.5m} = 10k\Omega$$

all resistors found

→ at $V_T = 1.5V$

V_{GS} and I_D will change



$$-IS + 10k I_D + V_{DS} + 10k I_D = 0$$

$$I_D = \frac{IS - V_{DS}}{20k}$$

$$V_G = V_{GS} + V_s = V_{GS} + I_D R_s$$

$$V_{GS} + 10k I_D = 7$$

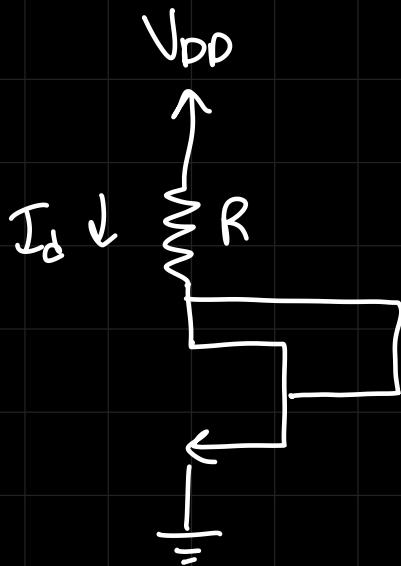
$$I_D = \frac{1}{2} (S.S - 10k I_D)^2$$

$$2I_D = 30.2S + 100m I_D^2 - 110k I_D$$

$$I_{D2} = 0.5\text{mA} , I_{D1} =$$

note: $K_n = \mu_n C_{ox}$

current mirror circuit



We know,

$$V_D = V_G \rightarrow$$

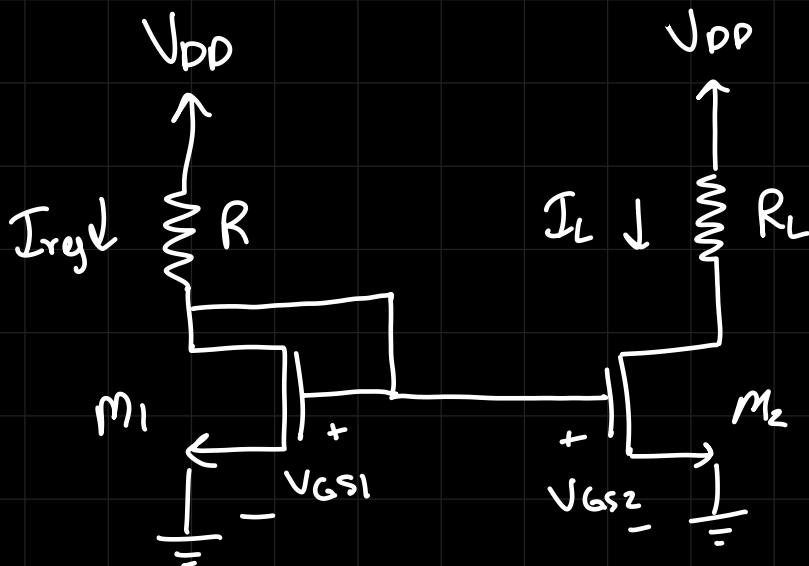
$$V_G > V_T \text{ or } C$$

$$V_D > V_G - V_T$$

always in
saturation mode

$$I_D = k (V_{GS} - V_T)^2$$

$$V_{GS} = \sqrt{\frac{I_D}{k}} + V_T$$



if $V_{T1} = V_{T2}$ and M_1, M_2 have
some characteristics

$$I_L = k(V_{GS2} - V_T)^2$$

$$I_{ref} = k(V_{GS1} - V_T)^2$$

Since both gate terminals are shorted

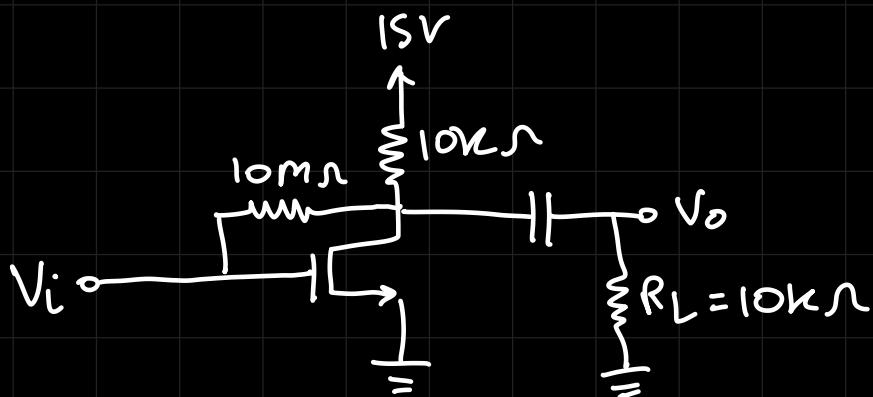
$$V_{GS1} = V_{GS2}$$

So, $I_{ref} = I_L$ only if R_L is
such that M_2 remains in saturation

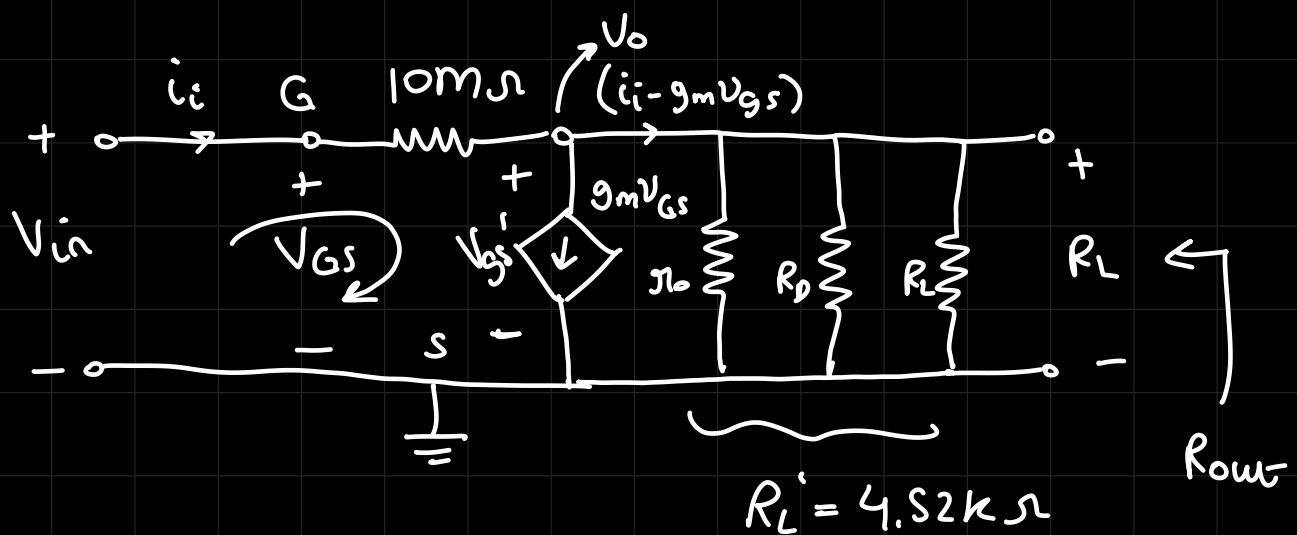
8th March \rightarrow Tut simulation

TUT(continuation)
previous TUT done on paper

g)



AC analysis $\rightarrow \pi$ model



$$V_o = (i_i - g_m v_{GS}) R'_L \quad \text{--- } ①$$

$$KVL = -V_{in} + (10M i_i) + V_o = 0$$

$$V_{in} - V_o = 10 \times 10^6 (i_i)$$

$$\frac{V_{in} - V_o}{R_G} = i_i \quad \text{--- } ②$$

$$V_o = \left(\frac{V_{in} - V_o}{R_G} - g_m V_{gs} \right) R_L'$$

$$V_o + \frac{V_o R_L'}{R_G} = \frac{V_{in} \cdot R_L'}{R_G} - g_m V_{gs} R_L'$$

$$V_o \left[1 + \frac{R_L'}{R_G} \right] = V_{in} \left(\frac{1}{R_G} - g_m \right) R_L'$$

↓

$$\frac{V_{out}}{V_{in}} = A_v = \frac{\left(\frac{1}{R_G} - g_m \right) R_L'}{\left(1 + \frac{R_L'}{R_G} \right)} \quad \begin{matrix} V_{gs} = V_{in} \\ \text{volt/volt} \end{matrix}$$

(overall gain)

mosfet gain = $\frac{V_o}{V_{gs}}$ Gain without R_G

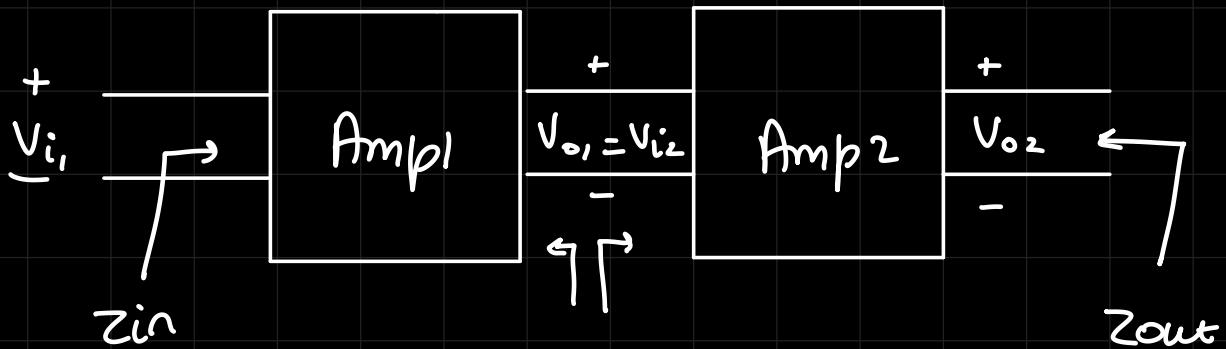
$$R_L' = 4.52 k\Omega \quad g_m = 0.72 m$$

$$A_v_{\text{overall}} = -3.259 \sim -3.3$$

$$R_{in} = \frac{V_i}{i_i} = \frac{V_i \times R_G}{V_i - V_o} = \frac{V_i \times R_G}{V_i + 3.3 V_i}$$

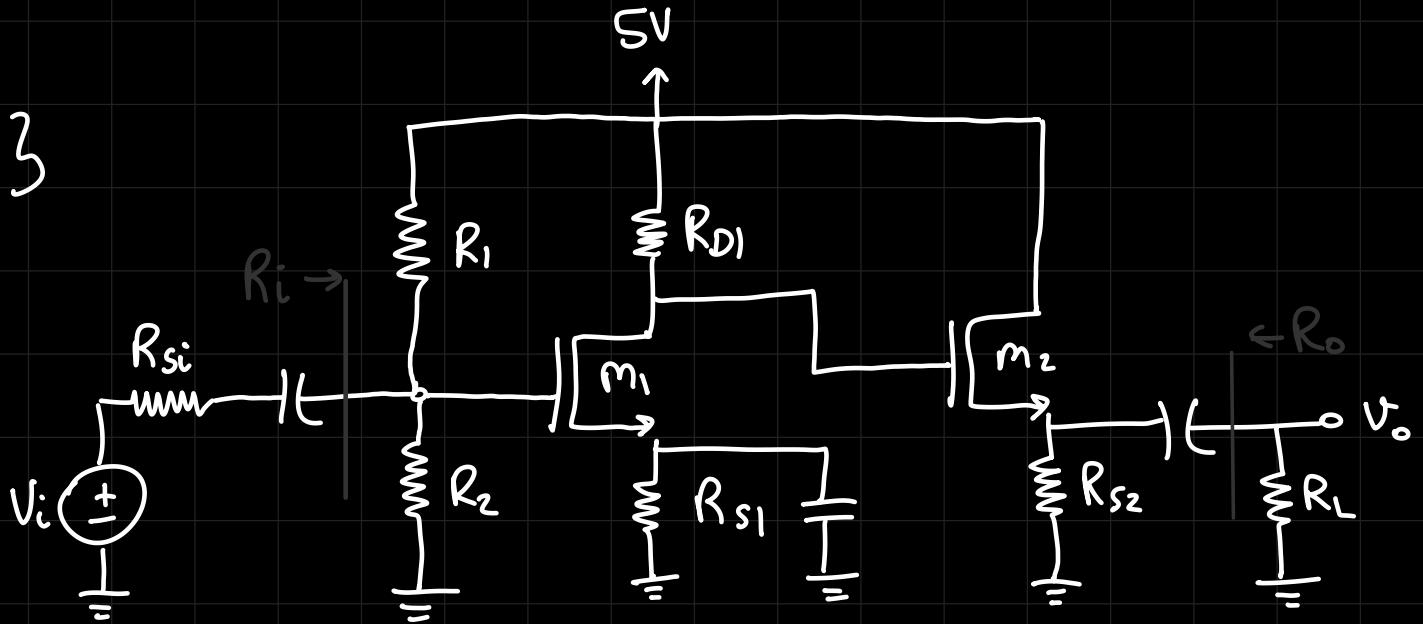
$$= \frac{R_G}{4.3} \Rightarrow 2.32 M\Omega$$

multistage / cascade amplifier



$$R_{out1} = R_{in2}$$

g3



$$K_{n1} = 0.5 \text{ mA/V}^2$$

$$K_{n2} = 0.2 \text{ mA/V}^2$$

$$V_{T1} = V_{T2} = 1.2 \text{ V}$$

$$I_{D1} = 0.2 \text{ mA}$$

$$I_{D2} = 0.5 \text{ mA}$$

$$V_{DS1} = V_{DS2} = 6 \text{ V}$$

$$R_i = 100 \text{ k}\Omega$$

$$R_{si} = 4 \text{ k}\Omega$$

assume

$$K_n = \frac{1}{2} \mu_n C_{ox} \frac{W}{L}$$

} AC \rightarrow BJT
 DC & AC \rightarrow MOSFET
 Current mirror

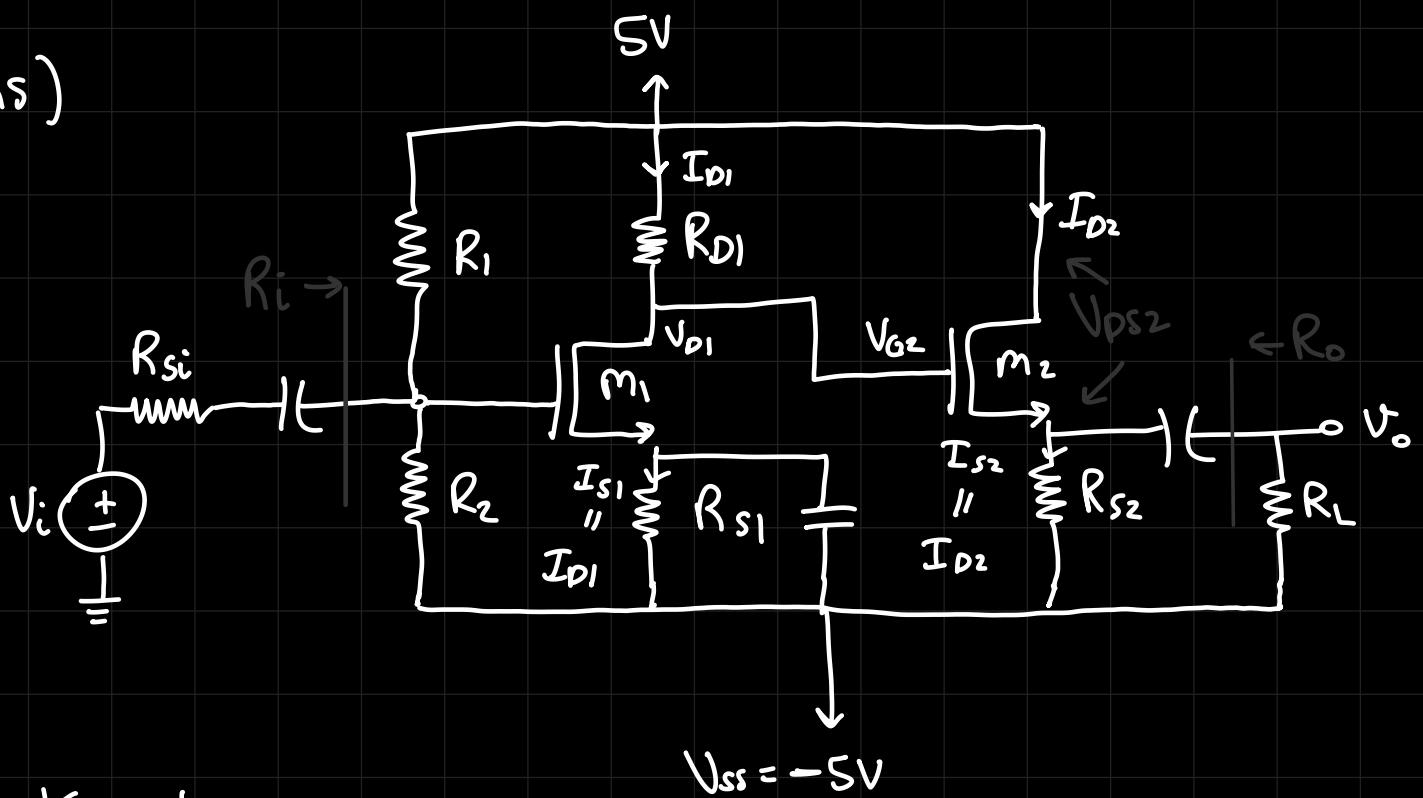
Quiz 2
 Syllabus

1st Amp \rightarrow π model

2nd Amp \rightarrow T model

assume that both work under saturation

Ans)



KVL (Outer loop)

$$-V_{DD} + V_{DS2} + I_{D2}R_{S2} + V_{SS} = 0$$

$$I_{D2}R_{S2} = 10 - 6 = 4V$$

$$R_{S2} = \frac{4}{0.5mA} = 8k\Omega$$

$$V_{GS2} = V_{G2} - V_{S2} = V_{G2} - (4 + V_{CS}) \\ = V_{G2} + 1$$

$$I_{D2} = k_n z (V_{GS2} - V_T)^2$$

$$0.5m = 0.2 \alpha 10^3 (V_{GS2} - 1.2)^2$$

$$2.5 = (V_{GS} - 1.2)^2$$

$$V_{GS}^2 + 1.44 - 2.4V_{GS} = 2.5$$

$$V_{GS2} = \underline{2.78}$$

$$V_{G2} = \underline{1.78 \text{ V}}$$

$$\text{KVL: } -S + I_{D1}R_{D1} + V_{GS2} + I_{D2}R_{S2} - S = 0$$

$$-S + 0.2m R_{D1} + 2.78 + 4 - S$$

$$R_{D1} = \frac{10 - 2.78 - 4}{0.2} \times k$$

$$R_{D1} = \underline{16.1 \text{ k}\Omega}$$

$$V_{G2} = V_{D1} = 1.78V$$

$$\textcircled{3} \quad -V_{DD} + I_{D1}R_{D1} + V_{DS1} + R_{S1}I_{D1} - s = 0$$

$$y = 0.2m(16.1k + R_{S1})$$

$$y = 3.22 + R_{S1}(0.2m)$$

$$R_{S1} = \underline{3.9k\Omega}$$

$$I_{D1} = k n_1 \times (V_{GS} - V_r)^2$$

$$0.2mA = 0.5mA \times (V_{GS} - 1.2)^2$$

$$0.4 = V_{GS}^2 + 1.44 - 2.4V_{GS}$$

$$V_{GS1} = 1.832V$$

$$V_{DS1} = V_{D1} - V_{S1}$$

$$V_{S1} = V_{D1} - 6 = V_{G2} - 6 = 1.78 - 6 = -4.22V$$

$$\begin{aligned}
 V_{GS1} &= V_{G1} - V_{S1} \\
 &= V_{G1} - I_{D1} R_{S1} \\
 &= \frac{R_2}{R_1 + R_2} [V_{DD} - V_{SS}] - I_D R_{S1}
 \end{aligned}$$

$$= \frac{R_2}{R_1 + R_2} (10) - 0.2 \times 10^{-3} \times 3.9 \times 10^3$$

$$\frac{1.832 + 0.28}{10} = \frac{R_2}{R_1 + R_2}$$

$$2.612 = 10 \times \frac{R_2}{R_1 + R_2}$$

We know $R_i = 100 \text{ k}\Omega$

$$R_i = \frac{R_1 \times R_2}{R_1 + R_2} \rightarrow \frac{R_i}{R_1} = \frac{R_2}{R_1 + R_2}$$

$$10 \times \frac{100 \text{ k}}{2.612} = R_1 \rightarrow R_1 = \underline{383 \text{ k}\Omega}$$

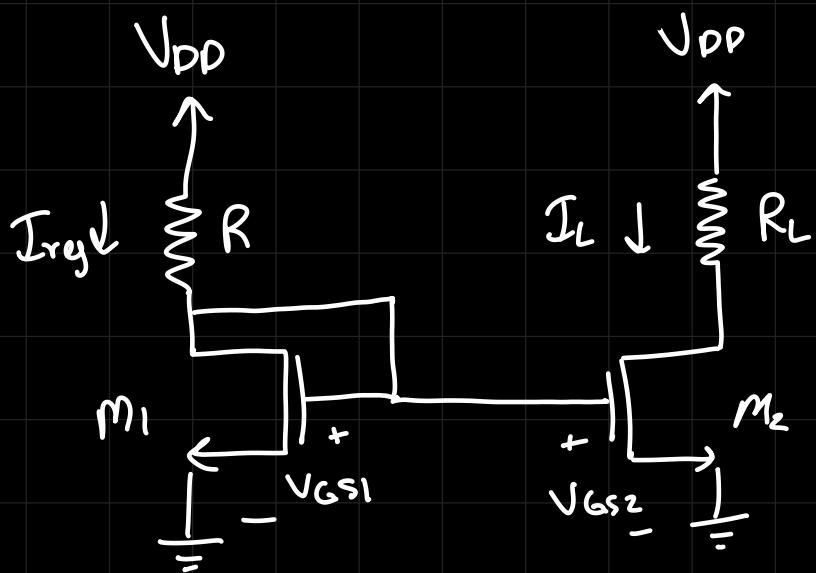
$$\underline{R_2 = 135.33 \text{ k}\Omega}$$

21st (Monday) → Tut Sim x 2 5-7pm

↳ MOSFET Biasing

↳ Current mirror/ cascode

lecture : current mirror



if M_1 and $M_2 \rightarrow k_n$ and V_T characteristics
are same and they are in saturation,

$$I_L = I_{ref}$$

but is this true w/ R_L ?

NO

we require M_2 to be in saturation.

$$V_{G2} > V_{T2}$$

$$V_{D2} > V_{G2} - V_{T2}$$

for M_1 ,

$$I_{ref} = \frac{V_{DD} - V_{D1}}{R}$$

now since $V_{D1} = V_{G1}$

$$I_{ref} = \frac{V_{DD} - V_{G1}}{R}$$

$$V_{G1} = V_{DD} - I_{ref} R$$

for $M_2 \rightarrow$

$$\begin{aligned} V_{D2} &> V_{G2} - V_{T2} \\ V_{D2} &> V_{G1} - V_{T1} \end{aligned} \quad \left. \begin{array}{l} \\ \end{array} \right\} \therefore M_1 \approx M_2$$

$$V_{DD} - I_{RL} R_L > V_{G1} - V_{T1}$$

$$V_{DD} - I_{ref} R_L > V_{G1} - V_{T1} \quad \left. \begin{array}{l} \\ \end{array} \right\} I_{ref} = I_L$$

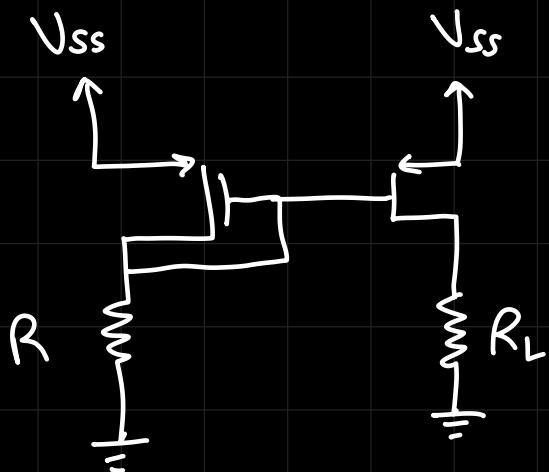
$$V_{G1} = V_{DD} - I_{ref} R \quad \text{(we want this)}$$

$$V_{DD} - I_{ref} R_L > V_{DD} - I_{ref} R - V_{T1}$$

$$I_{ref} R + V_{T1} > I_{ref} R_L$$

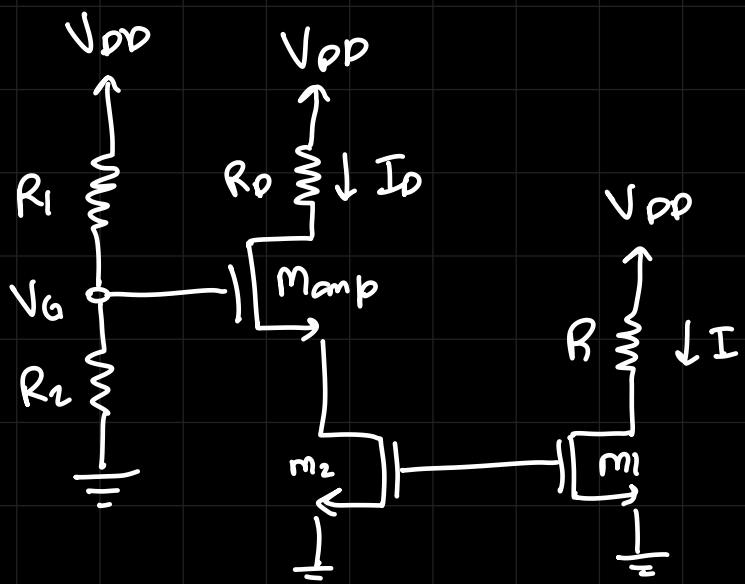
$$R_L < \frac{V_{T1}}{I_{ref}} + R$$

if $R_L < R + \frac{V_T}{I_{ref}}$ then M_2 would be in saturation and $I_L = I_{ref}$



PMOS
current mirror

We can use a current source to bias a MOSFET and for that we use the current mirror circuit



if $M_{amp} = \text{saturation}$
 $I_d = k(V_{GS} - V_T)^L$

$$\text{since } I_d = I \rightarrow V_{GS} = \sqrt{\frac{I}{k}} + V_T$$

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

$$V_{GS} = V_G - V_S$$

$$V_S = V_G - V_{GS}$$

$$= V_{DD} \left(\frac{R_2}{R_1 + R_2} \right) - \left(\sqrt{\frac{I}{k}} + V_T \right)$$

for saturation of Momp: $V_{DS} > V_{GS} - V_T$
 or to satisfy this, $V_{DS} \uparrow \uparrow \rightarrow V_S \downarrow \downarrow$



bias s.t. V_S is small
 by tweaking $R_2, R_1,$

but V_S shouldn't be that small
 because $V_S = V_{D2}$

{Optimization problem?}

Q, What is the limit to which we can reduce V_S ?

for $M_2 \equiv$ saturation \rightarrow

$$V_{DS2} > V_{GS2} - V_{T2}$$

Since $V_{S2} = V_{S1} = 0 \rightarrow$

$$V_{D2} > V_{G2} - V_{T2}$$

and since $V_S = V_{D2}$,

$$V_S^{\min} = V_{G2} - V_{T2} = V_{G1} - V_{\pi}$$

put V_S^{\min} in $V_G = V_{GS} + V_{G1} - V_{T1}$

$$V_G = V_{GS} + V_{G1} - V_{T1}$$

for M_{amp} : $V_{GS} = \sqrt{\frac{I}{k}} + V_T$

$$V_{GS1} = V_{G1} = V_{DD} - IR$$

$$V_G = \sqrt{\frac{I}{k}} + V_{T_{amp}} + V_{DD} - IR - V_{T1}$$

$$\hookrightarrow \text{and } V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

This is the min value of V_G

we need to maintain

R_1 and R_2 are input impedance
and hence for the opamp, R_1 and $R_2 \gg \infty$
to prevent signal loss

R_1, R_2 : as high as possible

now what about $R_D = ?$

$M_{amp} \equiv$ Should be in SATURATION

$$V_{DS} > V_{GS} - V_T$$

i.e. V_D should ↑

$$\text{and } V_D = V_{DD} - I_D R_D$$

so, R_D should be less

$$V_S^{\min} > V_{G1} - V_{T1}$$

$$V_D - V_S > \underbrace{V_{GS} - V_T}_{M_{amp}}$$

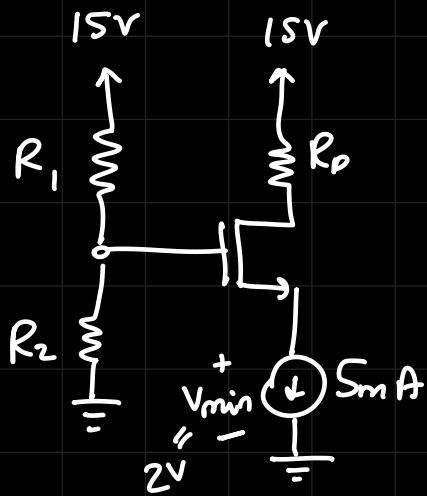
$$V_{DD} - I_D R_D - V_{S1} > V_{GS} - V_T$$

$$R_D < \frac{V_{DD} - V_S - V_{GS} + V_T}{I_D}$$

for $I_D = I$ (current mirror)

$$R_D < \frac{V_{DD} - V_G + V_T}{I}$$

$\wp \}$



$$K = 0.2 \times 10^{-3}$$

$$V_T = 1V$$

$$V_{GS} = \sqrt{\frac{I}{K}} + V_T$$

$$I_d = k(V_{GS} - V_T)^2$$

$$V_{GS} = \sqrt{\frac{S}{0.2}} + 1 = \underline{6V}$$

$$V_S^{\min} = 2V$$

$$V_G = \underline{8V}$$

$$V_G = IS \times \frac{R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = \frac{8}{15}$$

$$SR_1 + SR_2 = ISR_2$$

$$SR_1 = 7R_2$$

lets choose $R_i = 7M\Omega \rightarrow R_o = 8M\Omega$

$$R_D \leq \frac{V_{DD} - V_G - V_T}{I_D} = \frac{15 - 8 + 1}{5} k\Omega$$
$$= \frac{8}{5} k\Omega = 1.6 k\Omega$$

$$R_D \leq 1.6 k\Omega$$

check if Amp \rightarrow saturation mode

$$V_{DS} > V_{GS} - V_T$$

$$-15 + 8 + V_{DS} + 2 = 0$$

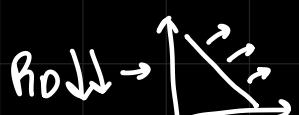
$$V_{DS} = 5V$$

$$V_D = 7V$$

$S > 6 - 1 \checkmark$ but just at the edge of saturation
for $R_D = 1.6 k\Omega$

Choosing $R_D = 1k\Omega$ would be more suited.

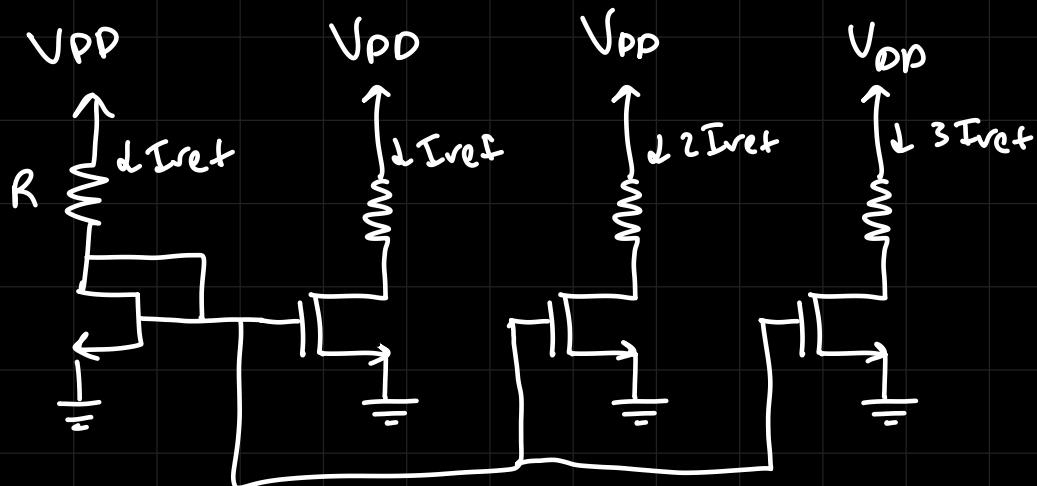
$\Rightarrow R_D$ will change the slope of the load line



slope: $\frac{1}{R_D}$

Current steering circuit

Create multiple I sources from a single reference current.



The current mirror circuit ensures V_{GS} to be same as reference branch so that same ref current flows through each identical branch (mosFETs)

$$V_{GS}^{ref} = V_{GS1} = V_{GS2} = \dots$$

if mos are identical,

$$K_{ref} = K_1 = K_2 = \dots$$

$$\text{and } V_T^{ref} = V_{T1} = V_{T2} = \dots$$

now if i want scaled ref current for diff branches,
eg: for n^{th} branch $\rightarrow I_{dn} = K_n (V_{GSn} - V_{Th})^2$

We know $I_D = k_{ref}(V_{GS}^{ref} - V_T)$

if $k_{ref} \neq k_n$, $\frac{I_{Dn}}{I_D} = \frac{k_n}{k_{ref}} \frac{(V_{GSn} - V_T)^2}{(V_{GSt} - V_T)^2}$

↑
scalar factor

$$I_{Dn} = \frac{k_n}{k_{ref}} I_D$$

current steering

$$I_{D1} = 25\mu A$$

$$I_{D2} = 50\mu A$$

$$I_{D3} = 125\mu A$$

$$I_{D4} = 25\mu A = I_{DS}$$

$$V_{GS1} = \sqrt{\frac{I}{k}} + V_T = \sqrt{\frac{25\mu}{5 \times 50\mu}} + 1$$

$$R = \frac{V_{G4} - V_{G1}}{I_{ref}}$$

PMOS: m_1

$$V_{SD} = V_s - V_D$$

$$V_A = V_D = S - V_{SD} = S - V_{SG} = S + V_{GS}^P$$

$$\text{for } M_1 : V_{DS} = V_D - V_S$$

$$V_{DS} = V_D + S$$

$$V_{GS} = V_D + S$$

$$V_B = V_D = V_{GS} - S$$

$$R = \frac{V_A - V_B}{I_{ref}} = \frac{V_{GS} + S + S - V_{GS}^p}{2S\mu A}$$

$$\text{for } M_2 \rightarrow I_{D2} = \frac{1}{2} \mu_p C_{ox} \left(\frac{\omega}{L} \right) (V_T - V_{GS})^2$$

$$\text{for } M_1 \rightarrow I_{D1} = \frac{1}{2} \mu_p C_{ox} \left(\frac{\omega}{L} \right) (V_{GS} - V_r)^2$$

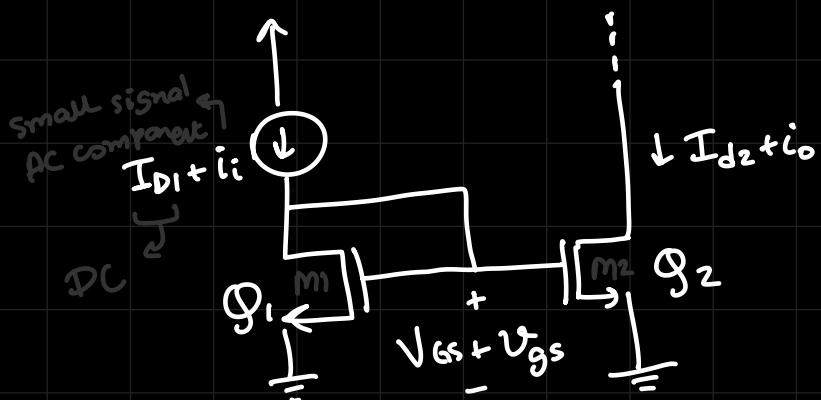
$$(V_{GS}^p + 1)^2 = \frac{2S\mu \times 2}{20\mu \times S}$$

Lecture 17

⇒ Current mirror as current amplifier

low input resistance

higher output resistance wrt R_L

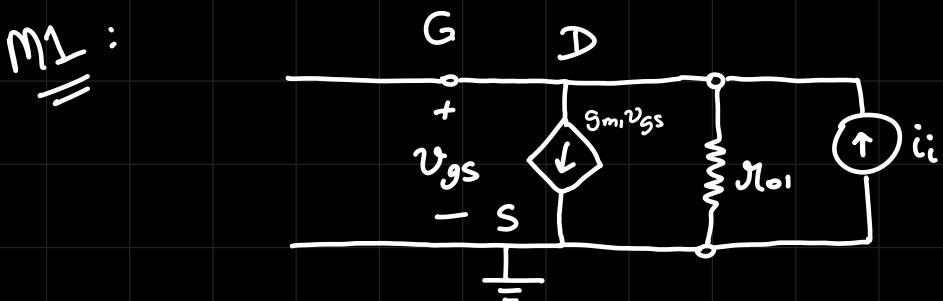


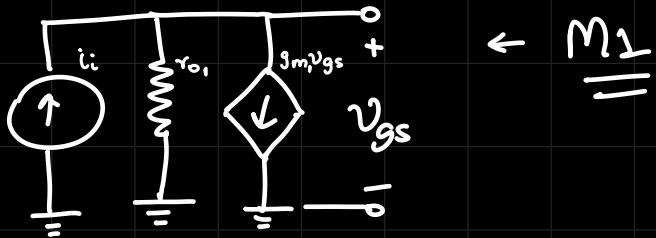
M₂ needs to be in saturation
for current mirror

$$V_{DS2} > V_{GS2} - V_{T2}$$

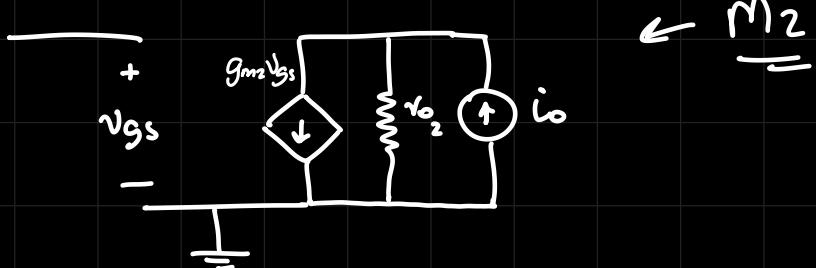
AC analysis

↪ small signal model (π)



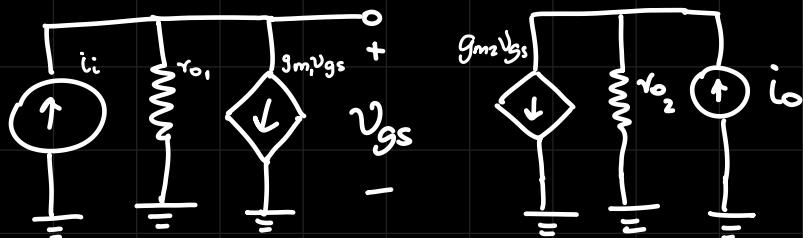


$\leftarrow M_1$

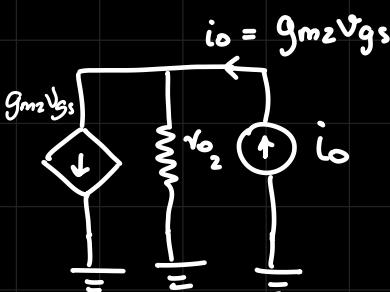
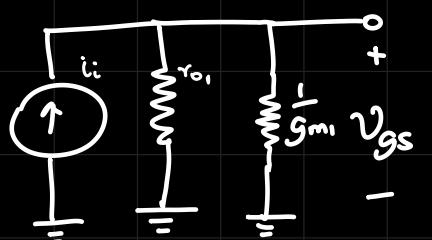


$\leftarrow M_2$

combined circuit :



dep I src \rightarrow resistor of $R = \frac{1}{g_m}$



: we don't want current to flow through r_{o2} hence r_{o2} should be very high so that I flows through load

$$Z_{in} = r_{o1} \parallel \frac{1}{g_m} \approx \frac{1}{g_m} ; Z_o = r_{o2}$$

inverse of Vamp

$$\text{Current gain: } A_i = \frac{i_o}{i_i} \Big|_{\text{OpR} \ll \gamma_{o2}} = \frac{g_{m2} v_{gs}}{i_i}$$

$$\text{and } v_{gs} = i_i \cdot R_{in} \approx i_i \cdot \frac{1}{g_{m1}}$$

$$\text{Assumption: } \frac{1}{g_{m1}} \gg \gamma_{o1} \quad \leftarrow$$

$$A_i \approx \frac{g_{m2} i_i / g_{m1}}{i_i} \approx \boxed{\frac{g_{m2}}{g_{m1}}} \leftarrow \begin{matrix} \text{current} \\ \text{gain} \end{matrix}$$

Note: we need gain ↑ and
hence we neglected M1's
early effect resistance
in our assumption
i.e. $\gamma_{o1} \rightarrow \infty$

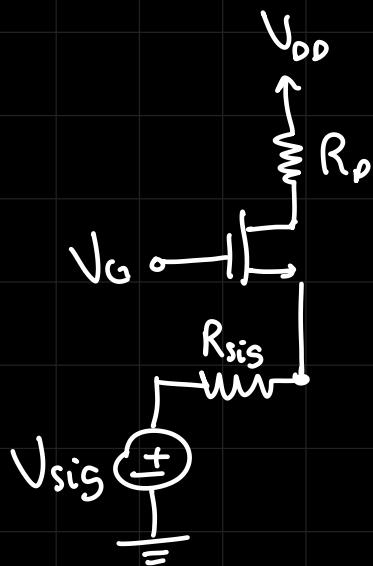
$$g_{m2} = 2K_2 (V_{GS2} - V_{T2})$$

$$g_{m1} = 2K_1 (V_{GS1} - V_{T1})$$

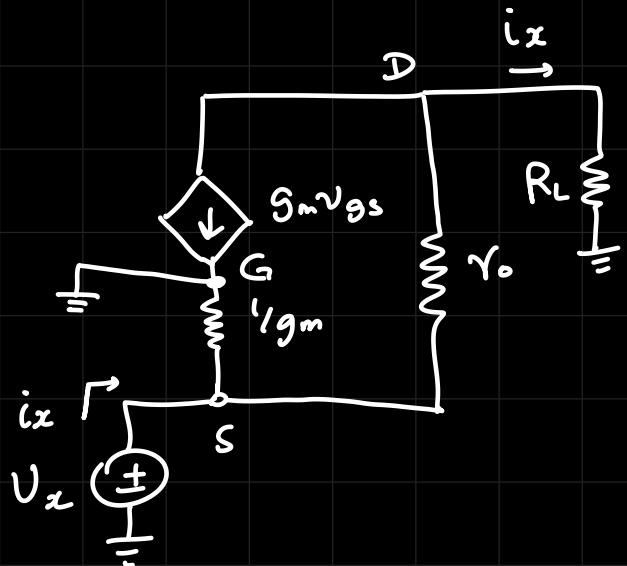
$$K_1 = \frac{1}{2} \mu_1 C_{ox} \left(\frac{W}{L} \right)_1, \quad K_2 = \frac{1}{2} \mu_2 C_{ox} \left(\frac{W}{L} \right)_2$$

COMMON GATE

we want to distribute the gain
over multiple amps to prevent clipping of input.



T model



$$I_{ro} = g_m v_{gs} + i_x$$

$$I_{RL} = i_x$$

$$-V_x + I_{ro} r_o + i_x R_L = 0$$

$$V_x = i_x (r_o + R_L) + g_m v_{gs} r_o$$

$$\text{note: } V_s = -V_{gs} = V_x$$

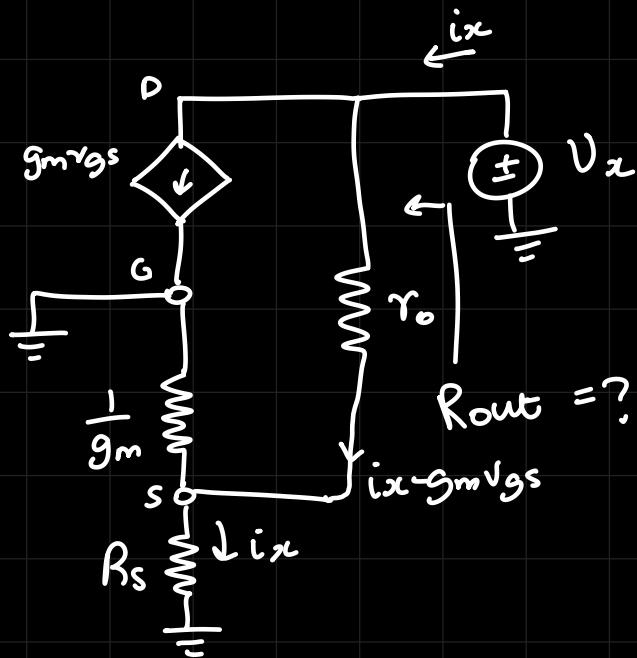
$$V_x (1 + g_m r_o) = i_x (R_L + r_o)$$

$$R_{in} = \frac{V_x}{i_x} = \frac{R_L + r_o}{1 + g_m r_o} \approx \frac{R_L}{g_m r_o} + \frac{1}{g_m} \quad \left\{ \text{assuming } g_m r_o \gg 1 \right\}$$

* \Rightarrow Even if $R_L \uparrow\uparrow$, R_{in} scales down R_L by $g_m r_o$ and prohibits the rise of R_{in} significantly.

and hence low input resistance achieved for current amp / buffer.

Now finding out output resistance



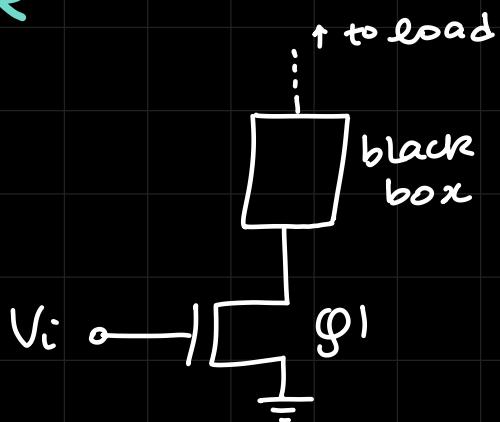
$$V_{GS} = -V_S = -i_x R_s$$

$$V_x = (i_x - g_m V_{GS}) r_o + i_x R_s = (i_x + g_m i_x R_s) r_o + i_x R_s$$

$$R_{out} = r_o + g_m R_s r_o + R_s = r_o + R_s (1 + g_m r_o)$$

The output resistance will be high : $R_{out} = R_s g_m r_o$

CASCODE AMPLIFIER



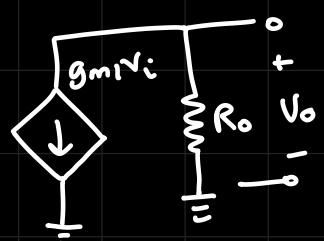
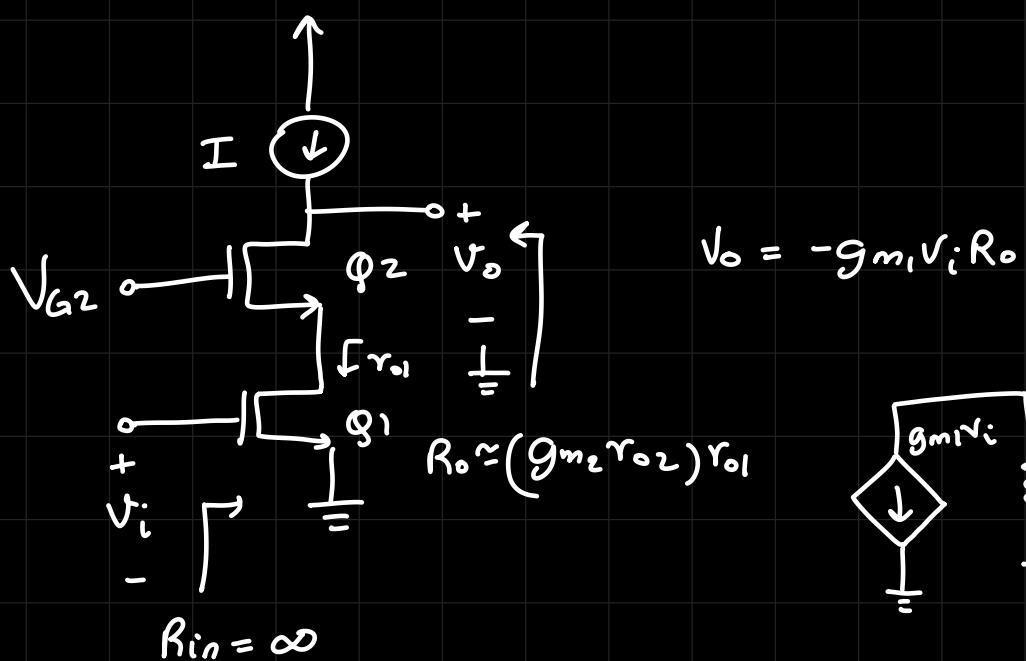
The black box can be a common gate transistor so that ...

- ① Input impedance is not high and $\text{out } R_L, \text{ Rin scales by } \frac{R_L}{g_m r_o}$

- ② Output impedance is very high.

$$R_{\text{out}} = R_s g_m r_o$$

- ③ Current gain = 1



for the CG config,

$$R_o = g_{m2} r_{o2} R_s : \text{derived earlier}$$

$R_s = r_{o1}$ because \emptyset_1 is the SRC for \emptyset_2

$$\text{So, } R_o = g_{m2} g_{m2} r_{o1}$$

$$A_v = -g_{m1} R_o = -g_{m1} g_{m2} r_{o2} r_{o1}$$

$$= -g_{m1} r_{o1} g_{m2} r_{o2}$$

Let $g_{m1} = g_{m2} = g_m$ and $r_o = r_{o1} = r_{o2}$

$$A_v = -(g_m r_{o2})^2 = -A_{v0}^2$$

where $A_{v0} = \text{volt gain of regular CS transistor}$

TRADEOFFS:

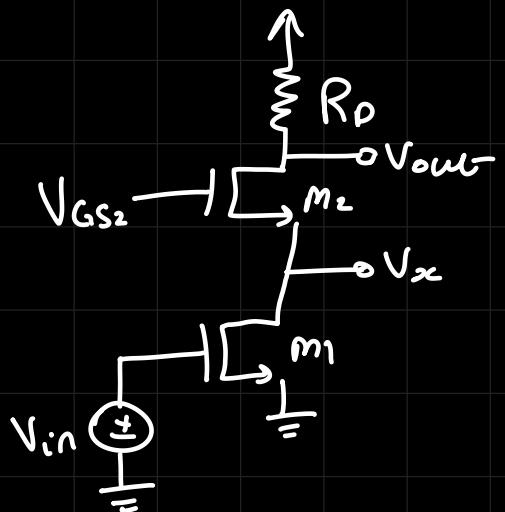
for $m1$: saturation,

$$V_x > V_{in} - V_{t1}$$

$$V_{GS2} = V_{G2} - V_{S2}$$

$$V_{S2} = V_{G2} - V_{GS2}$$

$$V_x = V_{S2} = V_{G2} - V_{GS2} > V_{in} - V_{t1}$$



for M2 : saturation \rightarrow

$$V_{DS2} > V_{GS2} - V_{T2}$$

$$V_{D2} - V_{S2} > V_{GS2} - V_{T2}$$

$$V_{out} - V_x > V_{GS2} - V_{T2}$$

$$V_{out} > V_{GS2} - V_{T2} + V_x$$

$$\text{and } V_x > V_{in} - V_{T1}$$

$$\text{but } V_x = V_{in} - V_{T1}$$

$$V_{out} \geq \underbrace{V_{GS2} - V_{T2}}_{V_{ov_2}} + \underbrace{V_{in} - V_{T1}}_{V_{ov_1}}$$

$$\underbrace{\quad\quad\quad}_{V_{ov}}$$

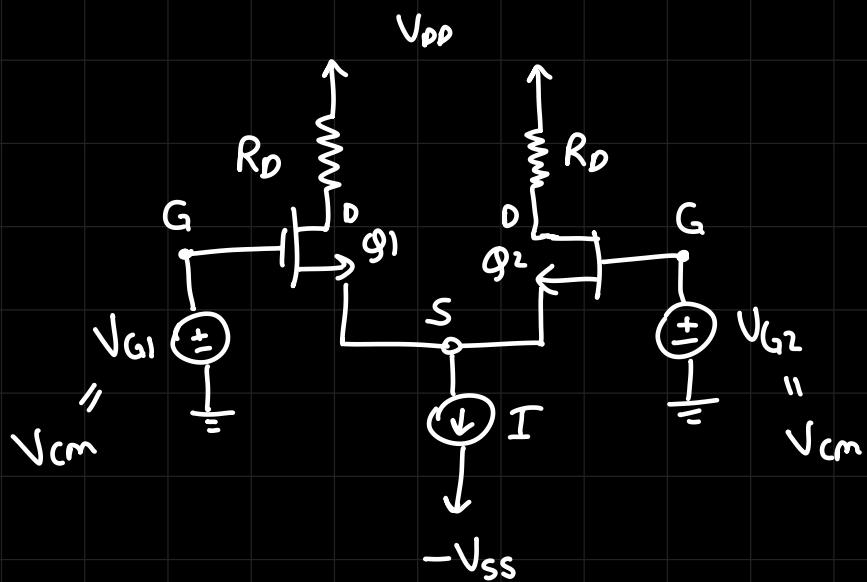
overdrive voltages

increasing more mosfets in cascode, will
keep on increasing V_{out} depending on V_{ovs}
which might distort the output signal
when $V_{out} < V_{ov_1} + V_{ov_2} + \dots$

HORIZONTALLY INCREASING: gain \uparrow , $\&$ stable ✓
VERTICALLY INCREASING : gain \uparrow , distortion \uparrow

→ Differential Amplifier

SNR: Signal to Noise Ratio
(maximize it)



Obj: to find the differential o/p given that some value of V_{G1}, V_{G2}
= V_{cm}

Q_1 and Q_2 are in saturation

←
common mode voltage

V_{cm} is the voltage applied at the 2 gate terminals V_{G1}, V_{G2}

Since Q_1, Q_2 are matched, they both will conduct a current I' i.e. $I_{D1} = I_{D2} = I'$ and since $I_{D1} + I_{D2} = I$ so $\boxed{I' = I/2}$

Biased by the current source I

$$V_s = ? \quad V_{GS} = V_G - V_S = V_{CM} - V_S$$

$$V_S = V_{CM} - V_{GS}$$

$$\text{but } K = \frac{1}{2} \mu_n C_o x \frac{\omega}{L}$$

$$\text{for } Q_1 \rightarrow \frac{I}{2} = \frac{1}{2} K_n \left(\frac{\omega}{L} \right) (V_{GS} - V_T)^2$$

$$\xrightarrow{\text{Mn Cox}} \mu_n C_o x$$

$$\text{we know } V_{GS} - V_T = V_{ov}$$

$$I = K_n \left(\frac{\omega}{L} \right) V_{ov}^2$$

$$V_{ov} = \sqrt{\frac{I}{K_n (\omega/L)}} \quad \text{--- (1)}$$

To find the output voltage i.e. differential
in nature $\rightarrow V_o = V_{D2} - V_{D1}$

$$V_{D1} = V_{DD} - \frac{I}{2} R_D = V_{D2}$$

$$V_o = 0$$

Range over which V_{CM} will give a valid
outcome for $V_o = 0$?

Note: Q_1 and Q_2 must remain in saturation



$$V_{DS} > V_{GS} - V_T \quad \downarrow \\ V_D > V_G - V_T$$

$$V_{DD} - \frac{I}{2} R_D > V_{cm} - V_T$$

$$V_{cm} < V_T + V_{DD} - \frac{I}{2} R_D$$

$$\boxed{V_{cm}^{max} = V_T + V_{DD} - \frac{I}{2} R_D}$$

② for the current SRC to give current bias,
we need some potential $\approx V_{CS}$

$$V_S - (-V_{SS}) > V_{CS}$$

$$V_S = V_{cm} - V_{GS}$$

$$V_{cm} - V_{GS} + V_{SS} > V_{CS}$$

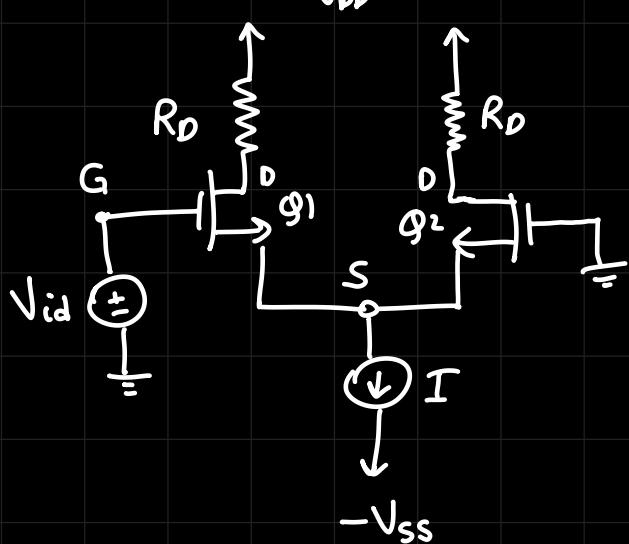
$$V_{cm} > V_{CS} + V_{GS} - V_{SS}$$

$$\text{we know, } V_{GS} = \underbrace{V_{GS} - V_T + V_T}_{\downarrow} \\ V_{ov}$$

$$V_{cm} > V_{CS} + V_{ov} + V_T - V_{SS}$$

So, range of V_{cm} :

$$V_{CS} + V_{ov} + V_T - V_{SS} < V_{cm} < V_T + V_{DD} - \frac{I}{2} R_D$$



for V_{id}^{max} , current will flow through Q_1 , only and through Q_2 for V_{id}^{min}

so, now find range for V_{id}
such that: $V_{id}^{min} \leq V_{id} \leq V_{id}^{max}$

$V_{id} \Rightarrow$ potential at which the bias current (I) will flow through Q_1 and no current will flow through Q_2 .

$$\text{for } Q_1: I = \frac{1}{2} R_n (\frac{\omega}{L})_{Q_1} (V_{GS1} - V_T)^2$$

$$V_{GS1} = V_T + \sqrt{\frac{2I}{R_n (\omega)_L} Q_1} =$$

$$\text{from ①: } V_{or} = \sqrt{\frac{I}{R_n (\omega)_L} Q_1}$$

$$V_{GS1} = V_T + \sqrt{2} V_{or} \quad \text{--- ②}$$

for Q_2 : $I = 0$

$$0 = k(V_{GS2} - V_T)^2$$

$$\rightarrow V_{GS2} = V_T$$

$$V_{G2}^{\rightarrow} - V_{S2} = V_T$$

$$-V_{S2} = -V_S = V_T$$

$$V_S = -V_T \quad \text{--- (3)}$$

from (2), (3)

$$V_{GS1} = V_T + \sqrt{2}V_{ov}$$

$$V_{G1} + V_T = V_T + \sqrt{2}V_{ov}$$

$$V_{G1} = \sqrt{2}V_{ov}$$

so, $V_{id}^{max} = \sqrt{2}V_{ov}$

for V_{id}^{min} : for $Q_1 \rightarrow I = 0$

$$V_{GS1} = V_T \rightarrow V_{G1} - V_T = V_S \quad (4)$$

for $Q_2 \rightarrow I = \frac{1}{2}K_n \frac{\omega}{L} (V_{GS2} - V_T)^2$

$$V_{GS2} = V_T + \sqrt{\frac{2I}{K_n(\omega)_L}} =$$

$$-V_S = V_T + \sqrt{\frac{2I}{k_n(\omega_L)Q_2}}$$

$$-V_S = V_T + \sqrt{2}V_{ov}$$

$$V_S = -\sqrt{2}V_{ov} - V_T$$

$$V_{G1} - V_T = -\sqrt{2}V_{ov} - V_T \quad \text{from ①}$$

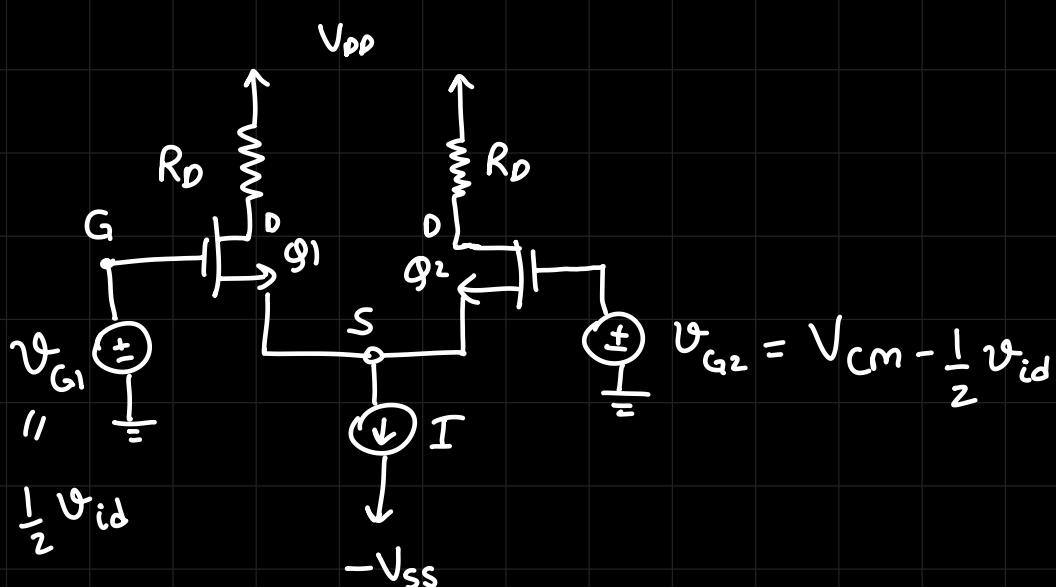
$$V_{G1} = -\sqrt{2}V_{ov}$$

$$V_{id}^{\min} = -\sqrt{2}V_{ov}$$

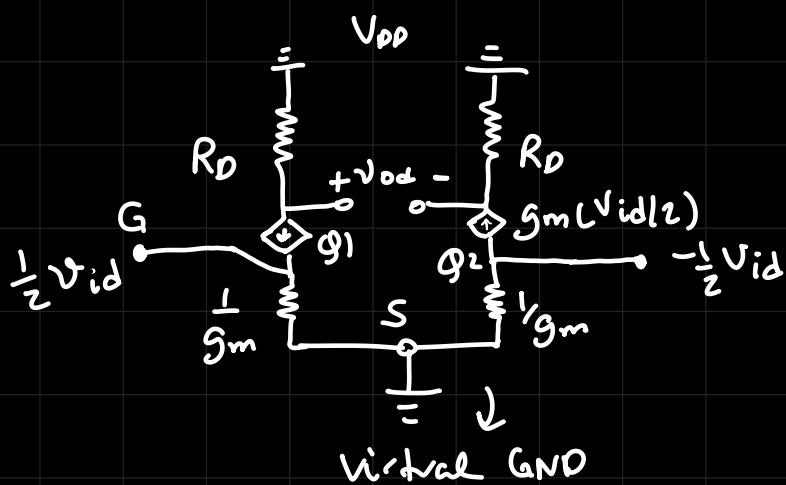
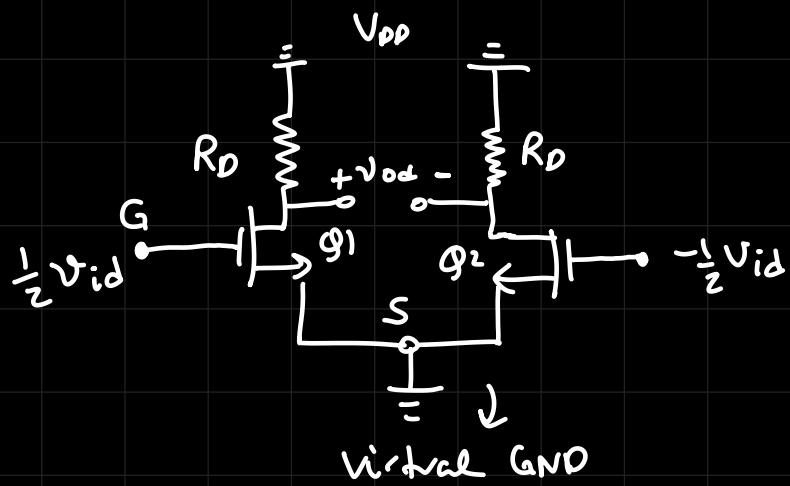
So, range for V_{id} :

$$-\sqrt{2}V_{ov} < V_{id} < \sqrt{2}V_{ov}$$

assuming Q_1 and Q_2 are in saturation



AC analysis → Remove DC SRC



$$I_D = g_m \frac{V_{id}}{2}$$

70% project

Filter

V amp

P amp

Aux out

$$V_{o1} = g_m \frac{V_{id}}{2} R_D$$

$$A_{v1} = \frac{V_{o1}}{V_{id}} = -\frac{1}{2} g_m R_D \quad \} \text{ 1st branch}$$

$$A_{v2} = \frac{V_{o2}}{V_{id}} = \frac{1}{2} g_m R_D \quad \} \text{ 2nd branch}$$

$$A_D = \frac{V_o}{V_{id}} = \frac{V_{o2} - V_{o1}}{V_{id}} = \frac{g_m R_D}{V_{id}} \quad \} \text{ Differential gain}$$

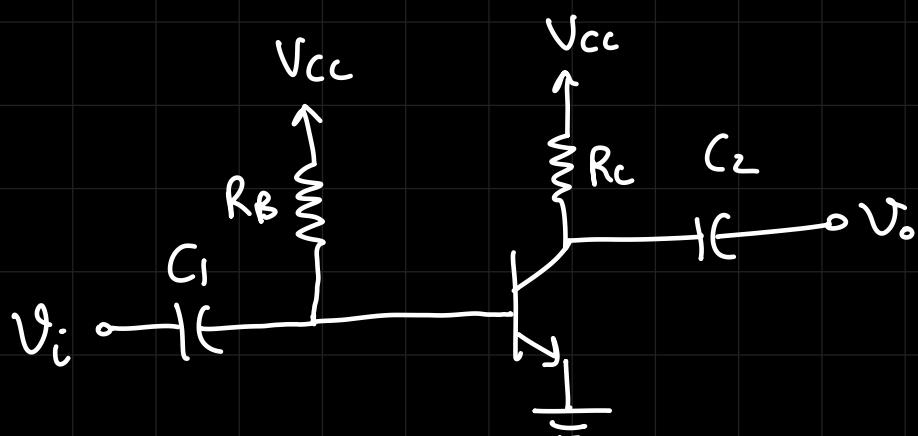
↳ double of that of individual branch gain

POWER Amplifier

1. CLASS A Power Amplifier / Direct coupled Power Amp
2. CLASS A Power Amplifier - Transformer Coupled
3. CLASS B Amplifier - Push Pull Amplifier
4. CLASS C Amplifier

CLASS A Amp / Direct coupled amplifier

it is called direct coupled amplifier because the input and output AC voltage is directly coupled to the Transistor (BJT/MOS)



C_1 and C_2 are coupling capacitors
for DC analysis, all the caps \rightarrow ∞

$$V_{CC} = V_{CE} + I_C R_C$$

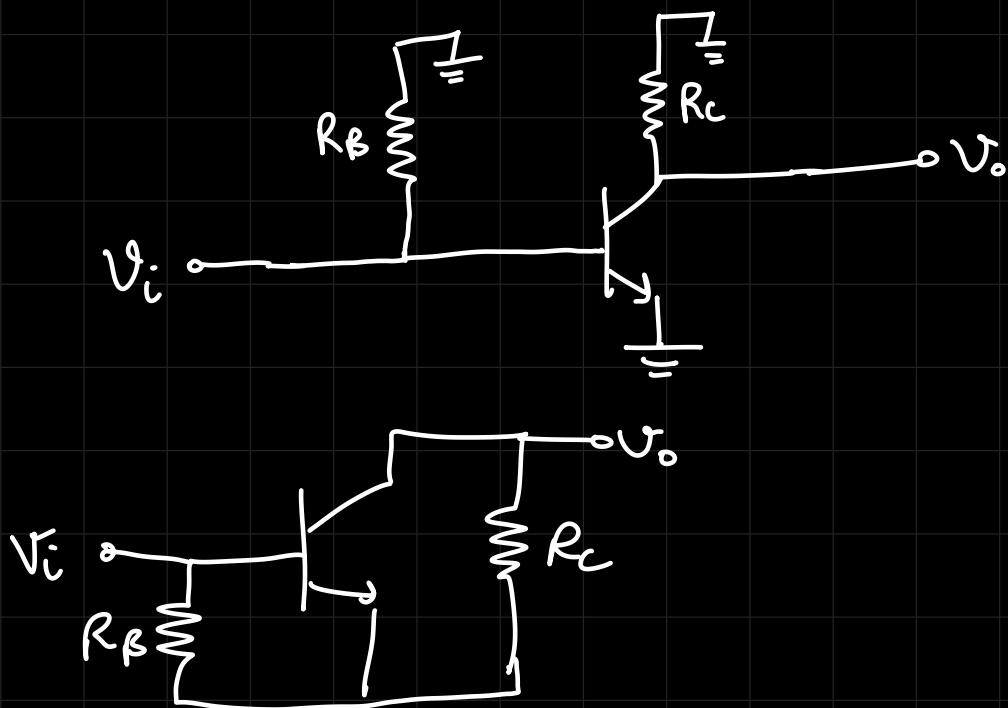
DC — $I_C = -\frac{1}{R_C} V_{CE} + \frac{1}{R_C} V_{CC}$ $\varnothing(V_{CE}, I_C)$

load line

$$I_C = 0 \rightarrow V_{CE} = V_{CC}$$

$$V_{CE} = 0 \rightarrow I_C = \frac{1}{R_C} V_{CC}$$

AC analysis:



$$-V_{CE} - i_C R_C = 0$$

$$i_C = -\frac{1}{R_C} \cdot V_{CE}$$

↳ slope

Note: we get the same slope for
 i_C vs V_{CE} and I_{CG} vs V_{CE}

(pure AC)

(pure DC)

$$i_C = i_C - I_{CG}$$

$$V_{CE} = V_{CE} - V_{CE}$$

$$i_C = -\frac{1}{R_L} V_{CE}$$

$$i_C - I_{CQ} = \frac{-1}{R_L} (V_{CE} - V_{CE,Q}) \quad - \textcircled{3}$$

$$(y - y_1) = m(x - x_1)$$

We observe that the φ point remains same for both, the AC case & the DC case

2x BJT/mosfet
cascade/cascode
CMOS
Power Amp
current mirror
Differential Amplifier

Eqn 3 is a generate straight line of slope $-\frac{1}{R_L}$ and is passing through the

φ point (V_{CE}, I_C)

Since the DC and AC load line same slope and both pass through the same point

$$\text{efficiency} : \eta = \frac{P_{dc}}{P_{ac}} \times 100$$

$$P_{dc} = V_{ce} \times I_{cq}$$

$$P_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$= \frac{V_m I_m}{2}$$

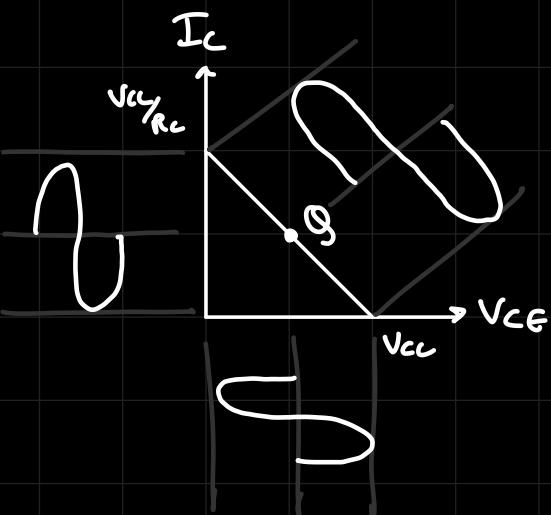
$$V_m = \frac{V_{max} - V_{min}}{2} = \frac{V_{cc} - 0}{2} = \frac{V_{cc}}{2}$$

$$I_m = \frac{I_{max} - I_{min}}{2} = \frac{2I_{cq} - 0}{2} = I_{cq}$$

$$\eta = \frac{\frac{1}{2} \times \frac{V_{cc}}{2} \times I_{cq}}{V_{cc} I_{cq}} = \frac{1}{4} = \boxed{25\%}$$

for class

A amplifier

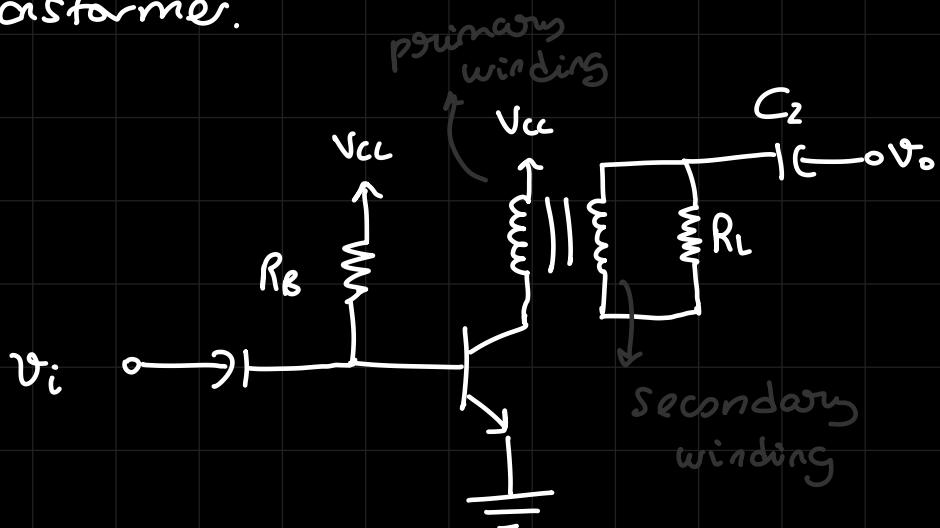


conduction angle : 360°

full swings

CLASS-A / TRANSFORMER COUPLED AMP

In this power amplifier the load is connected to the output node of the amplifier through a transformer.



for DC analysis, all caps \rightarrow OC

$$X_L = \omega L \approx \\ = 2\pi f L \approx$$

for DC $\rightarrow X_L = 0 \Omega$

KVL: $V_{cc} = I_c X_L + V_{CE}$

$$= I_c(0) + V_{CE}$$

$$\underline{V_{cc} = V_{CE}}$$
 equation of line parallel to Y axis

∞ slope

$$\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{N_1}{N_2} = n \quad \rightarrow \quad \frac{V_1}{V_2} \times \frac{I_2}{I_1} = n^2$$

$$\frac{V_1/I_1}{V_2/I_2} = n^2$$



$$\frac{V_2}{I_2} = R_L \rightarrow \frac{V_1/I_1}{R_L} = n^2$$

$$\text{let } \frac{V_1/I_1}{R_L} = R'_L$$

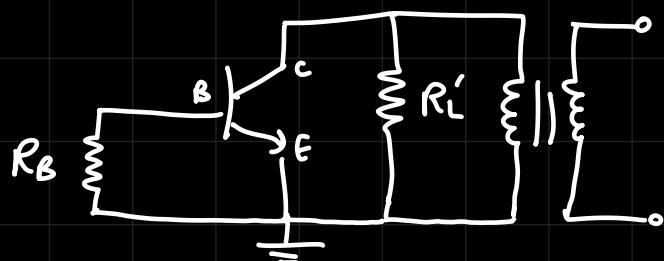
$$\text{So, } \frac{R'_L}{J} = n^2 \cdot R_L$$

reflected load

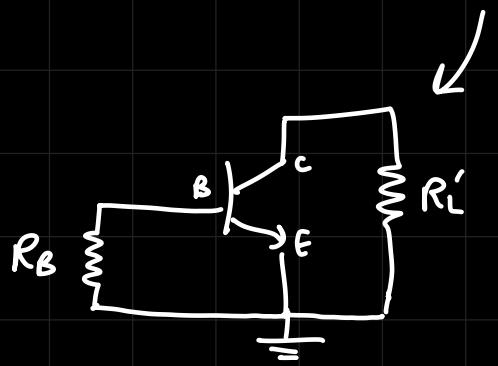
Resistance i.e R'_L is the reflection of R_L in primary winding ; we also replace secondary winding resistance with R'_L in the primary winding.

for AC analysis \rightarrow caps act as short circut and deactivate DC src

AC :



At medium frequencies, the inductive reactance of the primary and secondary winding will be large enough therefore, the resistance can be treated as open circut

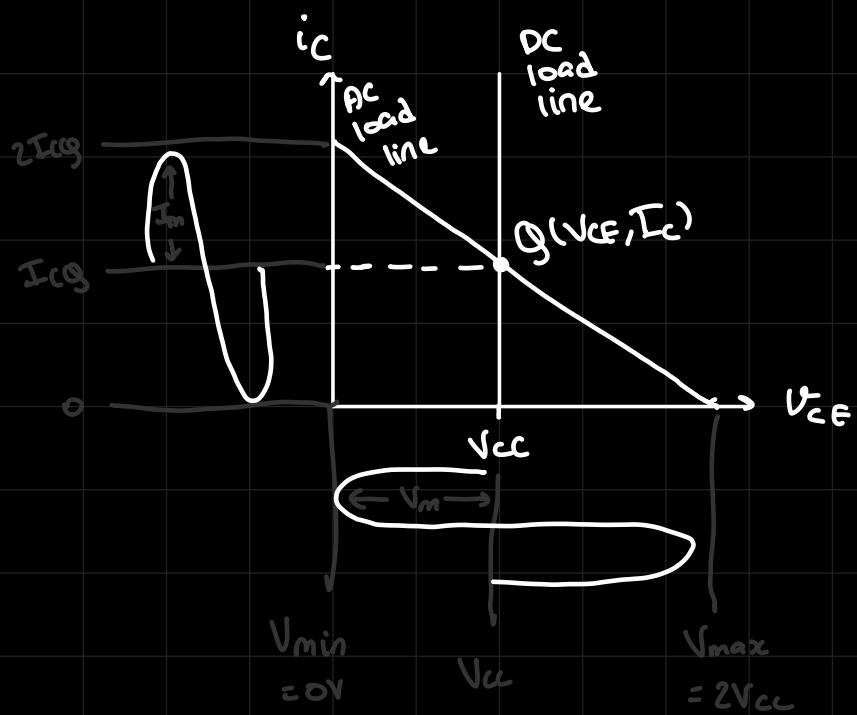


$$KVL: i_C R_L' + V_{CE} = 0$$

$$i_C = -\frac{1}{R_L'} V_{CE}$$

$$(i_C - I_{CG}) = -\frac{1}{R_L'} (V_{CE} - V_{CE,Q})$$

$$y - y_1 = m(x - x_1)$$



$$\eta_{\text{v.}} = \frac{P_{ac}}{P_{dc}} \times 100$$

$$P_{ac} = V_m I_m = \left(\frac{2V_{cc} - 0}{2} \right) \times$$

$$\frac{1}{2} \times \left(\frac{2I_{CG} - 0}{2} \right)$$

$$= V_{cc} \times I_{CG} \times \frac{1}{2}$$

$$P_{dc} = V_{cc} \times I_{CG}$$

conduct ∂v

angle:

360°

full swings

$$\eta = \frac{P_{ac}}{P_{dc}} = \frac{\frac{1}{2} \times V_{cc} \times I_{CG}}{V_{cc} \times I_{CG}} \times 100$$

$$\boxed{\eta = 50\%}$$

→ A class A / transformer coupled amplifier delivers max AC power of 5Watt at 4Ω load resistor. If the op pt is located for max symmetrical swing and the DC supply voltage is 20V (V_{CC}).

- (1) Transformer turn ratio
- (2) peak output current
- (3) op pt
- (4) conversion efficiency

Ans) $P_{AC} = \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}$

$$V_m = I_m R_L'$$

$$I_m = \frac{V_m}{R_L'}$$

$$P_{AC} = \frac{V_m^2}{2R_L'} \rightarrow$$

$$R_L' = n^2 R_L$$

$$n^2 = \frac{R_L'}{4}$$

$$\text{Symmetric} \rightarrow V_m = V_{CC} \rightarrow R_L' = \frac{\frac{2}{2} \times 20}{S} = \underline{40 \Omega}$$

$$n^2 = 10 \Rightarrow n = \sqrt{10} = 3.14 = \underline{\underline{\frac{N_1}{N_2}}}$$

$$(b) I_m = \frac{V_m}{R_L'} = \frac{20}{40} = 0.5A \quad \left| \begin{array}{l} V_{CEQ} = V_{CC} = 20V \\ Q(20V, 0.5A) \end{array} \right.$$

$$P_{dc} = V_{cc} \times I_{cg} = 20 \times 0.5 = 10$$

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100\% = \frac{5}{10} \times 100\% = 50\%$$

Lecture

→ Class B Power amplifier

TRANSFORMER COUPLED PUSH PULL Amp

→ It consists of 2 identical

transformers and 2 identical

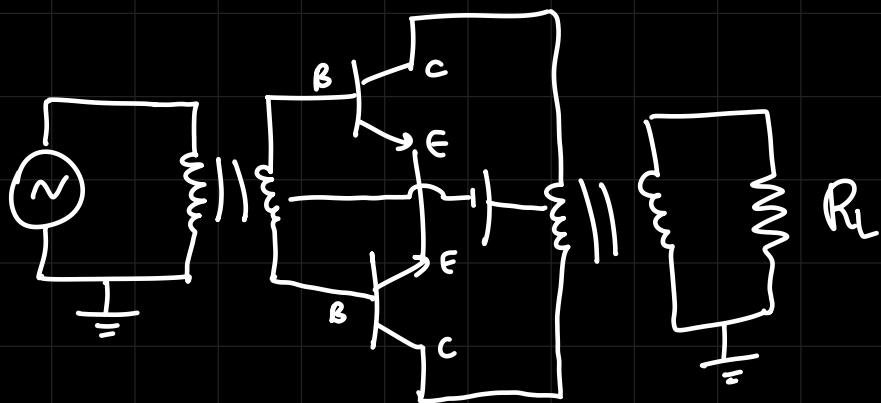
transistors \varnothing_1 and \varnothing_2

→ $\varnothing_1 \rightarrow$ NPN , $\varnothing_2 \rightarrow$ PNP

→ The secondary winding of the

1st transformer and the primary winding

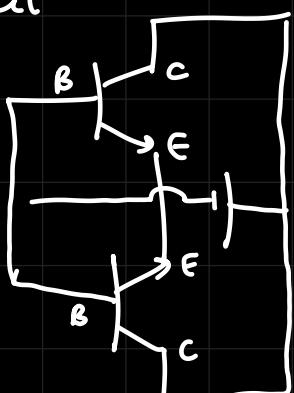
of the 2nd transformer is center tap.



$$DC \rightarrow X_L = 0 \text{ for both}$$

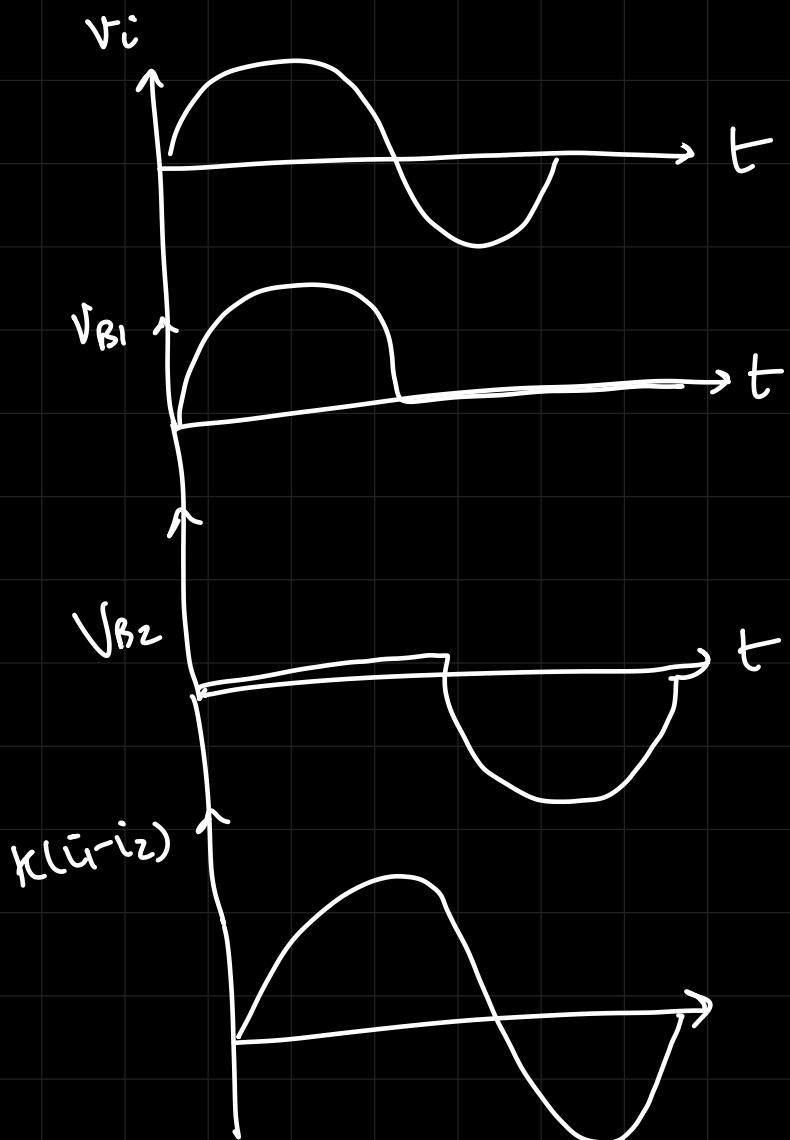
short circuit

$$V_{BE1} - V_{B2} = 0$$

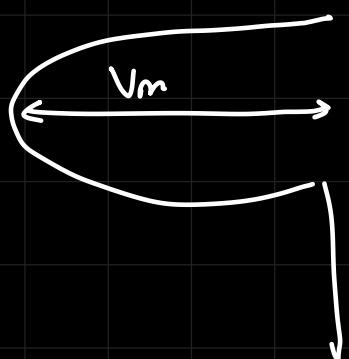
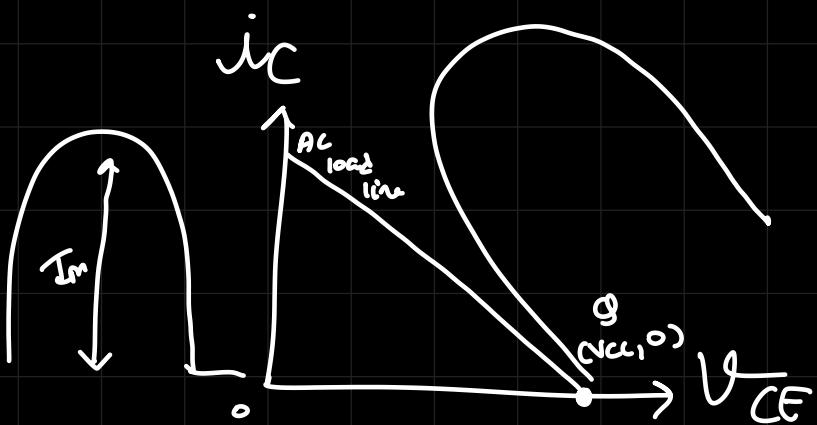


two transistors are used to obtain sinusoidal output. for each transistor, the base terminal are shorted & the emitter wrt DC as shown in the eqⁿ. Therefore, both the transistors remain off / cutoff when no AC input.

When AC input is applied at the Base 1, 2
 $V_{in} \Rightarrow$



Note: DC and AC load line
 Similar as class A transformer coupled amplifier but in class B amplifier operating point will be at extreme end point of the load line.



Conduction angle $\rightarrow 180^\circ$

$$\eta = \frac{P_{ac}}{P_{dc}} \times 100\%$$

$$P_{ac} = V_{rms} \times I_{rms}$$

$$\begin{aligned}
 &= \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}} = \frac{V_{ac} - 0}{\sqrt{2}} \times \frac{I_m - 0}{\sqrt{2}} \\
 &= \frac{V_{cc} \times I_m}{2}
 \end{aligned}$$

$$P_{DC} = V_{OC} I_{DC}$$

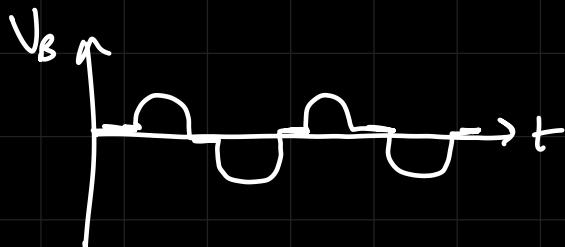
$$I_{avg} = I_{DC} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$$

$$\eta_{\text{v.}} = \frac{1}{2} \frac{V_{CC} \times I_m}{V_{CC} \times 2I_m / \pi} = \frac{\pi}{4} \times 100 = \frac{78.5\%}{\downarrow}$$

ideal
case

DRAWBACK of Class B Amplifier is
CROSS OVER DISTORTION

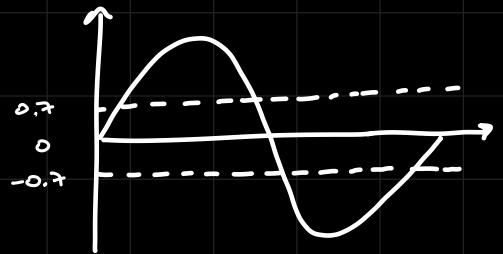
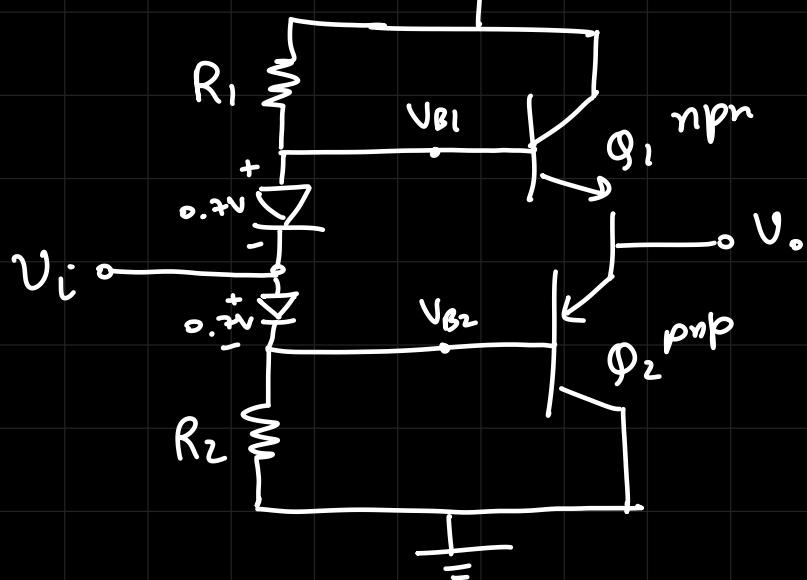
which is over come by class
AB amplifier



CLASS AB amplifier

$V_{CC} > V_D$ \rightarrow cutoff voltage of diode

$$\text{So, } V_{CC} > 1.4$$

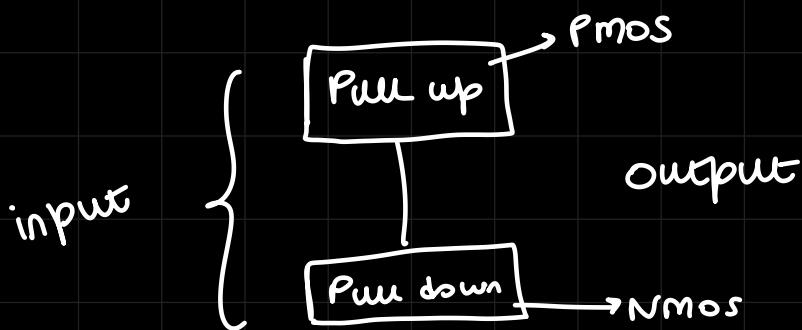


CLASS C Amplifier

will be discussed in Friday's tut

CMOSFET

complementary MOSFET

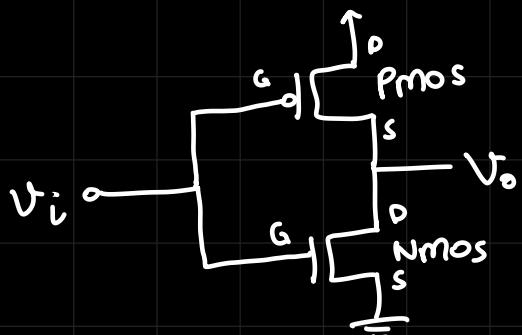


$$\lim_{x \rightarrow 8} \frac{1}{x-8} = \infty$$

$$\lim_{x \rightarrow 5} \frac{1}{x-5} = \text{L}\cap$$

from fig 12.14

with circle \rightarrow PMOS } no need for arrow
w/o circle \rightarrow NMOS



INVERTER

\equiv NOT Gate

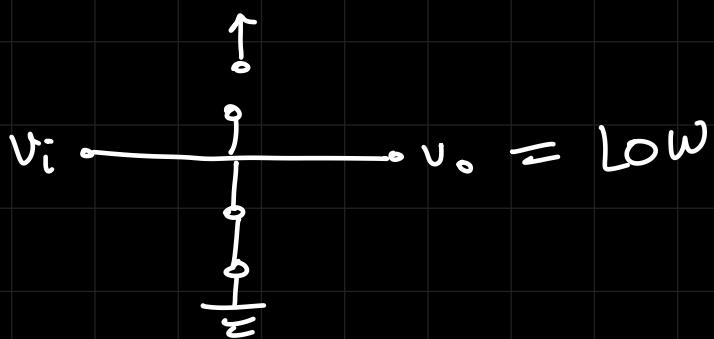
Shunt operation

$$V_i = V_{max}$$

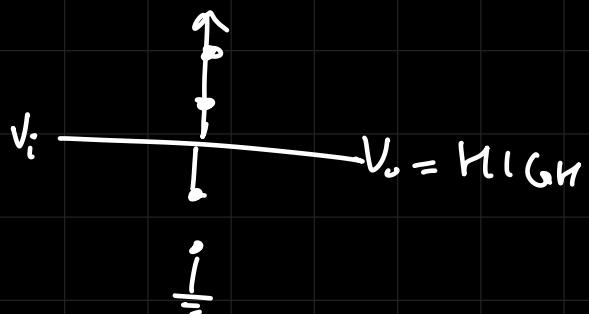
for P channel: PMOS $\rightarrow V_{GS}$: negative $V_{GS} < -V_T$
 n channel: NMOS $\rightarrow V_{GS}$: positive $V_{GS} > V_T$

for $V_i = \text{HIGH}$

$M_1 \rightarrow \text{OFF}, M_2 \rightarrow \text{ON}$



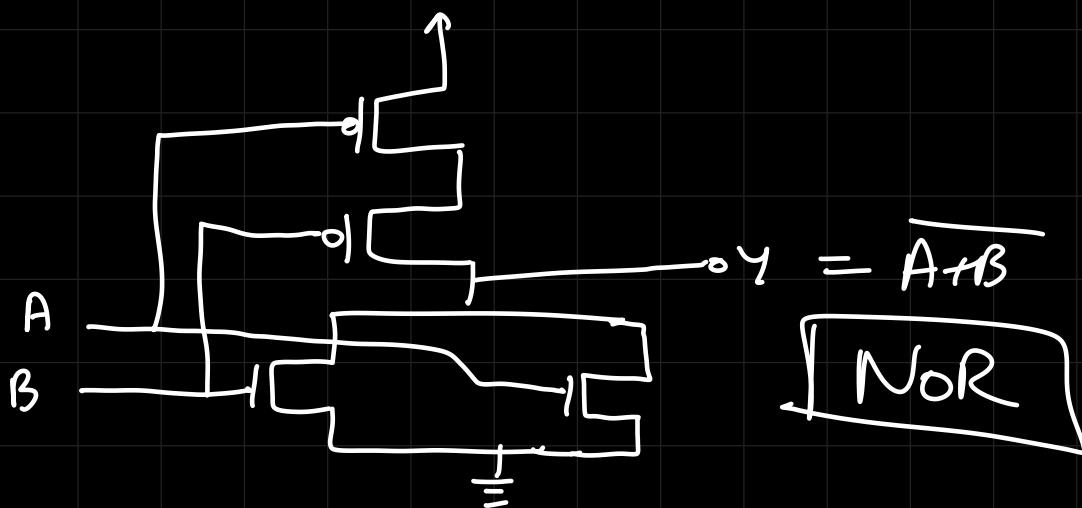
for $V_i = \text{LOW} \rightarrow$



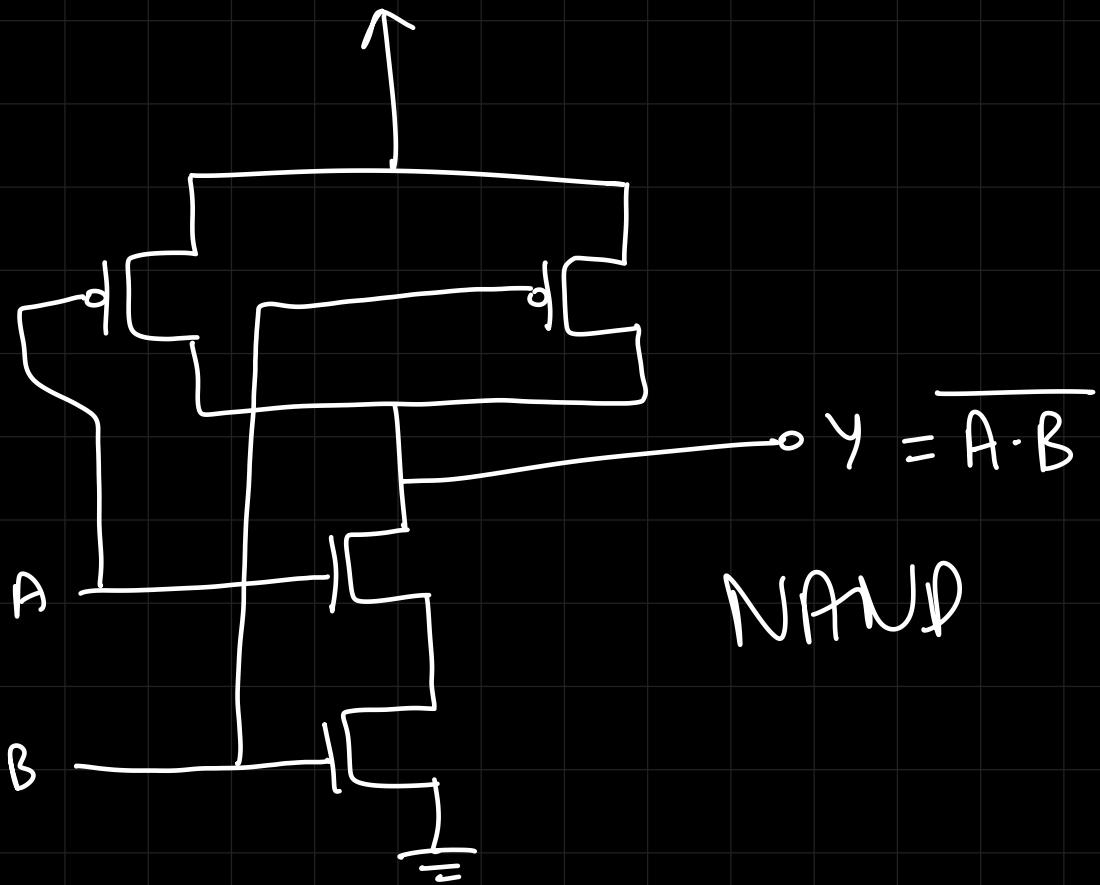
OR gate parallel

if pull down: parallel

↳ pull up: series



AND Gate series



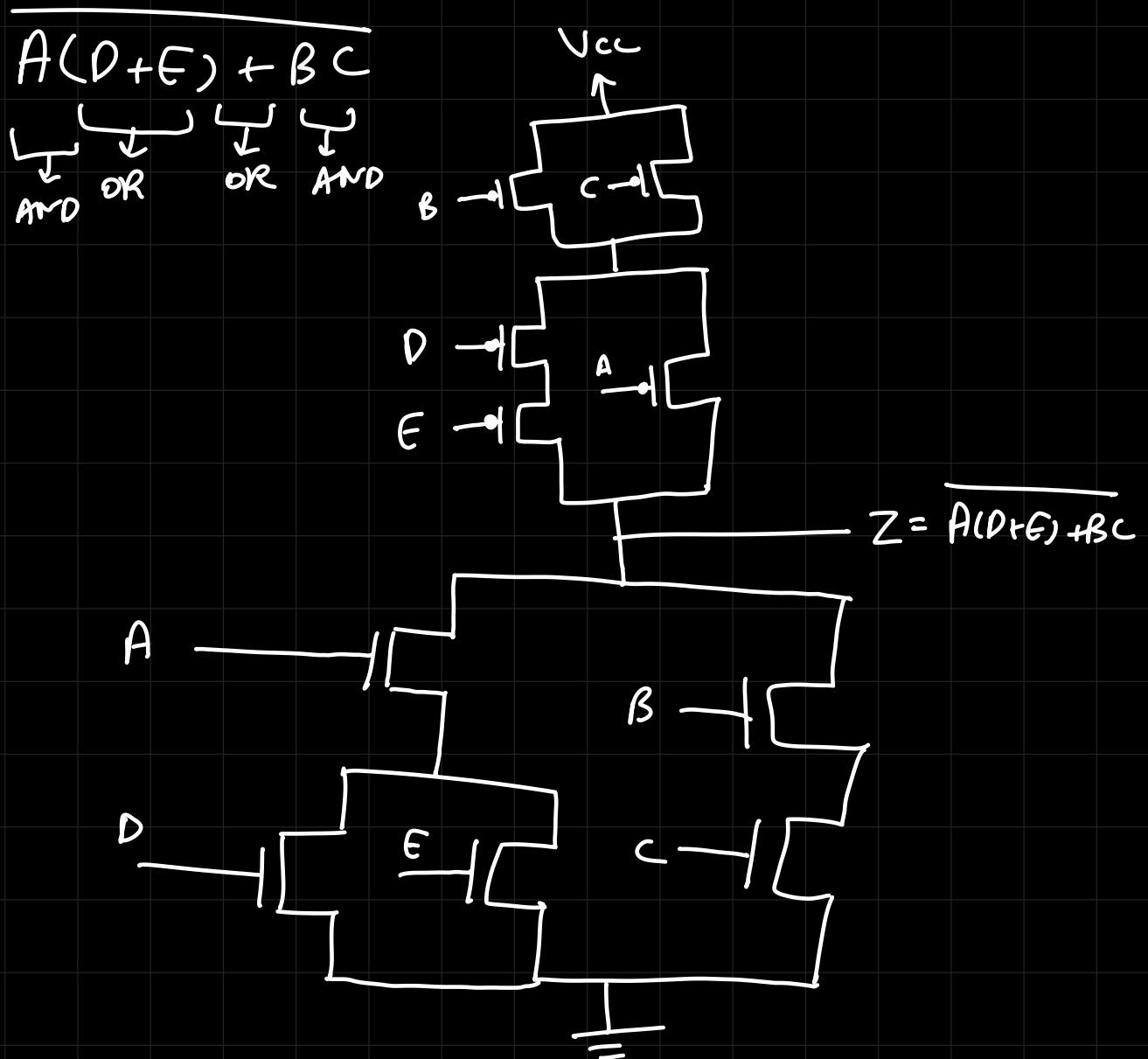
NAND

#Lecture / Tut

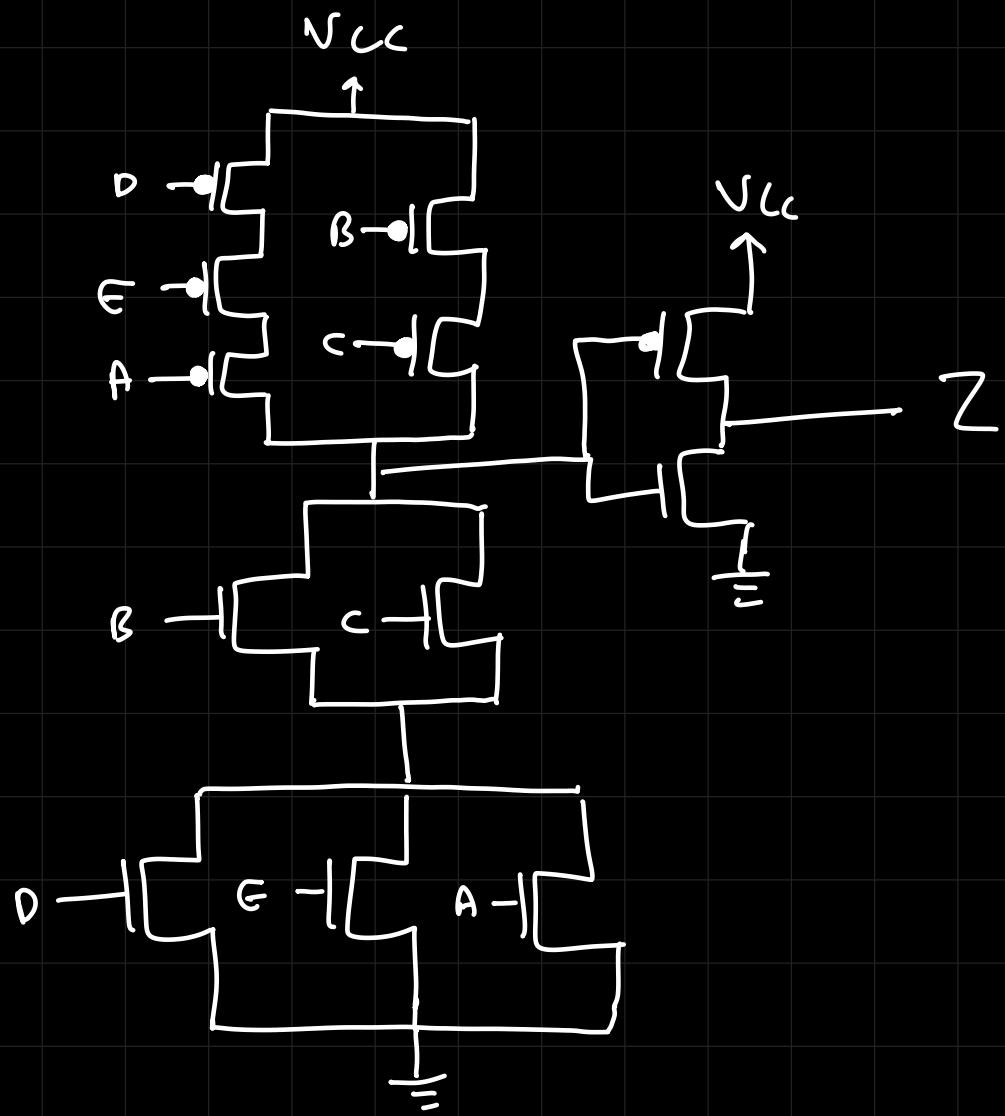
Q) Boolean expression :

$$Z = \overline{A(D+E) + BC}$$

realize Z with CMOS →



$$g) Z = (P + E + A)(B + C)$$

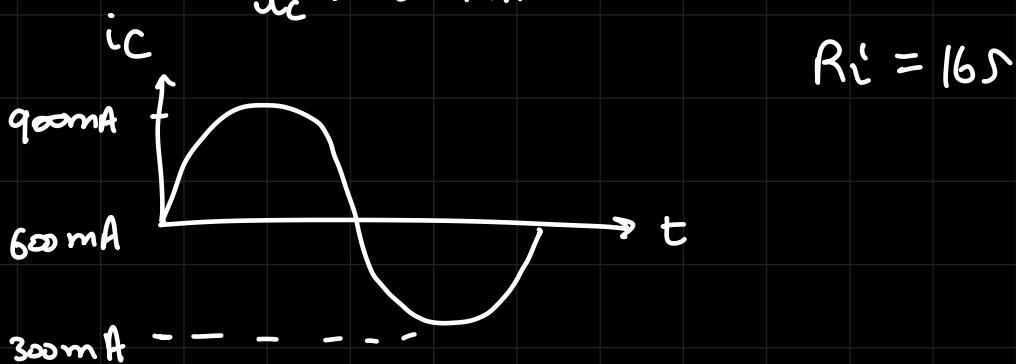


Q) for a single stage transformer coupled power amplifier, the supply voltage is 20V (DC) and the DC voltage at Q point = 10V and the DC current at Q point = 600mA
 Reflected Load = 16Ω
 AC current varies 300mA peak
 Calculate η.

Ans) $V_{CC} = 20V \quad V_{CE,Q} = 10V$

$$I_{CQ} = 600mA$$

$$i_c = 300mA$$



$$\eta = \frac{P_{AC}}{P_{DC}} \rightarrow P_{AC} = \sqrt{R_{rms} I_{rms}^2} = I_{rms}^2 R_L$$

$$P_{DC} = V_{CC} I_{CQ} = 20 \times 600m = 12W$$

$$P_{AC} = \frac{I_m^2}{2} \times 16 = 8 I_m^2 = 0.72W$$

$$8 \times 0.09 = 0.72W$$

$$\eta = 6\%$$

$R_{fC} \Rightarrow$ Inductor

Class C Amp

Condition: $V_{BB} <$ AC input swing

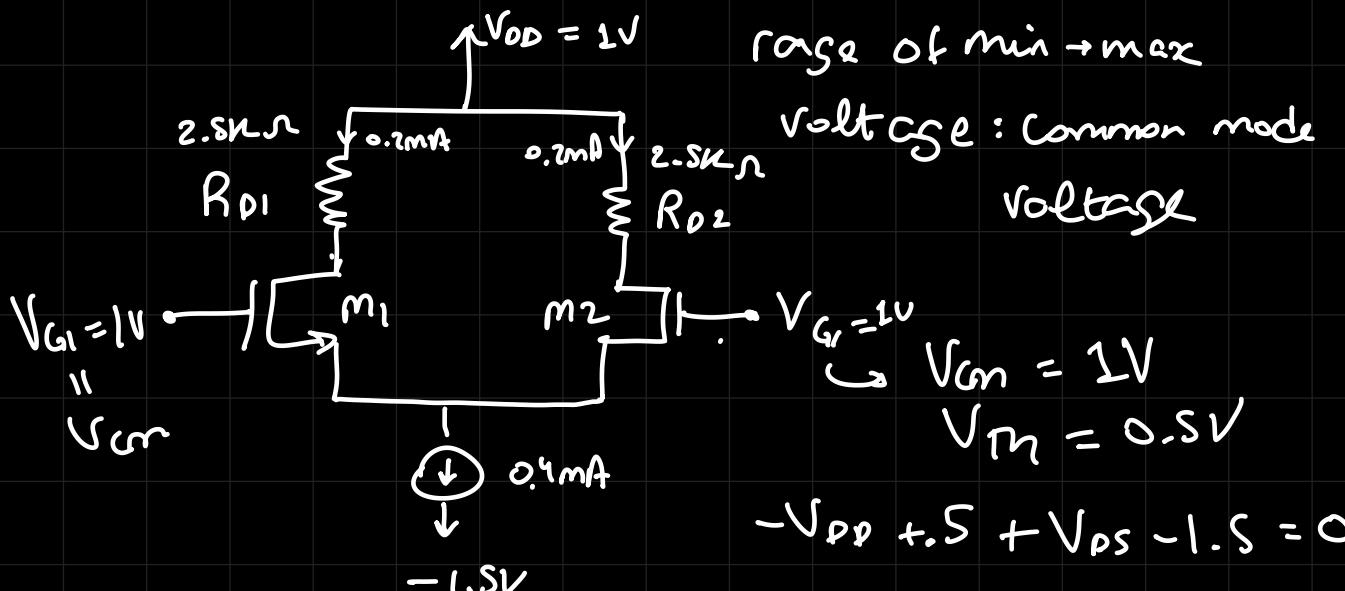
$$\eta = \left[1 - \frac{V_{min}}{V_{AC}} \right] \times 100\%$$

Conduction angle: $< 180^\circ$.

g) Differential Amplifier

i. Calculate V_o and V_{GS} of each Q_1 and Q_2 overdrive voltage

ii. calculate V_s , I_{d1} , I_{d2} , V_{d1} , V_{d2} when the common mode voltage = +1V



$$V_{D1} = V_{DD} - I_{D1}R_{D1} = 1.5 - 0.5 = 1.0V$$

$$Un \cos \frac{\omega L}{L} = 4mA \cdot V^{-2}$$

$$I_D^{SAT} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{DS}^2$$

~~$$10 \times 0.1 \times 0.2 = \frac{1}{2} \times 1 \times 10 \times V_{DS}^2$$~~

$$V_{DS}^2 = 0.1$$

$$V_{DS} = \sqrt{0.1} = 0.316V$$

$$V_{DS} = V_{GS} - V_T$$

$$V_{GS} = 0.616V$$

$$\begin{aligned} V_S &= V_G - V_{GS} \\ &= (-0.82) - 0.18V \end{aligned}$$

$$\begin{aligned} V_{CM}^{MAX} &= V_T + V_{DD} - I_D R_D \\ &= 0.5 + 1.5 - 0.5 = 1.5V \end{aligned}$$

$$\begin{aligned} V_{CM}^{MIN} &= V_{SC} + V_{CS} + V_t + V_{DS} \\ &= (-1.5) + 0.9 + 0.5 + 0.316 \\ &= -0.284 \end{aligned}$$

$$-0.284 \leq V_{CM} \leq 1.5V$$

V_{CS} is voltage needed across the current source

If V_{CS} is not given then consider ideal current source i.e. no drop across the current source
 $\hookrightarrow V_{CS} = 0$

In this numerical consider $\rightarrow V_{CS} = 0.4V$

CMRR : Common mode Rejection Ratio

$\hookrightarrow \frac{\text{The difference mode gain}}{\text{common mode gain}} = \frac{A_d}{A_c}$

$$CMRR_{dB} = 20 \log \frac{A_d}{A_c} dB$$

$$\begin{aligned} V_d &= V_1 - V_2 \\ V_c &= \frac{V_1 + V_2}{2} \end{aligned} \quad \left. \begin{array}{l} \\ \end{array} \right\} \quad \begin{array}{l} V_o = \text{common + difference} \\ \text{mode mode} \end{array}$$

$$\frac{V_o}{V_i} = A_v \rightarrow V_o = A_d V_d + A_c V_c$$

$$\text{for 2 stage} \rightarrow V_o = A_1 V_1 + A_2 V_2$$

$$\begin{aligned} V_1 &= \frac{V_d + 2V_c}{2} & \left\{ \begin{array}{l} V_d = V_1 - V_2 \\ V_c = \frac{V_1 + V_2}{2} \end{array} \right. \\ V_2 &= \frac{2V_c - V_d}{2} \end{aligned}$$

$$\begin{aligned}
 V_o &= A_1 \left[\frac{V_d + 2V_C}{2} \right] + A_2 \left[\frac{2V_C - V_d}{2} \right] \\
 &= V_d \left[\frac{A_1 - A_2}{2} \right] + V_C [A_1 + A_2] \\
 &= V_d A_d + V_C A_c
 \end{aligned}$$

$$A_d = \frac{A_1 - A_2}{2}, \quad A_c = A_1 + A_2$$

for practical case $\rightarrow CMRR$ is very high
 for ideal case $\rightarrow CMRR = \infty$

$$g_m = \frac{2I_D}{V_{ov}}$$

$$A_d = g_m R_D$$

$$A_{cm} = \frac{V_{od}}{V_{icm}} = -\frac{\Delta R_D}{R_{ss}}$$

$$A_d = g_m R_D$$

$$\begin{aligned}
 CMRR &= \left| \frac{A_d}{A_c} \right| = \frac{g_m R_D}{\frac{R_D}{2R_{ss}} \times \frac{\Delta R_D}{R_D}} = \frac{2g_m R_{ss}}{(\Delta R_D / R_D)} \\
 &\quad \hookrightarrow \text{error}
 \end{aligned}$$

EZ topic for endsem

- ↳ CMOS realization
- ↳ Power amplifier
- ↳ current mirror

Moderate topic →

- ↳ Differential Amp

Tough →

cascade + cascode

$$CMRR = \frac{2g_m R_s}{(4g_m/g_m)} = \frac{2g_m R_s}{(\Delta R_o/R_o)}$$

(Q) CMOS diff pair

bias current: 0.8mA

$$\frac{W}{L} = 100 \quad m_Co_2 = 0.2 \text{ mA/V}^2$$
$$K = 20m$$

$$R_D = 5k\Omega \quad R_{SS} = 2\Omega K \Omega$$

(i) find differential gain, A_d
common mode gain A_c

when the R_D have 1% mismatch

(ii) also find CMRR

$$\text{Ans) } g_m = \sqrt{2kI_d} = \sqrt{20m \times 0.4m \times 2} = 4 \times 10^{-3}$$

$$\text{make: } I_d = \frac{I_{bias}}{2} = 0.4m$$

$$R_d = g_m R_d = 4 \times 10^{-3} \times 5 \times 10^3 = 20V/V$$

$$A_C = -\frac{\Delta R_d}{2R_{SS}} = \frac{0.01 \times 5 \times 10^3}{2 \times 25 \times 10^3} = 10^{-3}$$

$$CMRR = \frac{20}{10^{-3}} = 20K$$

$$CMRR_{dB} = 20 \log_{10}(20K) = 20 \times 4 \log_{10} 2 \\ = 86dB$$