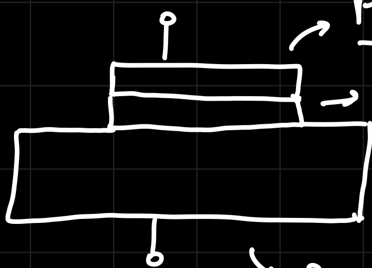
lecture

MOSCAP → MOSFET w/o S and D

output characteristic → I_D vs V_{DS}

transfer characteristic → I_D vs V_{GS}

#MOSCAP



metal OR Poly crystalline → heavily doped Si ↓ n : Nmos, p : Pmos channel

Gate oxide / insulator

↳ SiO_2

$E_G = 9eV$, $\varepsilon_r = 3.9$

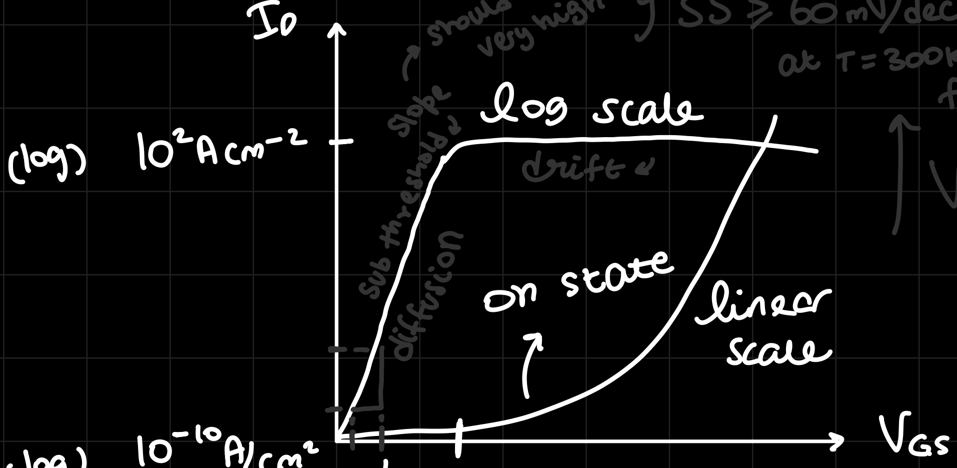
Semiconductor substrate

↳ Si

P type for NMOS

N type for PMOS

Remember →



} SS ≥ 60 mV/dec {min value}

at T = 300K for any MOSCAP based MOSFETS

for an ideal switch SS = 0

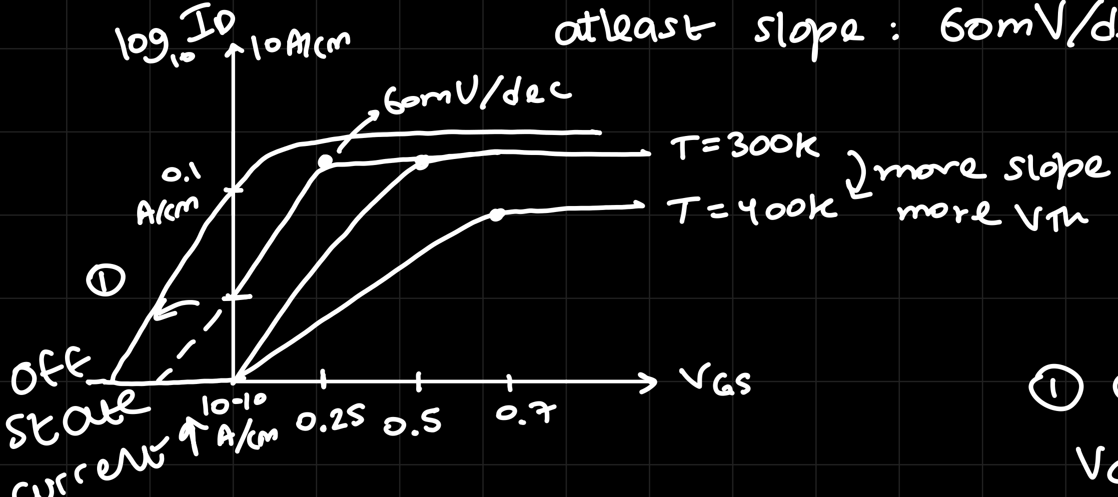
↑ V_{DS}

Off state

V_{Th} (threshold voltage) ~ 0.5V

↳ defines off state vs on state

quite a lot of power consumption for a single transistor for just switching on/off atleast slope : 60mV/dec



difference btw on & OFF ↓

① even at $V_{GS} = 0$ → there is some current I_d i.e. charge movement

if we go even left, the off state current ↑↑ and hence difficult to differentiate between HIGH & LOW
↳ Not good

ENHANCEMENT MODE MOSFET :

no chanel formed at no V_G

↳ off state without any gate voltage

DEPLETION MODE MOSFET :

-ve potential required for OFF state

there is some current even for no V_G

chanel already formed without V_G

depletion of charge carrier

depletion of holes in the n chanel [Nmos]

because of +ve $\bar{E}$, the holes move down from the chanel hence depletion

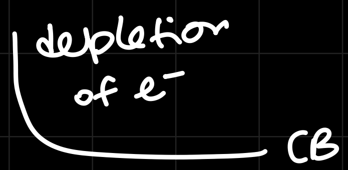
	M	O	S
we consider →	ϕ_m	—	χ_e
		d	ϕ_s

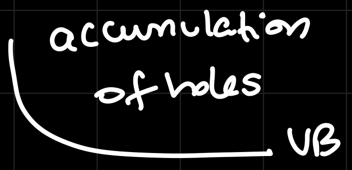
Why not considering stuff like fermi level?
even though $E_g = 8\text{-}9\,eV$ (big)

because $n_i = \sqrt{N_c N_v}\, e^{-E_g/k_B T}$

with so high E_g, $n_i \sim$ negligible
hence E_F, Φ, χ is not relevant

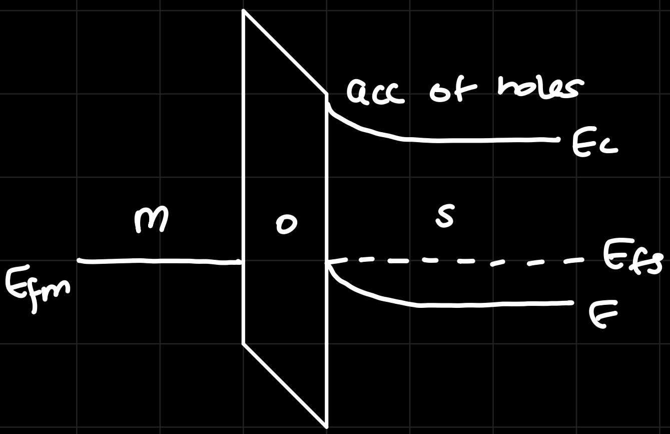
also, we observed potential drop across the oxide and hence $\sim$ resistance





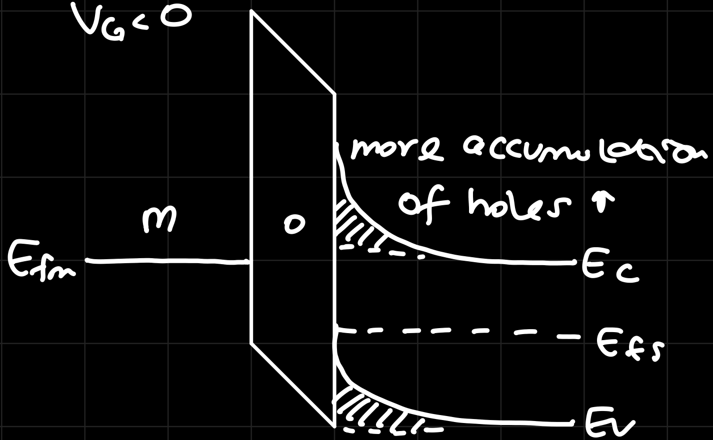
MOS

equilibrium



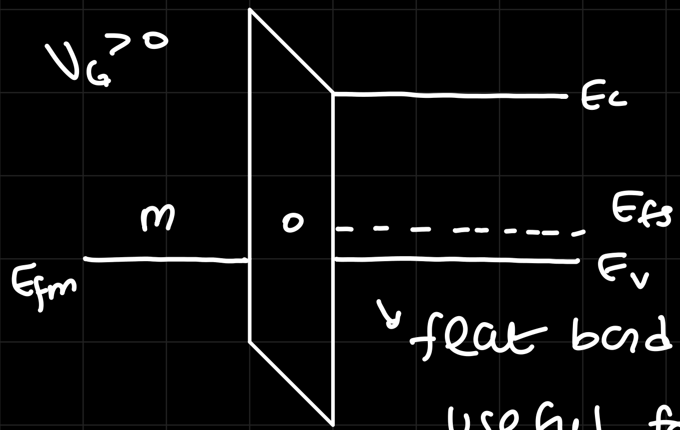
negative bias

→ $V_G < 0$



+ve bias

$V_G > 0$

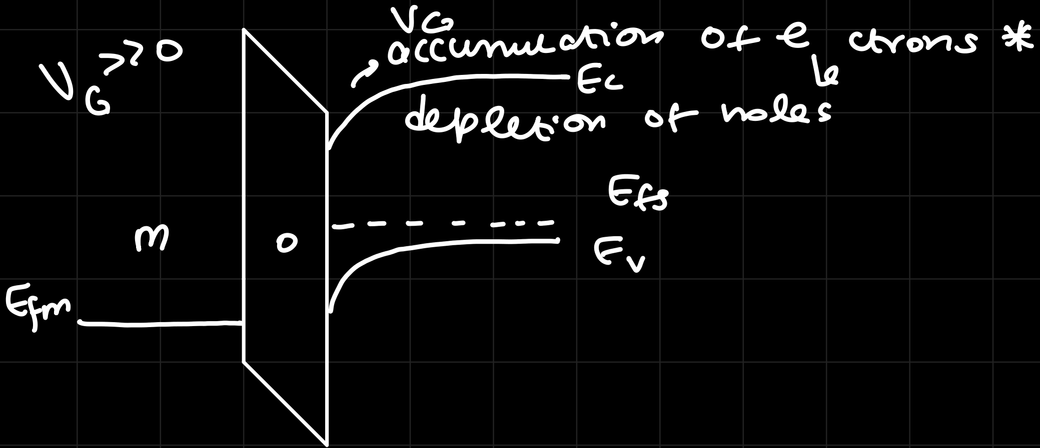


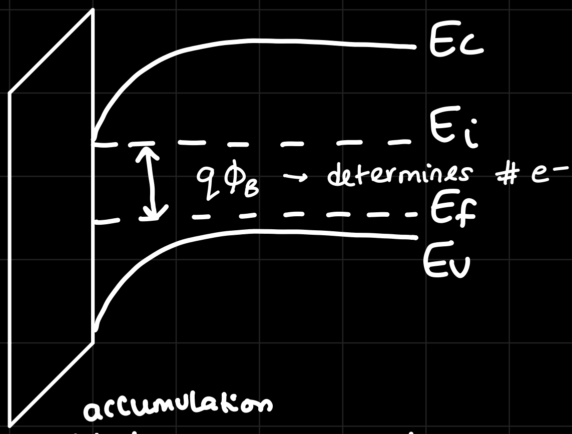
flat band

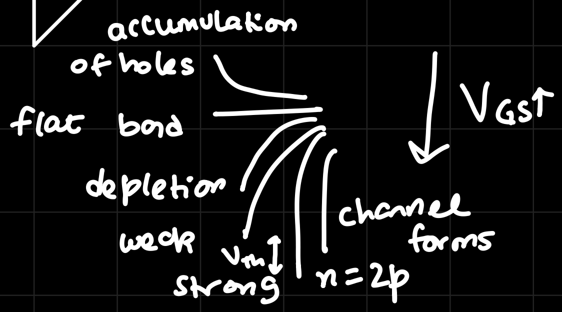
useful for determing threshold voltage

more +ve

$V_G >> 0$







numbers of e^- on the surface is greater than the hole concentration ≡ Inversal

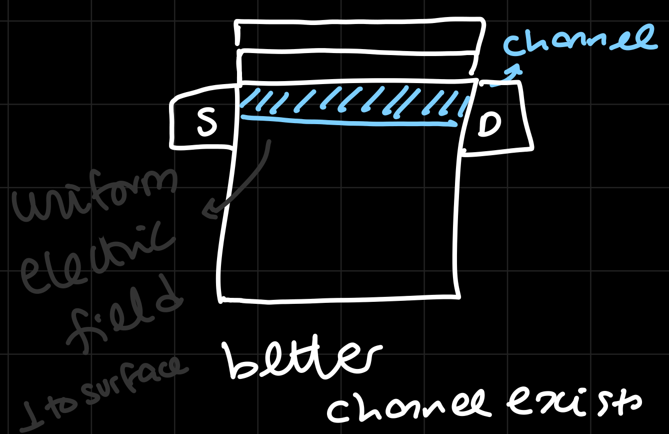
e^- get inverted at $V_{GS} \gg 0$

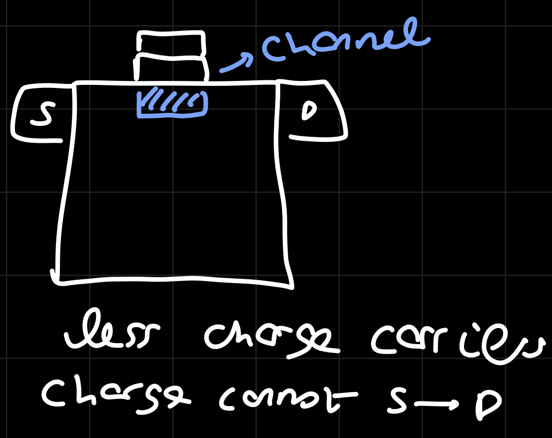
after weak inversal when $\#_{e^-} \simeq 2\,\#_{holes}$ ≡ strong inversal i.e. very strong $\vec{E}$ then channel forming takes place

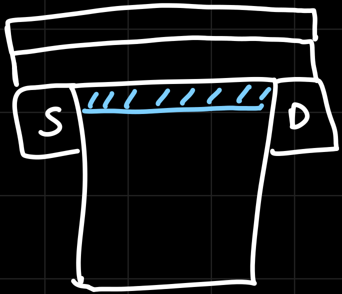
V at which inversion goes from weak to strong ≡ V_{TH} (threshold voltage)

$$\phi_B = V_{TH} \ln\left(\frac{N_a}{N_i}\right)$$

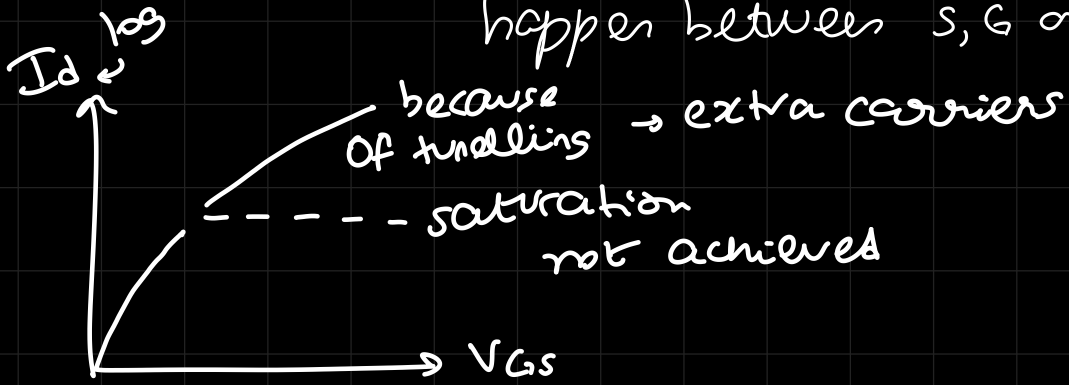
$$\left.\begin{array}{l} \text{flat band}: \ \phi_s = 0 \\ \text{hole accumulation}: \ \phi_s < 0 \\ e^- \text{ accumulation}: \ \phi_s > 0 \\ \text{inversion}: \ \phi_s > \phi_B \end{array}\right\} q\phi_s \rightarrow \text{band bending at the surface}$$

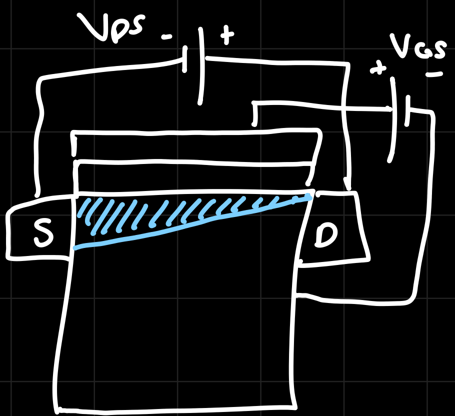






This is also not optimum because of parasitic capacitance and also some tunnelling can happen between S, G and G, D





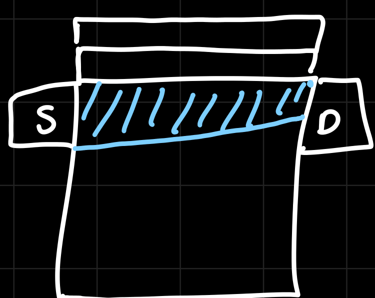
Pinch off condition when the corne touches the end point

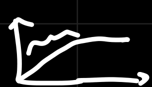
happens at the threshold voltage

$V_{GS} = V_T$

below threshold voltage no need for latitudinal $\vec{E}$ to push charges, the carrier concentration drives the carriers hence the linear property

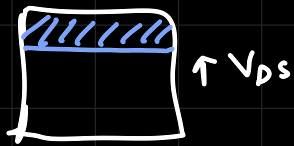
#e↑↑ diffusion →



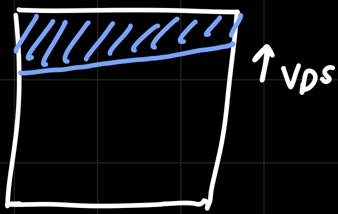


at $V_{DS} = 0$, uniform channel

for $V_{DS} = 0.1 - 0.5V$ (eg)



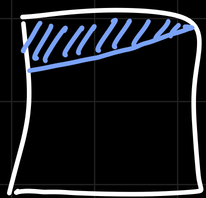
linear



$\#e^- \uparrow$

$\bar{E} \sim 0$

for $V_{DS} > V_{GS} - V_T$



$\#e^- \rightarrow$ const

very high $\bar{E}$ due to V_{DS} & V_{GS}

so, I_d saturates

Delay

↳ Intrinsic : within devices

↳ Extrinsic : within circuits

TRANSCONDUCTANCE

$$g_m = \left. \frac{\partial I_D}{\partial V_{GS}} \right|_{V_{GS}}$$

dependent on temp

= idea of speed of "switching"

Channel conductance

$$g_d = \left. \frac{\partial I_d}{\partial V_{DS}} \right|_{V_{GS}}$$

used for finding drive current for small bias input