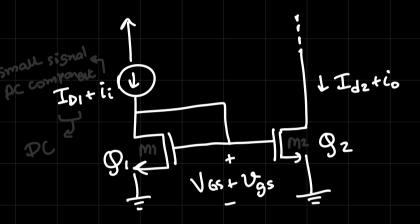
Lecture 17

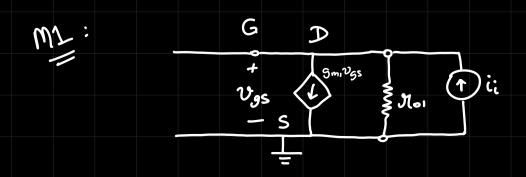
=> current micror as current emplifier

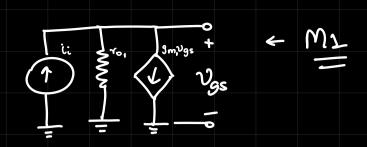
low input resistance higher output resistance wit Ri

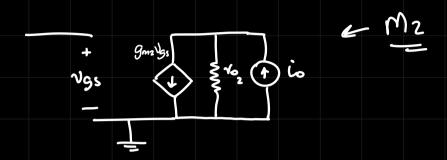


M2 needs to be in saturation for current mirror Vosz > VGSZ - VTZ

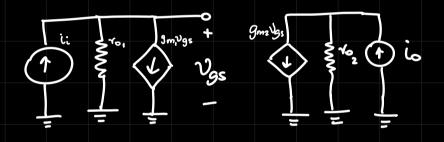
AC chalysis 4 small signal model (n)

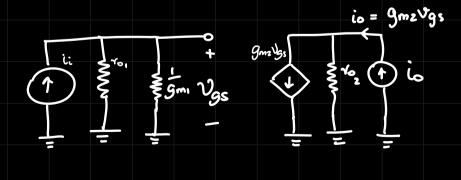






combined cut:





i we dont wont
current to flow
through Iroz
hence Yoz
showd be very
high so that
I flows through
Load

$$Zin = 9701 \parallel \frac{1}{9m1} \simeq \frac{1}{9m1}$$
; $Z_0 = 9702$

inverse of 1 amp

note: we need gain to ad

here we neglected Mis

early effect resistance

in our assumption

i.e. You - 00

$$g_{m2} = 2K_2 \left(V_{GS2} - V_{T2} \right)$$

$$g_{mi} = 2K_1 \left(V_{GS1} - V_{T1} \right)$$

$$K_1 = \frac{1}{2} \mu_1 \cos(\frac{w}{L})_1$$
, $K_2 = \frac{1}{2} \mu_2 \cos(\frac{w}{L})_2$

COMMON GATE

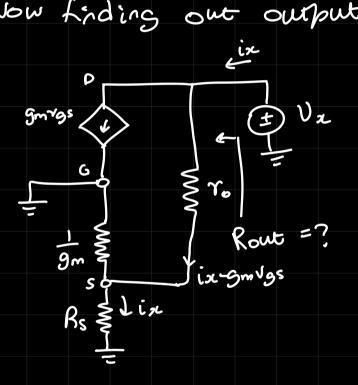
we wont to distribble the sain over multiple comps to prevont lipping og input.

$$Rin = V_{x} = \frac{R_L + V_0}{1 + g_m V_0} \simeq \frac{R_L}{g_m V_0} + \frac{1}{g_m} \left\{ \begin{array}{ll} assuming \\ g_m V_0 >>> 1 \end{array} \right\}$$

* Suen if RL 11 Rin Scales down RL by gmr. od prohibits the vise of Rin Significantly.

and here low input resistone aviared for current emp/buffer.

Now Linding out output resistance



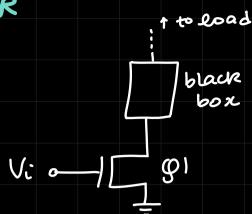
Vgs = -Vs = -ixRs

 $\forall x = (ix - gmigs) v_0 + ixRs = (ix + gmixRs) v_0 + ixRs$

Rout = no + gmRsno + Rs = no + Rs Li+gmVo)

The output resistance will be high: Rout = Rsgmr.

CASCODE AMPLIFIER



The black box con be a common gate trossistor so mat ...

- O Input impedance is not high and writ RL, Rin Scales by RL 9m 270
- © Output impedence is very high. Rout = Rsgmr.
- 3 Current gain = 1

I
$$Q$$
 V_0
 V_0

for the CG contig,

Ro = 9m2 Yoz Rs : derivad earlier Rs = vol because O1 is the SRC for Q2

So, Ro = gmz Moz Moi

Av = -gmiRo = -gmigmz Yoz Yoz

= - gmiroi gmiroz

let gmi= gmz= gm ord ro= roi = voz

 $Av = -(gmno)^2 = -A^2vo$

where Avo = volt-gain of regular
CS transistor

TRADEOFFS:

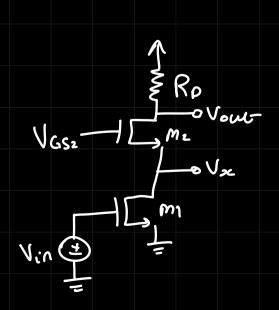
for M1: SOLVIALON,

Vx > Vin - V+1

VGSz = VGz - VSz

VSz = VGz - VGSz

Vx = Vsz = UG2 - VG52 > Vin - Vt1



for M2: Saturation >

Josz > VGSz - VTZ

VD2-VS2 > VGS2-VTZ

Vout - Vx > VGS2-VTZ

Vout > VGS2-VTZ + Vx

Ord Vx > Vin - VTI

Ult Vx = Vin - VTI

Vout 3 VGS2 - VT2+ Vin - V+1
Vov2 Vor,
overdrive voltages

increasing more only in cascode, will keep on increasing Vour depending on Vors which might distort the output signal when Vour 4 Vor, + Vor. +

HORIZONTALLY INCREASING: gain 1, g stable VERTICALLY INCREASING = gain 1, distation 1