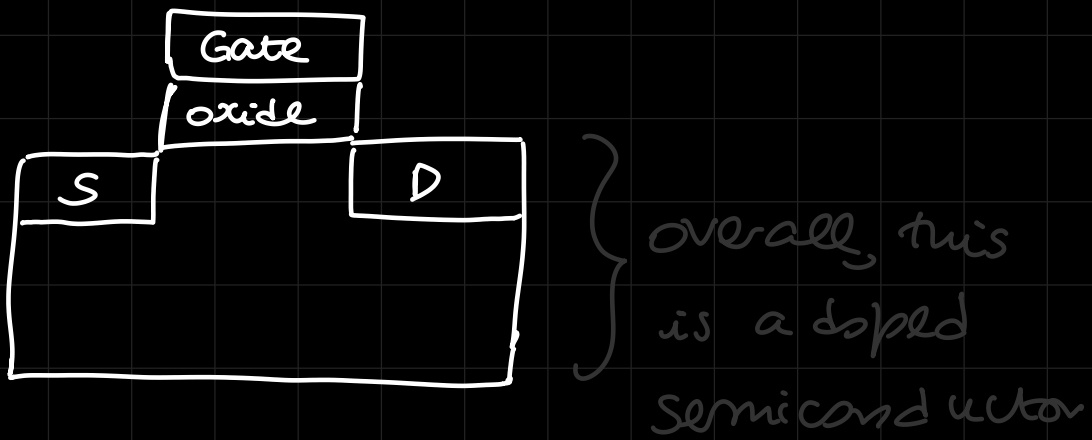
#MOS capacitor & MOSFET

since 180nm node ↓ metal gate $\xrightarrow{\text{replaced by}}$ Poly Crystalline (P-Si)

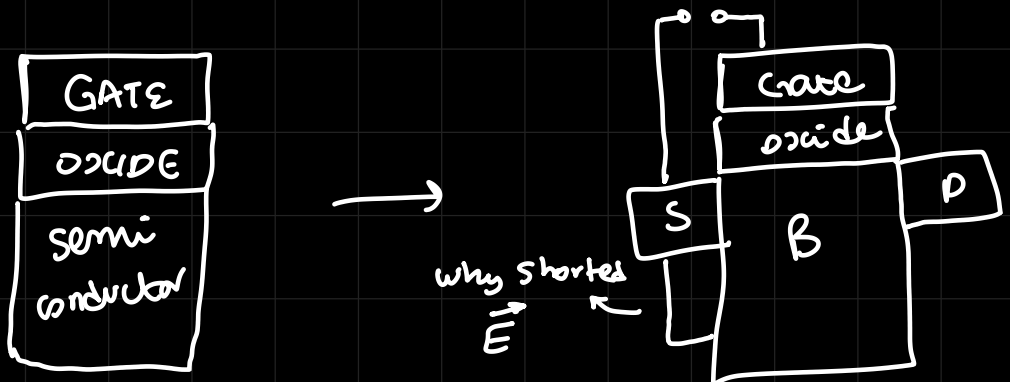
since 90nm node ↓ again back to metal because of performance issues

now also, SiO_2 (oxide) ⟶ high 'K' dielectric HfO_2 (gate dielectric)

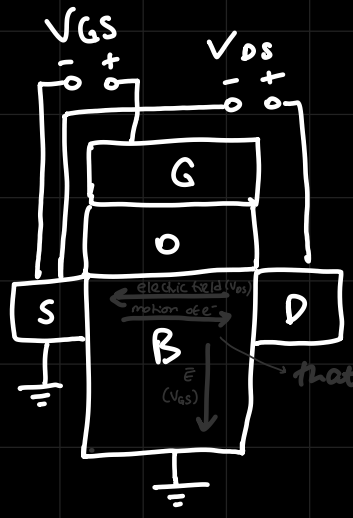
With less and less space with decrease in size (Moore's Law) SiO_2 couldn't provide optimum performance.



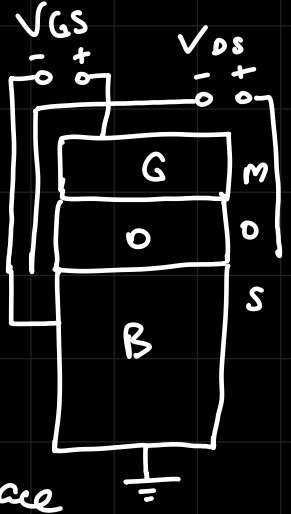
now what if S and D are not doped wrt body/substrate



typically :

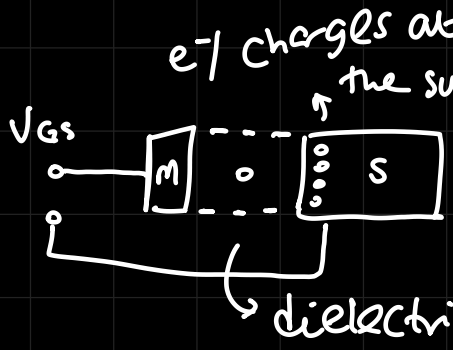


go back to when S, B, D had same doping



→ capacitor

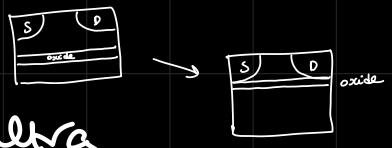
charges separated by a dielectric (oxide)



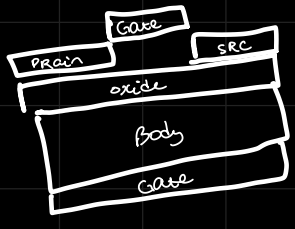
Variable capacitor

for NMOS → S: P type → $V_{GS} > 0$

PMOS → S: n type → $V_{GS} < 0$ (reversed)



Classical → Planar double gate → ultra thin body SOI

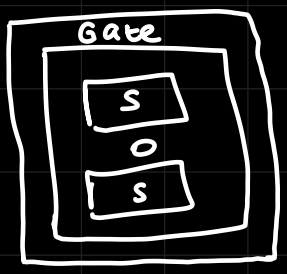


→ Tri Gate FinFET → Gate-All-Around NWFET

complementary mos → connection between
(cmos) PMOS & NMOS

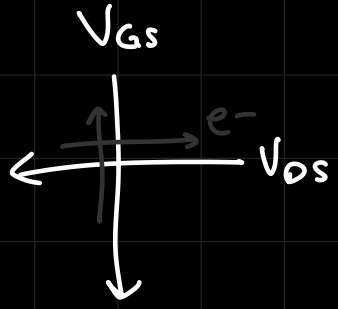
complementary FET → a single device acting
as both PMOS, NMOS

Sheet FET



over the evolution
of MOSFETs, # of gate is observed to have been
increasing

V_{GS} is pulling
e- from SRC
to DRAIN
and that flow
is controlled
by V_{GS}



AVG laptop Voltage rating → 12V
for phones → 5V

but there are multiple devices
we need to control power consumption

At very small dimension and very high $\bar{E}$, the dielectric creates a channel allowing the flow of e^- hence acting as a conductor (not intended)

↳ Dielectric Breakdown

and therefore we moved from

$SiO_2 \rightarrow HfO_2$

↓ ↓

4ε₀ ~25-27ε₀ (high K ✓)

we know, $C = \frac{\varepsilon A}{d}$ (A → const) $\rightarrow C_{Hf} >> C_{Si}$

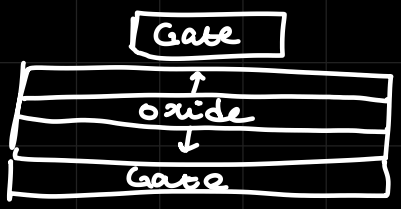
and $Q = CV$ (C → const) → high Q ✓

holds more surface charge

Charge density ✓

Going back:

double gate:

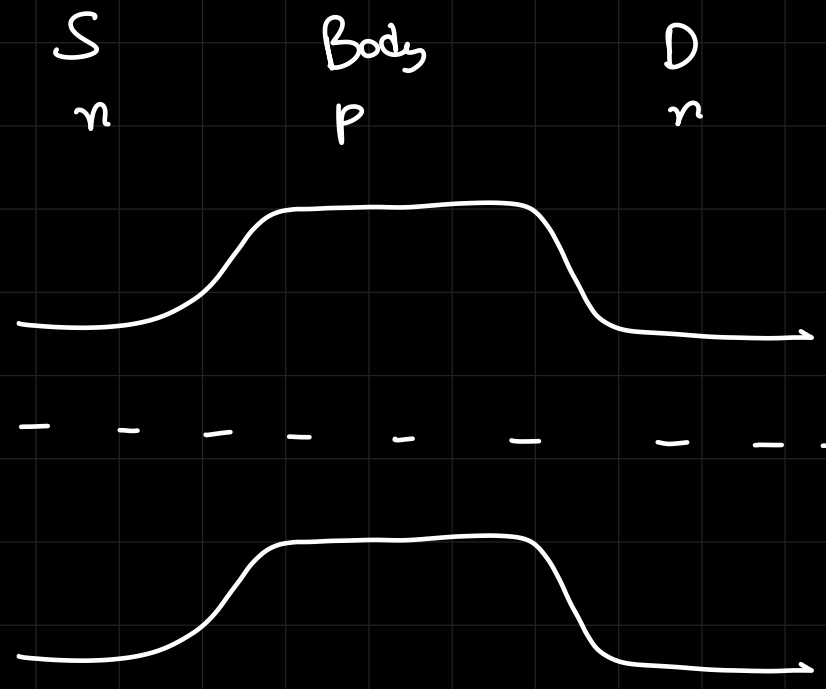


e^- are being pulled from both sides. Helps in keeping the charges at the surface

good capacitor ✓ (wrt classical)

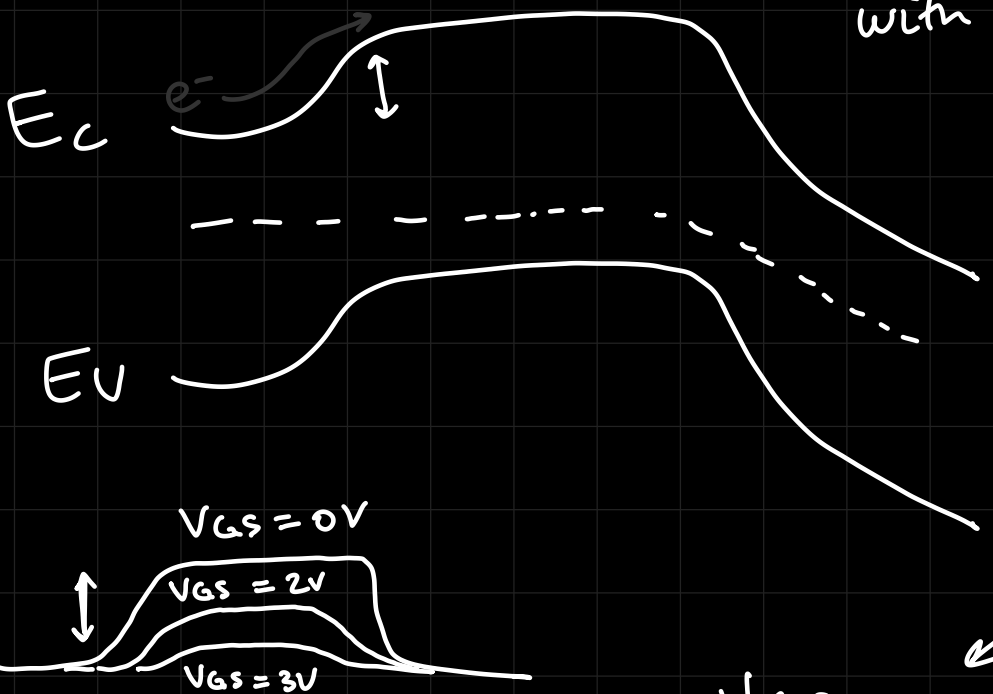
Therefore, # gates ↑ → carrier density ↑

NOTE: This is a surface mode device



When +ve V_{DS} is applied:

over the barrier



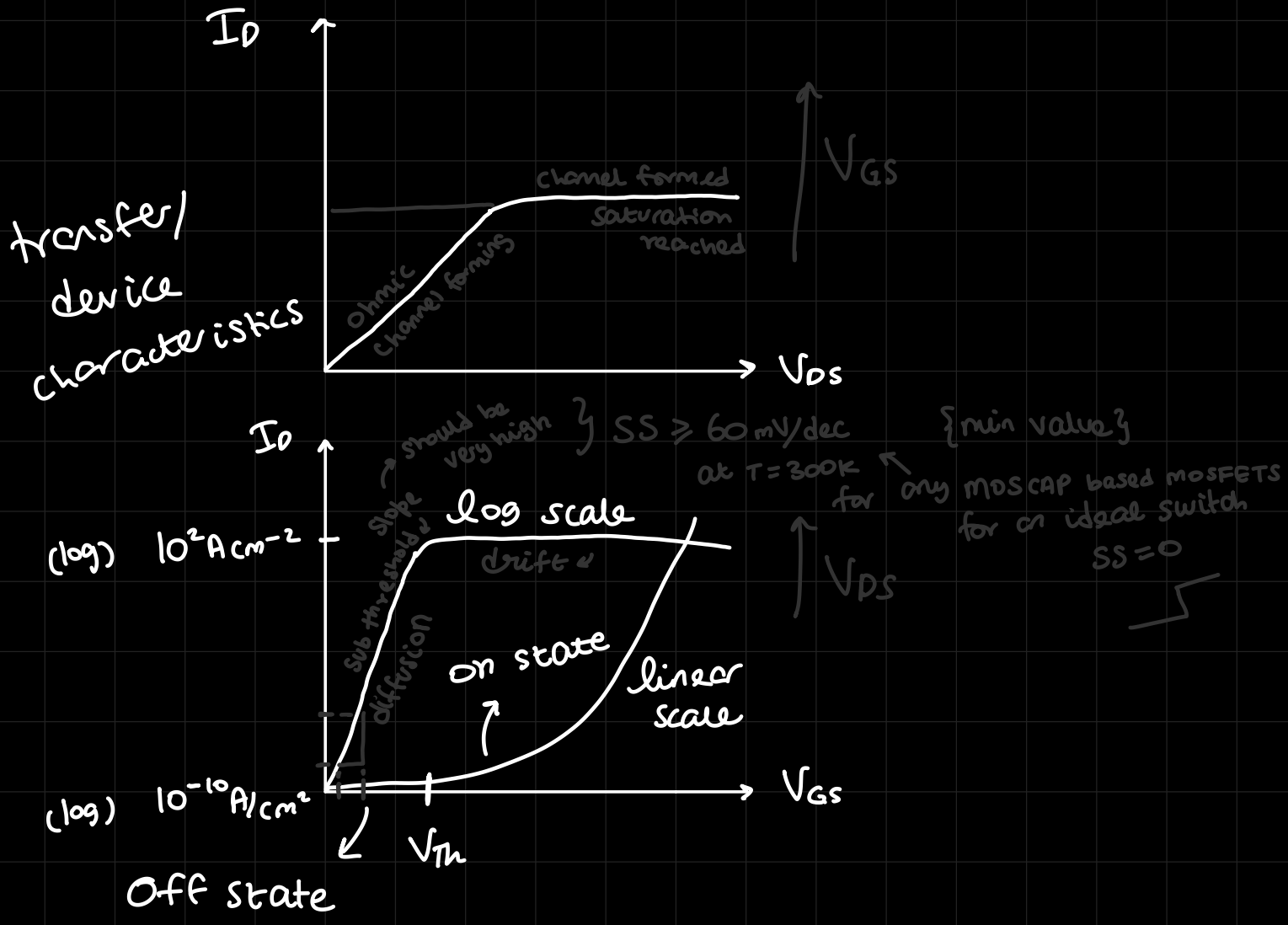
with $V_{DS} > 0$ biasing

we must now control the barrier height

reduce it to allow all e^- (max I)

V_{GS} does this

V_{GS} is the threshold voltage to trigger for better flow of e^-



Minimum ON-OFF state ratio $\sim 10^4 - 10^5$

compare characteristics with PN Junction

want better off state: improve diffusion

on state: drift transport mechanism

MOS CAP action: loosing carriers