

DC oralysis for 9 point

13 Open Ckt all capacitors

15 BE & CE Joop

15 common emitter config

Any variation in B will impact in Iz and hence will shift the & point. Therefore this amplifier bias is not ideal

* For multiple devices where fixed bias ckt may be a subsystem (i.e. we may trave multiple values of B), we may get different Q point which will result in the transistor being in indeterminant mode. We need standardized values. # Voltage Divider Bias

Adchias voltage
con be created using R, R.
Is con also be adjusted

simplified using Therenin's Equivalent

- Uth + IBRn + UBE + IERE = 0

IE = (Bt1) IB

IB(RTh + RE(B+1)) = Un-UBE

IB = Um-VBE Rm + RE(B+1)

IC = BIB = BLVTh - VBE)
Rn + Re(B+1)

due to variation in B, we have variation in It in the numerator but also a feedback pulling the value down in the denominator.

CE lop, - VCL + TCRC + VCG + IER = 0

VCE = VCC - IC (RC+RE)

assuming Ic~ IE

Since Ic is stabilized, Vce will be stabilized as well.

we also want > © Ra>> En lo make
Bri

If ond IL & invariant

VIN 1 -> IET -> ILT -> VCEV

The towards saturation

9

VCE

but if vmt, IEL, ILL, Væn 1 9 towards cutoff

So, uc need to maintain VTh such that transister romains in active made

Rule of thumb - VTh = I Vcc 3

VCB = 1 Vcc (or VBE) 3 ICRc = 1 Vcc 3

III = (0.1-1) x Iq

I VCC for Rc; I VCC for R2; TUST & for possible nugative signal suing

as per sulle of tumb -

$$V_{c} = \frac{2}{3} V_{cc} = \frac{8V}{3}$$

assume, IB ~ 0 - I = Vcc - I conbe Rithe [IE, 0.1 IF]

COSE 1:
$$T = 0.1T_C = 0.1mA = 12 \rightarrow R_1+R_2 = 12\times10^5$$

Vac Vac

 Vac
 Vac

IE = 0.925mA ~ 0.93mA

row ridro Ri by
$$\frac{RB}{101}$$
 $R_{1}' = R_{1} - R_{1} = 3.3 = 0.992 \text{ mA}$

The state of the s

9mitter stabilized circuit DC onalysis -VCC + TBRB+ VBE + IERE TO IB = IE (Bri) IB = VCC - VBC RB+ (B+1) RZ Ic = B(Vcc-VBE) RB+ (Br) RE

Note: ue have control/feedback urlike fixed bias

Vce = Vce - IRc - IFRE

DC bias with voltage Feedback RB IR IC -VCL+IRC + IBRB+ VBE+ TER: =0 assuming IBCC Ic -VCC + ICRC+ IBRB +VBE + ICRE = O -Vce + IBL BRC+RB+ (B+1) RE)+VBE=0 IB = VCC - VBC BRC+RB+(B+1)RE assuming Ica IE So, IB = VCC - VBE RB + BCRC+RE) VCL-VBE Ic = BIB = RB + RC+RE much better & robust as compared to emitter stabilized | What is the tradeoff? 1 bias

emplifier design -> adequate gain

prevents distortion - stabilize q point

in output infinite input resistance

low output impedance

linear criplification

CE: V comp = out of phase by 180° CB: V comp = in phase

CC: buffer comp