ELL201 Lab Project

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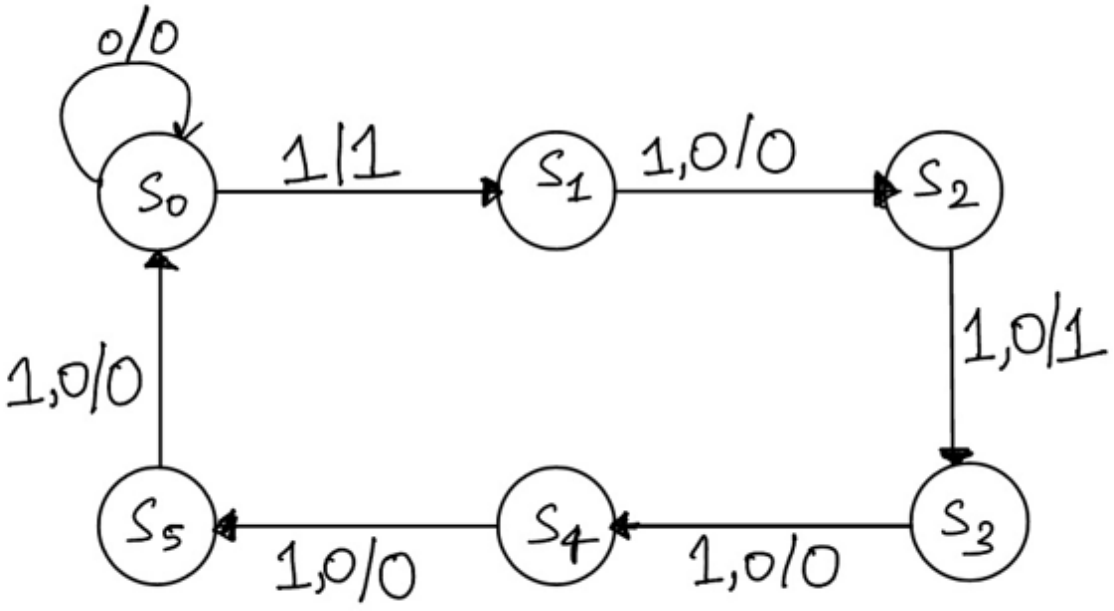
Problem: To Design A Circuit To Generate Serial Sequence Based On Entry Number

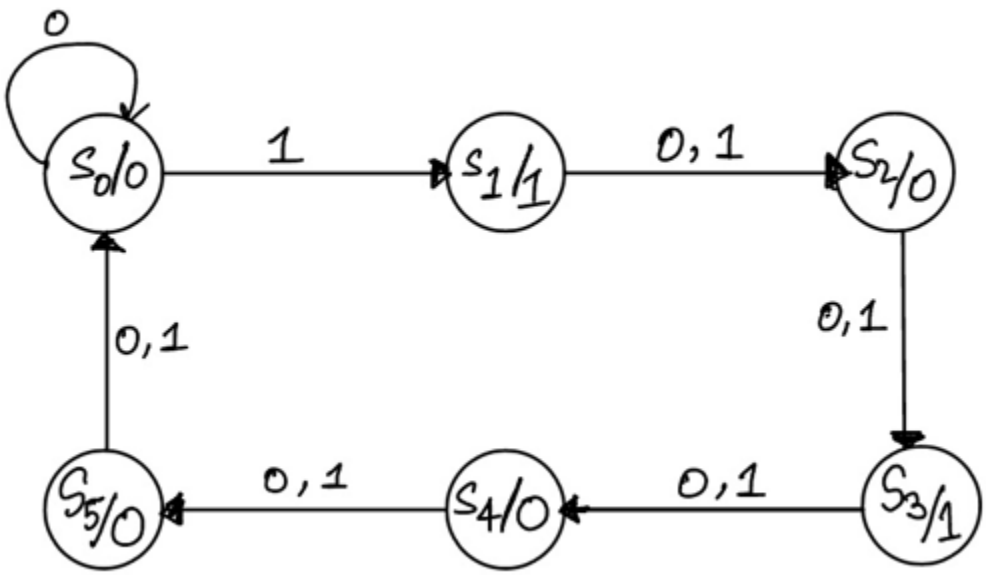
For Entry Number of the form:
2021MT6X1X2X3X4: X3 = 5; X4 = 8
Hence the sequence: X3 % 8 = 5; X4 % 8 = 0; -> {1, 0, 1, 0, 0, 0}

State Diagram For The Finite State Machine:

Mealy Machine-



Moore Machine-



No of Flip Flops Needed:

No of states=6.

Let, no of flip flops=n.

No of states due to flip flops > No of states needed. i.e $2^n > 6$. => n=3.

Assigning values to each state in the state diagram

The Idle state is S0 to begin with. The other states are S1, S2, S3, S4, and S5. S6 and S7 are the leftover states, where the machine outputs zero.

State Assignment

S0	000

S1	001
S2	010
S3	011
S4	100
S5	101

State Tables

Q_{an}	Q_{bn}	Q_{cn}	X	Q_{an+1}	Q_{bn+1}	Q_{cn+1}	Y	D_a	D_b	D_c
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1	0	0	1
0	0	1	0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	1	0	1	1
0	1	0	1	0	1	1	1	0	1	1
0	1	1	0	1	0	0	0	1	0	0
0	1	1	1	1	0	0	0	1	0	0
1	0	0	0	1	0	1	0	1	0	1

1	0	0	1	1	0	1	0	1	0	1
1	0	1	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

K-Maps

For D_a

AB\CX	00	01	11	10
00	0	0	0	0
01	0	0	1	1
11	0	0	0	0

10	1	1	0	0

$D_a=Q_a'Q_bQ_c+Q_aQ_b'Q_c'$

For D_b

AB\CX	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

$D_b=Q_a'Q'_bQ_c+Q'_aQ_bQ_c'$

For D_c

AB\CX	00	01	11	10
00	0	1	0	0
01	1	1	0	0

11	0	0	0	0
10	1	1	0	0

$D_c=Q_aQ'_bQ'_c+Q'_aQ_bQ_c'+Q_a'Q_c'X$

For Y

AB\CX	00	01	11	10
00	0	1	0	0
01	1	1	0	0
11	0	0	0	0
10	0	0	0	0

$Y= Q'_aQ_bQ'_c+Q_a'Q_c'X$

Verilog Implementation:

D Flip-Flop:

```
module d_ff(d,clk,reset,q);
	input d,clk,reset;
	output reg q;

	always @(posedge clk,negedge reset)
	begin
		if(reset==0)
		begin
			q<=1;
		end

		else if(d==1)
		begin
			q<=1;
		end

		else if(d==0)
		begin
			q<=0;
		end
	end
endmodule
```

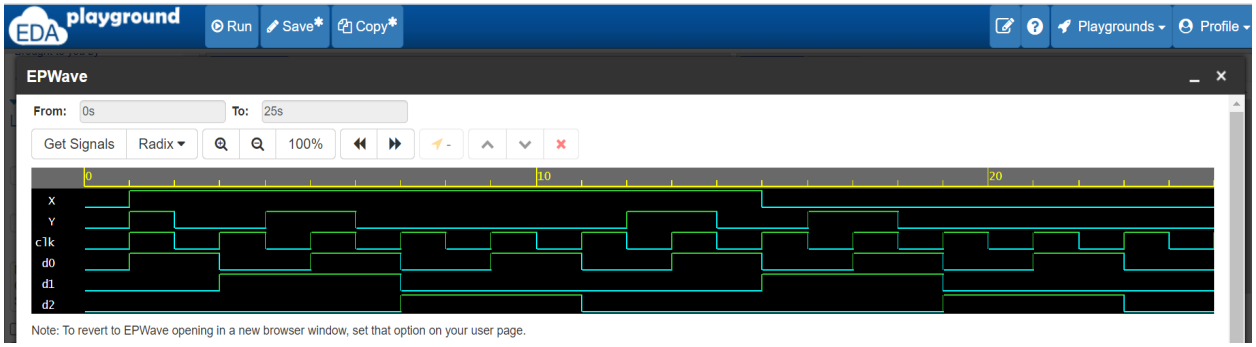
Finite State Machine:

```
module fsm(reset,clk,x,y);
	/*reg clk;*/
	input x, clk,reset;
	reg d2,d1,d0;
	wire [2:0] q;
	output y;
	assign y = (~q[2] & q[1] & ~q[0] ) |(~q[2] & ~q[0] & x);

	d_ff dff2(d2,clk,reset,q[2]);
	d_ff dff1(d1,clk,reset,q[1]);
	d_ff dff0(d0,clk,reset,q[0]);

	always @(negedge clk)
	begin
		d2 = (~q[2] & q[1] & q[0])|(q[2] & ~q[1] & ~q[0]);
		d1 = (~q[2] & ~q[1] & q[0])|(~q[2] & q[1] & ~q[0]);
		d0 = (~q[2] & ~q[0] & x)|(~q[2] & q[1] & ~q[0])|(q[2] & ~q[1] & ~q[0]);
	end
endmodule
```

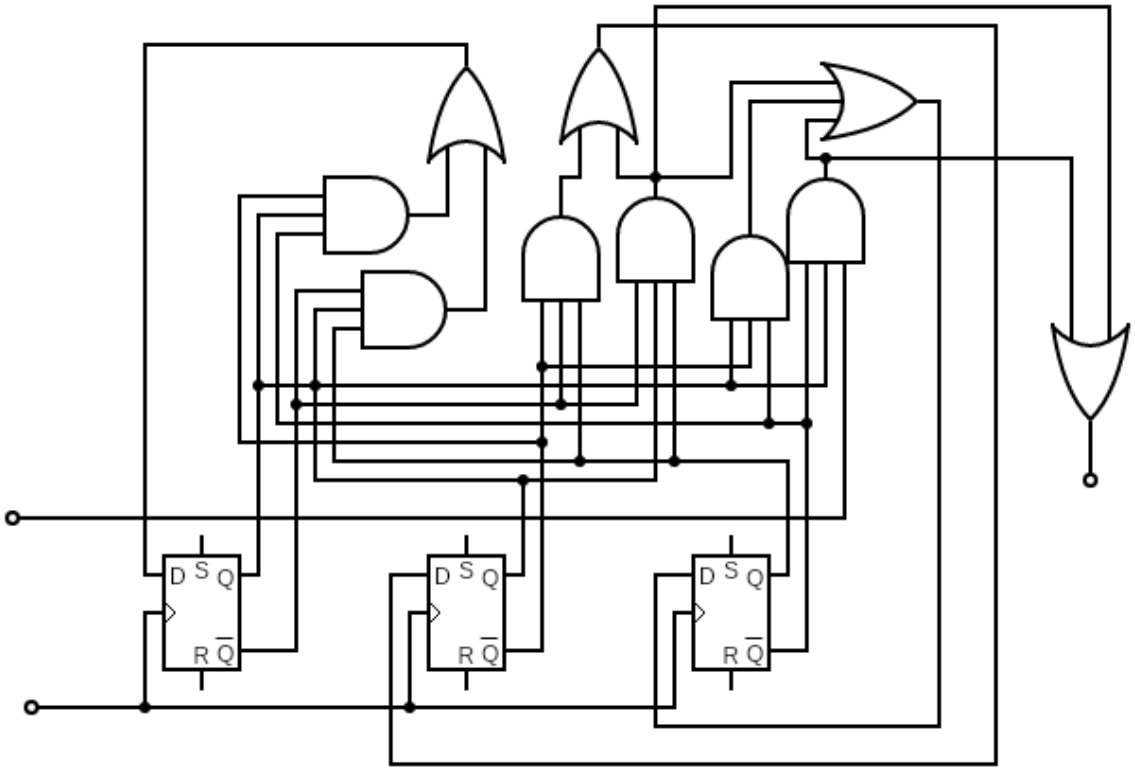
Output:

```
VCD info: dumpfile sequence.vcd opened for output.
Time:                    0clk: 0, Input : 0, States : 0 0 0, Output: 0;
Time:                    1clk: 1, Input : 1, States : 0 0 0, Output: 1;
Time:                    2clk: 0, Input : 1, States : 0 0 1, Output: 0;
Time:                    3clk: 1, Input : 1, States : 0 0 1, Output: 0;
Time:                    4clk: 0, Input : 1, States : 0 1 0, Output: 1;
Time:                    5clk: 1, Input : 1, States : 0 1 0, Output: 1;
Time:                    6clk: 0, Input : 1, States : 0 1 1, Output: 0;
Time:                    7clk: 1, Input : 1, States : 0 1 1, Output: 0;
Time:                    8clk: 0, Input : 1, States : 1 0 0, Output: 0;
Time:                    9clk: 1, Input : 1, States : 1 0 0, Output: 0;
Time:                   10clk: 0, Input : 1, States : 1 0 1, Output: 0;
Time:                   11clk: 1, Input : 1, States : 1 0 1, Output: 0;
Time:                   12clk: 0, Input : 1, States : 0 0 0, Output: 1;
Time:                   13clk: 1, Input : 1, States : 0 0 0, Output: 1;
Time:                   14clk: 0, Input : 1, States : 0 0 1, Output: 0;
Time:                   15clk: 1, Input : 0, States : 0 0 1, Output: 0;
Time:                   16clk: 0, Input : 0, States : 0 1 0, Output: 1;
Time:                   17clk: 1, Input : 0, States : 0 1 0, Output: 1;
Time:                   18clk: 0, Input : 0, States : 0 1 1, Output: 0;
Time:                   19clk: 1, Input : 0, States : 0 1 1, Output: 0;
Time:                   20clk: 0, Input : 0, States : 1 0 0, Output: 0;
Time:                   21clk: 1, Input : 0, States : 1 0 0, Output: 0;
Time:                   22clk: 0, Input : 0, States : 1 0 1, Output: 0;
Time:                   23clk: 1, Input : 0, States : 1 0 1, Output: 0;
Time:                   24clk: 0, Input : 0, States : 0 0 0, Output: 0;
Time:                   25clk: 1, Input : 0, States : 0 0 0, Output: 0;
```

Testbench Waveform:



Circuit Diagram:



Where the Flip Flop Outputs are Q_A, Q_B, and Q_C from the Left
The External Inputs Correspond To X, Clk
& External Output is Y