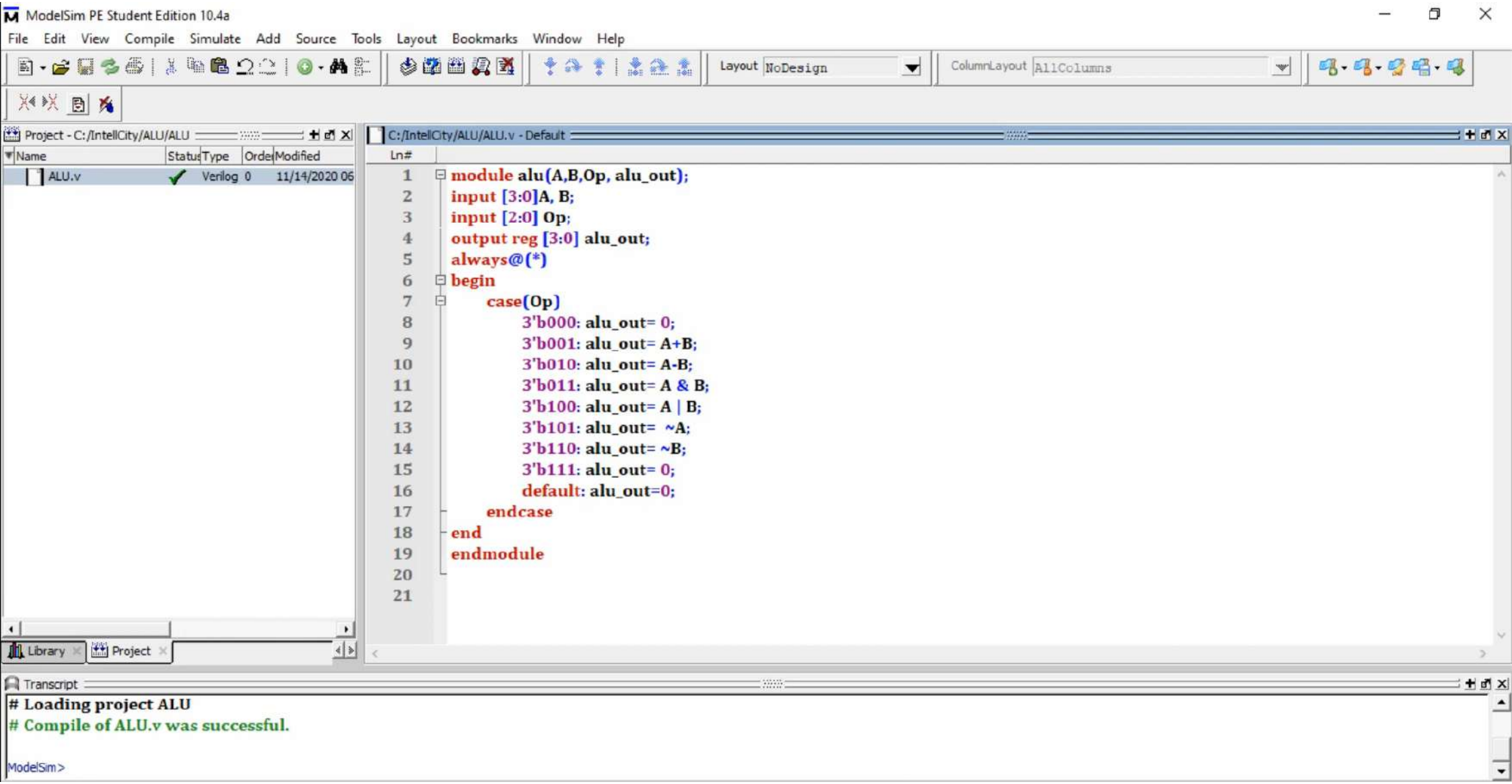
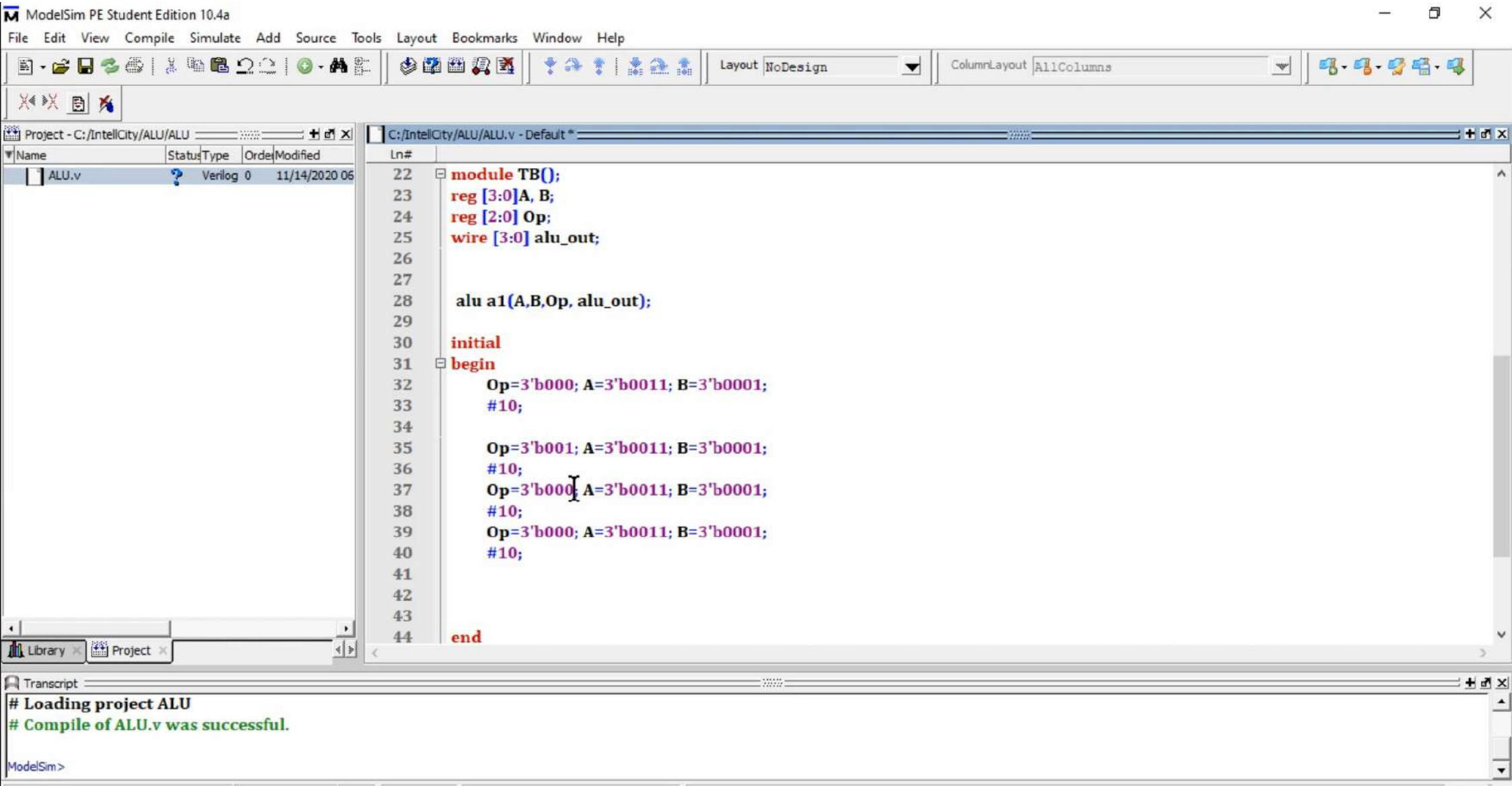
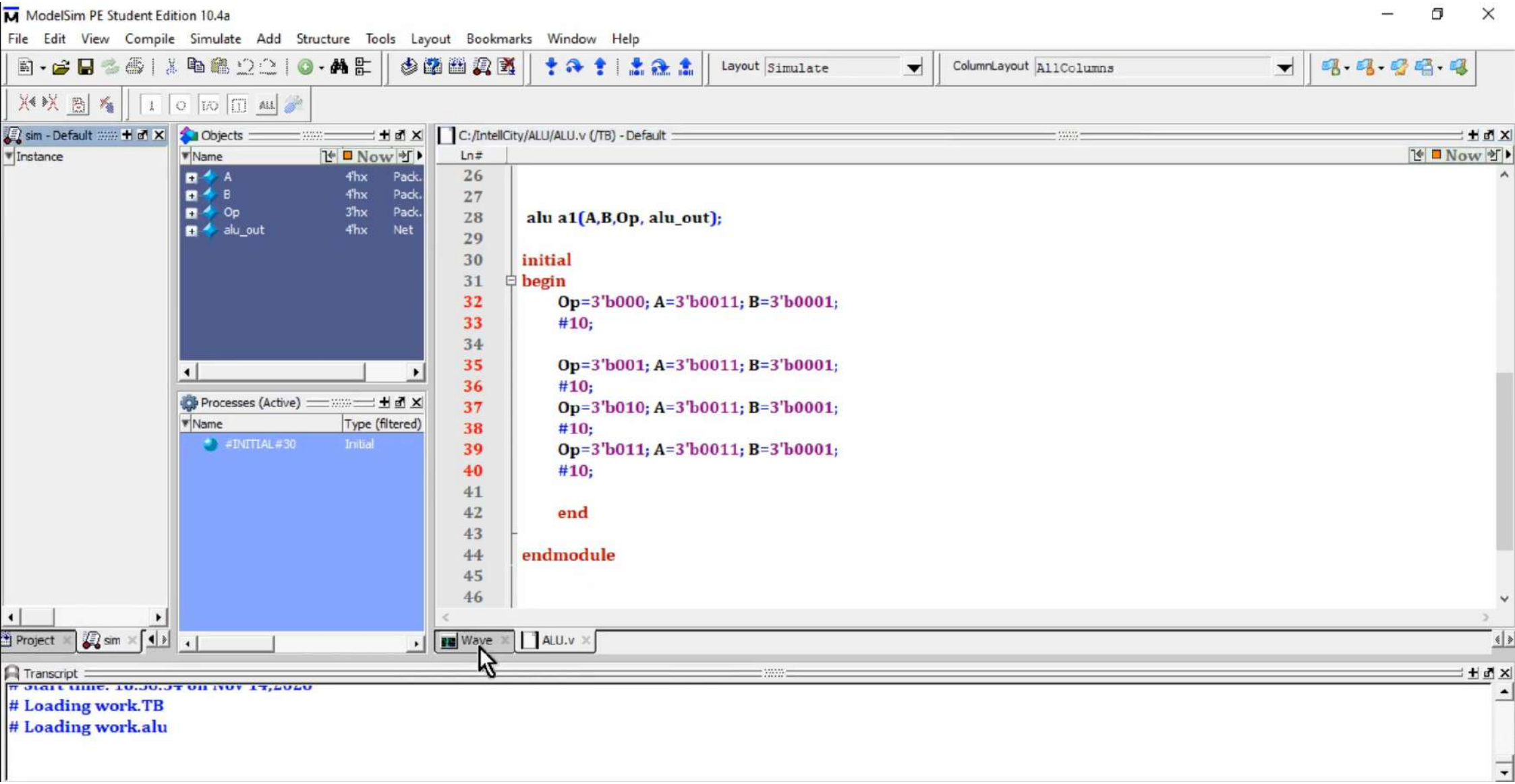
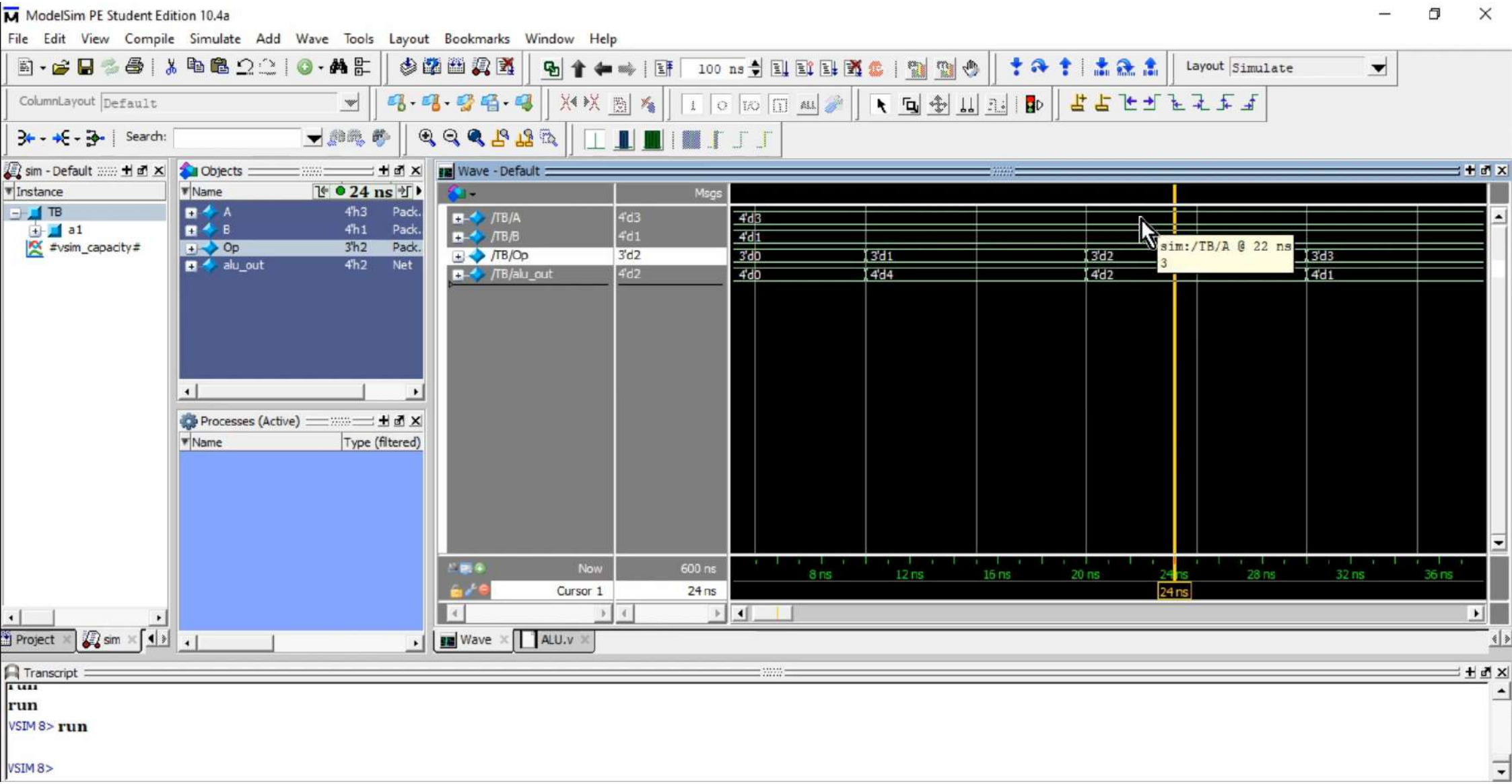

ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/IntelCity/ALU/ALU
Name Status Type Order Modified
ALU.v Verilog 0 11/14/2020 06
Library Project
C:/IntelCity/ALU/ALU.v - Default
Ln#
1 module alu(A,B,Op, alu_out);
2 input [3:0]A, B;
3 input [2:0] Op;
4 output reg [3:0] alu_out;
5 always@(*)
6 begin
7 case(Op)
8 3'b000: alu_out= 0;
9 3'b001: alu_out= A+B;
10 3'b010: alu_out= A-B;
11 3'b011: alu_out= A & B;
12 3'b100: alu_out= A | B;
13 3'b101: alu_out= ~A;
14 3'b110: alu_out= ~B;
15 3'b111: alu_out= 0;
16 default: alu_out=0;
17 endcase
18 end
19 endmodule
20
21
Transcript
Loading project ALU
Compile of ALU.v was successful.
ModelSim>


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help
Layout NoDesign
ColumnLayout AllColumns
Project - C:/IntelliCity/ALU/ALU
Name Status Type Order Modified
ALU.v Verilog 0 11/14/2020 06
Library Project
C:/IntelliCity/ALU/ALU.v - Default *
Ln#
22 module TB();
23 reg [3:0]A, B;
24 reg [2:0] Op;
25 wire [3:0] alu_out;
26
27
28 alu a1(A,B,Op, alu_out);
29
30 initial
31 begin
32 Op=3'b000; A=3'b0011; B=3'b0001;
33 #10;
34
35 Op=3'b001; A=3'b0011; B=3'b0001;
36 #10;
37 Op=3'b000; A=3'b0011; B=3'b0001;
38 #10;
39 Op=3'b000; A=3'b0011; B=3'b0001;
40 #10;
41
42
43
44 end
Transcript
Loading project ALU
Compile of ALU.v was successful.
ModelSim>


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Structure Tools Layout Bookmarks Window Help
Layout Simulate
ColumnLayout AllColumns
sim - Default
Instance
Objects
Name
Now
A 4'hx Pack.
B 4'hx Pack.
Op 3'hx Pack.
alu_out 4'hx Net
Processes (Active)
Name
Type (filtered)
#INITIAL#30 Initial
C:/IntelliCity/ALU/ALU.v (/TB) - Default
Ln#
26
27
28 alu a1(A,B,Op, alu_out);
29
30 initial
31 begin
32 Op=3'b000; A=3'b0011; B=3'b0001;
33 #10;
34
35 Op=3'b001; A=3'b0011; B=3'b0001;
36 #10;
37 Op=3'b010; A=3'b0011; B=3'b0001;
38 #10;
39 Op=3'b011; A=3'b0011; B=3'b0001;
40 #10;
41
42 end
43
44 endmodule
45
46
Project
sim
Wave
ALU.v
Transcript
Loading work.TB
Loading work.alu


ModelSim PE Student Edition 10.4a
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
sim - Default
Instance
TB
a1
#vsim_capacity#
Objects
Name
24 ns
A 4'h3 Pack.
B 4'h1 Pack.
Op 3'h2 Pack.
alu_out 4'h2 Net
Processes (Active)
Name
Type (filtered)
Wave - Default
Msgs
/TB/A 4'd3
/TB/B 4'd1
/TB/Op 3'd2
/TB/alu_out 4'd2
sim:/TB/A @ 22 ns
3
Now 600 ns
Cursor 1 24 ns
8 ns 12 ns 16 ns 20 ns 24 ns 28 ns 32 ns 36 ns
Project
sim
Wave
ALU.v
Transcript
run
VSIM 8> run
VSIM 8>