

U20ECCJ21

MICROPROCESSOR AND MICROCONTROLLER

UNIT III

PERIPHERAL INTERFACING & APPLICATION

Programmable Peripheral Interface (8255), keyboard display controller (8279), ADC, DAC Interface, Programmable Timer Controller (8254), Programmable interrupt controller(8259), Serial Communication Interface (8251).Interfacing and Programming 8279, 8259, and 8253

1) With a neat functional block diagram explain the functions of -mable Peripheral Interface [PPI]?

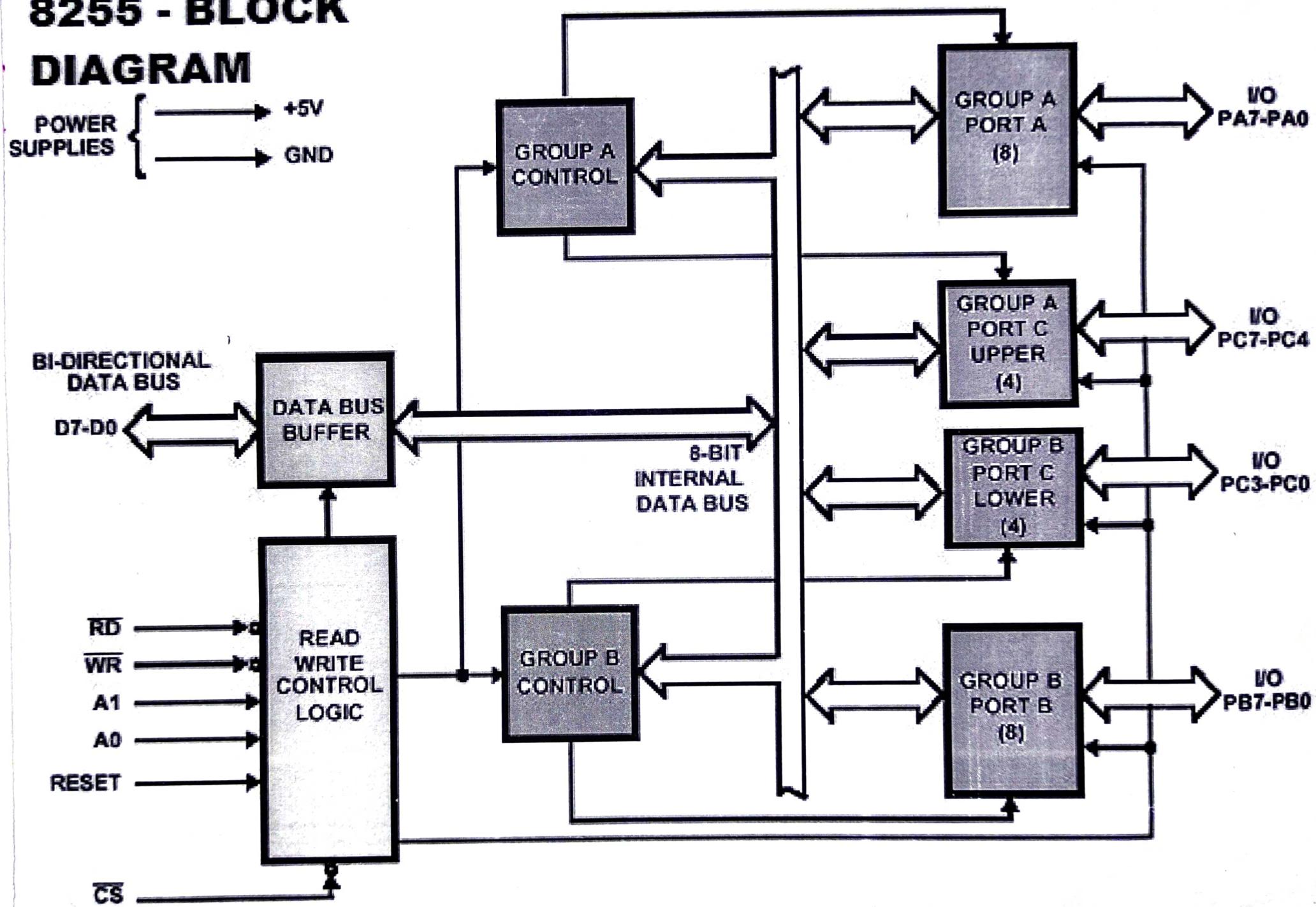
8255 - Programmable Peripheral Interface [PPI]

Features of 8255

- * It is a general-purpose Programmable I/O device used for parallel data.
- * It has 24 Input/output pins
- * It has 3 Port's
 - Port A - 8 pins
 - Port B - 8 pins
 - Port C - 8 pins
 - [Port Cupper - 4 pins & Port Clower - 4 pins]
- * It has two groups, Group A & Group B
 - Group A - Port A & Port Cupper
 - Group B - Port B & Port Clower.
- * It can program in 3-modes
 - mode 0 - Simple Input/output mode
 - mode 1 - I/O Ports with handShake
 - mode 2 ~~for~~ Bi-directional I/O data transfer.

8255 - BLOCK DIAGRAM

Block Diagram
of
8255.



A Programmable Peripheral Interface is a multiport device. The ports may be programmed in a variety of ways as required by the programmer. It has 3-Points Port A, Port B & Port C each of 8-Pins for Parallel Communication.

Port A:

It has 8-bit latched and buffered output and it can be programmed in three modes \rightarrow Mode 0, Mode 1, Mode 2.

Port B:

It has 8-bit latched and buffered output and it can be programmed in Mode 0 & Mode 1.

Port C:

It has 8-Bit unlatched input and latched & buffer output. Port C can be separated into two ports Port Cupper & Port CLower. It can be programmed for bit set / reset operation.

Data Bus Buffer :-

It is a tri-state bi-directional buffer. It is used to store the data from Microprocessor.

Control logic :-

The Control logic block accepts Control Signals. It has 6 Control Signal.

* \overline{RD} (Read) : It enables the read operation.

* \overline{WR} (Write) : It enables the write operation.

* $A_0 \& A_1$:- It is Used to Select Port's & Control Register.

$A_1 \quad A_0$

Select.

0 0

Port A

0 1

Port B

1 0

Port C

1 1

Control Register.

* RESET

:- It is Used to Reset 8255

* \overline{CS} (chip select) : It is used to chip select.

\overline{CS}	Select
0	8255 is selected
1	8255 is not selected.

to set the bit

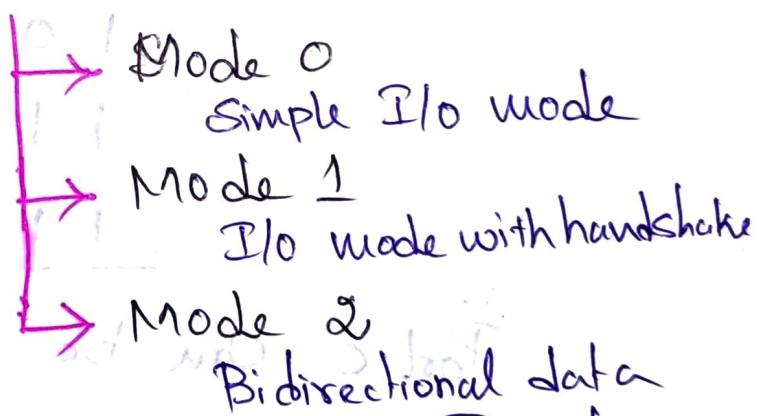
Modes of 8255:

If it is basically classified into two modes

Modes

* Bit Set Reset [BSR] mode

* Input/Output [I/O] mode.

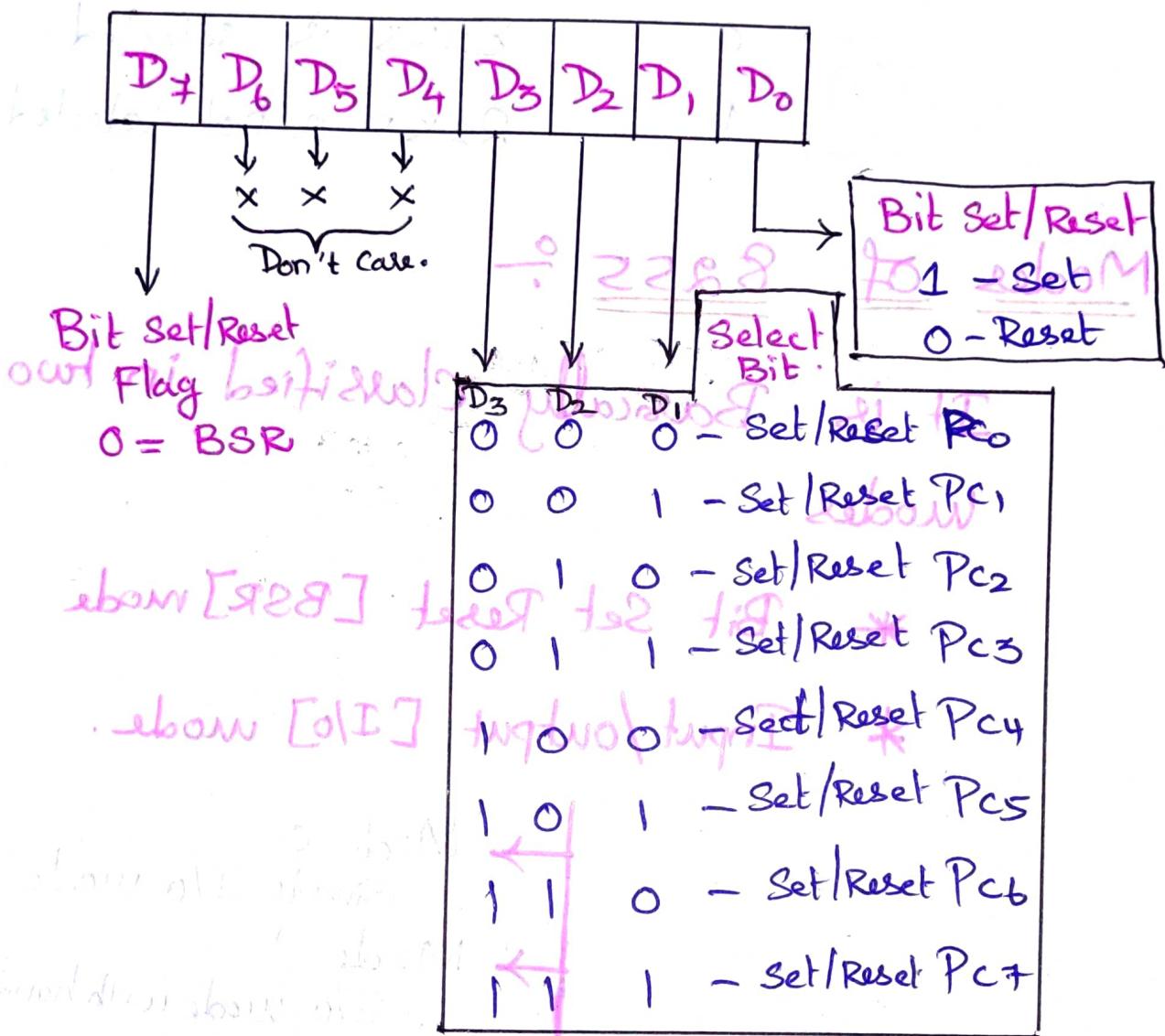


Bit Set Reset mode [BSR mode]:

The individual bits of Port C can be Set (or) Reset by Program.

↳ work with other pins of Port C
↳ work with Port B
↳ work with Port A

BSR Control word Format:



Port C Can be Set / Reset Depending on

the bit [D₀ and D₃ D₂ D₁] used to select

the bit.

I/O mode :

It has three modes

- * Mode 0: Simple I/O mode

- * Mode 1: I/O mode with handshake signal

- * Mode 2: Bidirectional I/O mode

Mode 0 ∵ Simple Input / output mode.

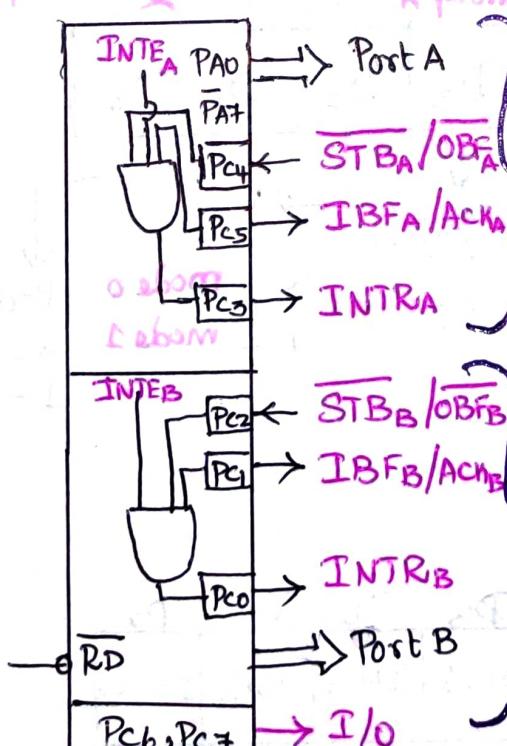
In this mode, the Port A, Port B and Port C is used as Input (or) Output Port.

Mode 1 ∵ Input / output mode with handshake

In this mode port A & Port B are used to transfer data and Port C is used for Control - Handshake Signals.

for Port A — \overline{PAO} , \overline{PAT} , $\overline{PC_3}$, $\overline{PC_4}$ and $\overline{PC_5}$ are used for Control

for Port B — $\overline{PC_0}$, $\overline{PC_1}$ and $\overline{PC_2}$ are used for Control



Port A with hand shake Signal

Input Control signal
STB - Strobe Input

IBF - Input Buffer Full.

Output Control Signal

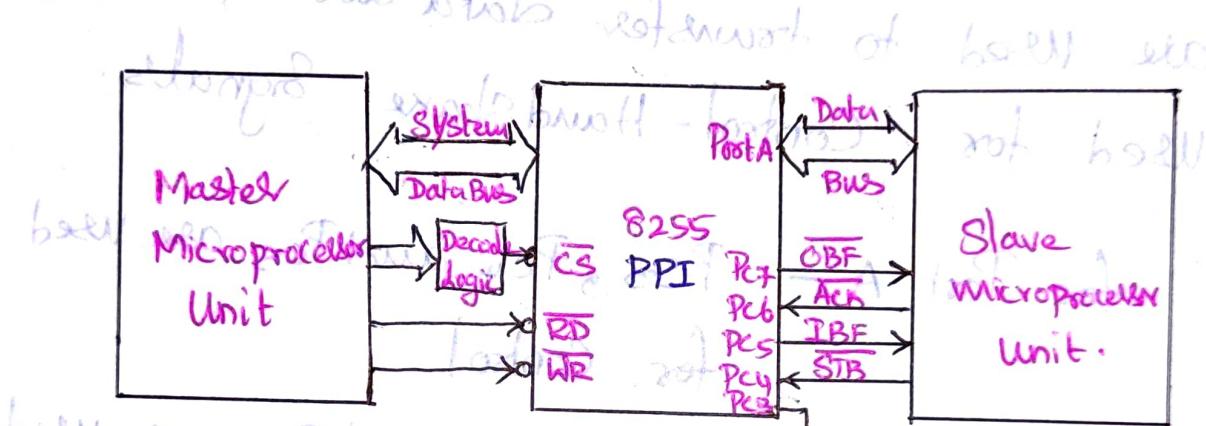
Post B with hand shake Signal.
 \overline{OBF} - Output Buffer full.
ACK - Acknowledge

Mode 2 : Bidirectional Bus I/O

When 8255 is operated in Mode 2, Port A can be used as bi-directional 8-bit

I/O bus using for handshaking.

Port B can be programmed in mode 0 or 1.



Control word for I/O mode

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
----------------	----------------	----------------	----------------	----------------	----------------	----------------	----------------

1 - I/O Mode

0 - mode 0
1 - mode 1
x - mode 2

Port A
1 - Input
0 - output

Port C (upper)
1 - Input
0 - output

Group B
0 - mode 0
1 - mode 1

Port C (lower)
0 - output
1 - Input

Port B
0 - output
1 - Input

Status word

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1/I	1/I	IBFA	INTE _A	INTR _A	INTE _B	IBFB	INTR _B

With a neat functional block diagram explain the functions of 8279 Keyboard/Display Controller?

Features of 8279

- * Key board and display can operate simultaneous.
- * Scanned keyboard mode
- * Scanned Sensor mode
- * 8-character Keyboard FIFO
- * 16-character display
- * Right to left entry 16-byte display RAM

It has Four Sections

* Keyboard

* Display

* Scan

* Cpu interface.

I/O Control and Data Buffers

The I/O Control Section Controls the flow of data to/from the 8279. It

is having four signal lines A_0 , \overline{CS} , \overline{WR} , \overline{RD} for control. PF88 to avoid conflicts

$DB_0 - DB_7$

These are bidirectional data bus

lines.

\overline{CS} \overline{RD} , \overline{RW}

Chip Selection, Read/Write.

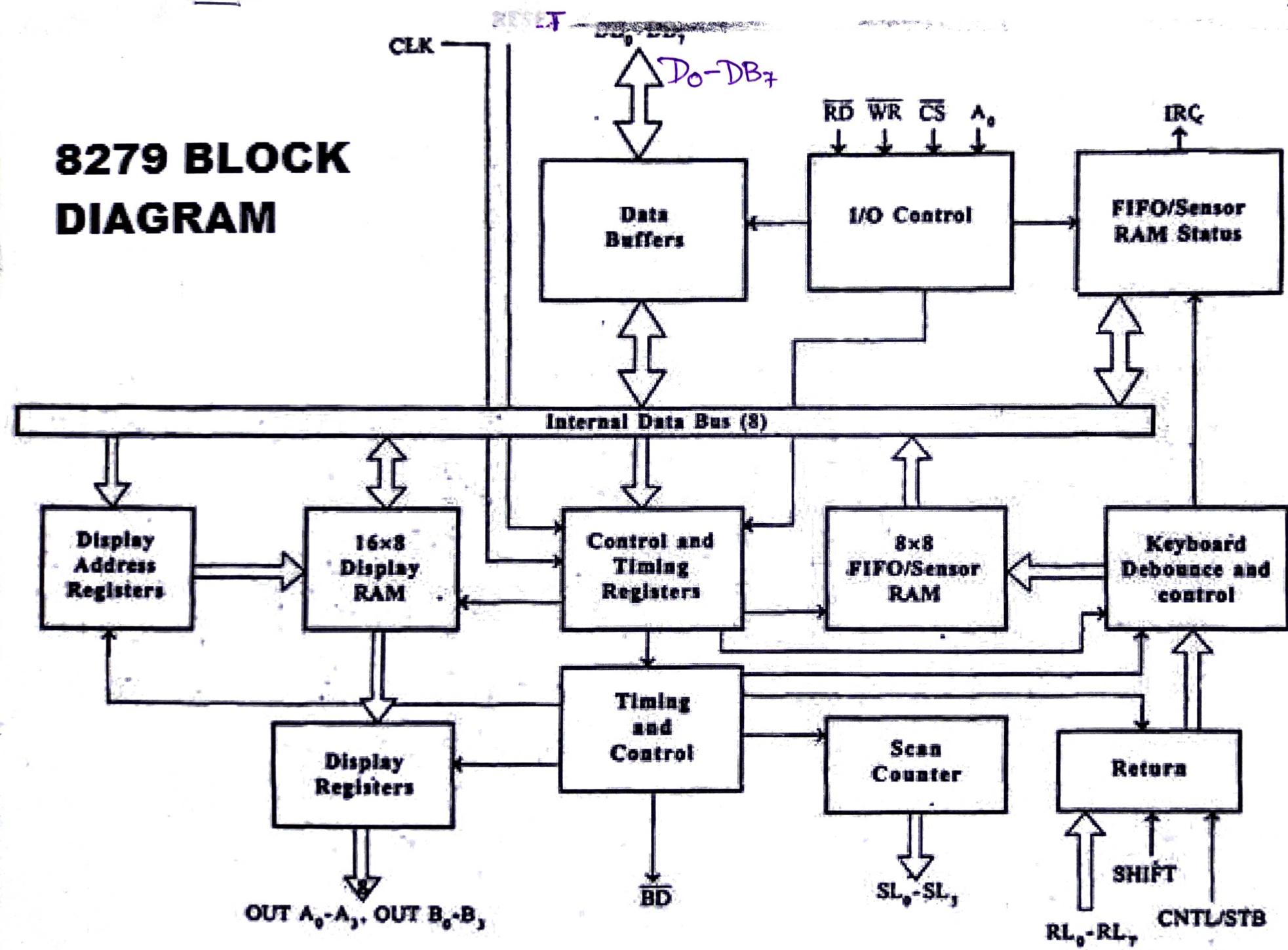
A_0 It is used to select internal registers.

\overline{RD} , \overline{RW} Read/Write.

Control and Timing Register and Timing Control.

These registers store the keyboard and display modes.

8279 BLOCK DIAGRAM



8279 - Block Diagram



BD - Blank Display.

Scan Counter :-

There are two ways

1) Encoded Mode

2) Decoded Mode.

SL₀ - SL₃ Scan lines :-

These lines are used to scan the key board matrix and display digits. Column.

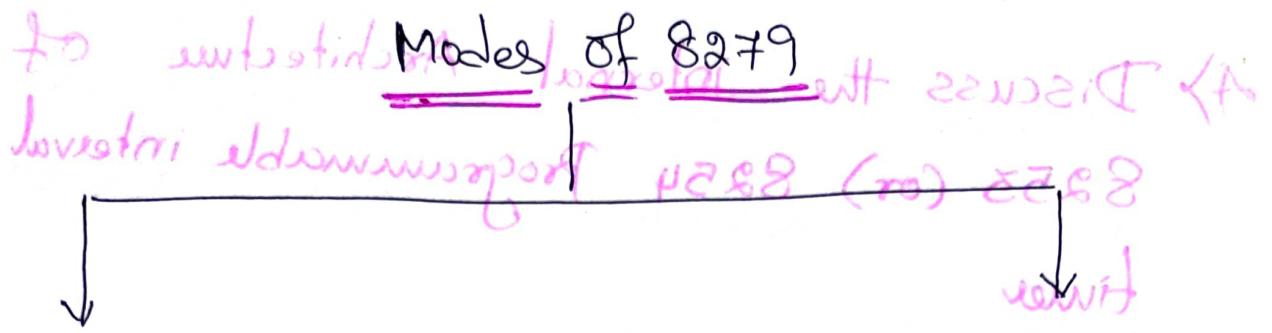
RL₀ - RL₇ - Return Lines :-

It is used to scan the rows of keyboard.

SHIFT :- Shift is used for Upper Case

Display RAM :-

It is used to store character for display. It can store 16-character of each 8-bit [16 byte].



Display Mode

Keyboard Mode

- 1) Eight 8-bit character \rightarrow Encoded Scan
Left entry \rightarrow 2 key lockout
- 2) Sixteen 8-bit character \rightarrow Decoded Scan
Left entry \rightarrow 2 key lockout
- 3) Eight 8-bit character \rightarrow Encoded Scan,
Right entry \rightarrow N-Key Roll over
- 4) Sixteen 8-bit character \rightarrow Decoded Scan,
Right entry \rightarrow N-Key Roll over
- 5) Encoded Scan, Sensor matrix
- 6) Decoded Scan, Sensor matrix
- 7) Strobed input Encoded Scan.
- 8) Strobed input Decoded Scan.

Control Word Format

0	0	0	D	D	K	K	K
---	---	---	---	---	---	---	---

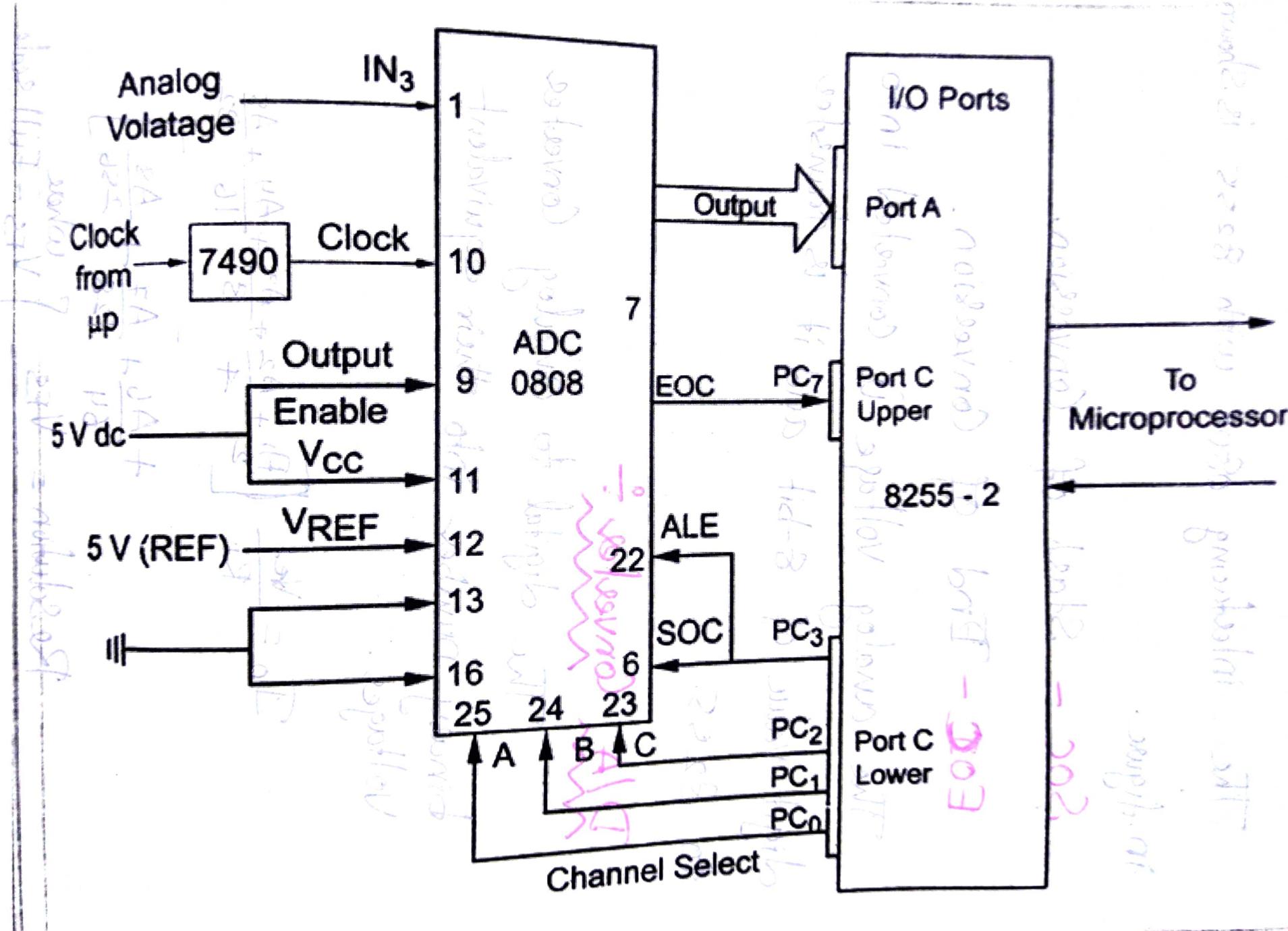
Display
Mode.

Key board
Mode.

7) Draw and describe the interfacing of A/D and D/A Converter interfacing to 8085 micro Processor.

Features of 0808/0809 ADC

- * 8-bit Successive approximation ADC
- * 8-channel multiplexer.
- * Conversion Time $100\mu s$
- * Easy to interface to all MP
- * Operates on single +5V
- * Output meets TTL Voltage.



The interfacing 0808 with 8255 is shown in figure.

SOC - Start of Conversion.

EOC - End of Conversion.

The analog voltage is converted into digit value of 8-bit and it is transferred to 8255

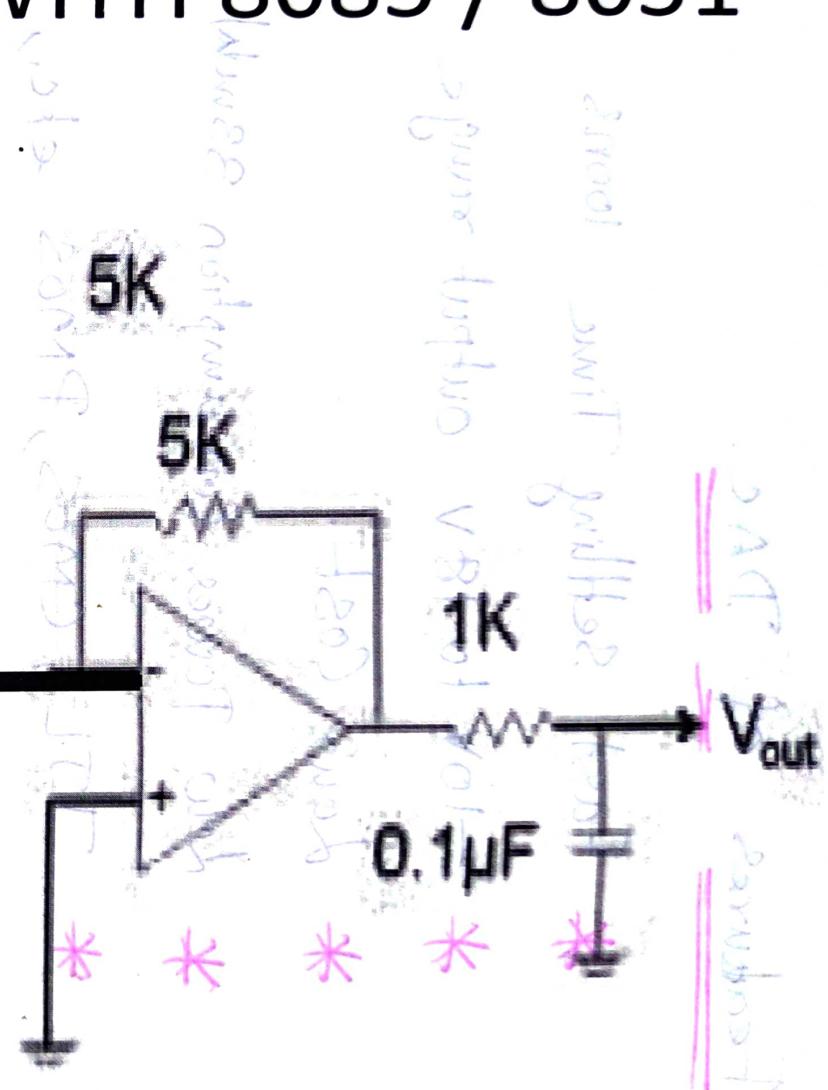
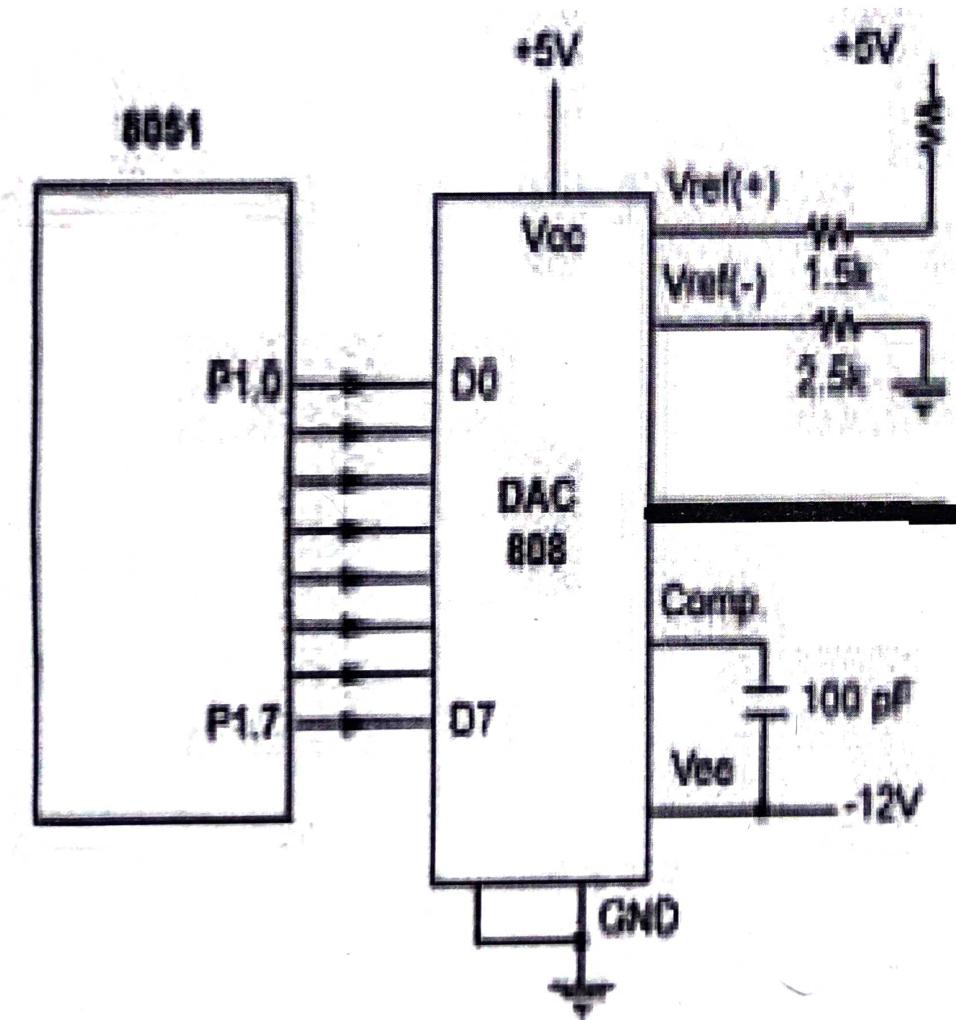
D/A Converter:

The digital to analog converter converts binary number into their equivalent voltages.

$$I_o = \frac{V_{ref}}{R_i} \left[\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right]$$

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1} \quad \begin{array}{l} \text{where} \\ V_{FS} - \text{Full scale} \\ \text{voltage} \end{array}$$

DAC INTERFACING WITH 8085 / 8051



Features of DAC.

- * Fast Settling Time (0ns)
 - * -10V to 18V output range
 - * Low Cost.
 - * Low Power Consumption (33mW)
 - * TTL, CMOS, PMOS etc.,
-
-

A) Discuss the internal Architecture of
8253 (or) 8254 Programmable interval
timer

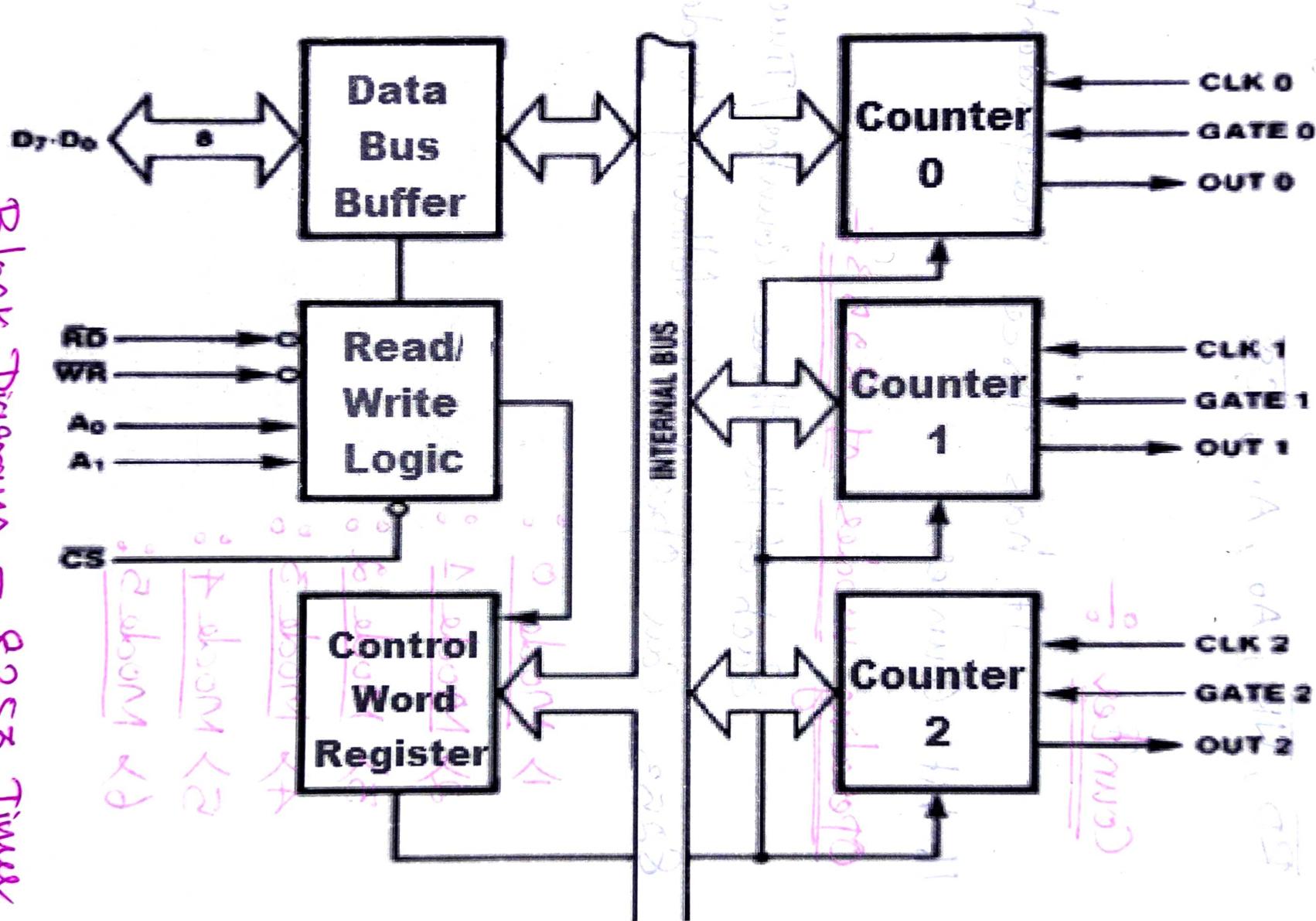
~~Key points~~
~~Topic~~

~~8081 project~~

Feature of 8253 Timer

- * Compatible with all Intel Microprocessors
 - * Handles Inputs from DC to 10MHz
 - * Clock frequency is 10MHz
 - * Status Read-Back Command
 - * 6- Counter Modes.
 - * 3- independent 16-bit counters
 - * Binary (or) BCD Counting
- Data Bus Buffer ~~forward~~ ~~backward~~ ~~loading~~
This 3-State, bi-directional, 8-bit buffer is used to store Data.

8253/8254 Block diagram



Read / write logic :-

It has 5 Control Signals.

\overline{RD} , \overline{WR} , A_0 , A_1 , \overline{CS}

Counter :-

It has three independent 16-bit Counter.

Operating modes of 8253 :-

Each of the three Counter/Timer of 8253 can operated in following modes.

- 1) Mode 0 : Interrupt on Timed Count
- 2) Mode 1 : Programmable one shot
- 3) Mode 2 : Rate Generator
- 4) Mode 3 : Square Wave Generator
- 5) Mode 4 : Software Triggered Strobe
- 6) Mode 5 : Hardware Triggered Strobe.

Unit 8 - microcontroller

Control Word Format

Hold	Mincount	Maxcount	Ext	Count	M2	M1	M0	BCD	bits count	LSB
Sc1	Sc0	R1	R0	M2	M1	M0	BCD	bits count	LSB	0 - Hexadecimal

(0000000000) PG PG 40 → 0 - Hexadecimal

Select Counter 0	0	0	0	0	0	0	0	1	BCD
Select Counter 1	0	1	Counter latch	0	0	1	0	0	Mode 1
Select Counter 2	1	0	LSB only	x	1	0	1	0	Mode 2
Select Counter 3	1	1	MSB only	x	1	1	1	0	Mode 3
			1 0 →	1	0	0	1	0	Mode 4
			1 1 →	1	0	1	1	0	Mode 5

Temporary & Frequency 8 Response FI *

First LSB

Next MSB

Condition function follows the expression below
 Mode 0 \div with Count is incremented when
 interrupt is given. *

about FI function and FI *

Mode 1 \div It is used as a monostable
 - Multivibrator trigger function.

Mode 2 \div It is used as divide by
 N Counter.

Mode 3 \div It is used as Square wave
 Generator mode.

Mode 4 \div It is used as Software
 Trigger mode. Strobe mode.

Mode 5 \div It is used as Hardware
 Trigger mode Strobe mode.

Ques 5) Draw and Explain the function block diagram of 8259 Programmable Interrupt Controller (PIC).

Features of 8259

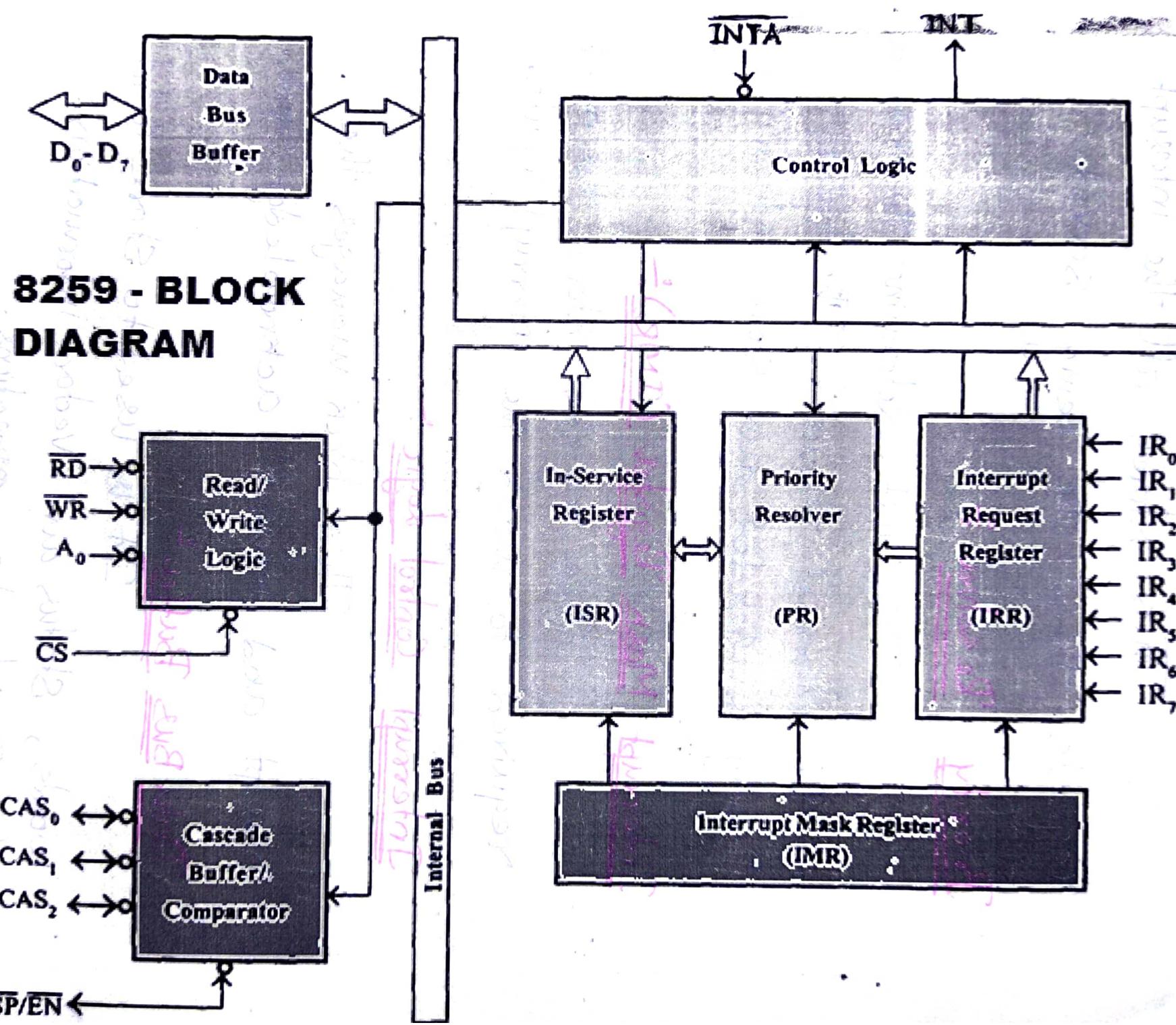
- * It manages 8 interrupt request.
- * Vector interrupt are mapped without additional hardware.
- * It extends up to 64 interrupt by cascading.
- * It has variety of modes.

Interrupt Request Register [IRR]

IRR Stores all the interrupt request in it in order to serve them one by one on the priority basis.

$IR_0 - IR_7$ (Interrupt Requests): These Pins act as inputs to accept interrupt request.

8259 - Programmable Interrupt Controller



In-Service Register (ISR) :-

This stores all the interrupt requests those are being served.

Priority Resolver :-

This unit determines the priorities of the interrupt requests. The highest Priority is Selected and stored into ISR.

Interrupt Mask Register (IMR) :-

This register stores the bits required to mask the interrupt inputs.

Interrupt Control logic :-

This block manages the interrupt and interrupt acknowledge Signals.

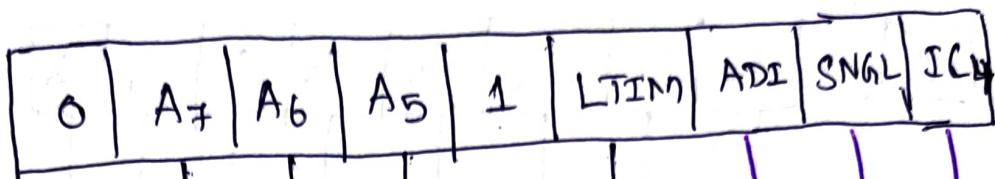
Data Bus Buffer :-

It is used to store control words, status and vector information.

for Read / write operations.
Question Answer - Page 8
www.allaboutcircuits.com

Initialization

Command word 1



soft trigger SI - 1

→ val 0

soft trigger SI - 0

→ A₇-A₅ bit

of interrupt

vector address

boot (brown) not initialized

1-ICW4
needed
0 - NO ICW4

1-single
0-cascaded

1 - Level Triggered

0 - Edge Triggered

asym - 1

sym - 0

1 - Interval of 4 bytes

0 - Interval of 8 bytes

W3 oWA - 1

W3 low - 0

Initialization x Command word 2

[sym] above last 4B - 0



T₇ - T₃ of
interrupt vector
Address.

Used to
Select
Vector
addresses

NEOM triggered

for NEOM - 1

for NEOM - 0

Initialization Command Word 3

Initialization I

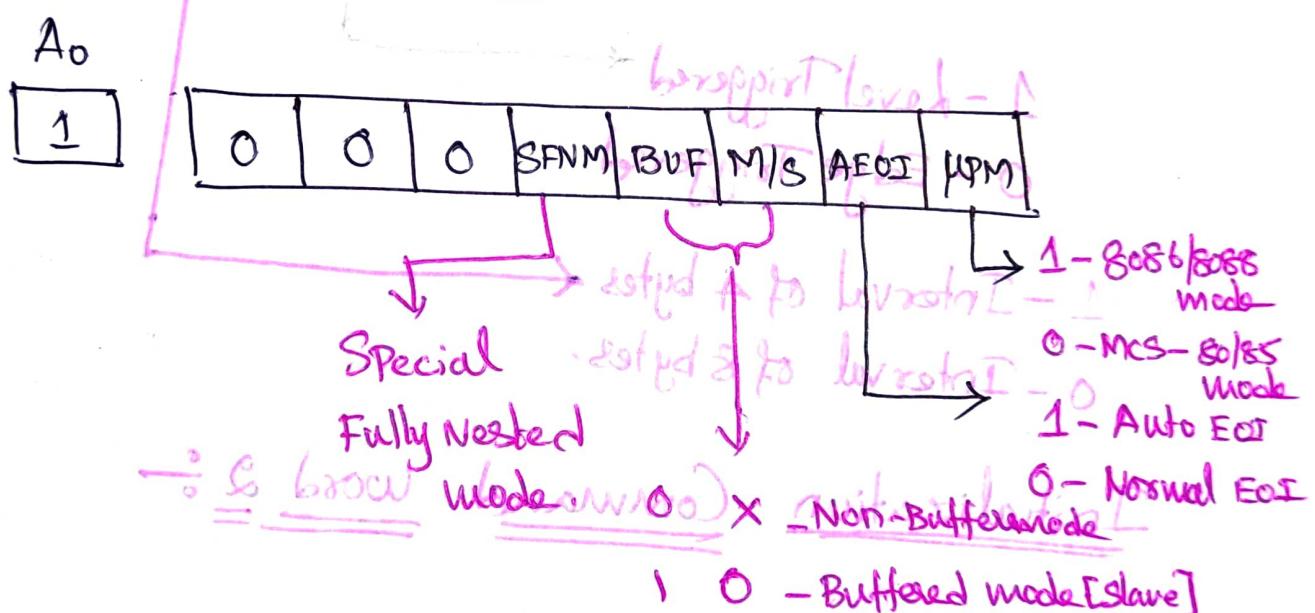


MWE-L
 between
 MWE-0

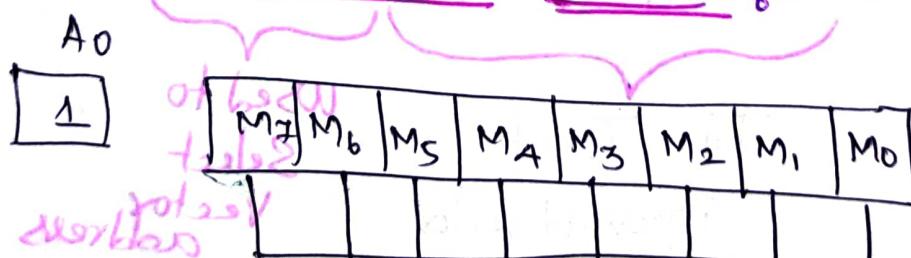
MZE-L
 between
 MZE-0

1 - IR input has a Slave
 0 - IR input does not have a Slave.

Initialization Command Word 4



Operational Command word 1



Interrupt Mask
 1 - Mask Set
 0 - Mask reset.

Operational Command Word 2.

Adjective noun verb adverb pronoun adjective adverb adjective adverb adjective adverb adjective adverb adjective adverb

IR level to be Acted
upon

1	R	SL	EOI	0	0	L ₂	L ₁	L ₀
---	---	----	-----	---	---	----------------	----------------	----------------

↓ ↓ ↓

0100101
0011001
00001111

0 0 1 - Non-Specific

0 1 1 - Specific EOI Command

1 0 $\frac{1}{2}$ Rotates on non-Specific EOI

1 0 0 - Rotate in automatic ECR-Set

0 0 0 - Rotate in automatic EOI - clear

1 10 10 10-9 * Rotate on Specific EOI

1 1 0 - * Set priority Command

0 1 0 - No operation.

Operational Command Word 3

Diagram illustrating the control register structure and its actions:

A0	O	ESMM	SMM	O	1	P	RR	RIS
----	---	------	-----	---	---	---	----	-----

Below the register:

- No action:** O, SMM, P
- Poll Command:** 1
- No poll p[0]:** RR
- Read IERON next RD:** RIS

Bottom row:

Reset Special mask → 1 0

Set special mask → 0 0 1 1

FEE8 → protipst

2) Draw the block diagram of 8251 USART
Serial Communication interface and Explain
each block.
Programmable Communication Interface

[Intel 8251 - Serial Communication]

USART - Universal Synchronous and
Asynchronous Receiver Transmitter

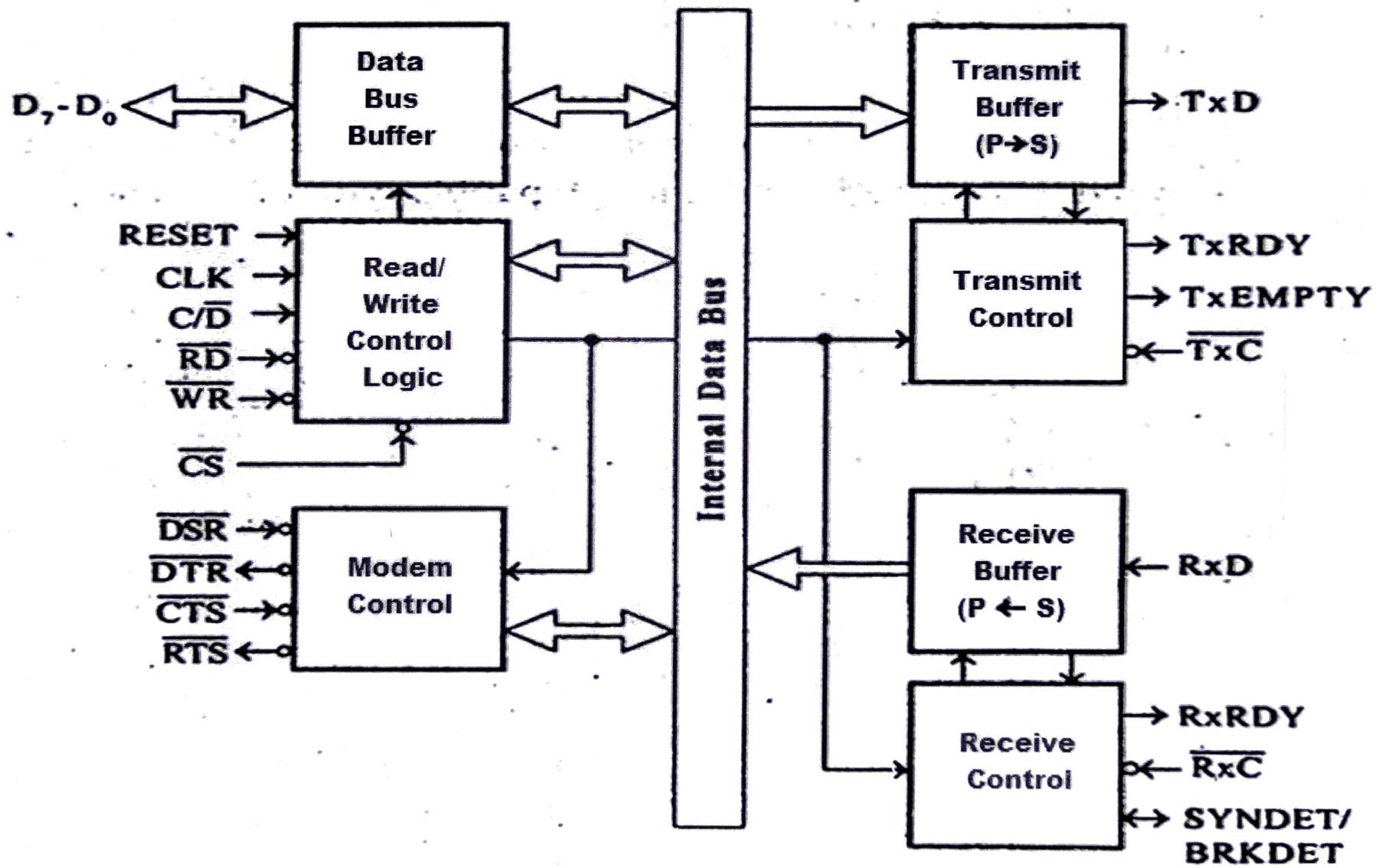
Features :-

- * The intel 8251 is an USART
- * 5 to 8 bit character Format
- Odd, Even (or) no Parity.
- Band rate from 0 to 19.2 K baud
- False Start Bit Detection.
- Break Character Generation.
- It allows full duplex transmission and reception.

Programmable Communication Interface (PCI)
is used for serial data transmission. It is a
Programmable chip designed for synchronous
and asynchronous data communication.

The 8251 can be used to transmit/
receive Serial data.

8251 - Architecture



Today we are going to understand about 8251, its architecture, communication interface, Communication modes, etc.

Block diagram of 8251

Page 10

Data Bus Buffer

It is used to store 8-bit data temporarily which is to be transmitted (or) received.

Read / write Control Logic

The R/W logic has 6 control signals.

C/D - control / data

WR - Write

RD - Read

RESET - Reset

CLK (Clock), RD and DI

This block consists of three Buffer

Registers (i) Control Register, (ii) Status Register

& (iii) Data Buffer.

Modem Control

It handles the modern handshake signals to coordinate the communication between the Modem.

Modem it has 4 control signals.

DSR - Data Set Ready

which indicates DTR - Data Terminal Ready.

RTS - Request to Send Data.

CTS - Clear to Send.

Transmitter Section

The transmitter accepts parallel data from the microprocessor unit and converts them into serial data. It has two registers.

(i) Buffer Register : To hold eight bits

(ii) Output Register : To convert 8-bit into a stream of serial bits.

It has following output signals

TxC - Transmitter Clock

TxD - Transmit Data

TxRDY - Transmitter Ready

TxEmpty - Transmitter Empty.

Receiver Section

The receiver accepts serial data on the RxD line from a peripheral and converts them into parallel data. It has two registers.

(i) Input Register (ii) Buffer Register.

It has RxD, RxC, RxRDY, SYNDET/BRKDET.

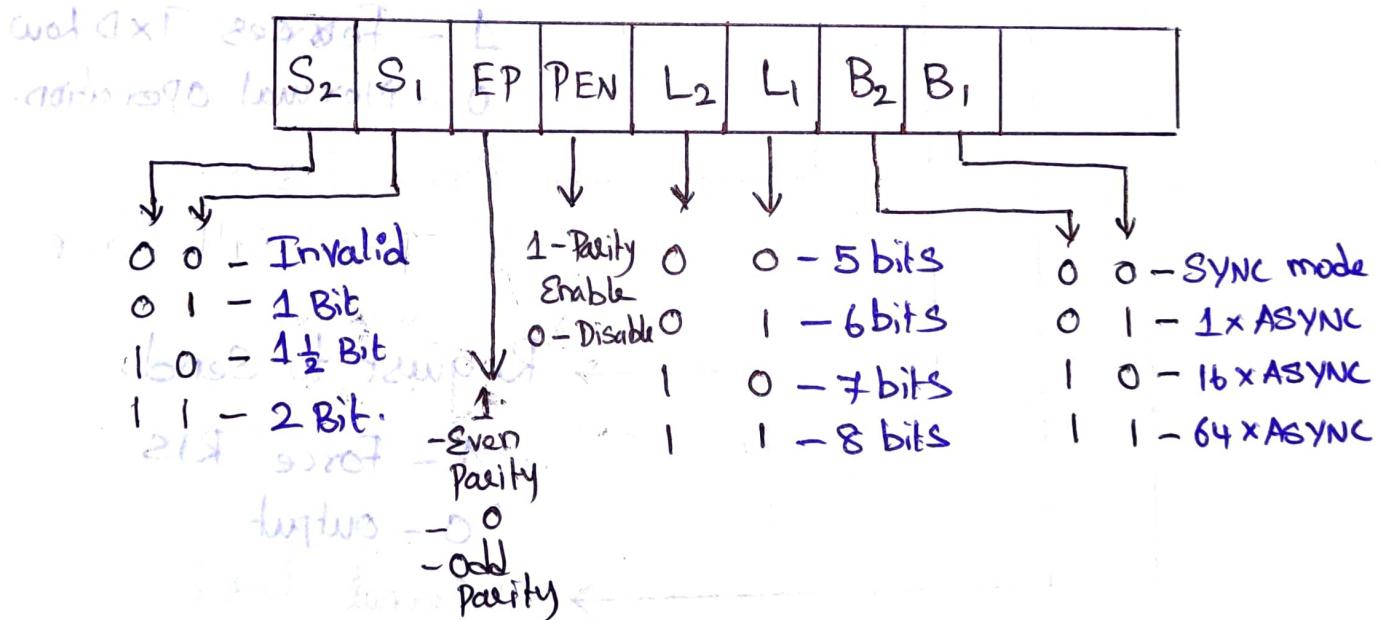
8251 Operating modes :-

Modes of 8251

- Asynchronous Mode (Transmission)
- Asynchronous Mode (Receive)
- Synchronous Mode (Transmission)
- Synchronous Mode (Receive).

Mode Instruction Control word :-

Instruction word bits :-



B₂ B₁ - Used to Select the Baud rate.

L₂ L₁ - Used to Select Character length.

PEN - Parity Enable.

EP - Even Parity.

S₂ S₁ - Used to Select the Stop bits

Status word format

