

# Pipelined Processor

EE309 Course Project

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[illegible]

FlowChart IITB-RISC-23								
		IF	ID	RR	EX	MA	WB	
NCU	R	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-3) => addr_Rc IR(2)=> complementBit IR(1-0)=>CZ	addr_Ra => RF_A1 addr_Rb => RF_A2	RF_A1=>alu_a not(RF_A2)=>alu_b alu_out=>data_out alu_cout => C alu_z=>Z	M_wr=0	addr_Rc => RF_A3 data_out => RF_D3	
			IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-3) => addr_Rc IR(2)=> complementBit IR(1-0)=>CZ					
			IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-3) => addr_Rc IR(2)=> complementBit IR(1-0)=>CZ					
NCC	R	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-3) => addr_Rc IR(2)=> complementBit IR(1-0)=>CZ	addr_Ra => RF_A1 addr_Rb => RF_A2	RF_A1=>alu_a not(RF_A2)=>alu_b alu_out=>data_out alu_cout => C alu_z=>Z	M_wr=0	addr_Rc => RF_A3 data_out => RF_D3	
NCZ	R	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-3) => addr_Rc IR(2)=> complementBit IR(1-0)=>CZ	addr_Ra => RF_A1 addr_Rb => RF_A2	RF_A1=>alu_a not(RF_A2)=>alu_b alu_out=>data_out alu_cout => C alu_z=>Z	M_wr=0	addr_Rc => RF_A3 data_out => RF_D3	
LLI	J	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-0) => imm9		imm9=>Ra(lower 9bit) 00_0=>Ra(higher 7bit)	M_wr=0		
LW	I	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6	addr_Rb => RF_A2	RF_D2=>alu_a imm6=>SE6=>alu_b alu_out=>data_out	data_out=>DMem_a	addr_Ra=> RF_A3 DMem_d => RF_D3	
			IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
SW	I	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode  IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6	addr_Rb => RF_A2	imm6=>SE6=> alu_a RF_D2 => alu_b alu_out=>data_out	data_out=>DMem_a	addr_Ra=> RF_A1 RF_D1=>DMem_d	
LM	J	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-0) => imm9					
SM	J	pc=>inc,IMem_A inc=>PC IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-0) => imm9					
BEQ	I	pc=>inc,IMem_A inc=>pc IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6	addr_Ra => RF_A1 addr_Rb => RF_A2	if reg A<reg B imm6 => alu1_a 2 => alu1_b alu1_out => alu2_a PC => alu2_b alu2_out=>PC	M_wr=0	NONE	
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
BLT	I	pc=>inc,IMem_A inc=>pc IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6	addr_Ra => RF_A1 addr_Rb => RF_A2	if reg A<reg B imm6 => alu1_a 2 => alu1_b alu1_out => alu2_a PC => alu2_b alu2_out=>PC	M_wr=0	NONE	
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
BLE	I	pc=>inc,IMem_A inc=>pc IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6	addr_Ra => RF_A1 addr_Rb => RF_A2	if reg A(<=)reg B imm6 => alu1_a 2 => alu1_b alu1_out => alu2_a PC => alu2_b alu2_out=>PC	M_wr=0	NONE	
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
			IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Rb IR(5-0) => imm6					
JAL	J	pc=>inc,IMem_A inc=>pc,pc_init IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-0) => imm9	addr_Ra => RF_A1	imm9 => alu1_a 2 => alu1_b alu1_out => alu2_a PC => alu2_b alu2_out=>pc	M_wr=0	addr_Ra=>RF_A3 pc_init => RF_D3	pc_init is carry forwarded till WB
JLR	I	pc=>inc,IMem_A inc=>pc,pc_init IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-6) => addr_Ra IR(5-0)=>0000000	addr_Ra => RF_A1	pc=>alu_a 2=>alu_b alu_out=>pc	M_wr=0	addr_Ra=>RF_A3 pc_init => RF_D3	
JRI	J	pc=>inc,IMem_A inc=>pc IMem_D=>IR	IR(15-12) => opCode IR(11-9) => addr_Ra IR(8-0) => imm9	addr_Ra => RF_A1	imm9 => alu1_a 2 => alu1_b alu1_out => alu2_a RF_A1 => alu2_b alu2_out=>pc	M_wr=0	NONE	

# DATAPATH

