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Survey on Bias Temperature Instability: Characterization, Modeling, and Security Implications in Advanced Process Nodes

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Abstract

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by

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This survey examines Bias Temperature Instability (BTI) [1] effects in advanced process nodes, with a focus on Negative Bias Temperature Instability (NBTI) in modern FinFET (Fin Field Effect Transistor) architectures. NBTI is critical, as it affects PMOS transistors more severely and causes larger threshold voltage shifts [2], impacting timing parameters in digital circuits, as compared to NMOS PBTI. This is increasingly significant for process nodes under 10 nm due to self-heating effects [3]. Several papers document the link between BTI aggravation and temperature, including the "Pentimento" phenomenon, where BTI-induced data remanence enables potential extraction of sensitive information from previously configured Field-Programmable Gate Arrays (FPGAs) [4]. Security vulnerabilities are exploited using side-channel attacks by using BTI to induce degradation in FPGAs. Results from the paper depict the stress and recovery profiles for NBTI and PBTI. The BTI effects were obtained as a result of analysis on a proprietary FPGA, with no information about the FPGA fabric. In order to investigate the circuits and BTI in detail, there are two components. One is accurately modeling BTI for advanced process nodes for FPGAs. Another element is creating a BTI-aware FPGA fabric using SPICE models created for BTI effects.

This survey analyzes various modeling approaches for BTI, ranging from the classical Reaction-Diffusion (R-D) model to advanced physics-based simulations. A SPICE-based BTI modeling of the open-source Sky130 Process Design Kit (PDK) [5] for a D Flip-Flop (DFF) was conducted. It reveals BTI-induced delays and threshold voltage shifts. While this workflow was sufficient in documenting the threshold voltage shifts, for a particular stress and temperature condition, it was insufficient to accurately model the stress and recovery process, especially for FinFET architectures.

By incorporating Technology Computer-Aided Design (TCAD) tools like Synopsys Sentaurus [6]–[9], suite into the workflow, a comprehensive and accurate workflow was created. It enables accurate characterization of both stress and recovery phases, which is crucial for understanding BTI's impact on circuit timing and security vulnerabilities. Comphy [10], a compact physics-based framework was evaluated, but found to be insufficient in characterizing BTI for 3-D structures. Future additions to this work can be the integration of this workflow with open-source predictive PDKs and integrating TCAD data with SPICE netlist and model card.

Chapter 1

Introduction

Bias Temperature Instability (BTI) has been a major topic of interest within the realm of the reliability of semiconductors. NBTI, specifically, has been a concern since 1966 [1]. Since then, The architectures have evolved from planar-based to FinFETs (Fin Field Effect Transistors) and GAAFETs (Gate All Around Field Effect Transistors), in combination with the aggressive scaling of technology nodes, owing to Moore's law. The scaling of gate oxides with the introduction of high-K metal gates has led to newer research areas on reliability and the evolution from planar FETs, to FinFETs and GAAFETs has ensured that reliability remains a major concern. Earlier research has shown an increase in PMOS NBTI when comparing 32nm, 28nm, 20nm and a 14nm Node, with the 14nm FinFET showing the largest increase in NBTI. While comparing planar and FinFET architectures, for the same 14nm node, FinFET showed a larger threshold Voltage shift [2]. As with any process, the device characteristics are directly

related to and affected by the orientation of semiconductor wafers in the crystallographic plane. This is further supported by the results of Young et.al, which bolsters the claim of FinFET reliability characteristics being orientation dependent [11]. Self-heating in FinFETs and GAAFETs, caused by limited heat dissipation paths, causes an increase in temperature. This leads to a faster and larger threshold voltage shift over time, which increases circuit delays [12]. As reported, up to 25% degradation in FinFETs for 7nm is due to self-heating-induced BTI and Hot Carrier Injection (HCI) effects, and 39% in 5 nm GAAFETs owing to self-heating.

In parallel, Hardware Security has been an ever-growing concern, especially with transistor scaling and 3D-ICs (Integrated Circuits). The density of transistors has increased significantly, enabling higher performance in a smaller form factor as compared to 2-D ICs. With the interconnect scaling and newer interconnect technologies like Through Silicon Vias (TSVs), heat dissipation becomes a major issue. These conditions provide impetus to reliability effects like BTI. There are several methods where BTI and NBTI, in particular, are used to cause hardware security attacks. This involves the use of NBTI to age and degrade the target faster to extract sensitive data. As per Calimera et.al, NBTI is a well-known circuit aging mechanism [13].

Attackers exploit this mechanism to age the circuit, which leads to threshold voltage shifts. Trojan Gates can be inserted and hidden in the 3D-IC, and threshold voltage shifts can be analyzed to recreate '0' or '1' [14]. In Cloud-based FPGAs, due to FPGA burn-in effects and 'pentimento', long-removed data can be accessed by using BTI

degradation [4]. As documented by Zick et.al, Lookup Table (LUT) burn-in in FPGAs can be used by attackers to recover intellectual property or even cryptographic secrets [15].

This may involve Trojan insertion to accelerate aging through NBTI to recover data. There could be hardware-based targeting for specific cores, where enable signals for the cores are applied with NBTI stress causing input vectors, or through software which attacks through reverse engineering as documented by Sengupta et.al. Another method is via obtaining the most threatful stress patterns [16]. TCAD-based simulation can be integrated while analyzing security challenges, in order to accurately model wear out, particularly for ones that use NBTI for degradation.

1.1 Scope and Contributions

- A survey on background, challenges, modeling and TCAD for Bias Temperature Instability.
- Demonstrating SPICE-based BTI modeling for planar CMOS, specifically for a DFF in Skywater 130 with clock to Q delay, and threshold voltage shifts for two temperatures (368 Kelvin, 423 Kelvin).
- Demonstrating TCAD-based BTI modeling for an advanced 7nm FinFET PDK with threshold voltage shifts for two temperatures (368 Kelvin and 423 Kelvin).
- Evaluating hardware security attacks and the use of BTI.

- Comparison of results from TCAD to results from the pentimento paper by Drewes et.al [4].
- Future work including extracting SPICE parameters from TCAD to create BTI-aware FPGA fabric.

Chapter 2

Background

2.1 Physical Mechanism of BTI

BTI is a degradation phenomenon wherein transistors degrade over time due to stress (gate bias) and elevated temperatures, leading to an increase in threshold voltages. The increase in threshold voltages leads to slower transistor switching, leading to time delays in circuits. This delay reduces reliability and shortens the Mean Time Between Failure (MTBF). BTI causes threshold voltage increase and degrades mobility, drain current, and transconductance of p-channel MOSFETs [17]. A negative gate voltage bias at elevated temperatures leads to NBTI degradation in PMOS devices. The mechanism is attributed to the breaking of Si-H bonds at the SiO2/Si substrate.

Silicon (Si) is a chemical element with atomic number 14, and an electron configuration $1s^2\,2s^2\,2p^6\,3s^2\,3p^2$. Silicon is bonded to Hydrogen atoms, and these bonds

are present at the interface between the silicon substrate and the gate oxide in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Under stress conditions, particularly high negative gate bias voltage and elevated temperature, these Si-H bonds break, causing the release of hydrogen. The broken Si-H bonds lead to the creation of "interface traps". These traps often capture electrons or holes, which directly relate to a shift in the electric field in the channel region of the MOSFET. This shift requires a higher gate voltage to turn on the transistor, leading to an increase in the threshold voltage (V_{th}). The rise in V_{th} degrades the performance of the transistors, through reduced transistor switching, directly causing timing delays.

2.2 NBTI in Advanced Technology Nodes

NBTI continues to be a reliability concern with the scaling of process nodes and with changing architectures from planar to FinFETs and GAAFETs. Choi et.al establishes that despite better electrostatics, narrower fins with increased (1 1 0) sidewall area led to enhanced PMOS NBTI reactions under negative gate bias and elevated temperature conditions [3]. The key finding from this research is that NBTI remains a concern for the processes that were studied, ranging from 28 nm planar devices to 5nm FinFET devices. Self-heating being a substantial contributor to NBTI, incorporating self-heating effects into TCAD and compact reliability models would increase the accuracy of the predictions of the lifetime of the transistors. GAAFETs show a similar degradation due to NBTI that is enhanced by self-heating. However, GAAFETs

have a faster recovery, especially in (1 0 0) surfaces due to faster re-passivation, i.e. faster hydrogen re-binding at the Si-H interface, when compared to FinFETs. The 3nm GAAFET/ 'MBCFET' (multi-bridge channel FET) shows a notable improvement in NBTI by around 20 % compared to 4nm and 8nm FinFETs, for (1 0 0) according to Kim et.al [18]. Amongst other reliability concerns like TDDB (Time Dependent Dielectric Breakdown) and HCI (Hot Carrier Injection), BTI remains the most prominent reliability concern.

2.3 Modeling approaches for BTI

BTI affects sequential and combinational circuits in a distinctive manner and the degradation rate varies significantly depending on the switching activity, with differences of up to 5x between various operating conditions [19]. Lower temperature helps in mitigating BTI effects, which in turn would help in prolonging the circuit lifespan. BTI has been mathematically described using equations to calculate threshold voltage shifts, using either the power-law or the physics-based reaction-diffusion model (R-D model) [20]. The tradeoff, in terms of deciding a modeling framework, is computational speed vs accuracy of modeling.

2.3.1 Power Law

Amongst the simpler modeling approaches, the power-law model is one of the easiest, to obtain threshold voltage shifts and visualize them graphically. Power-Law ensures

quick computation at the cost of accuracy. Several circuit reliability papers analyze BTI at a circuit level and approximate degradation as a power-law function of time. It serves as an elegant way to represent the degradation caused by BTI. It, however, does not model the underlying mechanism of trap generation and recovery to simulate degradation. Power-law-based modeling is computationally efficient, thus allowing for quick estimation of long-term degradation caused by BTI. This data-fitting model is SPICE-ready and can be directly used to analyze voltage shifts. One of the major drawbacks of this model is that it cannot predict recovery beyond the fitted range. It has an extremely high accuracy near the fit range, but accuracy is abysmal when extrapolated.

$$\Delta V_{th} = A \times t^n \tag{2.1}$$

Symbol	**Definition**
A	Prefactor constant; depends on oxide thickness, electric field, temperature, and process variations
t	Stress time (in seconds)
n	Time exponent; determines the rate of degradation over time

Table 2.1: Definitions of Power-Law Model Parameters

A smaller 'n' indicates a slower degradation rate, and a larger value suggests a

rapid degradation. The length of the channel has a major influence on BTI. Shorter channel lengths in sub-20nm FinFETs worsen BTI due to higher lateral electric fields. Gate oxide quality, arrangements in the structure like (1 1 0), (1 0 0), strain directly affect the prefactor 'A' [21].

2.3.2 R-D Modeling

The Reaction-Diffusion (R-D) model is based on bond-breaking and diffusion physics. It is computationally expensive and has very high accuracy in modeling 3-D structures with stress and recovery parameters for given gate bias and temperature conditions. The main advantage of the R-D model over the power-law model is the insight into mechanisms of trap formation and dissipation. It has a considerably large number of parameters as compared to the four to five parameters required for the power-law model. This model is fundamental in understanding TCAD applications, as it is a popularly used modeling technique. For this proposed workflow, the TCAD tool, Synopsys Sentaurus TCAD, uses R-D modeling in addition to the other models listed. The reaction-diffusion model is a combination of two effects - reaction and diffusion, As described by Entner et.al [22].

Reaction Phase : A chemical reaction at the Si/SiO2 interface breaks the Si-H bonds, which results in the creation of interface traps. This effectively generates (Si^{+}). The electrically active interface and the mobile hydrogen form X. The trap generation is influenced by the forward rate constant (K_f).

Diffusion Phase : The freed hydrogen atoms diffuse away from the interface into the oxide, which lowers the local H concentration and causes further Si-H dissociation. On removal of stress, some H migrates back, which enables partial repair of recovery. This mechanism is used to demonstrate the stress and recovery phases of degradation caused by BTI. The annealing is influenced by a reverse rate constant for trap annealing (K_r).

$$\text{Si} - \text{H} \rightleftharpoons \text{Si}^{\cdot} + X_{\text{interface}} \tag{2.2}$$

The hydrogen moves away from the interface to the dielectric and is represented by

$$X_{\text{interface}} \rightleftharpoons X_{\text{bulk}} \tag{2.3}$$

This process can also work in the reverse direction, i.e. transport of diffusing hydrogen species back to the interface and re-passivation of a Si^{+} dangling bond. The equation for this process at the interface is given by a rate equation.

$$\frac{\partial N_{it}(t)}{\partial t} = k_f(N_0 - N_{it}(t)) - k_r N_{it}(t) N_X(0,t)^{1/a} \tag{2.4}$$

Symbol	Definition
K_f	Forward rate constant (reaction rate for bond dissociation or trap generation)
K_r	Trap annealing rate constant (associated with passivation or bond reformation)
N_0	Initial number of electrically inactive Si-H bonds
$N_x(0,t)$	Surface concentration of the diffusing species at position 0 and time t
a	Order of the chemical reaction (typically 1 or 2 depending on the mechanism)
t	Time in seconds

Table 2.2: Definitions of Reaction-Diffusion Model Parameters

Reaction-Drift-Diffusion (RDD) model : This model is an extension of the RD model, with the difference in modeling being that RDD also generates hydrogen ions (H_2^+) in addition to hydrogen atoms and molecules.

Activated barrier double-well thermionic (ABDWT) model : ABDWT model calculates the transition rate between the uncharged and charged states on the thermionic barrier.

Transient trap occupancy model (TTOM): This model uses the ABDWT model formulation to compute the charge occupancy and calculate the total traps generated at both interfaces.

Chapter 3

Modeling BTI in Sky130 PDK

This chapter presents a workflow to model BTI for a D Flip-Flop using Skywater 130 (Sky130 nm) PDK. The aim of using a 130nm PDK is to investigate the effect of BTI in planar nodes. The use of SPICE-based analysis tools helps in rapid analysis of BTI for a large number of transistors.

In order for the open-source PDK to integrate with proprietary SPICE tools, several regex-based edits are made to the `libs.ref` and `libs.tech` files. The models for pfet and nfets used in the D Flip-Flop, are converted from being subcircuit definitions to model definitions. This enables integration with the tools. The results are obtained in several file formats, and present two major observations:

- The temperature dependence of BTI and clock to q delay, as depicted in Figures 3.2 and 3.4.

- The threshold voltage shifts ΔV_{th} due to NBTI and PBTI as shown in the Figure

3.6.

3.1 Experimental Setup

This workflow presents the modeling of BTI degradation in a Sky130-based DFF standard cell using the Synopsys PrimeSim MOSFET Reliability Analysis (MOSRA) [23]. This tool is an add-on to the Synopsys PrimeSim HSPICE [24] tool. The objective is to simulate transistor-level BTI effects in a DFF `sky130_fd_sc_hd__dfxtp_4` with `sky130_fd_pr__pfet_01v8_hvt`, `sky130_fd_pr__nfet_01v8`.

The outputs of MOSRA include several files as shown in table 3.1. The SPICE netlist A for this contains SPICE commands along with MOSRA specific commands to model BTI. The netlist includes an extracted DFF subcircuit with manually instantiated transistors. The MOSRA block controls BTI simulation with parameters like `reltotaltime` which is the reliability test time, `aging start` and `aging stop` which define the start and stop time of aging in transient simulation. Some of the BTI parameters are approximated or use the Synopsys provided default values due to the lack of availability of such reliability parameters for a PDK. As previously mentioned equation 2.1 , the 'A' and 'n' are PDK-dependent and would require PDK specific data for accurate analysis. and The accuracy of this workflow can be further improved by using PDK-relevant accurate BTI parameters for MOSRA. The bias direction and it's effects on BTI, also will require further work.

The workflow begins with SPICE netlist which defines the subcircuit (DFF in this

case), with BTI parameters and appends these MOSRA-enabled models to the pre-existing Sky130 pfet and nfet models . The output is obtained as shown in 3.1. The transient simulation is analyzed using Synopsys Waveview [25]. The setup is divided into step intervals of 72000 for a total reliability test time of 7200000 seconds or 200 hours. The temperature is manually set to 94.85 ° Celsius or 368 Kelvin and 149.85 ° Celsius or 423 Kelvin.

Symbol	**Definition**
$RADEG(.radeg0)$	Contain degradation data, particularly ΔV_{th} shifts which can be obtained in a .csv format.
$MT0(.mt0), ST0(.st0)$	Contain measurement values, status files.
$TR(.tr0)$	Transient analysis output files which can be viewed using Synopsys Waveview.

Table 3.1: Definitions of MOSRA outputs

3.2 Challenges in PDK compatibility

The sky130 PDK uses certain mathematical symbols such as $+$, $-$, $*$, and $\hat{}$ in the libs.tech and libs.ref files. However, Synopsys PrimeSim MOSRA does not support such characters in model expressions. To resolve this, a regex-based script was used to convert the characters to an HSPICE-compatible format [26]. This involved copying

the entire libs.tech and libs.ref directory to a separate folder in which the script was used. While Sky130 provides transistor models, these are often used inside subcircuits, rather than stand alone model declarations. Synopsys MOSRA requires BTI modeling to be enabled using models instead of the subcircuit. In order to resolve this

- The transistor-level instances from the standard cell are extracted and the subcircuit is flattened into explicit transistor statements i.e. M 0, M1 instead of X0, X1 as documented in the SPICE netlist A.
- All Xn subcircuit calls are replaced with Mn transistor elements, in order for the appendmodel statement to associate the MOSRA models with each device.
- Model definitions for the pfet and nfet being used are copied into two separate files, where each file includes the transistor model parameters from the PDK, instead of being defined as subcircuit parameters.

```
55 .appendmodel mosra_n mosra sky130_fd_pr__nfet_01v8__model* nmos
56 .appendmodel mosra_p mosra sky130_fd_pr__pfet_01v8_hvt__model*
     pmos
```

Listing 3.1: `appendmodel` applied to all transistor bins.

Each PDK categorizes transistors across manufacturing or simulation corners such as TT for typical timing, FF for Fast PMOS, Fast NMOS into 'bins'. Here, the wildcard `'*'` is used to append all bins in the spice model, as depicted in 57. This workflow requires well-established parameters in order to accurately model BTI, in particular,

access to fitting parameters is required, which are closely guarded secrets. If such parameters are available, MOSRA can work with parameters extracted from the PDK in order to model BTI with a greater accuracy.

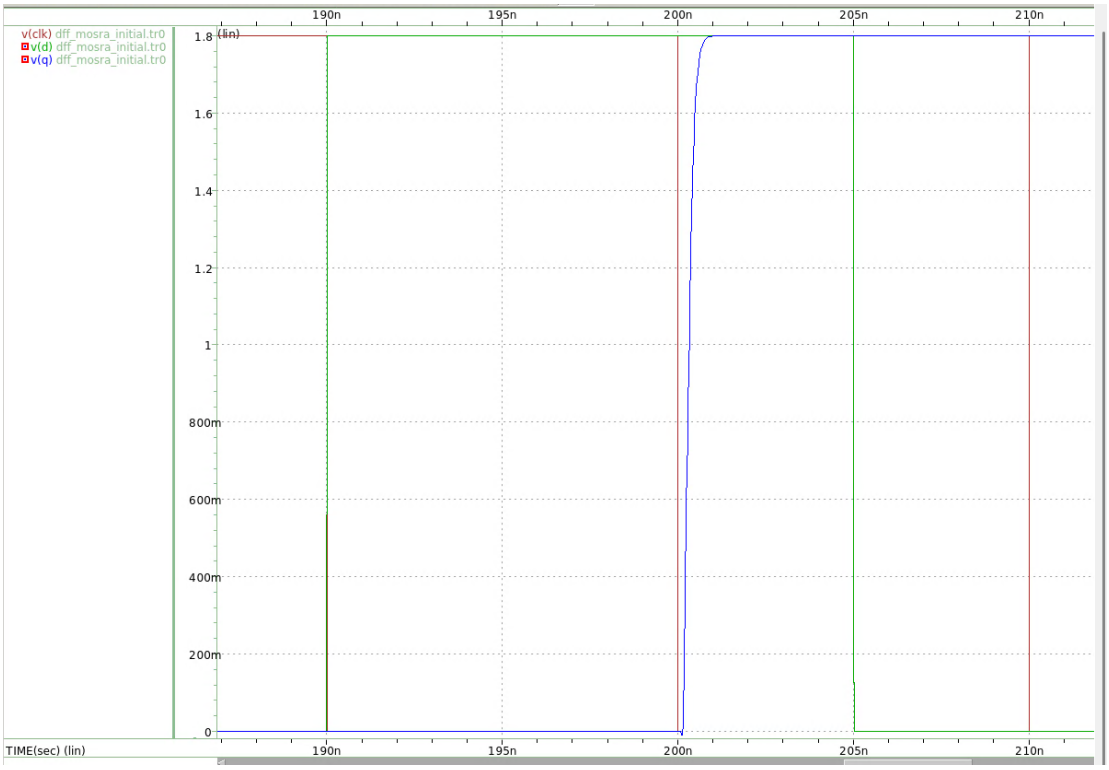

Figure 3.1: The waveview plot shows a D-FF in sky130. Clock (v(clk), data v(d), and output v(q) are depicted with no aging.

3.3 Results

This section presents the impact of BTI-induced degradation on the threshold voltage and clock-to-q delay in Sky130 DFF `sky130_fd_sc_hd__dfxtp_4` across two temperature conditions: 94.85 ° Celsius or 368 Kelvin and 149.85 ° Celsius or 423 Kelvin. As depicted in the Figure 3.1 shows a typical DFF with input D, clock clk, and output

Q without any BTI. A transistor-level simulation for 30-transistors in the DFF was conducted using HSPICE with MOSRA aging enabled. The clock to q delays are depicted in the Figures 3.2, 3.3 and 3.4, 3.5. Transistors speed up as they get hotter with the increased temperatures, as seen in the results of the plots 3.2 and 3.4. This explains the earlier start baseline for the 149.85 ° Celsius condition. The aging effects for these are as follows:

- The Clock to Q delay $\Delta clk2q$ for 149.85 ° Celsius: $306.494 - 303.868 = 2.626$ ps
- The Clock to Q delay $\Delta clk2q$ for 94.85 ° Celsius: $311.943 - 310.338 = 1.605$ps

This shows the effect of temperature on BTI, and BTI-induced delay. As per the Figure 3.6 shifts in threshold voltage are observed, for both PMOS and NMOS instances of the 30 transistors at each simulation step, obtained using the `.radeg0.csv`, which was enabled using a command in the netlist `.option radegoutput=csv`.

As observed in previous studies, the degradation is more significant for PMOS (NBTI) than NMOS (PBTI) for lower as well as higher temperatures. For example, xdff.m0 and xdff.m1, as depicted in Figure 3.6 showed a greater threshold voltage shift ΔV_{th} for PMOS than for NMOS. These results establish the need for accurate PDK-specific BTI parameters, and how PMOS devices are more prone to degradation due to BTI. The delay degradation, and threshold voltage shift ΔV_{th} may vary with availability of PDK specific parameters. This lead the workflow to use the TCAD approach in absence of PDK-specific BTI parameters.

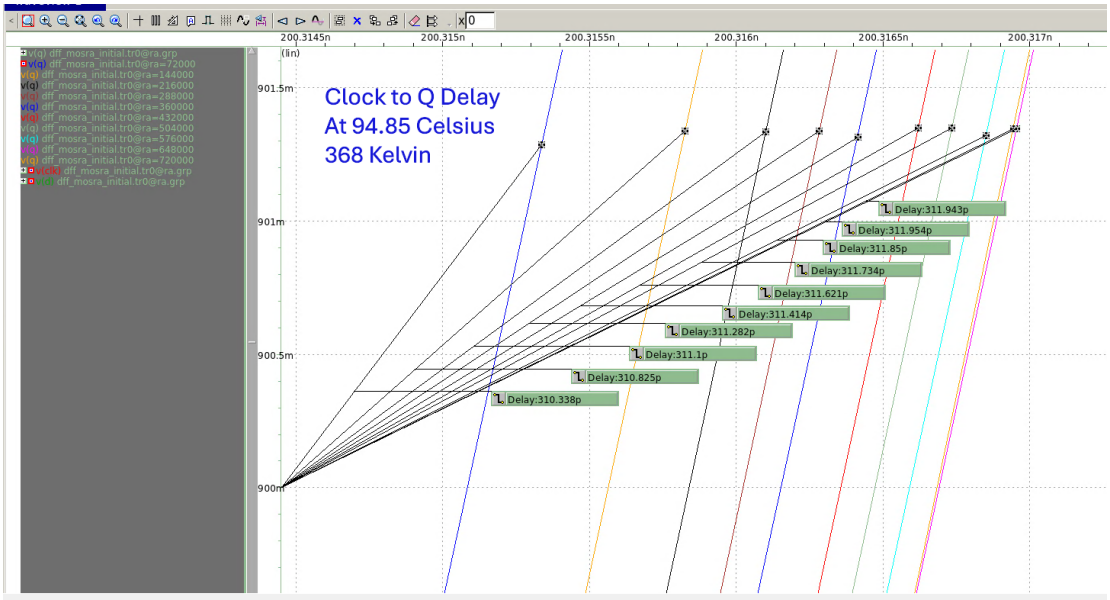

Figure 3.2: Waveview output shows BTI-induced delays for total age time of 200 hours for a DFF `sky130_fd_sc_hd__dfxtp_4` at 94.85 ° Celsius or 368 Kelvin. The $\Delta clk2q$ is 1.605ps

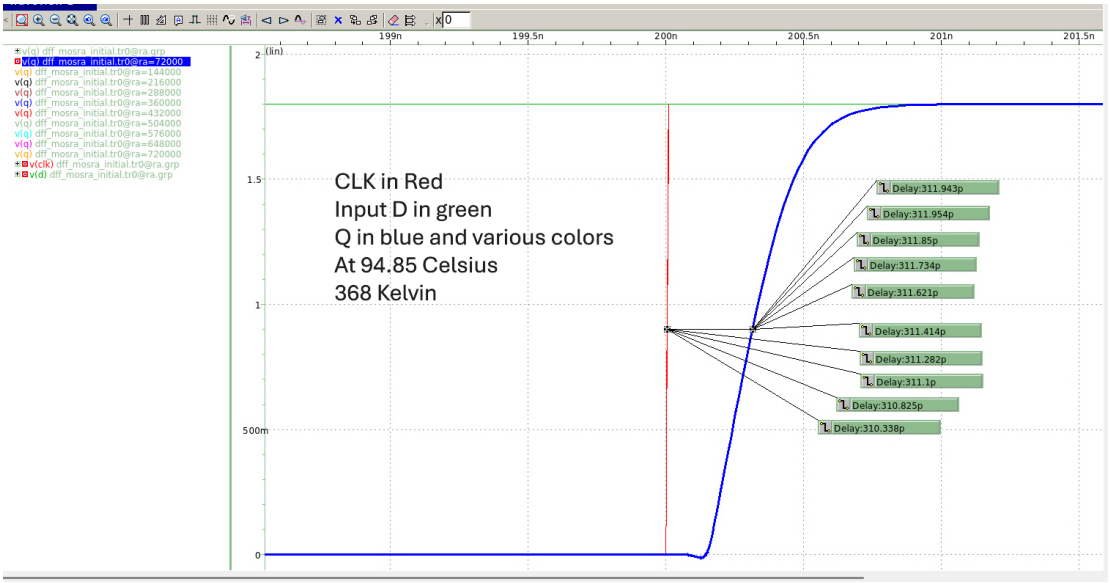

Figure 3.3: Waveview output shows BTI-induced delays with reference to the clock CLK and the input D at 94.85 °Celsius or 368 Kelvin.

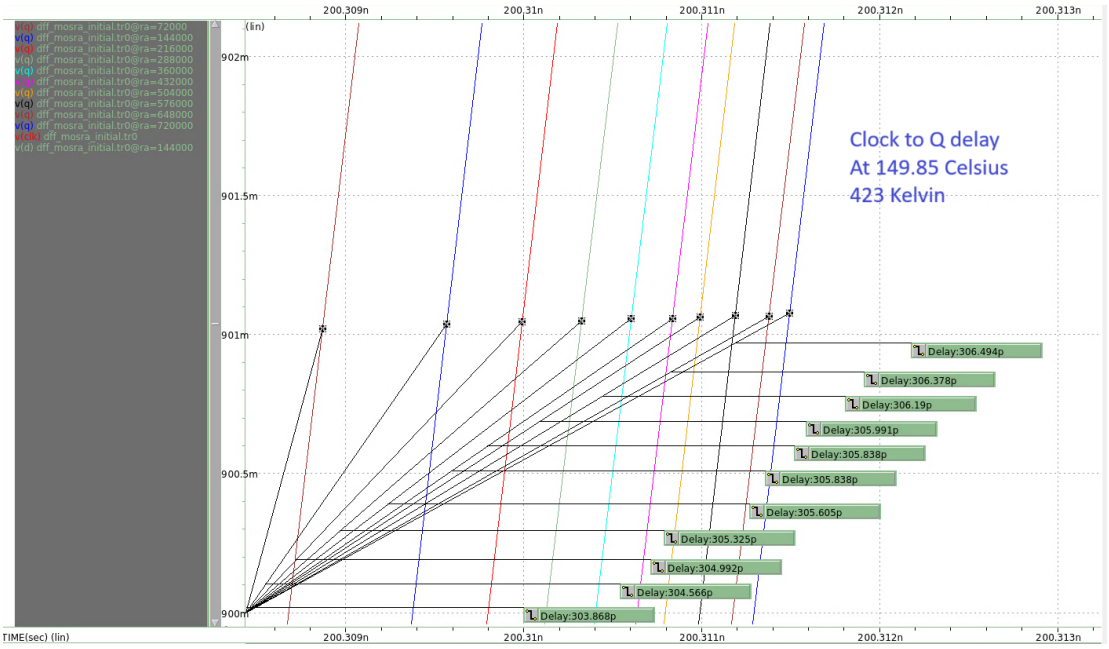

Figure 3.4: Waveview output shows a BTI-induced delays for total age time of 200 hours for a DFF `sky130_fd_sc_hd__dfxtp_4` at 149.85 °Celsius or 423 Kelvin. The $\Delta clk2q$ is 2.626ps

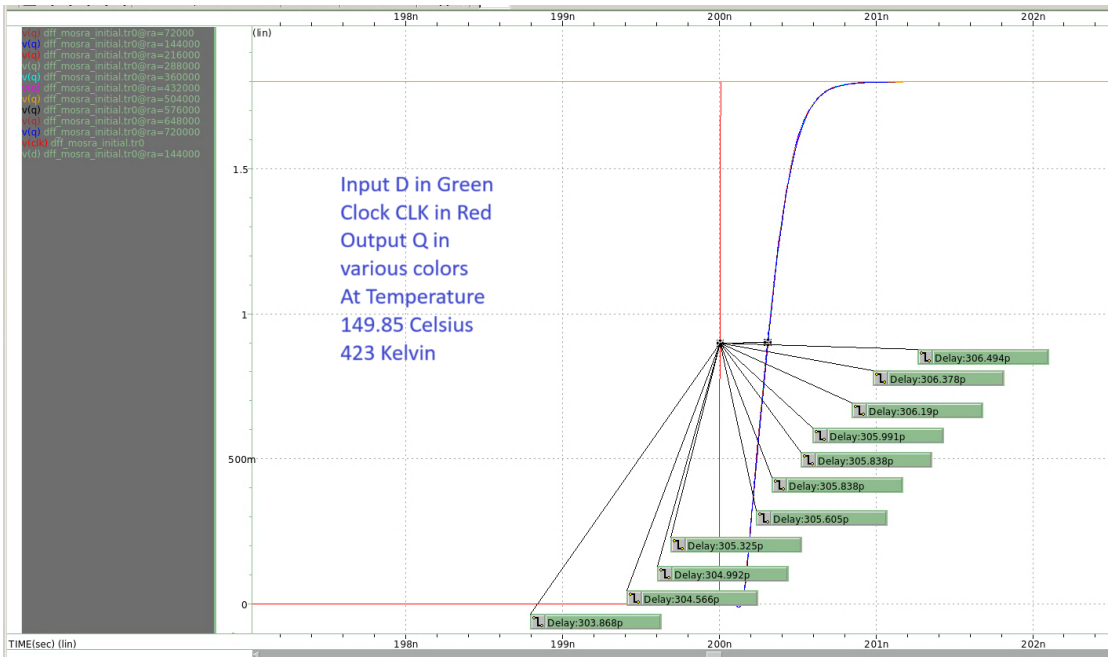

Figure 3.5: Waveview output shows a BTI-induced delays with reference to the clock CLK and the input D at 149.85 °Celsius or 423 Kelvin

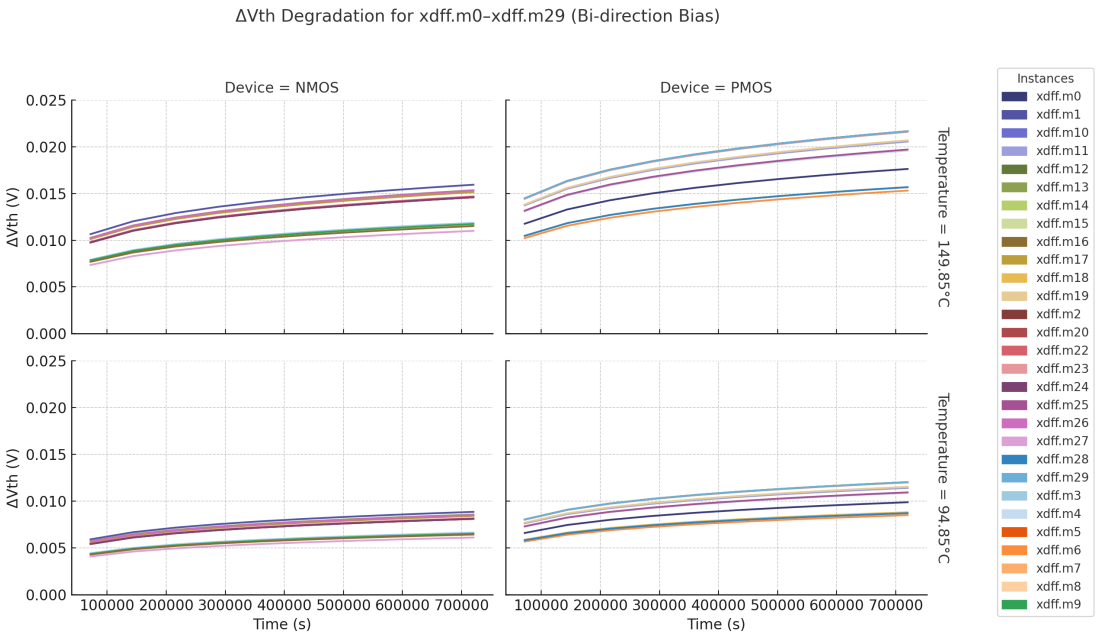

Figure 3.6: This composite Sky130 analysis plots the ΔV_{th} shifts for 30 transistors in the DFF `sky130_fd_sc_hd__dfxtp_4` cell. PMOS devices show consistently higher aging at both temperatures, across transistors due to sizing and stress exposure

Chapter 4

Modeling BTI in a 7nm FinFET predictive PDK

This chapter presents a workflow which models BTI in 7nm FinFET predictive PDK using TCAD. While the earlier workflow enables rapid modeling for a larger number of transistors, the accuracy is greater when using TCAD. BTI analysis requires modeling degradation mechanisms like charge trapping. TCAD enables superior accuracy for characterizing BTI through detailed physical models, with a slower speed as compared to SPICE-based modeling.

The implementation of the study on BTI is done by using the Synopsys Sentaurus Workbench. Tools like SProcess, SDevice, and SVisual are added to the workbench, with each tool having specific input and output file types, as depicted in Figure 4.2. The PDK used was a 7nm predictive FinFET PDK provided by Synopsys with the TCAD

tool suite. Stress was specifically applied to PMOS to model NBTI, and to NMOS to model PBTI.

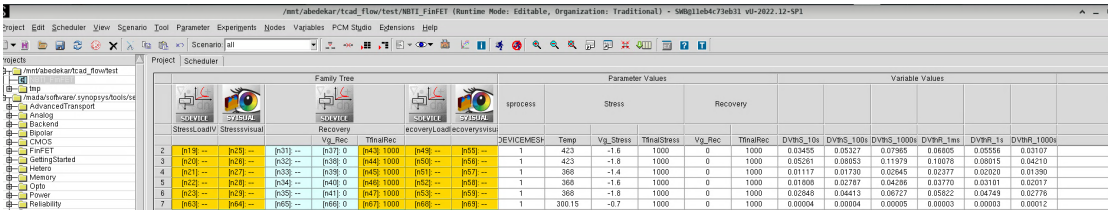

Figure 4.1: The Sentaurus Workbench environment shows a structured matrix of simulation parameters. The columns represent nodes for structure (SProcess), stress and recovery (SDevice), visualization (SVisual) with parameter values like Stress, Temperature, extracted V_{th} value at various times.

Two major parameters are varied: temperature and stress voltage. The nodes are defined per tool, which are reference points in the simulation. The flow starts with SProcess and interfaces with the other tools. In the later part of this chapter, the plots for stress and recovery are compared with a result reported by Drewes et.al [4].

4.1 Experimental Setup

In order to accurately model NBTI and PBTI specifically for advanced process nodes and FinFET structures, a TCAD tool like Synopsys Sentaurus was chosen. Sentaurus provides a comprehensive range of simulation options and a variety of tools that involve structure creation, editing, process simulation, device simulation, and visualization of NBTI. Sentaurus Workbench provides a graphical environment for TCAD simulations, which enables simulation regardless of 1D, 2D, or 3D structures.

This comprehensive workflow begins with the Sentaurus Process as depicted in Fig-

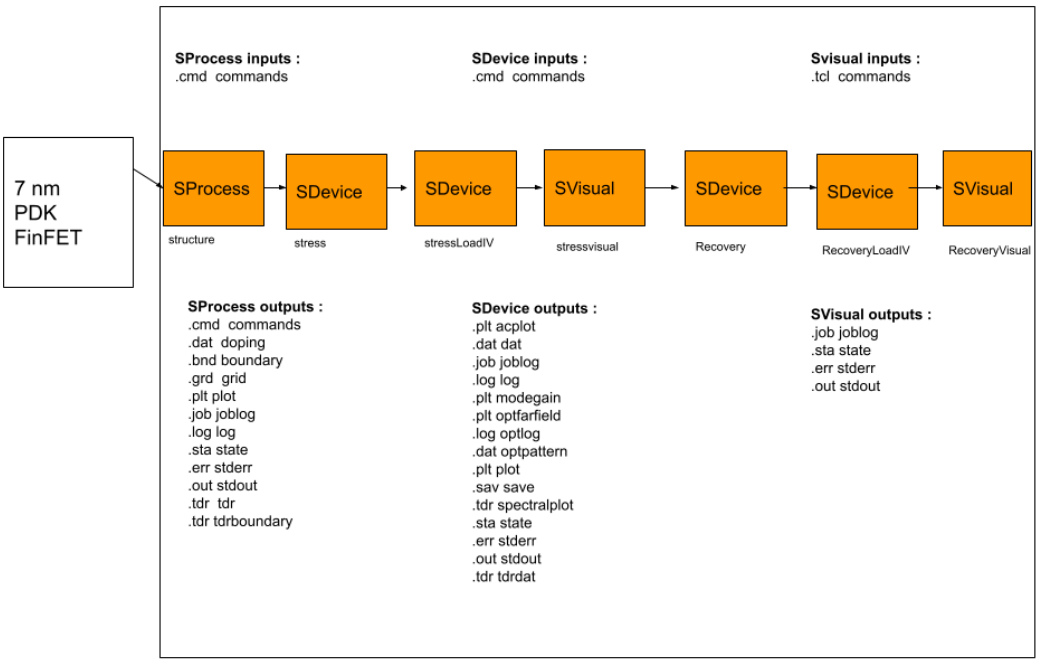

Figure 4.2: This diagram presents a TCAD workflow for simulating BTI in a 7nm FinFET PDK. The process begins with SProcess for structure generation, followed by SDevice for stress, IV characterization, recovery. SVisual handles visualization of stress and recovery. Each tool includes input and output file types. The flow reflects how accurately the simulation and modeling of BTI are structured.

ure 4.1, which creates the 3-D FinFET structure with precise geometry. The required input files for this tool are commands (.cmd). Sentaurus Device deals with pre-stress characterization, which includes electrical characteristics, and defines electrical parameters before stress as depicted in Figure 4.2. Another instance of SDevice is used for the application of negative voltages at elevated temperatures. Sentaurus Visual is used to analyze threshold voltage shifts, meanwhile, electrical parameters for recovery are applied using SDevice.

The experimental setup for this includes temperature variations of 368 Kelvin and 423 Kelvin. Stress Voltage variation of -1.6V, -1.8V for a PMOS in 7nm FinFET. The stress and recovery times are 1000 seconds each. For NMOS, the stress voltages are 1.6V, 1.8V for the same temperatures. After applying gate bias for 1000 seconds, the shift in threshold voltage is calculated. In the recovery phase, the bias is removed, and the threshold voltage shift is measured for recovery over the next 1000 seconds.

This TCAD-based analysis of BTI underscores how stress and recovery are influenced by stress voltage and temperature conditions. These shifts in threshold voltages cause timing delays in the circuits. This leads to setup and hold time violations directly affecting the device.

4.2 Results

Figures 4.3, 4.4 depict the threshold voltage shift ΔV_{th} over time during the NBTI, PBTI stress phase conducted at various temperature and voltage conditions. The plots show an increase in threshold voltage shifts with an increase in stress voltage and temperature. As documented, the shift in voltage for PMOS due to NBTI, is much larger.

The recovery phase is illustrated by Figures 4.5, 4.6 which show the recovery profile after BTI stress is removed. It exhibits partial recovery over time, which is consistent with the R-D model where hydrogen bonds are re-passivated or de-trapped on the removal of stress. The recovery profile is gradual and slow for PMOS NBTI. This is contrasted with the recovery profile depicted in 4.6 which shows rapid recovery.

The Figure 4.7 presents the evolution of delay degradation due to BTI over stress time for a proprietary FPGA. The x-axis represents stress duration in hours, while the y-axis plots the change in propagation delay, ΔPS, indicating how the delay increases over time.From prior research on NBTI, it is expected that NBTI would have a gradual and slow recovery as compared to PBTI. This claim is supported by the fact that PBTI is more elastic, and NBTI recovers much more slowly [2], [27].

The degradation profile, with increase in stress and a gradual and partial recovery, is akin to the recovery behavior observed in Figures 4.4 and 4.3. In this workflow,ΔV_{th}

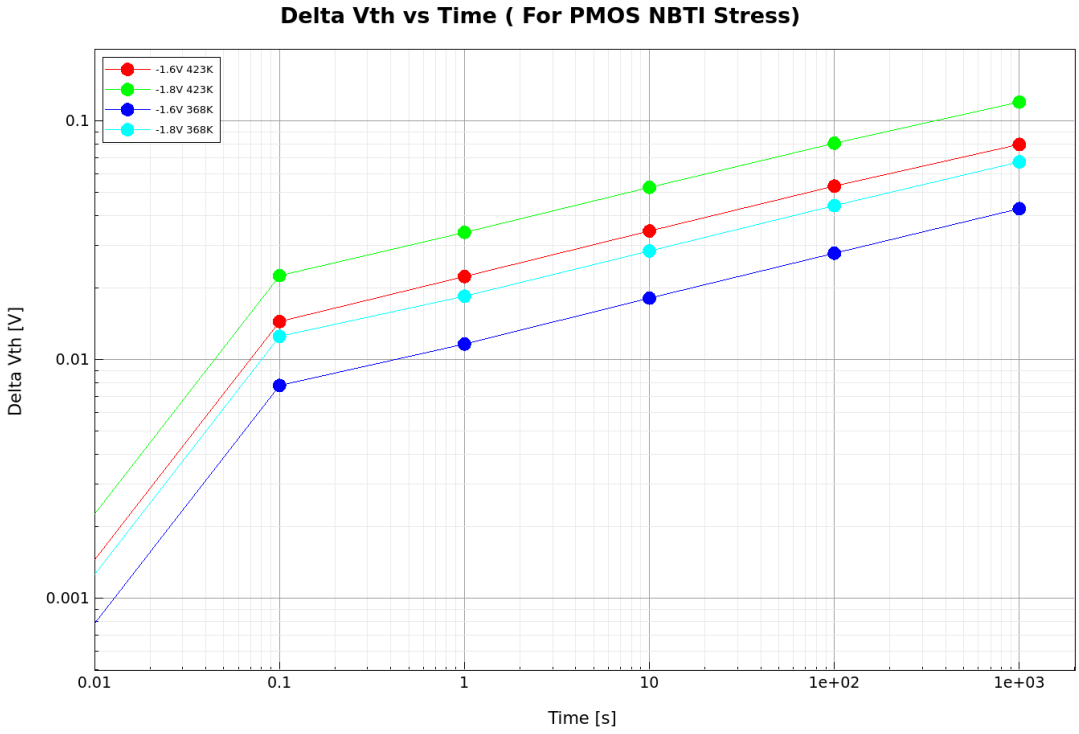

Figure 4.3: Stress induced V_{th} shift is compared across temperatures and stress voltages for 7nm PMOS. The conditions (-1.6 V, 368 K) show lesser degradation, which underscores the critical role of temperature in BTI mechanisms. All elevated temperature conditions demonstrate a significant degradation.

is included to measure degradation. In order to calculate ΔPS against time, access or creation of SPICE models from TCAD data is required. From this investigation, it is evident that the green plot even though inverted, aligns closely with the stress and recovery behavior observed for a 7nm FinFET NBTI simulation. This can further be substantiated by the PBTI Figure 4.6for the same conditions and PDK, by comparing both PBTI and NBTI with the green and pink plot profiles. Thus, the stress and recovery profiles of this workflow closely align with the 4.7 green plots for NBTI, and pink plots for PBTI. This motivates future work to analyze the stress and recovery behavior

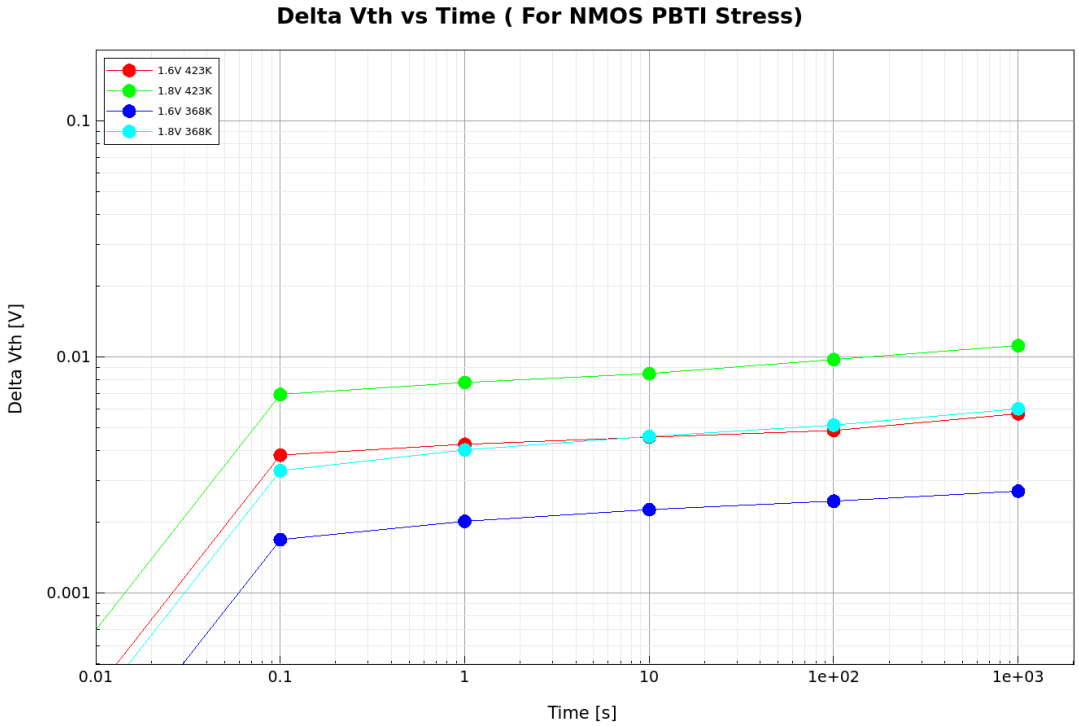

Figure 4.4: Stress induced V_{th} shift is compared across temperatures and stress voltages for 7nm NMOS. The conditions (1.6 V, 368 K) show lesser degradation, which underscores the critical role of temperature in BTI mechanisms. All elevated temperature conditions demonstrate a significant degradation, which is lesser when compared to a PMOS .

for BTI-induced degradation during burn-in. Such investigation should also extend to exploring the effects of FPGA architecture, stress conditions, duty cycles, and activity patterns on BTI recovery [19].

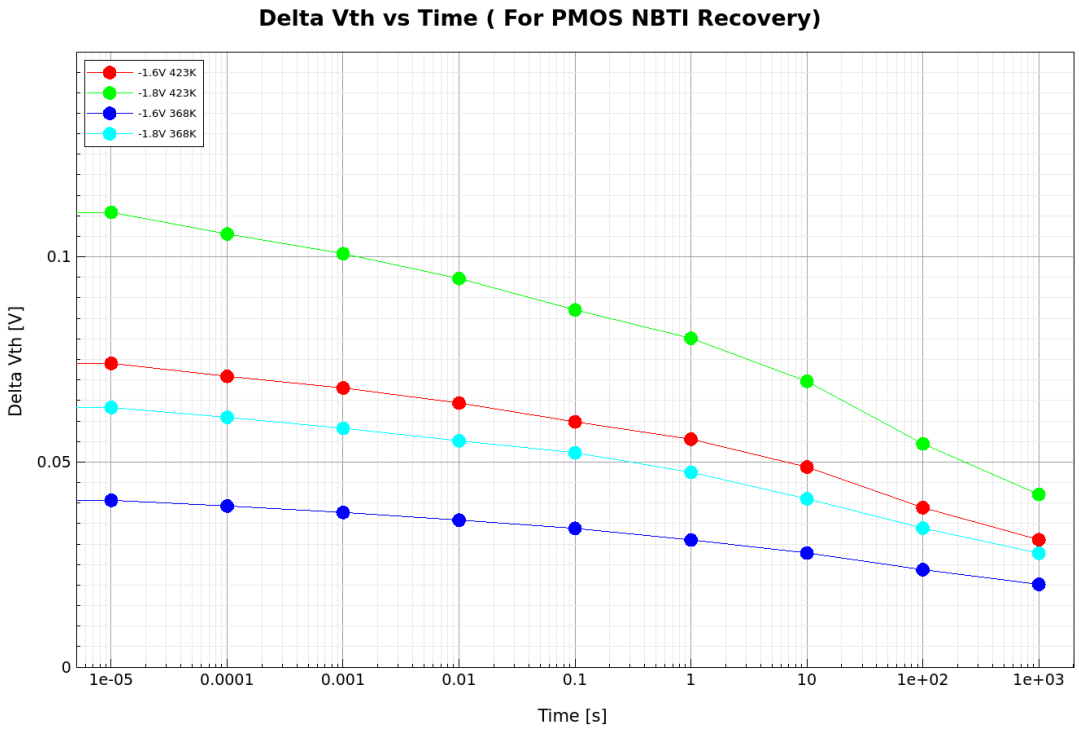

Figure 4.5: V_{th} Recovery is compared across temperatures and stress voltages for 7nm PMOS. The recovery is slow and gradual for PMOS NBTI

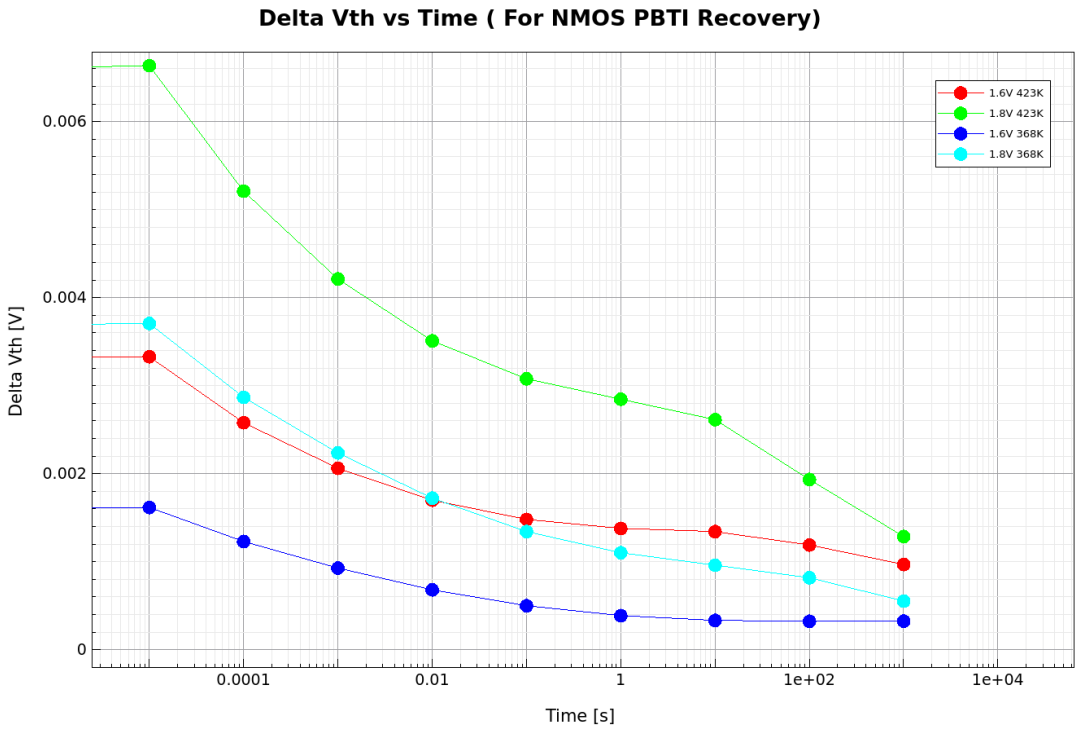

Figure 4.6: V_{th} Recovery is compared across temperatures and stress voltages for 7nm NMOS. The recovery is rapid for NMOS PBTI.

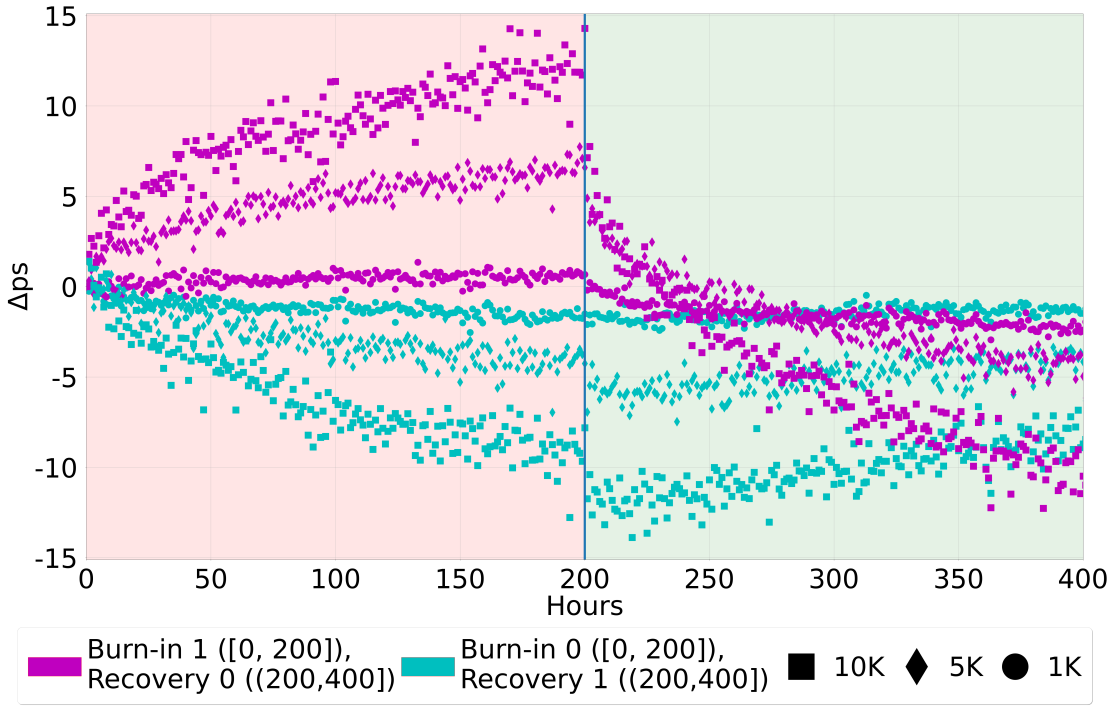

Figure 4.7: Image used from [4] which shows Burn-in effects in FPGAs causing by BTI. *Included with permission from the authors of [4]*

Chapter 5

Conclusion and Future Directions

This survey examines the background, physical causes, various modeling frameworks, and hardware security implications of BTI. It also documents challenges with integrating proprietary tools with open-source PDKs and methods to resolve them. It provides a thorough description of the proposed workflow, while also documenting previous approaches which were not as accurate. In recent years, several open-sourced 7 and 5nm FinFET predictive PDKs (PPDKs) have been presented namely ASAP7 and ASAP5 [28], [29]. These PPDKs are not manufacturable as they do not correlate to a specific production node.

Nevertheless, they may potentially help in the academic study of advanced process nodes. Implementing these open-sourced PPDKs is an open challenge and will require collaboration with the developers to determine precise parameters to input to Sentaurus Process in terms of the input files like the commands file. A prominent limitation of

this approach could be a lack of SPICE integration. Although TCAD provides accurate BTI modeling, extracting SPICE parameters from TCAD and appending them to a SPICE model card or netlist would enable a faster analysis without diminishing the benefits of using TCAD. This would enable the creation of a BTI-aware FPGA fabric. For this particular case, comparative analysis of using MOSRA-based modeling and TCAD modeling for analyzing FPGA fabric wear out could be conducted. It would provide a reasonable estimate of choosing a modeling technique with respect to speed and accuracy.

Integrating TCAD data with SPICE to create SPICE models for BTI, would help in studying BTI and hardware security with a higher granularity than earlier. It would be critical in mitigating security attacks like side-channel attacks. Merging these SPICE models with an FPGA tapeout flow, would help in understanding BTI effects in security like the results observed in [4]. To resolve and analyze the BTI burn-in behavior, targeted experiments that isolate PMOS devices with negative stress and minimal recovery can be created.

The shift in threshold voltages is well-documented to directly impact circuit delay as noted by Fang et.al [30]. From the context of hardware security, BTI is used to cause degradation in side-channel attacks. The effects of BTI and NBTI are analyzed using TCAD which would aid in creating BTI-aware FPGA fabric.

Appendix A

Synopys HSPICE , PrimeSim MOSRA netlist

This contains the SPICE netlist used to simulate BTI-induced degradation in Skywater 130nm (Sky130 PDK).

```
*DFF Aging for Sky130 with MOSRA
.lib "../sky130A_hspice/libs.tech/ngspice/sky130.lib.spice" tt
.include "msky130_fd_pr__nfet_01v8_tt.sp"
.include "msky130_fd_pr__pfet_01v8_hvt_tt.sp"
.subckt sky130_fd_sc_hd__dfxtp_4 CLK D VGND VNB VPB VPWR Q
M0 a_891_413# a_193_47# a_975_413# VPB
   sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
M1 a_1062_300# a_891_413# VGND VNB
   sky130_fd_pr__nfet_01v8__model w=650000u l=150000u
```

```
8  M2 Q a_1062_300# VGND VNB sky130_fd_pr__nfet_01v8__model w
       =650000u l=150000u
9  M3 a_475_413# a_193_47# a_572_47# VNB
       sky130_fd_pr__nfet_01v8__model w=360000u l=150000u
10 M4 a_1062_300# a_891_413# VPWR VPB
       sky130_fd_pr__pfet_01v8_hvt__model w='1e+06*1e-06' l=150000u
11 M5 VPWR a_1062_300# Q VPB sky130_fd_pr__pfet_01v8_hvt__model w=
       '1e+06*1e-06' l=150000u
12 M6 a_634_183# a_27_47# a_891_413# VPB
       sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
13 M7 Q a_1062_300# VPWR VPB sky130_fd_pr__pfet_01v8_hvt__model w=
       '1e+06*1e-06' l=150000u
14 M8 VGND a_1062_300# Q VNB sky130_fd_pr__nfet_01v8__model w
       =650000u l=150000u
15 M9 a_381_47# a_27_47# a_475_413# VNB
       sky130_fd_pr__nfet_01v8__model w=360000u l=150000u
16 M10 VPWR D a_381_47# VPB sky130_fd_pr__pfet_01v8_hvt__model w
       =420000u l=150000u
17 M11 VPWR a_475_413# a_634_183# VPB
       sky130_fd_pr__pfet_01v8_hvt__model w=750000u l=150000u
18 M12 VPWR a_1062_300# Q VPB sky130_fd_pr__pfet_01v8_hvt__model w
       ='1e+06*1e-06' l=150000u
```

```
19 M13 a_572_47# a_634_183# VGND VNB
      sky130_fd_pr__nfet_01v8__model w=420000u l=150000u
20 M14 a_975_413# a_1062_300# VPWR VPB
      sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
21 M15 a_1020_47# a_1062_300# VGND VNB
      sky130_fd_pr__nfet_01v8__model w=420000u l=150000u
22 M16 a_891_413# a_27_47# a_1020_47# VNB
      sky130_fd_pr__nfet_01v8__model w=360000u l=150000u
23 M17 VGND a_475_413# a_634_183# VNB
      sky130_fd_pr__nfet_01v8__model w=640000u l=150000u
24 M18 a_475_413# a_27_47# a_568_413# VPB
      sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
25 M19 a_568_413# a_634_183# VPWR VPB
      sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
26 M20 Q a_1062_300# VGND VNB sky130_fd_pr__nfet_01v8__model w
      =650000u l=150000u
27 M30 VGND a_27_47# a_193_47# VNB sky130_fd_pr__nfet_01v8__model
      w=420000u l=150000u
28 M22 a_27_47# CLK VGND VNB sky130_fd_pr__nfet_01v8__model w
      =420000u l=150000u
29 M23 a_27_47# CLK VPWR VPB sky130_fd_pr__pfet_01v8_hvt__model w
      =640000u l=150000u
```

```
30 M24 VGND a_1062_300# Q VNB sky130_fd_pr__nfet_01v8__model w
      =650000u l=150000u
31 M25 VPWR a_27_47# a_193_47# VPB
      sky130_fd_pr__pfet_01v8_hvt__model w=640000u l=150000u
32 M26 VGND D a_381_47# VNB sky130_fd_pr__nfet_01v8__model w
      =420000u l=150000u
33 M27 a_634_183# a_193_47# a_891_413# VNB
      sky130_fd_pr__nfet_01v8__model w=360000u l=150000u
34 M28 a_381_47# a_193_47# a_475_413# VPB
      sky130_fd_pr__pfet_01v8_hvt__model w=420000u l=150000u
35 M29 Q a_1062_300# VPWR VPB sky130_fd_pr__pfet_01v8_hvt__model w
      ='1e+06*1e-06' l=150000u
36 .ends
37  .param sky130_fd_pr__nfet_01v8__toxe_slope_spectre = 0.0
38  .param sky130_fd_pr__nfet_01v8__vth0_slope_spectre = 0.0
39  .param sky130_fd_pr__nfet_01v8__voff_slope_spectre = 0.0
40 .model mosra_n mosra level=3 BTIFLAG = 1 BTIAP = 0.01 BTIM = 3
41 .model mosra_p mosra level=3 BTIFLAG = 1 BTIAP = 0.01 BTIM = 3
42 .param reltotaltime=720000
43 .param agingstop=100n
44 .MOSRA
45 +reltotaltime=reltotaltime
```

```
+relstep=72000
+RelMode=2
+SimMode=2
+bti=1
+hci=0
+tddb=0
+agingstart=10n
+agingstop=agingstop
.temp 94.85
.appendmodel mosra_n mosra sky130_fd_pr__nfet_01v8__model* nmos
.appendmodel mosra_p mosra sky130_fd_pr__pfet_01v8_hvt__model*
   pmos
*CKT
*Power
VDD VPWR 0 1.8V
VGND VGND 0 0V
*Instance of DFF
XDFF CLK D VGND VGND VPWR VPWR Q sky130_fd_sc_hd__dfxtp_4
*Capacitance
COUT Q 0 0.1pF
CIN D 0 0.1pF
*Inputs D and CLK
```

```
67 VCLK CLK 0 DC 0V PULSE(0V 1.8V 0s 10ps 10ps 10ns 20ns)
68 VD D 0 DC 0V PULSE(0V 1.8V 10ns 10ps 10ps 15ns 30ns)
69 .ic V(Q)=1.8V
70 .measure tran delayQ1 TRIG v(CLK) VAL=0.9 RISE=1 TARG v(Q) VAL
      =0.9 RISE=1
71 .measure tran delayQ2 TRIG v(CLK) VAL=0.9 RISE=2 TARG v(Q) VAL
      =0.9 RISE=2
72 .measure tran delayQ3 TRIG v(CLK) VAL=0.9 RISE=3 TARG v(Q) VAL
      =0.9 RISE=3
73 .measure tran delayQ4 TRIG v(CLK) VAL=0.9 RISE=4 TARG v(Q) VAL
      =0.9 RISE=4
74 .measure tran delayQ5 TRIG v(CLK) VAL=0.9 RISE=5 TARG v(Q) VAL
      =0.9 RISE=5
75 .measure tran delayQ6 TRIG v(CLK) VAL=0.9 RISE=6 TARG v(Q) VAL
      =0.9 RISE=6
76 .measure tran delayQ7 TRIG v(CLK) VAL=0.9 RISE=7 TARG v(Q) VAL
      =0.9 RISE=7
77 .measure tran delayQ8 TRIG v(CLK) VAL=0.9 RISE=8 TARG v(Q) VAL
      =0.9 RISE=8
78 .measure tran delayQ9 TRIG v(CLK) VAL=0.9 RISE=9 TARG v(Q) VAL
      =0.9 RISE=9
79 .measure tran delayQ10 TRIG v(CLK) VAL=0.9 RISE=10 TARG v(Q)
```

```
   VAL=0.9 RISE=10
.tran 0.05ps 400ns UIC
.option post accurate
.option radegoutput=csv
.end
```

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