4.2 Photodiode Transimpedance Amplifier circuit

Following the power supply, the Photodiode TIA circuits were built in succession.

4.2.1 Design and procedure

The objective of this project was to create two Photodiode Transimpedance amplifier circuits to read incoming signals coming from two different diode lasers.
The initial gain settings for the TIA circuit were 10, 100 and 1000 V/V but were later modified to 10k, 110k and 1M V/V. The output from the TIA circuit should meet the following specifications:
Gain: 10k, 110k and 1M V/V.
Voltage output: > 2V

To give an overview of the design, the following image is the schematic for the Linear Power Supply.

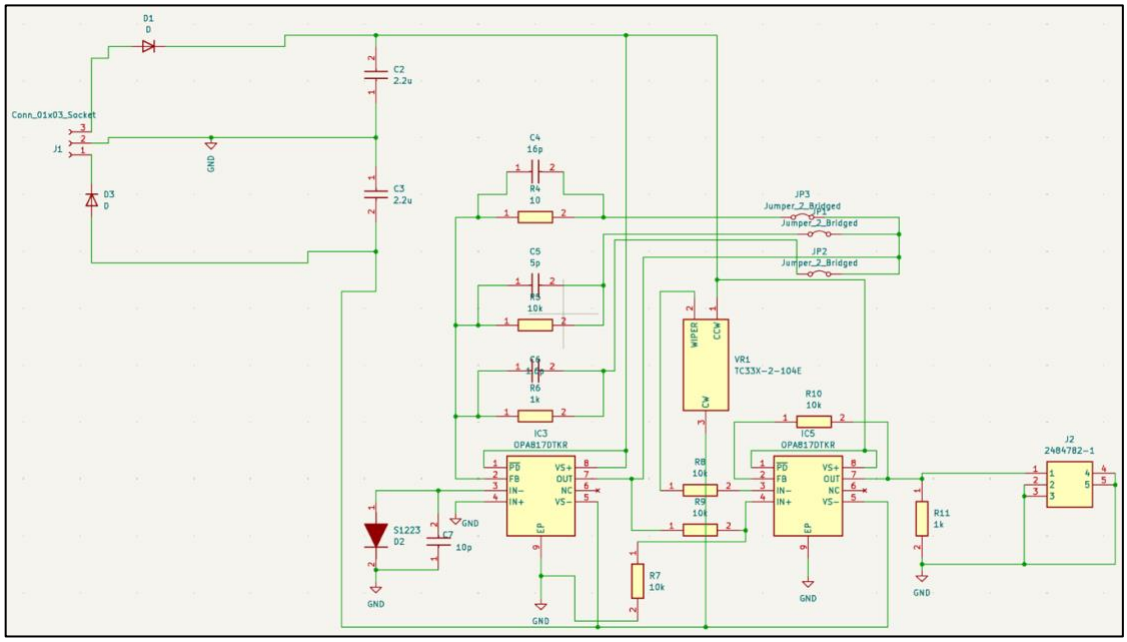

Figure 1. TIA circuit schematic

The power supply system was divided into the following key stages:

1) Photodiode

The Photodiode converts incident light to Photocurrent due to Photoelectric effect. For our application, we use the Photodiode in the Photovoltaic mode. In this mode, the diode is essentially zero-biased, meaning no voltage is applied across it. This allows photocurrent (the flow of electrons generated by light) to flow from the anode to the cathode, creating a voltage when the circuit is open or restricted. Since there is no reverse bias, no leakage current and very low dark

current are present. This makes it an excellent choice for our low-noise DC based application. Fig 19. below shows the dimensions and built of the photodiode (Hamamatsu S1223) being used-

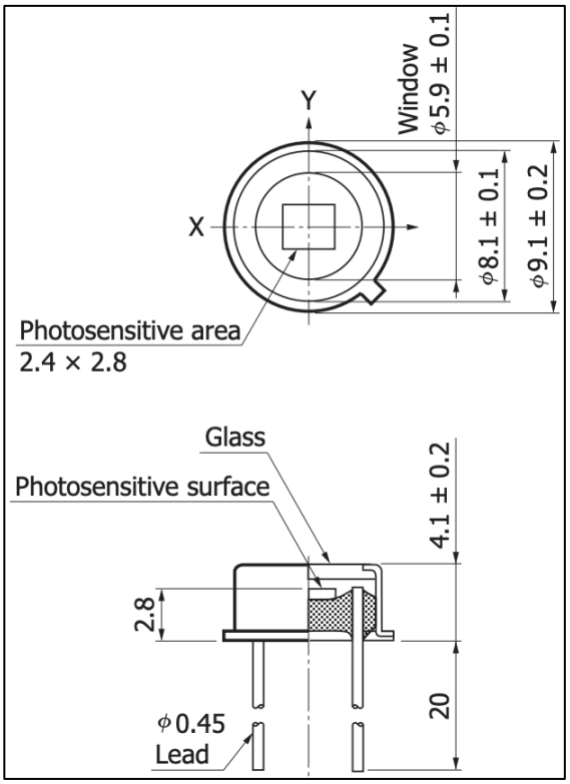

Figure 2. Photodiode Hamamatsu S1223

The Photosensitivity of a Photodiode is a measure of how efficiently it can detect and respond to light signals. Fig 20. below shows how Photosensitive the Photodiode is to a given Wavelength. Our application uses a HeNe laser with a wavelength of 632.8.6 nm

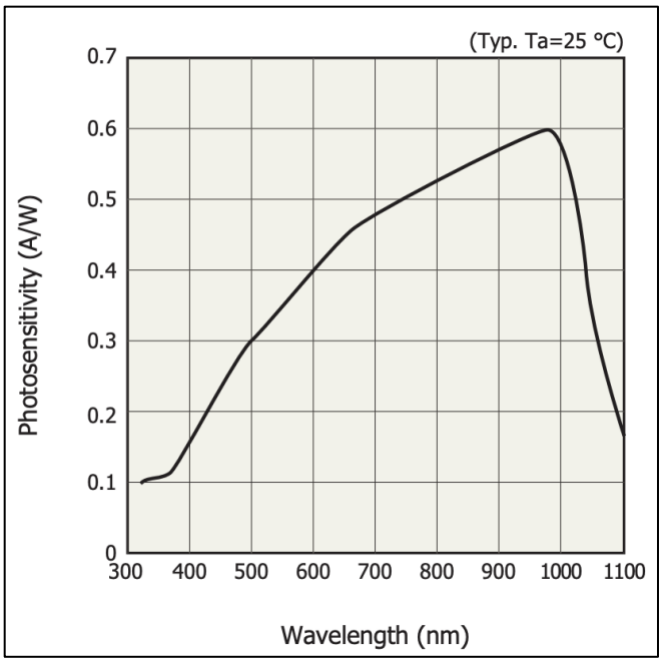

Figure 3. Spectral response of Hamamatsu S1223

The photodiode's photocurrent is calculated by eq (4.8)-

$$I_{ph} = S \times P \tag{4.8}$$

Where P = Power from the HeNe laser which is ~50μW
S = Photosensitivity of the Photodiode which is 0.45 A/W (for λ=660nm)
Therefore, after substituting values in eq (1.8), Photocurrent is-

$$I_{ph} = 0.45 \times 50 \times 10^{-6}$$

$$I_{ph} = 22.5\ \mu A$$

Dark current in a photodiode is the small amount of current that flows through it when it's not illuminated by light. It's essentially a leakage current that results from thermally generated charge carriers, even without incident light. Since there is no reverse bias voltage applied, I_{Dark} is negligible.

In a photodiode, shunt resistance (R_{SH}) is the resistance that current can take through undesired paths, like leakage across the p-n junction or through the edges of the cell. It's essentially the inverse of the slope of the current-voltage (I-V) curve at zero voltage (V=0). Ideally, a photodiode should have infinite shunt resistance and, given by eq (4.9)-

$$R_{SH} = \frac{V_{Bias}}{I_{Dark}} = \frac{0}{< 1pA} = \infty \tag{4.9}$$

The junction capacitance is the capacitance formed at the p-n junction when the diode is reverse-biased. It decreases with increasing reverse bias voltage due to the widening of the depletion region. The Junction capacitance of a Photodiode is given by eq (4.10)-

$$C_J = \frac{C_{J0}}{\sqrt{1 + \frac{V_R}{\emptyset_B}}} \tag{4.10}$$

Where, C_{J0}: Junction capacitance at zero bias

$\emptyset_B$: Built in Voltage of the photodiode Junction (0.7 for silicon)

As mentioned in the datasheet, C_J = 10pF, when V_R = 20V

For our TIA circuit, V_R = 5V

Thus, the Junction Capacitance after substituting values in eq (4.10) when V_R = 5V is-

$$10pF = \frac{C_{J0}}{\sqrt{1 + \frac{20}{0.7}}}$$

$$10pF = \frac{C_{J0}}{5.43}$$

$$C_{J0} = 10 \times 10^{-12} \times 5.43$$

$$C_{J0} = 54.3\ pF$$

The I-V Characteristics of the Photodiode demonstrate the relationship between the current flowing through it and the voltage applied across it, both in the forward and reverse bias conditions. Fig 21. below shows the I-V characteristics of photodiode.

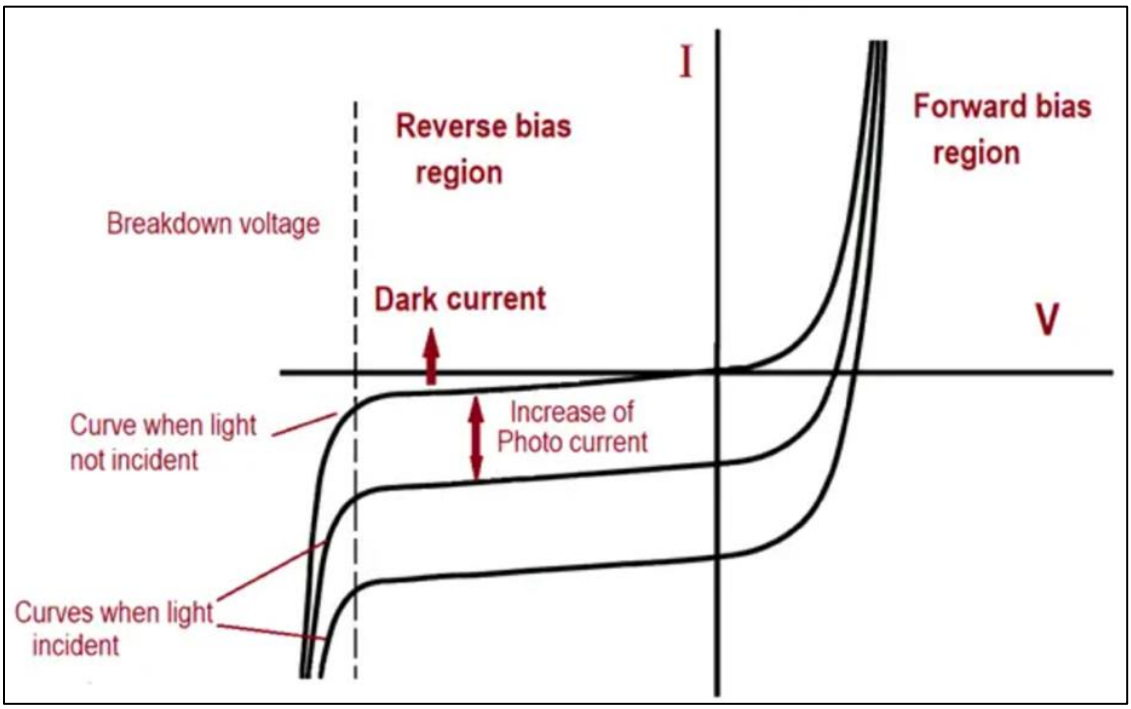

Figure 4. I-V Characteristics of the Photodiode

The chart consists of 4 areas, called quadrants. Photodiode mode corresponds to the work in the 3rd quadrant.
With no light applied, the photodiode acts as a conventional rectifier.
Diode Characteristic curves are shifted by applied light.

2) Transimpedance Amplifier

The Photocurrent (22.5 μA) generated by the Photodiode cannot be measured easily so the Op-Amp converts the Photocurrent to a measurable voltage

There are 3 gain settings 10k, 110k and 1M V/V. Each with the help of 3 resistors 10kΩ, 110kΩ and 1MΩ respectively.
Each resistor has a capacitor in parallel. The minimum value of the Capacitor for the circuit to be stable can be calculated by eq (4.11).

$$C = \frac{C_{in}}{2\,\pi RF} \tag{4.11}$$

Where R = feedback resistor, F = unity gain bandwidth which is 800Mhz

After Substituting values in eq (4.11)-

For R = 10k Ω

$$C = \frac{60 \times 10^{-12}}{2\,\pi \times 10{,}000 \times 800 \times 10^{6}} = 1pF$$

For R = 110k Ω

$$C = \frac{60 \times 10^{-12}}{2\,\pi \times 110{,}000 \times 800 \times 10^{6}} = 0.33pF$$

For R = 1M Ω

$$C = \frac{60 \times 10^{-12}}{2\,\pi \times 1{,}000{,}000 \times 800 \times 10^{6}} = 0.1pF$$

The photodiode circuit can be susceptible to oscillations due to parasitic capacitances at the inverting input node. The feedback capacitor helps compensate for these capacitances, ensuring that the loop gain remains stable and does not trigger oscillations. By limiting the bandwidth of the amplifier, the feedback capacitor helps reduce the amount of high-frequency noise that can be amplified and introduced into the circuit. The feedback capacitor also limits the bandwidth of the amplifier, which is a trade-off for stability.

RC time constant (τ) is the time required to charge the capacitor, through the resistor, from an initial charge voltage of zero to approximately 63.2% of the value of an applied DC voltage, or to discharge the capacitor through the same resistor to approximately 36.8% of its initial charge voltage. τ is given by eq (4.12)

$$\tau = R_F \times C_T \tag{4.12}$$

Eq (4.13) explains how C_T is calculated

$$C_T = C_J + C_{Op-amp} + C_{par} \tag{4.13}$$

$$60\text{pF} = 54.3\text{pF} + 1.6\text{pF} + 4\text{pF}$$

Therefore, the total capacitance entering the TIA circuit is 60pF.

Eq (4.14) explains how f_{-3dB} is calculated-

$$f_{-3dB} = \frac{1}{2 \times \pi \times \tau}$$

Now, substituting values in eq (4.12) and eq (4.14) respectively,

For R_F = 10k,

$$\tau = 10{,}000 \times 60 \times 10^{-12}$$

$$\tau = 0.6\ \mu\text{S}$$

Therefore,

$$f_{-3dB} = \frac{1}{2 \times \pi \times \tau} = \frac{1}{2 \times \pi \times 0.6 \times 10^{-6}}$$

$$f_{-3dB} = 265k\ Hz$$

For R_F = 110k,

$$\tau = 110{,}000 \times 60 \times 10^{-12}$$

$$\tau = 6.6\ \mu S$$

Therefore,

$$f_{-3dB} = \frac{1}{2 \times \pi \times \tau} = \frac{1}{2 \times \pi \times 6.6 \times 10^{-6}}$$

$$f_{-3dB} = 24k\ Hz$$

For R_F = 1M,

$$\tau = 1{,}000{,}000 \times 60 \times 10^{-12}$$

$$\tau = 60\ \mu S$$

Therefore,

$$f_{-3dB} = \frac{1}{2 \times \pi \times \tau} = \frac{1}{2 \times \pi \times 60 \times 10^{-6}}$$

$$f_{-3dB} = 2.6k\ Hz$$

The –3 dB point is the frequency at which the output power drops to half, or the voltage drops to 70.7% of the max value.

The following calculations indicate the circuit performance for designing the TIA circuit-

Closed loop Signal Bandwidth (SBW) is given by eq (4.15) :

$$f_C = \frac{1}{2 \times \pi \times R_f \times C_f} \tag{4.15}$$

Substituting values in eq (4.15),

For R_f=1kΩ, C_f=16pF

$$f_C = \frac{1}{2 \times \pi \times 1000 \times 1.6 \times 10^{-12}}$$

$$f_C = 10M\ Hz$$

For R_f=110kΩ, C_f=5pF

$$f_C = \frac{1}{2 \times \pi \times 1000 \times 1.6 \times 10^{-12}}$$

$$f_C = 290k\ Hz$$

For R_f=1MΩ, C_f=1.6pF

$$f_C = \frac{1}{2 \times \pi \times 1000 \times 1.6 \times 10^{-12}}$$

$$f_C = 100k\ Hz$$

In an ideal filter, noise would only exist exactly inside the -3 dB bandwidth. But real circuits have a gradual roll-off . Thus, noise "leaks" slightly beyond f_{-3dB} .
Closed loop Noise Bandwidth (NBW) is given by eq (4.16):

$$NBW = K_n \times SBW = \frac{\pi}{2} \times SBW \qquad (4.16)$$

For R_f=1kΩ, C_f=16pF

$$NBW = \frac{\pi}{2} \times 10M\ Hz$$

$$NBW = 15.7M\ Hz$$

For R_f=110kΩ, C_f=5pF

$$NBW = \frac{\pi}{2} \times 290k\ Hz$$

$$NBW = 455.5k\ Hz$$

For R_f=1MΩ, C_f=1.6pF

$$NBW = \frac{\pi}{2} \times 100k\ Hz$$

$$NBW = 157k\ Hz$$

3) Noise Analysis

There are 3 subsections for TIA noise analysis-
-Photodiode noise model
-Op amp noise model
-Resistor noise model
All 3 subsections will be combined to calculate total output noise voltage

Noise will be determined by-
Input Capacitance C_{in}
Feedback Capacitance C_F
Shunt Resistance R_{SH}
Feedback Resistance R_F

For the following calculations let us take -
R_f=1MΩ and C_f=1.6pF
Input capacitance: C_{in} = 60pF

Zero Frequency f_Z given by eq (4.17)

$$f_Z = \frac{1}{2 \times \pi \times R_f \times (C_{in} + C_f)} \tag{4.17}$$

Substituting values in eq (4.17)

$$f_Z = \frac{1}{2 \times \pi \times 110{,}000 \times ((60 + 1.6) \times 10^{-12})}$$

$$f_Z = 22k\ Hz$$

Arbitrary lower boundary in the 1/f noise region f_L= 0.1Hz

1/f noise and broadband noise intersection frequency f_f is given by eq (4.18)

$$\left(\frac{e_{fnorm}}{e_{nbb}}\right)^2 \tag{4.18}$$

Substituting values in eq (4.18)

$$\left(\frac{80nV/\sqrt{Hz}\sqrt{0.1Hz}}{4.5nV/\sqrt{Hz}}\right)^2$$

$$\left(\frac{25.3\ nV_{RMS}}{4.5nV/\sqrt{Hz}}\right)^2$$

$$5.62\ Hz$$

Noise gain and open loop gain intersection frequency f_i is given by eq (4.19)

$$\frac{C_F}{C_F + C_{in}} \times f_t \tag{4.19}$$

Substituting values in eq (4.19)

$$\frac{5pF}{5pF + 60pF} \times 800MHz$$

$$61.5\ MHz$$

Fig 22. below is a Bode plot showing how the Photodiode TIA system behaves across change in frequency.

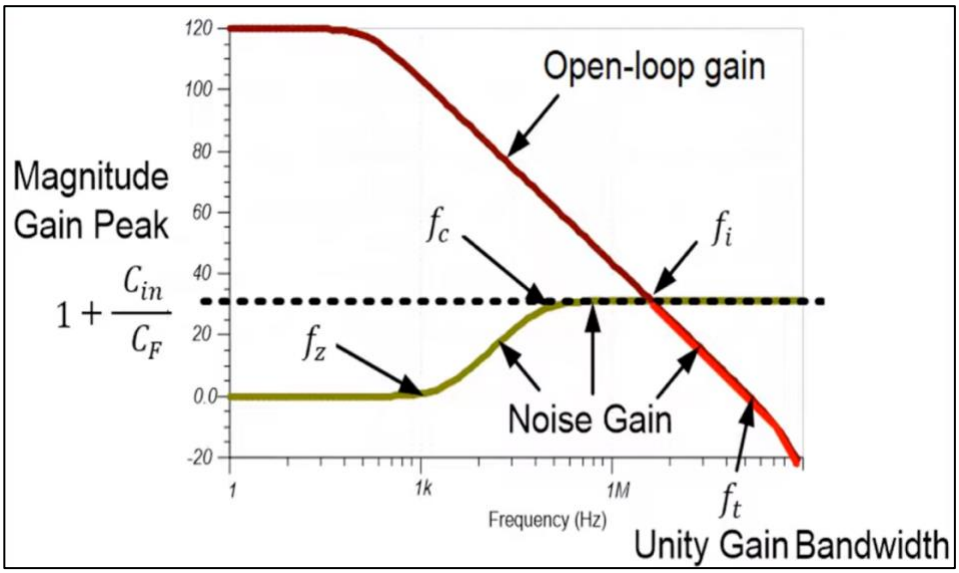

Figure 5. Noise voltage due to op-amp noise voltage source

Gain peaking is given by eq (4.20) below

$$Gain\ Peaking\ = 1 + \frac{C_{in}}{C_f} = 13 \tag{4.20}$$

And values known are,

$$f_i = 61.5MHz$$

$$f_c = 290kHz$$

$$f_z = 22kHz$$

$$f_t = 800MHz$$

Thermal noise voltage of the feedback resistor R_F can be calculated using the formula for the Johnson noise given by eq (4.21).

$$E_{nr,out} = \sqrt{4kTR_F \times NBW} \tag{4.21}$$

Substituting calculated values in eq (4.21)

$$E_{nr,out} = \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 110{,}000 \times 455{,}500}$$

$$E_{nr,out} = \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 110{,}000 \times 455{,}500}$$

$$E_{nr,out} = 28.8\mu V_{RMS}$$

Photodiode noise current is the RMS value of 3 different noise sources-
Thermal noise of the shunt resistance
Shot noise due to dark current
Shot noise due to light current
Thermal Noise Current spectral density due to shunt resistance is given by eq (4.22)

$$I_{SH} = \sqrt{\frac{4kT}{R_{SH}}} \tag{4.22}$$

Substituting values in eq (4.22)

$$I_{SH} = \sqrt{\frac{41.38 \times 10^{-23} \times 300}{10^{12}}}$$

$$I_{SH} = 128.7\ fA/\sqrt{Hz}$$

I_{SH} is negligible. Similarly Shot noise due to dark current and Shot noise due to light current tend to 0. The value for Total photodiode noise current density $I_{n,ph}$ would be close to 0.

Input noise current = 18fA/Hz (from datasheet)

Total noise current spectral density is given by eq (4.23)

$$I_{n,tot} = \sqrt{I_{n,ph}{}^2} + \sqrt{I_{n,opa}{}^2} \tag{4.23}$$

$$I_{n,tot} = 130\ fA/\sqrt{Hz}$$

The total output noise voltage spectral density due to noise current source of the op-amp and photodiode is given by eq (4.24)-

$$e_{ni,out} = i_{ni,out} R_f \tag{4.24}$$

Substituting values in eq (4.24)

$$e_{ni,out} = 130 \frac{fA}{\sqrt{Hz}} \times 110k\Omega$$

$$e_{ni,out} = 14.3nV/\sqrt{Hz}$$

The total RMS output noise voltage due to noise current source of the op-amp and photodiode is given by eq (4.25)-

$$E_{ni,out} = e_{ni,out} \times \sqrt{NBW} \tag{4.25}$$

Substituting values in eq (4.25)

$$E_{ni,out} = 14.3nV/\sqrt{Hz} \times \sqrt{455{,}500}$$

$$E_{ni,out} = 9.65\mu V_{RMS}$$

The total output noise spectrum of a TIA system consists of several distinct regions: low-frequency flicker noise, a flat broadband thermal noise floor, gain peaking due to capacitive effects, rising noise due to current noise at high frequencies, and eventual roll-off due to amplifier bandwidth limits. Optimal design seeks to operate primarily within the flat broadband noise region to maximize SNR and ensure stable, low-noise operation.

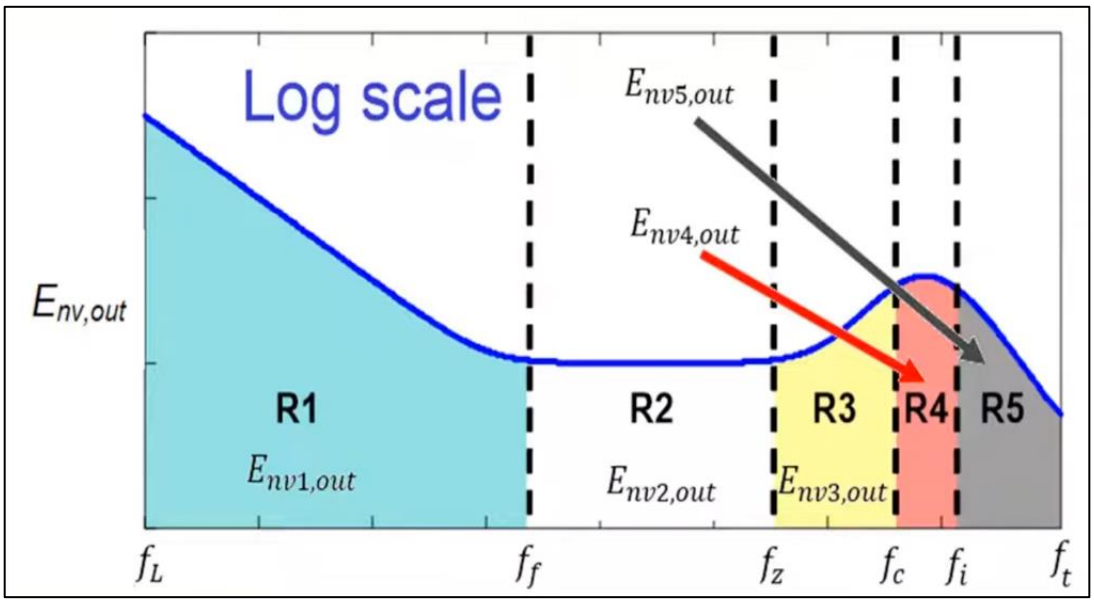

Figure 6. Noise voltage due to op-amp noise voltage source

Fig 23. Above shows the change in noise voltage due to change in op-amp noise voltage source. Describing the 5 regions in fig 23. –

Region 1: Low-Frequency 1/f Noise (Flicker noise)
Typically from Op-amp internal mechanisms and Low-frequency traps and recombination. Noise drops roughly -10 dB/decade until it meets flat white noise.

Region 2: White Noise (Flat broadband noise)
Typically from Johnson (thermal) noise from resistors. This is the lowest noise region. Ideally, the operating bandwidth is here.

Region 3: Rise due to Capacitive Gain Peaking. Minor gain peaking due to interaction between feedback capacitance and input capacitance.

Region 4: Op-Amp Current Noise Coupled with Capacitance
As frequency increases, input current noise starts to dominate. This noise is multiplied by the input impedance. Noise rises with frequency because capacitive impedance falls.

Region 5: Roll-Off - Amplifier Bandwidth Limit
The amplifier's own gain-bandwidth product (GBW) limit is reached.

Noise voltage due to op-amp noise voltage source is divided into 5 regions. Given Below Eq (4.26), eq (4.27), eq (4.28), eq (4.29), eq (4.30) respectively represent expressions for each region-

Region 1:

$$E_{nv1,out} = e_{nbb}\sqrt{f_f ln\frac{f_f}{f_L}} = 22.33\ nV_{RMS} \tag{4.26}$$

Region 2:

$$E_{nv2,out} = e_{nbb}\sqrt{f_Z - f_f} = 67.37\ nV_{RMS} \tag{4.27}$$

Region 3:

$$E_{nv3,out} = e_{nbb}\sqrt{\frac{f_c^3 - f_z^3}{3f_z^2}} = 22.58\ \mu V_{RMS} \tag{4.28}$$

Region 4:

$$E_{nv4,out} = e_{nbb}\left(1 + \frac{C_{in}}{C_f}\right)\sqrt{f_i - f_c} = 547.68\ \mu V_{RMS} \tag{4.29}$$

Region 5:

$$E_{nv5,out} = e_{nbb}\sqrt{\frac{f_t^2}{f_i}} = 459\ \mu V_{RMS} \tag{4.30}$$

The total RMS output noise voltage due to op-amp noise voltage source $E_{nv,out}$ is given by eq (4.31)

$$E_{nv,out} = \sqrt{(E_{nv1,out})^2} + \sqrt{(E_{nv2,out})^2} + \sqrt{(E_{nv3,out})^2} + \sqrt{(E_{nv4,out})^2} + \sqrt{(E_{nv5,out})^2} \quad (4.31)$$

Substituting values calculated from Eq (4.26), eq (4.27), eq (4.28), eq (4.29), eq (4.30) respectively represent in eq (4.31)

$$E_{nv,out} = \sqrt{0.498\mu V} + \sqrt{445.382\mu V} + \sqrt{509.85\mu V} + \sqrt{209{,}471\mu V} + \sqrt{210{,}681\mu V}$$

$$E_{nv,out} = 649.222\mu V$$

Total output noise voltage is obtained from the calculated values below

$E_{ni,out} = 9.65\mu V_{RMS}$

$E_{nv,out} = 649.222\mu V_{RMS}$

$E_{nr,out} = 28.8\mu V_{RMS}$

To calculate Total output noise voltage, we substitute above values in eq (4.32)

$$E_{n,out} = \sqrt{(E_{ni,out})^2} + \sqrt{(E_{nv,out})^2} + \sqrt{(E_{nr,out})^2} \quad (4.32)$$

$E_{n,out} = 650\mu V_{RMS}$

SNR is the ratio of the useful signal power (from the photodiode photocurrent) to the total noise power at the TIA output given by eq (4.33).

$$SNR = 20\log\frac{1}{E_{n,out}} \quad (4.33)$$

$$SNR = 63.741\ dB$$

Therefore, SNR of TIA circuit is 63.74 dB.

4) Output Voltage

The output Voltage for the Photodiode TIA is calculated from eq (4.44)

$$V_{OUT} = -I_{IN} \times R_F \tag{4.44}$$

As calculated from eq (4.44) above,

$$-I_{IN} = -I_{PH}$$

$$-I_{IN} = -22.5\mu A$$

$$R_F = 110k\ \Omega$$

Therefore, substituting values in eq (4.44)

$$V_{OUT} = -22.5uA \times 110k\ \Omega$$

$$V_{OUT} = -2.475V$$

The negative sign comes from inverting op-amp, therefore the voltage output for the above parameters comes out to approximately 2.475V.

4.2.2 Component Selection

The following critical components were chosen for reliability and efficiency:

Photodiode: Hamamatsu S1223
Spectral response range: 320 to 1100nm
Photosensitivity: 0.45 A/W (for λ=660nm)
Dark current: 0.1nA
Cutoff Frequency: 30MHz
Terminal Capacitance: 10pF (for V_R=20V)
Photosensitive area size: 2.4 x 2.8 mm
Effective photosensitive area: 6.6 mm^2
Reverse Voltage: 30V

Op Amp: OPA817DK
Unity Gain Bandwidth: 800MHz
Gain Bandwidth Product: 400MHz
Large-signal Bandwidth (2VPP): 250MHz
Slew rate: 1000V/µs
Input voltage noise: 4.5nV/√Hz
Input offset voltage: 250µV

10k Ω: RC1206FR-07110KL-Yageo
Capacitance Tolerance: ± 1%
Power (W): 250mW

110k Ω:
Capacitance Tolerance: ± 1%
Power (W): 250mW

1M Ω:
Capacitance Tolerance: ± 1%
Power (W): 250mW

TC33X-2-104E:
Resistance: 100k Ω
Power (W): 0.15W
Capacitance Tolerance: ± 25%
Number of turns: 1.0

1k Ω: AC1206FR-071K2L-Yageo
Capacitance Tolerance: ± 1%
Power (W): 250mW

1.6pF: GJM0335G2A1R6CB01J
Tolerance: 0.1pF

5pF: MCASU105SCG050BFNA01
Tolerance: 0.1pF

10pF: MBASU105SCG100CFNA01
Tolerance: 0.25pF

16pF: GJM1555C1H160FB01J
Tolerance: 1%

2.2µF: KEMET C430C225K5R5TA
Tolerance: ± 10%

4.2.3 Simulation

After the initial designing of the TIA circuit, the simulation for said was carried out using TINA-TI. TINA was chosen over other simulation software's as it is much more robust in simulating TI specific systems like op amps.

Fig 24. shows the circuit diagram for TIA circuit with 100kΩ feedback resistor and 5pF capacitor

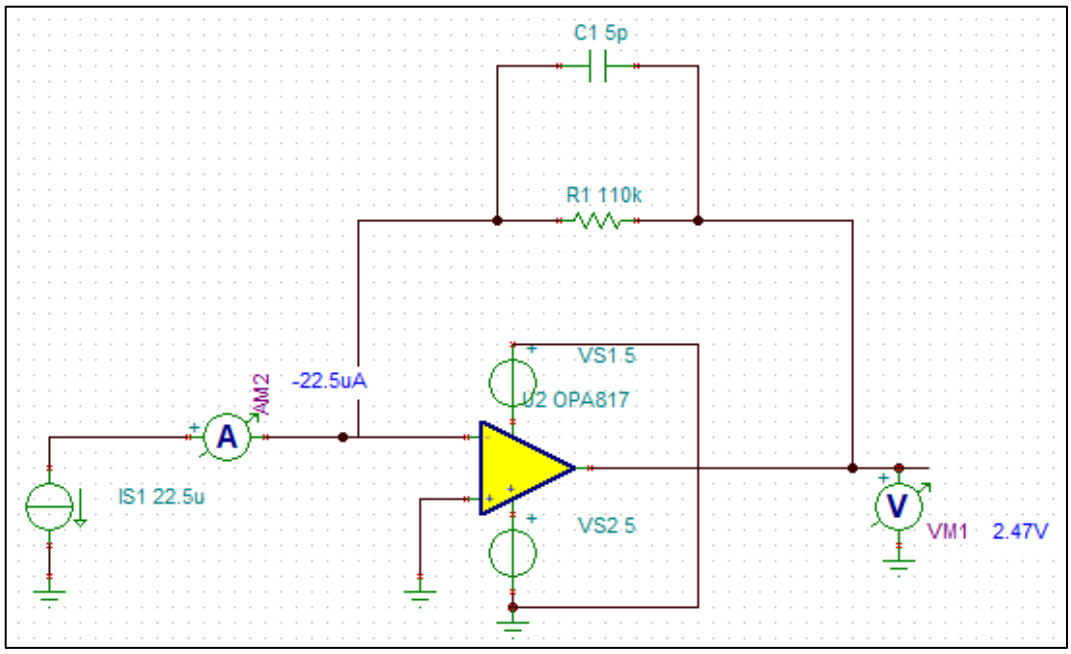

Figure 7. TIA circuit in TINA-TI

1) Nyquist plot

Fig 25. shows the Nyquist plot for TIA circuit with 100kΩ feedback resistor and 5pF capacitor

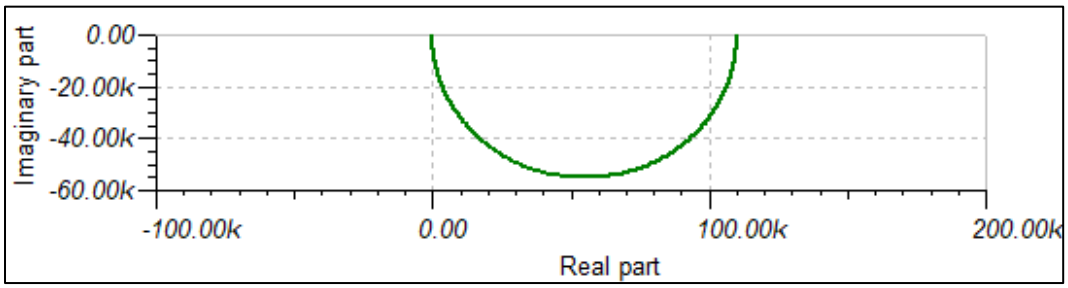

Figure 8. TIA circuit in TINA-TI

This Nyquist plot represents how the open loop gain, and phase of the TIA vary with frequency. It maps the transfer function onto the complex plane as frequency sweeps from low to high.
X-axis (Real Part): Represents the in-phase component of the gain.
Y-axis (Imaginary Part): Represents the quadrature (90° phase-shifted) component.
The plot forms a semi-circle in the left half-plane, indicating stable phase margin.

The Nyquist curve does not encircle the critical point (−1,0), meaning: The loop gain never reaches instability. The system has a positive phase margin, confirming loop stability. The curve remains well away from the origin, implying the TIA does not introduce oscillation or excessive feedback peaking. The trajectory shows that as frequency increases, the gain and phase roll off smoothly, as expected from a well-compensated TIA.

2) Magnitude and Phase Bode plot

Fig 26. shows the Magnitude and phase bode plot for TIA circuit with 100kΩ feedback resistor and 5pF capacitor.

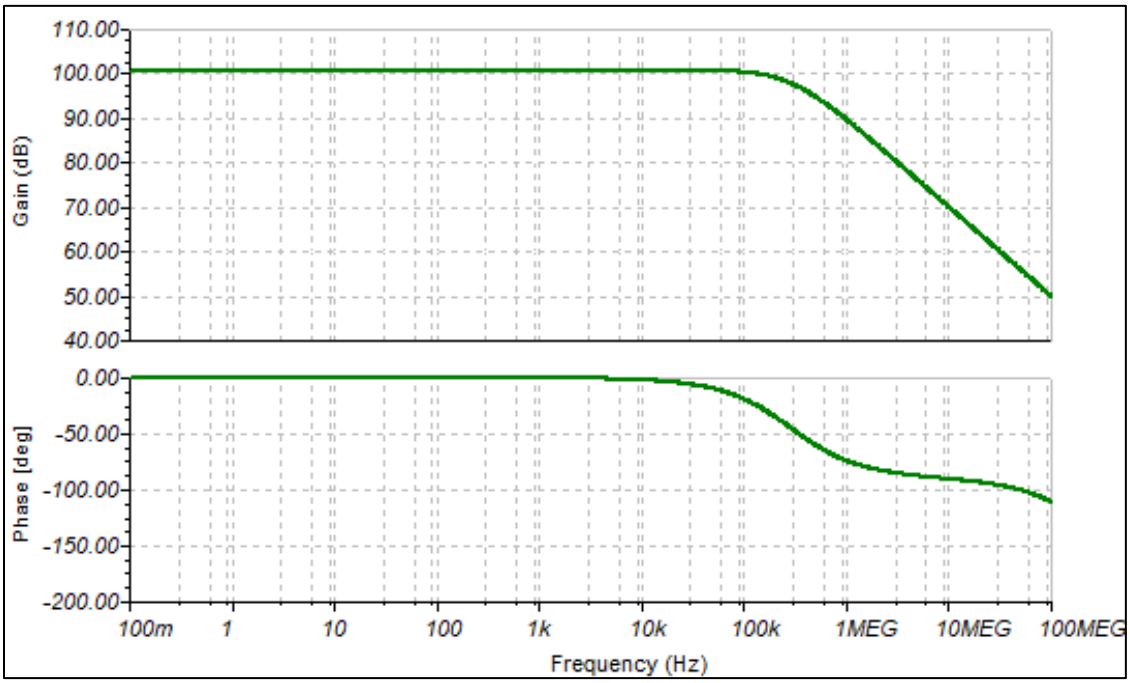

Figure 9. Bode plot in TINA-TI

Gain vs Frequency (Magnitude Bode Plot)
Y-axis (dB): $20 \cdot \log_{10}|\text{Gain}|$, representing the amplifier's gain at each frequency.
X-axis: Frequency sweep from ~0.1 Hz to 100 MHz (logarithmic scale).
Corner frequency around ~300 kHz**.** This matches the previously calculated frequency of 290kHz

Phase remains near 0° at low frequencies (ideal inverting behavior). It gradually drops, approaching -90° and beyond, due to the capacitive effects from the photodiode junction and feedback network. The gain-bandwidth product is maintained, and the op-amp does not saturate or clip. The smooth roll-off and phase lag indicate a well-compensated system. Phase crossing –180° does not happen near unity gain, so no risk of instability.

4) Time delay vs frequency

Fig 27. shows the Time delay vs frequency plot for TIA circuit with 100kΩ feedback resistor and 5pF capacitor.

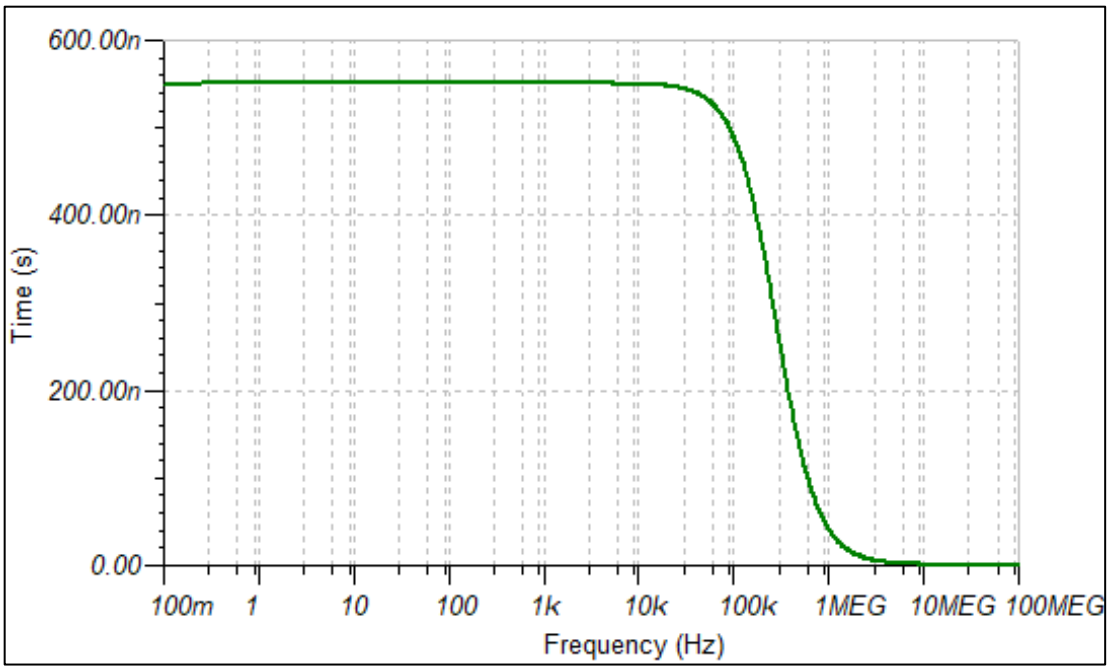

Figure 10. Time delay vs Frequency plot

The plot shows group delay (a measure of phase change per frequency unit), which in a physical sense represents how much the signal is delayed as it passes through the amplifier. Measured in seconds, plotted vs frequency (log scale).

Constant delay (~575 ns) at low frequencies: This represents the effective integration delay of the TIA — very low and stable. At higher frequencies (~>100 kHz), the delay starts to drop off sharply, indicating the amplifier is no longer tracking input changes linearly due to bandwidth limitations.

4.2.4 PCB design

After the design and simulation, a 4 layer PCB was designed and printed in Kicad. Fig 28. shows the overall PCB design for the Photodiode transimpedance amplifier circuit-

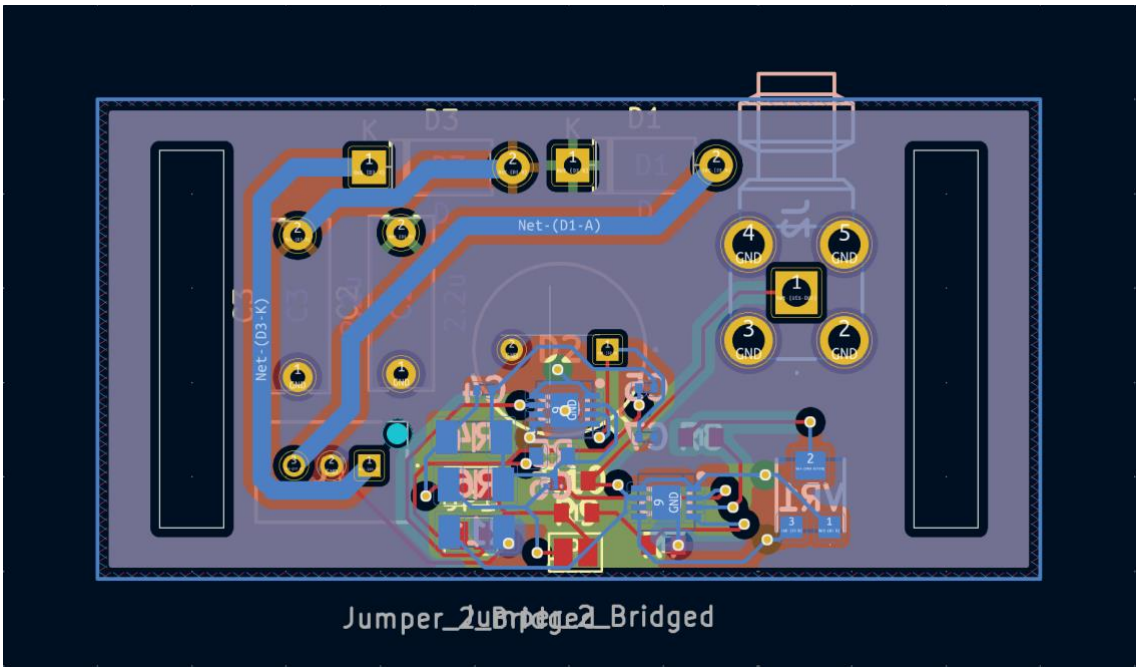

Figure 11. Linear power supply PCB

Key features such as solid ground planes, separated power routing, tight feedback loops, and extensive decoupling contribute to the high stability and accuracy of the TIA, enabling reliable detection of interference fringes in the wavelength meter system.
The power plane separately routes +5V and –5V rails with careful decoupling.
The amplified output is routed to a SMA 2484782-1 high-quality connector, providing a secure and low-noise connection.

The front layer (top side) of the PCB hosts the main active circuitry**:**
The low-noise OPA817 operational amplifier responsible for transimpedance amplification.
The feedback network forms a tight, minimal area loop**.**
Input protection diodes and supply decoupling capacitors.

The back layer of the PCB has the photodiode (S1223) mounted perfectly centred
The photodiode is positioned to:
Minimize parasitic capacitance and inductive pickup.
Keep the input leads as short as possible, thereby reducing input noise and preserving bandwidth**.**

Direct and shielded traces connect the photodiode anode and cathode to the TIA input stage, ensuring low impedance paths for the weak photocurrent signal.

This careful mechanical and electrical arrangement ensures that maximum SNR**,** minimal input capacitance**,** and stable, low-noise operation are achieved.

4.2.5 Enclosure design

After the PCB printing stage, a custom enclosure was designed to accommodate the PCB. The enclosure supported the following physical dimensions:

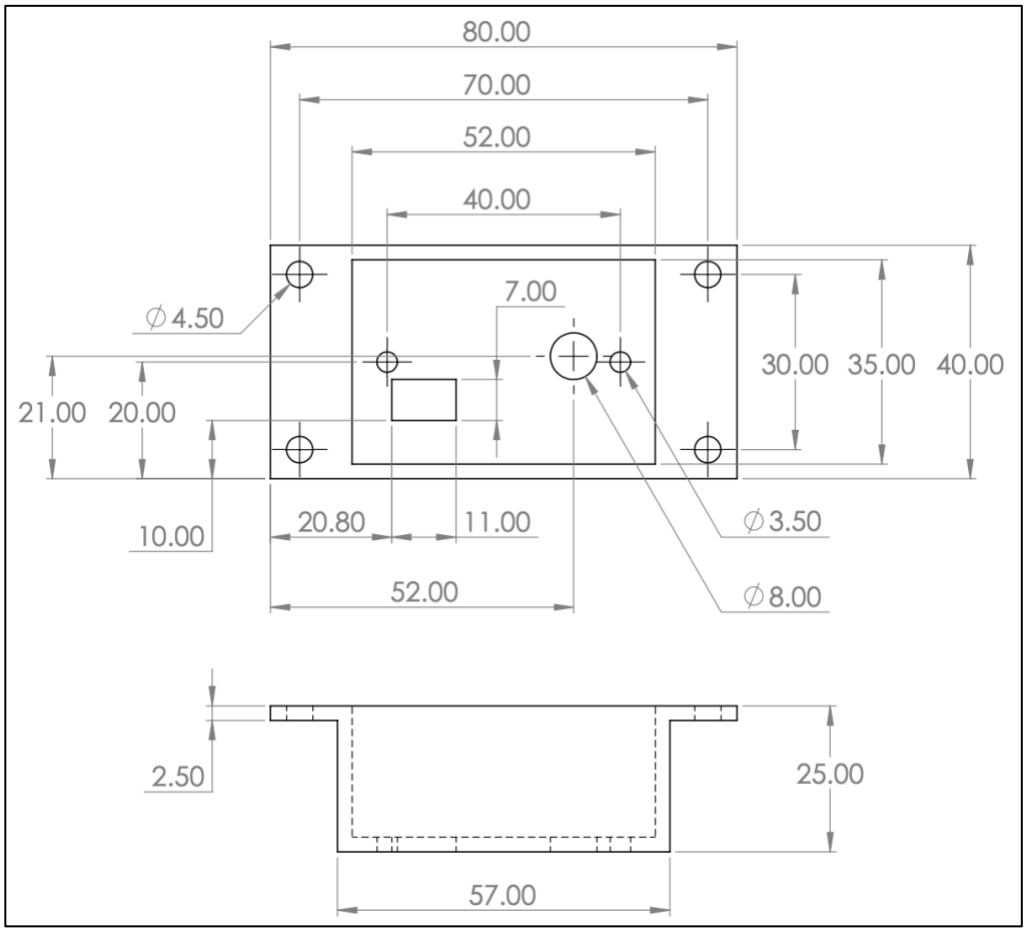

Figure 12. Linear power supply PCB

The Power supply Enclosure has dimensions-
Length: 80mm
Width: 40mm
Height: 25mm
Mounting hole diameters: 4.5mm

Fig 29. shows the detailed mechanical drawing of the custom metal enclosure designed for the TIA used in the interferometer project. The enclosure is machined from metal and finished with a matte black paint, matching the overall aesthetic and functional setup of the interferometer system.

The enclosure provides mechanical protection**,** thermal management, and electromagnetic shielding to ensure high reliability and low-noise performance.

4.2.6 Challenges and resolutions

1) Design

Earlier designs used different models of op-amps but were changed due to bandwidth and gain constraints.

2) Simulation

Due to the lack of availability of a few components (such as the variable resistor), Calculated Voltage values were used for simulating the circuit.

A current generator generating 22.5μA current is placed instead of a photodiode

3) PCB

Earlier design included a single layer PCB but was switched out for a 4 layer PCB due to size restrictions.

Removal of power entry circuit due to size constraints.

4) Enclosure and connections

Earlier models of the enclosure required fine tuning as the PCB wasn't centred resulting in partial laser beam falling on the photodiode.