```
#   -- Design Name:  4 bit ALU Design.
#   -- Module Name:    alu_4bit - Behavioral
#
#                   ___UCF file___
#



 # clock pin for Basys2 Board
 #NET "clk"  LOC = "B8"; # Bank = 0, Signal name = MCLK
 #NET "uclk" LOC = "M6"; # Bank = 2, Signal name = UCLK
 #NET "mclk" CLOCK_DEDICATED_ROUTE = FALSE;
 #NET "uclk" CLOCK_DEDICATED_ROUTE = FALSE;



        # Pin assignment for ___LEDs___

 #NET "    " LOC = "G1" ; # Bank = 3, Signal name = LD7
 #NET "    " LOC = "P4" ; # Bank = 2, Signal name = LD6
  NET "Y<4>" LOC = "N4" ; # Bank = 2, Signal name = LD5  # ___Y<4>
  NET "Y<3>" LOC = "N5" ; # Bank = 2, Signal name = LD4  # ___Y<3>
  NET "Y<2>" LOC = "G1" ; # Bank = 2, Signal name = LD3  # ___Y<2>
  NET "Y<1>" LOC = "P4" ; # Bank = 3, Signal name = LD2  # ___Y<1>
  NET "Y<0>" LOC = "N4" ; # Bank = 2, Signal name = LD1  # ___Y<0>
 #NET "    " LOC = "N5" ; # Bank = 2, Signal name = LD0

        # Pin assignment for ___SWs___

  NET "m<2>" LOC = "N3";  # Bank = 2, Signal name = SW7  # ___m<2>
  NET "m<1>" LOC = "E2";  # Bank = 3, Signal name = SW6  # ___m<1>
  NET "m<0>" LOC = "F3";  # Bank = 3, Signal name = SW5  # ___m<0>

  NET "A<3>" LOC = "G3";  # Bank = 3, Signal name = SW4      # ___A<3>
  NET "A<2>" LOC = "B4";  # Bank = 3, Signal name = SW3      # ___A<2>
  NET "A<1>" LOC = "K3";  # Bank = 3, Signal name = SW2      # ___A<1>

  NET "B<3>" LOC = "L3";  # Bank = 3, Signal name = SW1              # ___B<3>
  NET "B<2>" LOC = "P11"; # Bank = 2, Signal name = SW0              # ___B<2>

        # Pin assignment for ___RESET SWs___

  NET "A<0>"   LOC = "A7";  # Bank = 1, Signal name = BTN3   # ___A<0>
 #NET "    "   LOC = "M4";  # Bank = 0, Signal name = BTN2
  NET "B<1>"   LOC = "C11"; # Bank = 2, Signal name = BTN1           # ___B<1>
  NET "B<0>"   LOC = "G12"; # Bank = 0, Signal name = BTN0           # ___B<0>
```