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#           -- Design Name:  FIFO Memory
#           -- Module Name:    fifo - Behavioral
#
#                              ___UCF file___




# clock pin for Basys2 Board

 NET "mclk" LOC = "B8"; # Bank = 0, Signal name = MCLK
#NET "uclk" LOC = "M6"; # Bank = 2, Signal name = UCLK
#NET "mclk" CLOCK_DEDICATED_ROUTE = FALSE;
#NET "uclk" CLOCK_DEDICATED_ROUTE = FALSE;



#                       Pin assignment for LEDs

 NET "mememp"  LOC = "G1" ; # Bank = 3, Signal name = LD7
 NET "memfull" LOC = "P4" ; # Bank = 2, Signal name = LD6
#NET "Led<5>"  LOC = "N4" ; # Bank = 2, Signal name = LD5
#NET "Led<4>"  LOC = "N5" ; # Bank = 2, Signal name = LD4

 NET "dataout<3>" LOC = "G1" ; # Bank = 2, Signal name = LD3
 NET "dataout<2>" LOC = "P4" ; # Bank = 3, Signal name = LD2
 NET "dataout<1>" LOC = "N4" ; # Bank = 2, Signal name = LD1
 NET "dataout<0>" LOC = "N5" ; # Bank = 2, Signal name = LD0


#                       Pin assignment for SWs

 NET "rd"    LOC = "N3";  # Bank = 2, Signal name = SW7
 NET "wr"    LOC = "E2";  # Bank = 3, Signal name = SW6
#NET "sw<5>" LOC = "F3";  # Bank = 3, Signal name = SW5
#NET "sw<4>" LOC = "G3";  # Bank = 3, Signal name = SW4

 NET "datain<3>" LOC = "B4";  # Bank = 3, Signal name = SW3
 NET "datain<2>" LOC = "K3";  # Bank = 3, Signal name = SW2
 NET "datain<1>" LOC = "L3";  # Bank = 3, Signal name = SW1
 NET "datain<0>" LOC = "P11"; # Bank = 2, Signal name = SW0



#                       Pin assignment for RESET SW

 NET "rst"    LOC = "A7";  # Bank = 1, Signal name = BTN3
#NET "btn<2>" LOC = "M4";  # Bank = 0, Signal name = BTN2
#NET "btn<1>" LOC = "C11"; # Bank = 2, Signal name = BTN1
#NET "btn<0>" LOC = "G12"; # Bank = 0, Signal name = BTN0
```