COL216 Assignment 3
List of Assumptions

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Simulation Assumptions for Assignment 3

- Caches are blocking, meaning if a cache miss occurs, the core halts and does not issue any new instruction until the miss is serviced and the data is available.
- Snooping is passive, meaning caches always listen to the bus even if the core is stalled or the bus is busy. No additional bus transaction is needed for snooping.
- Only one active bus transaction can happen at any time, including memory fetches, cache-to-cache transfers, and invalidates. Other bus requests must wait.
- Cache-to-cache data transfer requires bus ownership. If the bus is busy, the transfer must wait until the bus is free.
- A snooping cache immediately detects a relevant transaction when it appears on the bus, even if the bus is busy for other purposes.
- Once a cache detects that it needs to respond to a transaction, such as supplying a cache line, it logically holds the data and does not evict it until the response is completed. No modeling of eviction races is required.
- After a cache miss, the core waits for the data to arrive, then spends one additional cycle to perform the actual cache hit and complete the instruction.
- Bus transactions include memory fetch, cache-to-cache transfer, and invalidation broadcasts. Simple reads or writes that hit in cache do not occupy the bus.
- In case of cache miss, assume 100 cycles are spent on memory fetch and the 101st cycle completes the instruction with a cache hit.

- Execution cycles count cycles during which the core is actively processing instructions. Idle cycles count cycles during which the core is stalled waiting for cache miss or bus availability.
- Once a core finishes executing all its instructions, it is considered done. Further cycles are not counted under idle cycles for that core.
- You should model everything logically and simply. Do not simulate internal bus arbitration, snoop delays, or race conditions unless explicitly stated.

The above assumptions would be strictly followed. Please reread these assumptions carefully. If a behavior is not mentioned explicitly in the assignment or above, you should assume the simplest and most logical behavior to maintain coherence and progress.