EE 705 VLSI DESIGN LAB

Problem Statement: The code for a 16-bit Single-cycle implementation of MIPS processor is given in VHDL and Verilog with its instruction set architecture (ISA). With the help of this implementation, you have to design a Single-cycle implementation of the MIPS processor with added instructions in Verilog or VHDL (only one).

New Instruction:

Name	Format	Opcode (3 bits)	rs (3 bits)	rt (3 bits)	rd (3 bits)	Funct (4 bits)
mul	R-type	0				5
Sll	R-type	0				6
Srl	R-type	0				7

Description of these extra instruction is given below:

1. mul (Multiply):
   R[rd](15 downto 0) = R[rs](7 downto 0) * R[rt](7 downto 0)

   where R[rs], R[rt] and R[rd] are the 16-bit data and rs and rt is the location of source registers and rd is the location of the destination register.
   The operands should be 8-bits only for the multiplication operation, since the output will be more than 16-bits, if operands are more than 8 bits.

2. sll (shift left logical):
   R[rd](15 downto 0) = R[rs](15 downto 0)<<R[rt](2 downto 0)

3. srl (shift right logical):
   R[rd](15 downto 0) = R[rs](15 downto 0)>>R[rt](2 downto 0)

   The contents of register Rs is shifted Right or Left according to the value specified by lower 3-bits of register Rt.

- **Design an entity or module for Logarithmic Barrel Shifter for sll and srl instruction and instantiate within ALU entity or module.**

Resources Available:

VHDL code:
https://www.fpga4student.com/2017/09/vhdl-code-for-mips-processor.html

Verilog code and ISA (along with data path and control signals):
https://www.fpga4student.com/2017/01/verilog-code-for-single-cycle-MIPS-processor.html

Submission Format: On MS-TEAMS inside class-notebook area as explained in the videos at the following (basically create a page in "Homework" section of your class notebook and entitle the page "Homework-1" or "HW-1" and put into it the URL to video-clip, as well as the zip file of the complete project along with screenshots of simulation results)