EE739: Processor Design

Project 1

Team Members

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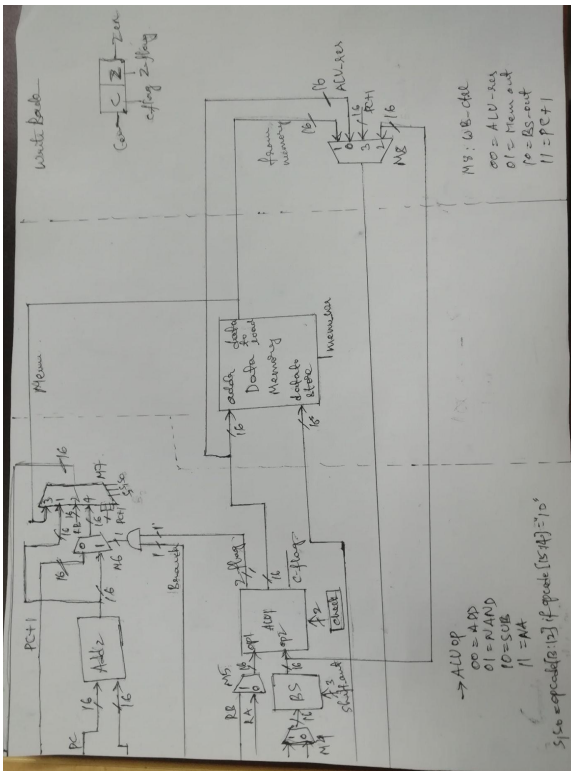
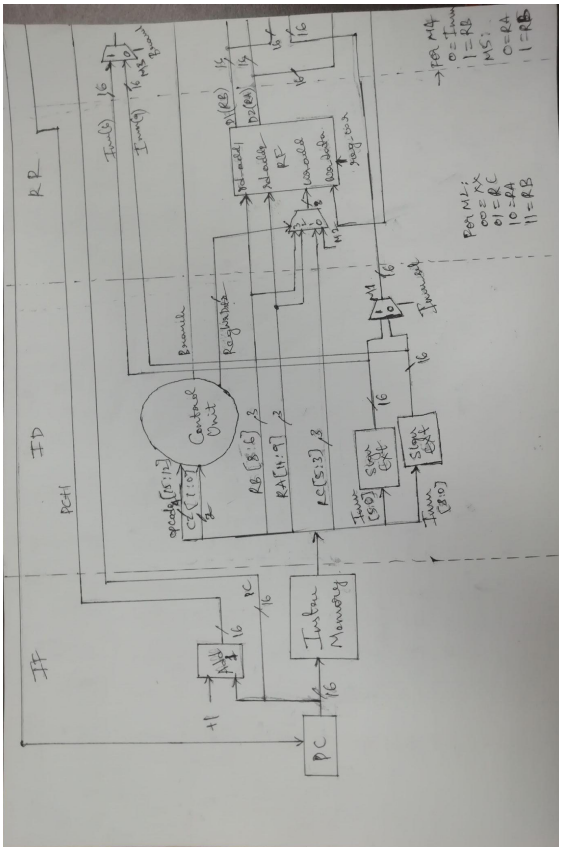
Single-cycle Datapath:





Control Signals:

Instruction	ADD	ADC	ADZ	ADL	ADI	NDU	NDC	NDZ	LHI	LW	SW	BEQ	JAL	JLR	JRI
Instruction type	R	R	R	R	I	R	R	R	J	I	I	I	J	I	J
M1 => Imm_sel	X	X	X	X	1	X	X	X	0	1	1	1	0	X	0
M2 => RegWrDst	"01"	"01"	"01"	"01"	"11"	"01"	"01"	"01"	"10"	"10"	"XX"	"XX"	"10"	"10"	"XX"
RegWrite	1	1	1	1	1	1	1	1	1	1	0	0	1	1	0
M3 => if_branch	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0
M4 => ALU1OP2_SEL	1	1	1	1	0	1	1	1	0	0	0	1	X	X	0
M5 => ALU1OP1_SEL	0	0	0	0	0	0	0	0	X	1	1	0	X	X	0
Barrel Shifter (shft_amt by no. of bits)	"000"	"000"	"000"	"001"	"000"	"000"	"000"	"000"	"111"	"000"	"000"	"000"	"000"	"000"	"000"
Rtype	1	1	1	1	0	1	1	1	0	0	0	0	0	0	0
ALU1 (ALU_Op)	"00"	"00"	"00"	"00"	"00"	"01"	"01"	"01"	"11"	"00"	"00"	"10"	"11"	"11"	"00"
M6 => If_Beq (If_branch AND Z_flag)	X	X	X	X	X	X	X	X	X	X	X	1	0	0	0
M7 => PC_target_addr	"000"	"000"	"000"	"000"	"000"	"000"	"000"	"000"	"000"	"000"	"000"	"100"	"001"	"010"	"011"
MemWrite	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
M8 => WB_Ctrl	"00"	"00"	"00"	"00"	"00"	"00"	"00"	"00"	"10"	"01"	"XX"	"XX"	"11"	"11"	"XX"
CWrite	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
ZWrite	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0

Pipelined Datapath Block Diagram (exported from Quartus):

High Resolution Image:
https://drive.google.com/drive/folders/1fC7fEL1zOtiAxo19sg7bPF6B7xqhtX5E?usp=sharing