Timeline

Date	Milestone
6 Apr 2018	Design Document Submission
13 Apr 2018	Implementation of basic modules
20 Apr 2018	Integration of modules
27 Apr 2018	Testing completion

Module Division

Aditya Gupta	Love Mehta
Bus	Cache Set & Line
Simulator	Cache (basic structure and few requests)
Cache (remaining requests)	Testing state transitions
Testing address management & statistics	