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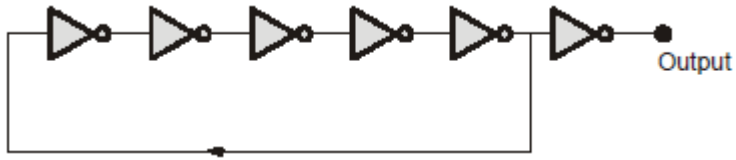
Solution Report For Digital Logic-1

Represent whole test solution with correct and incorrect answers.

View Your Test Analysis

Q. No	Question Status

Q.1 **In the circuit shown below, the propagation delay of each NOT gate is 2 nsec (2 nano sec), then the time period of generated square wave is –**



a. 10 nsec
b. 14 nsec
c. 18 nsec
d. 20 nsec

Not Attempt | **Correct Ans.** | d | FAQ? | Have any doubt? | bookmark

Solution. 1

(d)

$$N = 5,$$
$$t_{pd} = 2\,\text{nsec}$$
$$T = 2N t_{pd}$$
$$\Rightarrow \quad T = 2 \times 5 \times 2 \times 10^{-9}$$
$$= 20\,\text{nsec}$$

Q.2 **The minimal logic expression corresponding to the *K*-map shown below is**

WX \ YZ	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

a. XZ

b. $\bar{W}X\bar{Y} + \bar{W}YZ + W\bar{Y}Z + WXY$

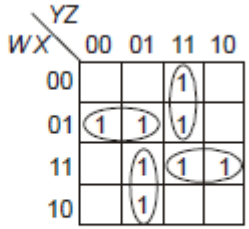
c. $\bar{W}X\bar{Y} + \bar{W}YZ + W\bar{Y}Z + WX\bar{Y}$

d. $XZ + \bar{W}YZ + \bar{W}X\bar{Y} + WXY + W\bar{Y}Z$

Attempt | **Correct** **Correct Ans.** | **b** | FAQ? | Have any doubt? | bookmark

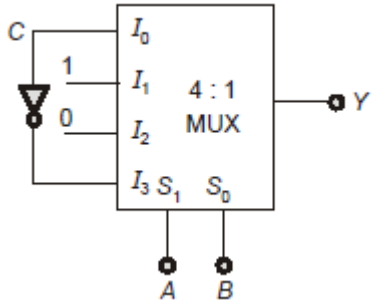
Solution. 2

(b)



$$Z = \bar{W}X\bar{Y} + WXY + \bar{W}YZ + W\bar{Y}Z$$

Q.3 **The output of the given 4 : 1 MUX will be**



a. Σm (1,2, 3, 6)
b. Σm (2, 4, 5, 7)
c. Σm (1,3, 4, 7)
d. Σm (1,2, 6, 7)

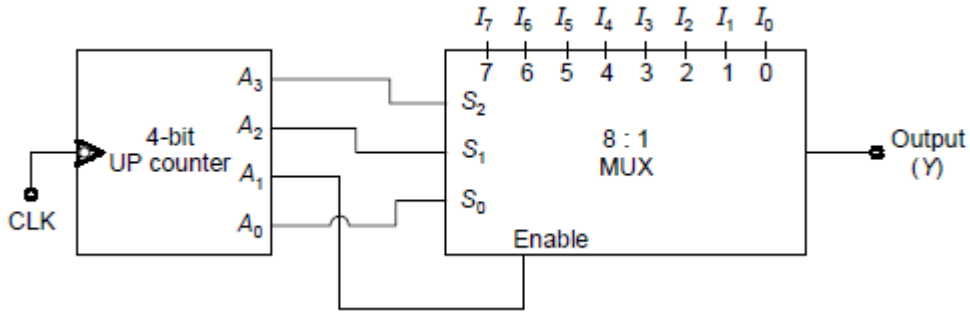
Attempt | **Correct** **Correct Ans.** | **a** | FAQ? | Have any doubt? | bookmark

Solution. 3

(a)

$$
\begin{aligned}
Y &= \bar{S}_0\bar{S}_1I_0 + S_0\bar{S}_1I_1 + \bar{S}_0S_1I_2 + S_0S_1I_3 \\
&= \bar{A}\bar{B}C + \bar{A}B\cdot 1 + A\bar{B}\cdot 0 + AB\cdot\bar{C} \\
&= \bar{A}\bar{B}C + \bar{A}B\cdot(C+\bar{C}) + AB\bar{C} \\
&= \bar{A}\bar{B}C + \bar{A}BC + \bar{A}B\bar{C} + AB\bar{C} \\
&\approx 001, 011, 010, 110 \\
f(A,B,C) &= \Sigma m\,(1,2,3,6)
\end{aligned}
$$

Q.4 **A 4-bit Down counter is used to control the output of the multiplexer as shown in figure. The counter is initially at $(1111)_2$, then the output of the multiplexer will follow the sequence –**



a. $I_7, 0, I_6, 0, I_5, 0 \ldots$

b. $I_7, 0, 0, I_6, 0, 0, I_5 \ldots$

c. $I_7, I_6, I_5, I_4, I_3 \ldots$

d. $I_7, I_6, 0, 0, I_5, I_4, 0, 0 \ldots$

Not Attempt | **Correct Ans.** d | FAQ? | Have any doubt? | bookmark

Solution. 4

(d)

Counter output =

	S_2 A_3	S_1 A_2	E A_1	S_0 A_0		
1st clock	1	1	1	1	– 15	I_7
2nd	1	1	1	0	– 14	I_6
3rd	1	1	0	1	– 13	0
4th	1	1	0	0	– 12	0
5th	1	0	1	1	– 11	I_5
6th	1	0	1	0	– 10	I_4

For 1st and 2nd clock pulses, enable is 1

	S_2	S_1	S_0		
1st clock pulse –	1	1	1	→	1_7
2nd clock pulse –	1	1	0	→	1_6

For 3rd and 4th clock pulse, enable is 0,

So, Y is 0

Q.5 **Consider the following boolean expression:**

$$F = \left[x + z\left\{\overline{y} + (\overline{z} + x\overline{y})\right\}\right]\left[\left\{\overline{x} + z(x + y)\right\}\right] = 1$$

If *x* = 1 in above expression then the value of *z* is _____.

Attempt | **Correct** **Correct Ans.** | **1** | FAQ? | Have any doubt? | bookmark

Solution. 5

1

Given boolean expression

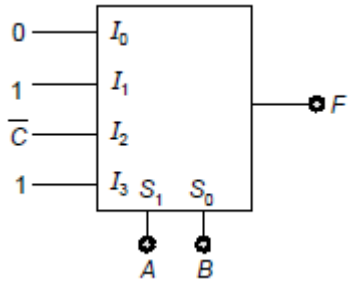
$$\left[x+z\left\{\overline{y}+(\overline{z}+x\overline{y})\right\}\right]\left[\left\{\overline{x}+z(x+y)\right\}\right]=1$$

put $x = 1$ and $\overline{x} = 0$

$$\underbrace{\left[1+z\left\{\overline{y}+(\overline{z}+\overline{y})\right\}\right]}_{1}\underbrace{\left[0+z(1+y)\right]}_{z}=1$$

So minimum expression is [1][z([1]] = 1
Then to satisfy equation z must be 1.

Q.6 **The number of minimum terms of the following function F which is implemented by MUX _____.**



Attempt | **Incorrect** **Your Ans.** | **2** | **Correct Ans.** | **5** | FAQ? | Have any doubt? | bookmark

Solution. 6

5

$$F = \overline{A}\overline{B}\cdot 0+\overline{A}B\cdot 1+A\overline{B}\overline{C}+AB\cdot 1$$

$$= \underset{2,3}{\overline{A}B}+\underset{4}{A\overline{B}\overline{C}}+\underset{6,7}{AB}$$

$$= \Sigma m\,(2, 3, 4, 6, 7)$$

Q.7 **Total number of AND gates present inside a 6-bit carry look ahead generator circuit is _____**

Attempt | Correct | Correct Ans. | 21 | FAQ? | Have any doubt? | bookmark

Solution. 7

21

Total AND gates for a n-bit carry look ahead generator is $1 + 2 + 3 + 4 + \ldots + n = \frac{n(n+1)}{2}$

Here $n = 6$

$\therefore$ Total AND gates $= \frac{6 \times 7}{2} = 21$

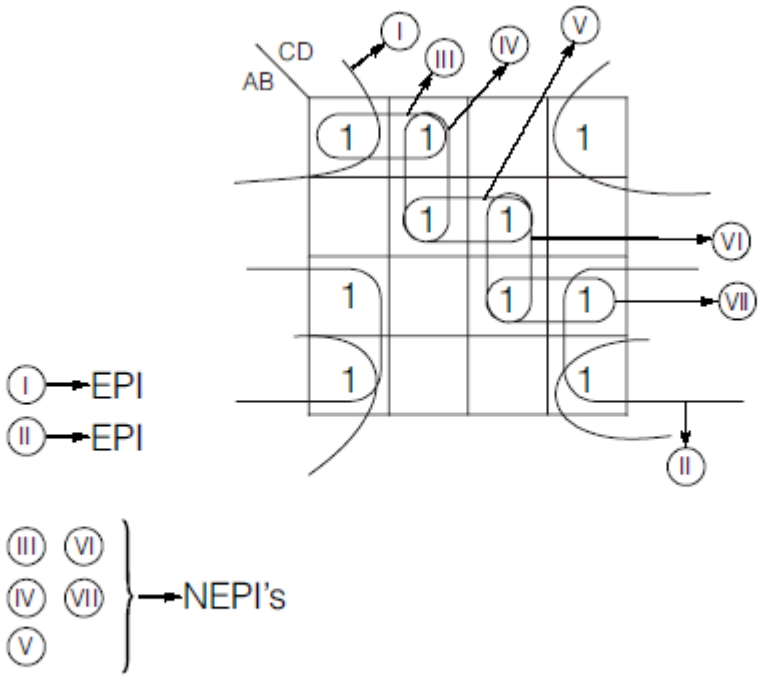
Q.8 **Consider the Boolean function f(A,B,C,D) = Σm (0, 1, 2, 5, 7, 8, 10, 12, 14, 15). Function is having how many number of essential prime implicants?**

a. 2
b. 3
c. 4
d. 5

Attempt | Incorrect | Your Ans. | c | Correct Ans. | a | FAQ? | Have any doubt? | bookmark

Solution. 8

(a)



EPI = Essential Prime Implicant [which cover a minterm not covered by any other prime implicant
NEPI = Non Essential Prime Implicant. Number of EPI's = 2, number of NEPI's = 5.

Q.9 **The Boolean function can be expressed in canonical SOP and POS forms. So, for $Y = A\bar{B} + B\bar{C}$, the SOP and POS forms will be –**

a. $Y = \Sigma(0, 2, 4, 6);\ Y = \pi(1, 3, 7)$

b. $Y = \Sigma(1, 2, 5, 7);\ Y = \pi(0, 3, 4, 6)$

c. $Y = \Sigma(2, 4, 5, 6);\ Y = \pi(0, 1, 3, 7)$

d. $Y = \Sigma(1, 2, 4, 5);\ Y = \pi(0, 3, 6)$

Attempt | **Correct** **Correct Ans.** | **c** | FAQ? | Have any doubt? | bookmark

Solution. 9

(c)

Plotting the K-map for $Y = A\bar{B} + B\bar{C}$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	3	1 (2)
A	1 (4)	1 (5)	7	1 (6)

So, $\Sigma m\,(2, 4, 5, 6)$ = SOP

$\Sigma \pi\,(0, 1, 3, 7)$ = POS

Q.10 **A half adder is implement with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 μsec. A 4-bit ripple carry binary adder is implemented by using full adders. The total propagation delay of this 4-bit binary adder is**

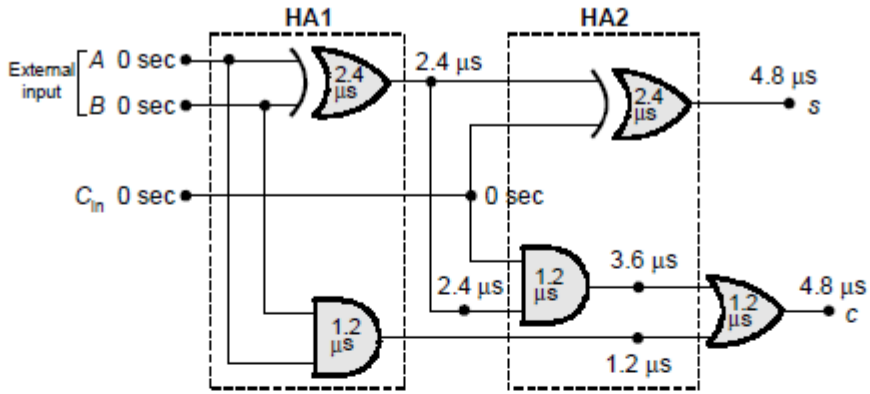
a. 19 μsec
b. 19.2 μsec
c. 12 μsec
d. 38.4 μsec

Attempt | **Incorrect** **Your Ans.** | **b** | **Correct Ans.** | **c** | FAQ? | Have any doubt? | bookmark

Solution. 10

(c)

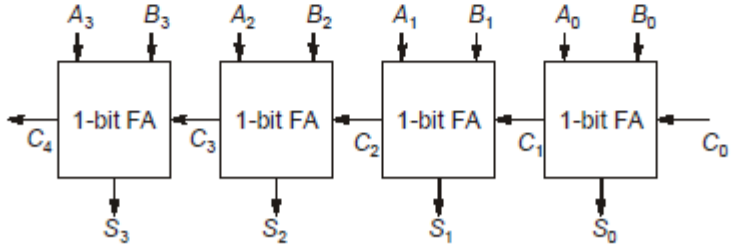
For one full Adder :



The propagation delay of AND / OR gate t_{pd} = 1.2 µ sec.

The propagation delay of EX-OR gate $2t_{pd}$ = 2.4 µ sec.

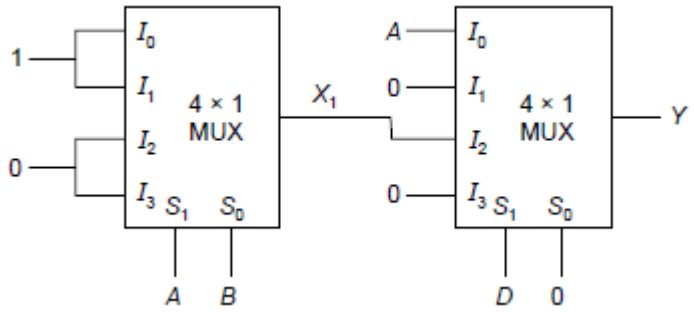
- Binary Adder external inputs are available to all HA1's simultaneously.
- First HA1 output of all full adders are available simultaneously with delay of 2.4 µsec (i.e., $2t_{pd}$).
- Carry generate from previous Full adder is passing only through HA2 of next full adder.
- The delay of LSB full adder = $4t_{pd}$.
- The 4 bit ripple carry binary delay:



$= 4t_{pd} + 2t_{pd} + 2t_{pd} + 2t_{pd} = 10t_{pd}$

$= 10 \times 1.2$ µsec $= 12$ µsec

Q.11 **What will be the output of multiplexer shown below –**



a. $A \oplus D$

b. $A \odot D \odot B$

c. $A + D + \bar{B}$

d. $A \cdot D$

Attempt | **Correct** **Correct Ans.** | **a** | FAQ? | Have any doubt? | bookmark

Solution. 11

(a)

For 1st 4 × 1 MUX –

$$X_1 = \bar{A}\bar{B} \cdot 1_B + \bar{A}B \cdot 1 + A\bar{B} \cdot 0 + AB \cdot 0$$

$$\Rightarrow \quad = \bar{A}\bar{B} + \bar{A}B = \bar{A}(B + \bar{B}) = \bar{A}$$

For 2nd 4 × 1 MUX –

$$Y = \bar{D}\bar{0} \cdot A + \bar{D} \cdot 0 \cdot 0 + D\bar{0} \cdot X_1 + D \cdot 0 \cdot 0$$

$$= \bar{D} \cdot 1 \cdot A + D \cdot 1 \cdot \bar{A} = A \oplus D$$

Q.12 **Match List-I with List-II and select the correct answer using the codes given below the lists:**

List-I	List-II
A. $(A \oplus B) \oplus (B \oplus C)$	**1.** $(A \odot C)$
B. $AB + \bar{A}C + BC$	**2.** $(A + B) \odot (A + C)$
C. $(A \odot B) \odot (B \odot C)$	**3.** $AB + \bar{A}C$
D. $A + (B \odot C)$	**4.** $(A \oplus C)$
	5. $\bar{A}B \oplus AC$

Codes

	A	B	C	D
(a)	4	3	1	2
(b)	3	4	1	2
(c)	2	3	1	2
(d)	4	3	5	2

a. a
b. b
c. c
d. d

Attempt | **Correct** | **Correct Ans.** | **a** | FAQ? | Have any doubt? | bookmark

Solution. 12

(a)

$$(A \oplus B) \oplus (B \oplus C)$$

$$\Rightarrow \quad (\overline{A \oplus B})(B \oplus C) + (A \oplus B)(\overline{B \oplus C})$$

$$\Rightarrow \quad (AB + \bar{A}\bar{B})(A\bar{B}C + B\bar{C}) + (\bar{A}B + A\bar{B})(BC + \bar{B}\bar{C})$$

$$\Rightarrow \quad AB\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C}$$

$$\Rightarrow \quad \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$$

$$(\bar{A}C + A\bar{C}) = A \oplus C$$

(A) matches with (4)

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

This is concensus law in XOR algebra.

(C) matches with (1)

(B) matches with (3)

$$A + (B \odot C) = \underbrace{(A + B) \odot (A + C)}_{\text{Follows distributive law}}$$

(D) matches with (2)

Q.13 **The maximum number of Boolean expressions that can be formed for the function f(x, y, z) satisfying the relation** $f(\bar{x}, y, \bar{z}) = f(x, y, z)$ **is _____.**

Not Attempt | **Correct Ans.** 16 | FAQ? | Have any doubt? | bookmark

Solution. 13

16

For every combination of x, y, z the function value remains same for input $\overline{x}, y, \overline{z}$.

x y z	f(x, y, z) = f($\overline{x}$, y, $\overline{z}$)
0 0 0 1 0 1	} either 0 or 1
0 0 1 1 0 0	} either 0 or 1
0 1 0 1 1 1	} either 0 or 1
0 1 1 1 1 0	} either 0 or 1

Effectively there are only four rows for the truth table of the function f (x, y, z).

$\therefore$ Total Boolean expressions possible is $2^4 = 16$.

Q.14 **How many numbers of 8 : 1 MUX is required to implement 256 : 1 MUX ?**

Attempt | **Incorrect** **Your Ans.** | **32** | **Correct Ans.** | **37** | FAQ? | Have any doubt? | bookmark

Solution. 14

37

$$\text{Number of MUX} = \frac{256}{8} = 32 \quad \Rightarrow \frac{32}{8} = 4$$

$$\Rightarrow \quad \frac{4}{8} = 1$$

$$\text{Total} = 32 + 4 + 1 = 37$$

Q.15 **A Boolean function of two variables *X* and *Y* is defined as follows:**

***f* (0, 0) = *f* (0, 1) = *f* (1, 1) = 1 and *f* (1, 0) = 0**

Assume complement of *X* and *Y* are not available, then the minimum cost solution for implement *f* using 2 input Nand gate and 2 input OR gate is (Total cost) _____. (Let each 2 input OR or Nand gate have 2 unit cost).

Attempt | Correct | Correct Ans. | 4 | FAQ? | Have any doubt? | bookmark

Solution. 15

4

The Boolean function of two variables X and Y are

$$f(0, 0) = f(0, 1) = f(1, 1) = 1 \text{ and } f(1, 0) = 0$$

Truth table is:

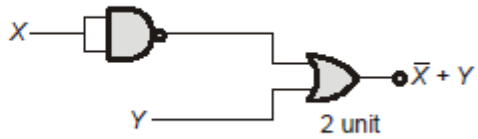
X	Y	F
0	0	1
0	1	1
1	0	0
1	1	1

Function f boolean expression is $= \bar{X}\bar{Y} + \bar{X}Y + XY$

$$= \bar{X} + XY$$

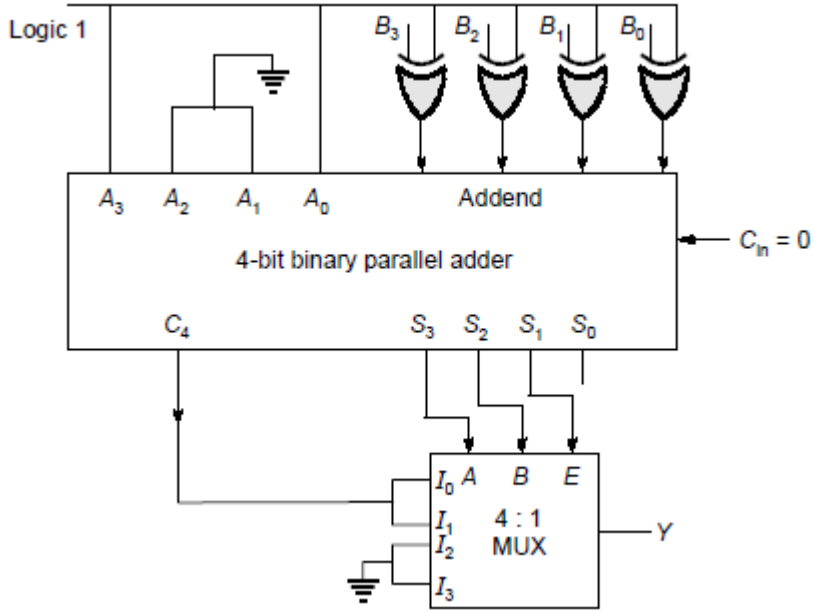
$$= \bar{X} + Y$$

Since function implement using 2 input Nand gate or OR gate



So total cost = (2 + 2) unit = 4 unit.

Q.16 **Consider the digital circuit shown below. What will be the output *Y*, if the number $B_3\ B_2\ B_1\ B_0 = 0101$**



Not Attempt | **Correct Ans.** 1 | FAQ? | Have any doubt? | bookmark

Solution. 16

1

$$\text{Addend will be} = 1010$$
$$S_3\ S_2\ S_1\ S_0 = 1010 + A_3\ A_2\ A_1\ A_0 + C_{in}$$
$$= 1010 + 1001$$
$$= 0011 \qquad (C_4 = 1)$$
$$AB = 00$$

and $E = C_4 = 1$

So, $Y = 1$