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Solution Report For Computer Organization and Architecture-1

Represent whole test solution with correct and incorrect answers.

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Q. No	Question Status

Q.1

Consider the following statements with respect to control unit.

S_1 : Operating speed of vertical microprogramming is higher than that of horizontal micropgramming.

S_2 : Horizontal microprogramming needs signal decoders as like vertical microprogramming.

Which of the following option in correct?

a. Both S_1 and S_2 are correct
b. Only S_1 is correct
c. Only S_2 is correct
d. None of S_1 or S_2 is correct

Attempt | **Incorrect** **Your Ans.** c | **Correct Ans.** d | FAQ? | Have any doubt? | bookmark

Solution. 1

(d)
• Since, vertical microprogram encode the control signals hence a signal decoder is needed which decrease the operation speed of vertical micro-programming in comparison with horizontal microprogramming.
• Since, the control signal bits under horizontal microprogram control unit are not encoded. Hence no signal decoder is needed.

Q.2 **Consider a CPU, where all the instructions require 6 clock cycles to complete their execution. Under the instruction set there are 215 instructions and a total of 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic. What is the minimum size of control word and control address register.**

a. 136, 11
b. 7, 12
c. 7, 11
d. 125, 12

Attempt Correct **Correct Ans.** a FAQ? Have any doubt? bookmark

Solution. 2

(a)
Since, it uses horizontal micro-programmed that requires 1 bit control / signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = 215 × 6 = 1290
It requires 11 bit.

Q.3 **In a 16 bit computer instruction format, the size of address field is 5 bits. The computer uses expanding opcode technique. It has two 2-address instructions and 1024 one address instruction. How many zeroaddress instruction can be formulated?**

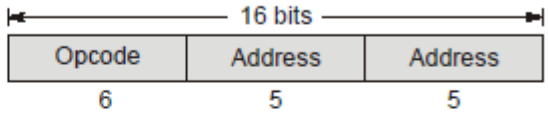
a. 28720
b. 30704
c. 30720
d. 32704

Attempt | Correct **Correct Ans.** | c | FAQ? | Have any doubt? | bookmark

Solution. 3

(c)

Address format



Number of operations = $2^6 = 64$

Number of free opcodes after 2-address = 64 – 2 = 62

Number of 1 add instruction = 62 × 32 = 1984

Free opcodes = 1984 – 1024 = 960

Number of 0 add instruction = 960 × 32 = 30720

Q.4 **The following assembly code is to be executed in a 3-stage pipelined processor with hazard detection and resolution in each stage. The stage are IF, OF (one or more as required) and execution (including writeback operation). What are the number of possible RAW, WAW and WAR hazards in the execution of the code.**

Instruction	Meaning
I_1: Inc R_0	$R_0 \leftarrow (R_0) + 1$
I_2: Mul ACC, R_0	Acc $\leftarrow$ (ACC) $\times$ (R_0)
I_3: Store R_1, ACC	$R_1 \leftarrow$ (ACC)
I_4: Add ACC, R_0	Acc $\leftarrow$ (ACC) + (R_0)
I_5: Store M, ACC	M $\leftarrow$ (ACC)

a. 6, 1, 2
b. 5, 3, 3
c. 5, 3, 2
d. 5, 1, 2

Attempt | Correct **Correct Ans.** | d | FAQ? | Have any doubt? | bookmark

Solution. 4

(d)
RAW hazards: $I_1 - I_2, I_1 - I_4, I_2 - I_3, I_2 - I_4, I_2 - I_5$
WAW hazards: $I_2 - I_4$
WAR hazards: $I_3 - I_4$ and $I_2 - I_4$

Q.5 **Consider a scenario where instruction operation codes are represented in 8 bits, memory addresses are 64 bits and register addresses are 6 bits and data values are 32 bit integers.**
Consider the code sequence for "C = A + B" is as follows:

Stack	Accumulator	Register (Register-Memory)	Register (Load-store)
Push A Push B Add Pop C	Load A Add B Store C	Load R_1, A Add R_3, R_1, B Store R_3, C	Load R_1, A Load R_2, B Add R_3, R_1, R_2 Store R_3, C

Note that the add instruction has implicit operands for stack and accumulator architectures explict operands for register architectures. It is assumed that A, B and C all being in memory and that the values of A and B can not be destroyed. The total code size is _____ (in bits).

Attempt | **Incorrect** **Your Ans.** | **136** | **Correct Ans.** | **940** | FAQ? | Have any doubt? | bookmark

Solution. 5

940

Stack	
Push (A)	8 + 64
Push (B)	8 + 64
Add	8
Pop (C)	8 + 64

= 224 bits

Accumulator	
Load A	8 + 64
Add B	8 + 64
Store C	8 + 64

= 216 bits

Register-Memory	
Load R_1, A	8 + 6 + 64
Add R_3, R_1, B	8 + 6 + 6 + 64
Store R_3, C	8 + 6 + 64

= 240 bits

Load-store	
Load R_1, A	8 + 6 + 64
Load R_2, B	8 + 6 + 64
Add R_3, R_1, R_2	8 + 6 + 6 + 6
Store R_3, C	8 + 6 + 64

= 260 bits

Total size = 224 + 216 + 240 + 260 = 940 bits

Q.6 **Assume that there are 251 different opcode and 32 registers in the machine. Every instruction has 3 register as input and 1 register as output [opcode R_1, R_2, R_3, R_4]. The number of bits to encode an instruction is _____.**

Attempt | **Correct** **Correct Ans.** | **28** | FAQ? | Have any doubt? | bookmark

Solution. 6

28

251 opcodes ⇒ 8 bits for each register

$\therefore$ | Opcode | R_1, R_2, R_3, R_4 |

8 bits + 5 × 4 bits = 8 + 20 = 28 bits

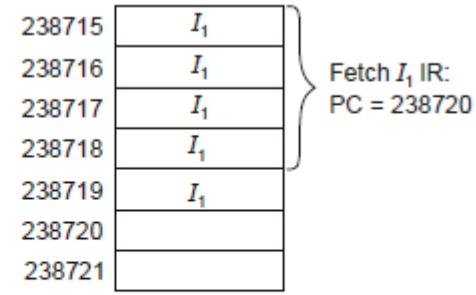
[$\because$ 4 for 4 registers i.e., R_1, R_2, R_3, R_4].

Q.7 **A PC relative mode branch instruction is 5 B long. The address of the instruction in decimal is 238715. The branch target address if the signed displacement is –32 is _____.**

Attempt | **Incorrect** **Your Ans.** | **238643** | **Correct Ans.** | **238688** | FAQ? | Have any doubt? | bookmark

Solution. 7

238688



Effective address = PC + Relative value

= 238720 + (–32)

= 238688

Q.8

Consider the following statements:

S1: Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a nonpipelined but identical CPU we can say that $T_1 \leq T_2$.

S_2: The performance of pipelined processor suffers if the pipeline stages have different delays.

Which of the following option is correct?

a. Both S_1 and S_2 are correct
b. only S_1 is correct
c. Only S_2 is correct
d. None of S_1 or S_2 is correct

Attempt | Correct **Correct Ans.** | c | FAQ? | Have any doubt? | bookmark

Solution. 8

(c)
• In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
• Structural dependencies cause hazards during pipelining.

Q.9

Consider an instruction of indirect addressing mode. What are the number of memory reference by theprocessor when instruction is a computation that requires a single operand and when it is a branch instruction respectively?

a. 3, 3
b. 2, 3
c. 3, 2
d. 2, 2

Attempt | Incorrect **Your Ans.** | b | **Correct Ans.** | c | FAQ? | Have any doubt? | bookmark

Solution. 9

(c)

When instruction is a computation:

Memory reference : Fetch instruction
Fetch reference of the operand
Fetch operand

Total 3 memory references.

When instruction is a branch:

Memory reference : Fetch instruction
Fetch operand reference and loading program counter

Total 2 memory references.

Q.10 **Consider a scenario where a non-pipelined processor has a clock rate of 5 GHz which has a average CPI of 5. An upgrade to the processor includes a 5-stage pipeline where the clock rate is 3 GHz. What is the speed-up achieved by using upgrated processor?**

a. 3.03
b. 4.02
c. 4.62
d. 2.34

Attempt | **Correct** **Correct Ans.** | **a** | FAQ? | Have any doubt? | bookmark

Solution. 10

(a)

For non-pipelined processor:

For p-instruction execution time = $\frac{(p \times 5)}{5} = p$ ns

Pipelined processor:

For p-instruction execution time = $\frac{p}{3} = 0.33p$ ns

Speed-up = $\frac{p}{0.33p} = 3.03$

Q.11

Consider the following program segment:

	Instruction	Meaning	Instruction size (in word)
I_1	Load r_0, 300	$r_0 \leftarrow$ [300]	2
I_2	MOV r_1, 5000	$r_1 \leftarrow$ Mem [5000]	2
I_3	MOV r_2, (r_1)	$r_2 \leftarrow$ Mem [r_1]	1
I_4	Add r_0, r_2	$r_0 \leftarrow r_0 + r_2$	1
I_5	MOV, 6000, r_0	Mem [6000] $\leftarrow r_0$	2
I_6	HALT	Machine Halts	1

Consider that the memory is byte addressable with size 16 bits, and the program has been loaded starting from memory location $(2000)_{10}$. What will be the return address saved in the stack, if an interrupt occurs while the CPU has been halted after executing the HALT instruction?

a. 2015
b. 2016
c. 2017
d. 2018

Attempt Correct **Correct Ans.** b FAQ? Have any doubt? bookmark

Solution. 11

(b)

	Instruction	Instruction size	Location
I_1	Load r_0, 300	2 word	2000-2003
I_2	MOV r_1, 5000	2 word	2004-2007
I_3	MOV r_2, (r_1)	1 word	2008-2009
I_4	Add r_0, r_2	1 word	2010-2011
I_5	MOV, 6000, r_0	2 word	2012-2015
I_6	HALT	1 word	2016-2017

∴ Since 1 word is of 2 bytes.
If an interrupt occurs, the CPU has been halted after executing the HALT instruction, the return add
2016 is saved in the stack.

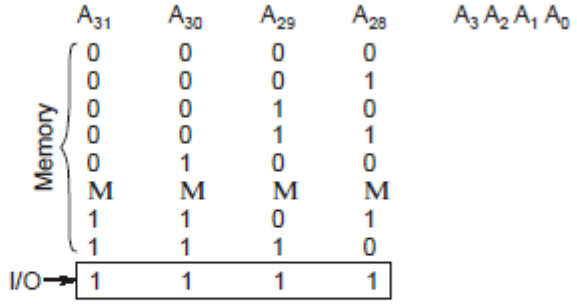
Q.12 **A computer system that uses memory mapped I/O configuration, has a 32 bit address space. Address with 1's in 4 MSB refers to devices. What is the maximum amount of memory and port addresses that can be referenced in such system respectively?**

a. 15×2^{25} and 1×2^{28}
b. 15×2^{32} and 1×2^{32}
c. 15×2^{28} and 1×2^{30}
d. $12 \times 2^{28}$and 1×2^{28}

Not Attempt | **Correct Ans.** | a | FAQ? | Have any doubt? | bookmark

Solution. 12

a



$\therefore$ Memory address space: 15×2^{28}

I/O address space = 1×2^{28}

Q.13 **A branch mark program is running on a 40 MHz processor. The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count.**

Instruction Type	Instruction Count	Cycles per Instruction
Integer arithmetic	45000	1
Data transfer	32000	2
Floating point	15000	2
Control transfer	8000	2

The execution time in msec is _____.

Attempt | **Correct** **Correct Ans.** | **3.87 (3.86-3.88)** | FAQ? | Have any doubt? | bookmark

Solution. 13

3.87 (3.86-3.88)

$$\text{CPI} = \frac{\sum(J_i \times CP_i)}{I_C} = \frac{[45000\times1+32000\times2+15000\times2+8000\times2]}{10^5}$$

$$= \frac{155000}{10^5} = \frac{155}{10^2} = 1.55$$

$$\text{Execution time} = \frac{I_C \times CPI}{f} = \frac{10^5 \times 1.55}{40\times10^6} = 3.87 \text{ msec.}$$

Q.14 **Consider a hypothetical control unit that supports 5 groups of mutually exclusive control signals. Also assume that group-1 and group-2 are using horizontal micro-programming whereas group-3, 4 and 5 are using vertical micro-programming. The total number of bits used for control words are _____.**

Groups	G_1	G_2	G_3	G_4	G_5
Control signals	3	9	6	13	10

Not Attempt | **Correct Ans.** 23 | FAQ? | Have any doubt? | bookmark

Solution. 14

23

Group-1 and 2 are using horizontal micro-programming,
Hence, total bits are:

$$3 + 9 = 12$$

Group-3, 4 and 5 are using vertical micro-programming,
Hence, total bits are:

$$\lceil \log_2 6 \rceil + \lceil \log_2 13 \rceil + \lceil \log_2 10 \rceil = 3 + 4 + 4 = 11$$

Total bits for control word = 12 + 11 = 23 bits

Q.15 **A computer has a cache, main memory and a hard disk used for virtual memory. If referenced word is in cache, 20 ns are required to access it. If it is in main memory but not in cache 60 ns are needed to load it into cache and then reference is started again. If word is not in main memory, 12 ms are required to fetch the word from disk followed by 60 ns to copy into cache, the reference is started again. The cache hit ratio is 0.9 and main memory hit ratio is 0.6. The average time in nano seconds required to access a referenced word on this system is _____.**

Attempt Incorrect **Your Ans.** 480007.8 **Correct Ans.** 480026

FAQ? Have any doubt? bookmark

Solution. 15

480026

There are 3 cases to consider

Location of referenced word	Probability	Total time for access in ns
In cache	0.9	20
In main memory but not in cache	(0.1)(0.6) = 0.06	60 + 20 = 82
Not in main memory	(0.1)(0.4) = 0.04	12ms + 60 + 20 = 12000080

So average access time should be

$$= 0.9(20) + (0.06)(80) + (0.04)(12000080)$$
$$= 480026 \text{ nsec}$$

Q.16 **Consider a non-pipeline processor has clock rate of 25 MHz and CPI of 6, another processor designed with same clock rate and 8 stage instruction pipeline. If program containing 500 instructions is executed on both processors, then the speedup factor is _____.**

Attempt Correct **Correct Ans.** 5.91 (5.90-5.92)

FAQ? Have any doubt? bookmark

Solution. 16

5.91 (5.90-5.92)

$$\text{Speed-up (S)} = \frac{\text{Non-pipe}}{\text{Pipeline}} = \frac{nt_n}{k+n-1}$$

$n = 500$

$t_n = 6$ (for non-pipeline)

$K = 8$ (for pipeline)

$$S = \frac{500 \times 6}{500+8-1} = \frac{3000}{507} = 5.91$$