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# Assignment no. 5

Roll no : 23152
Batch : G9

1. Write a note on difference between Timer 0, 1, 2 and 3
a) Timer control registers
b) Timer registers
c) Timer interrupt flag
d) Delay calculations

Ans.

A. Timer 0

① The Timer control registers
The TOCON is a ee readable & writeable register

| T0RUN | T08BIT | T0CS | T0SE | PSA | T0PS2 | T0PS2 | T0PS0 |
|---|---|---|---|---|---|---|---|

Bit-0-2 : Prescaler select bits

| | |
|---|---|
| 111 = 1:256 | 011 = 1:16 |
| 110 = 1:128 | 010 = 1:8 |
| 101 = 1:64 | 001 = 1:4 |
| 100 = 1:32 | 000 = 1:2 |

Bit 3 : Prescaler assignment bit
1 = Timer 0 Prescaler not assigned
0 = Prescaler assigned
Bit 4 : Source edge select bit
1 = Increment on high-to-low
0 = Increment on low-to-high
Bit 5 : Clock source select bit
1 = Transition on T0CLK pin
0 = Internal instruction cycle block

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Bit 6 : Timer 0-8 bit
1 = Timer 0 is configured as an 8 bit
0 = configured as 16-bit
Bit 7 : on/off control bit
1 = Enable
0 = Stop

② Timer registers

| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | value on POR, BOR | value on other Reset |
|---|---|---|---|---|---|---|---|---|---|---|
| TMR0L | Low byte Register | | | | | | | | xxxxxxxx | uuuuuuuu |
| TMR0H | High byte Register | | | | | | | | 00000000 | 00000000 |
| INTCON | GIE/ GIEH | PEIE/ GIEL | TMR0IE | INT0E | RBIE | TMR0IF | INT0IF | RBIF | 0000000x | 0000000u |
| T0CON | TMR0ON | T08bit | T0CS | T0SE | PSA | T0PS2 | T0PS1 | T0PS0 | 11111111 | 11111111 |
| TRISA | - | Port A Data direction register | | | | | | | -1111111 | -1111111 |

③ Delay calculation :
Reg Value = 256 - ((Delay * Fose) / (Prescaler * 4))

④ Timer interrupt flag
The TMR0 interappt is generated when the TMR0 register overflow from FFH to 00h in 8-bit mode or FFFFh to 0000h in 16-bit mode. This overflow sets TMR0IF bit in INTCON register.

B Timer 1

① Timer 1 control register

RD16 - TICKPS1 TICKPS0 TIOSCEN TMRICS TMRION
TISYNC

Bit 7 - RD16 Read / write mode enable
1 = Enables register in one 16-bit
0 = Enables in 2 8-bit register
Bit 6 - Unimplemented
Bit 5-4 - Input clock prescaler select bits
Bit 3 : Oscillator enable bit
1 = Timer 1 oscillator enabled
0 = shut off
Bit 2 : External clock input synchronization select bit
Bit 1 : Timer 1 clock source select bit
1 = External clock
0 = Internal clock
Bit 0 : On bit
1 = Enables
0 = Stops

② Delay :
Reg value = 65536 - ((Delay * Fosc)/(Prescaler * 4))

③ Timer interupt flag
The TMR1 register pair increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interupt if enabled is generated on overflow which is latched in interupt flag bit TMR1F.

④ Timer register

| Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Value on POR, BOR | Value on Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| INTCON | GIE/ GIEH | PEIE/ GIEL | TMR0IE | INT0IE | RBIE | TMR0IF | INT0IF | RBIF | 000000x | 000000u |
| PIR1 | PSPIF | HDIF | AOIF | RCIF | TX1F | SSPIF | CCIF | TMRIF | 00000000 | 00000000 |
| PIE1 | PSPIE | ADIE | RCIE | TX1E | SSPIE | CCP1IE | TMR2IE | TMR1IE | 00000000 | 00000000 |
| IPR1 | PSPIP | ADIP | RCIP | TX1P | SSPIP | CCP1IP | TMR2IP | TMR1IP | 11111111 | 11111111 |
| TMR1L | least significant byte of 16 bit TMR1 | | | | | | | | xxxxxxxx | uuuuuuuu |
| TMR1H | Most significant byte of 16 bit TMR1 | | | | | | | | xxxxxx | uuuuuuu |
| T1CON | RD16 | - | T1CKPS1 | T1CKPS0 | T1OSCEN | T1SYNC | TMR1CS | TMR1ON | 0-00000 | u-uuuuu |

C. Timer 2

① Timer control register

- TOUTPS3 TOUTPS2 TOUTPS1 TOUTPS0 TMR2ON T2CKPS1 T2CKPS

bit 7: Unimplemented
bit 6-3: Timer 2 output Postscale select bits
TMR2ON: Timer 2 on bit
1 = on
0 = off

Bit 1-0 : Prescale Select bits
00 = Prescaler 1
01 = Prescaler 4
1x = Prescaler 16

② Timer 2 registers

| Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | Value on POR, BOR | Value on Resets |
|---|---|---|---|---|---|---|---|---|---|---|
| IntCON | GIE/ GIEH | PEIE/ GIEL | TMR0 IE | RBIT 0IE | RBIE | TMR0IF | INT 0IF | RBIF | 000000x | 000000u |
| PIR1 | PSPIF | ADIF | RCIF | TX1F | SSPIF | CCP1IF | TMR2IF | TMR1IF | 000000 | 000000 |
| PIE1 | PSPIE | ADIE | RCIE | TX1E | SSPIE | CCP1IE | TMR2IE | TMR1IE | 000000 | 00000000 |
| IPR1 | PSPIP | ADIP | RCIP | TX1P | SSPIP | CCP1IP | TMR2IP | TMR1IP | 11111111 | 11111111 |
| TMR2 | Timer 2 module register | | | | | | | TMR1IP | 0000000 | 000000 |
| T2CON | - | TOUTP S3 | TOUT PS2 | TOUT PS1 | TOUT PS0 | TMR2 ON | T2CKP S1 | T2CKP S0 | -000000 | -0000000 |
| PR2 | Timer 2 period register | | | | | | | | 11111111 | 11111111 |

③ Delay calculation :
Reg value = 256 - ((Delay * Fosc) / (Prescaler * 4))

④ Interrupt
It has an 8 bit period register, PR2. Timer 2 increment from 00h until it matches PR2 and then resets to 00h.

D. Timer 3

① Timer control register

RD16 R3ECCP1 T3CKPS1 r3CKPS0 r3CCP1 r3SYNC TMR3CS TMR3ON

bit 7: 16 bit read/write mode enable
1 = Enables one 16-bit operations
0 = Enables in two 8-bit operations
bit 6-3: Timer 3 and Timer 1 to CCP/ECCP1
1x = Timer 3 is clock source for compare/capture CCP1/ECCP1 Enable
01 = Timer 3 clock source for ECCP1, Timer1 is the clock source for ccp1
00 = Timer 1 clock source for CCP1 and ECCP1
Bit 2: External clock input synchronization control bit
When TMR3CS = 1
1 = does not synchronize external clock input
when TMR3CS = 0
Bit is ignored
When TMR3CS = 0, internal clock is used
Bit 1: Timer 3 clock source select bit
1 = External clock input from Timer 1 oscillator
0 = Internal clock (fosc/4)
Bit 0: on bit
1 = Enable
0 = Stops

② Timer register
a) TMR3 : TMR3L and TMR3H
b) TMR3ON
c) TMR3IF
d) T1OSO
e) T1OSI
f) TMR3CS
g) T1OSCEN

③ Interrupt
The TMR3 increments from 0000h to FFFFh and rolls over. The TMR3 interupt, it enables is generated on overflow which is latched in interupt flag bit TMR3IF.

④ Delay calculation
Input freq = $\frac{fosc}{4}$ TickCounter freq = $\frac{Prescaler}{Fosc/4}$

Delay required = Timer Count * TickCounter freq

Reg value = TimerMaxValue (65525) - Timer count + 1