PICT, PUNE

23272

Assignment - 2

Q.1]. Write a short note on Working Register (WREG) of PIC18.

→. 1]. The Working Register or WREG is a temporary storage for information at the CPU.

2. It has a size of 8 bits.

3. It is also called as "Program Memory Space".

4. It can be used for arithmetic and logical instructions like Move or Add.

Eg. MOVLW N

means, move literal value N in the WREG.

Eg. A program to add two numbers in WREG

```
MOVLW 11H
ADDLW 22H
```

33H is stored in the WREG.

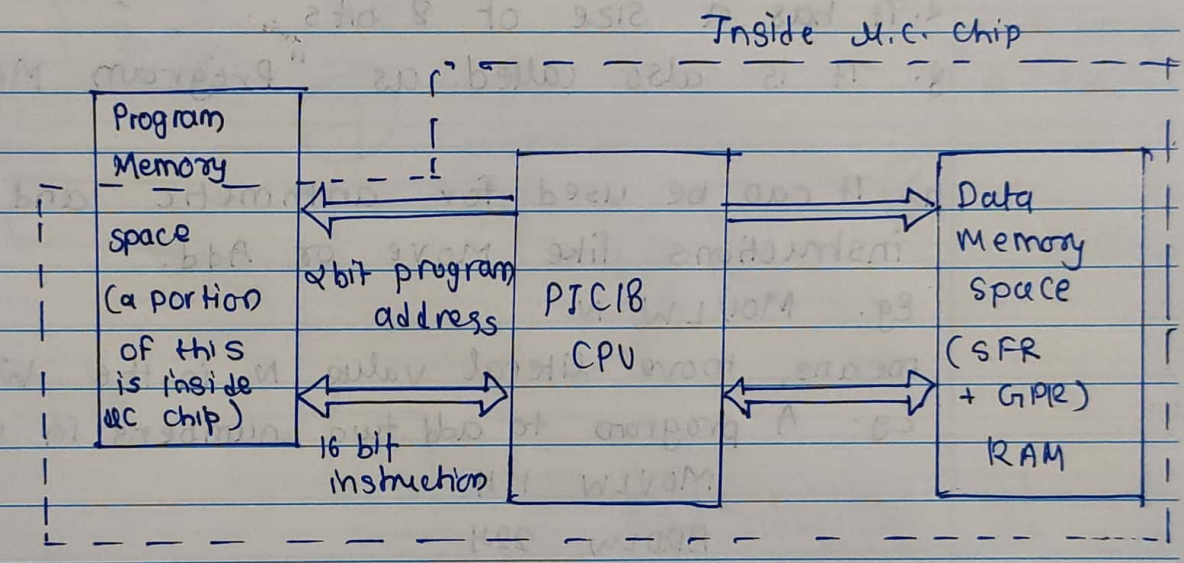
5. It is the same as an accumulators in other microprocessors.

2]. Memory of PIC18F458 (all types) and memory banking.

→. Memory consists of a sequence of directly addressable locations. A location is reffered to as an information unit. A memory location can be used to store data, instruction and

status of peripheral devices. A memory location has two components : an address and its contents.

2. Data memory and Program memory are separated. This means it possible to simultaneously access data and instruction.



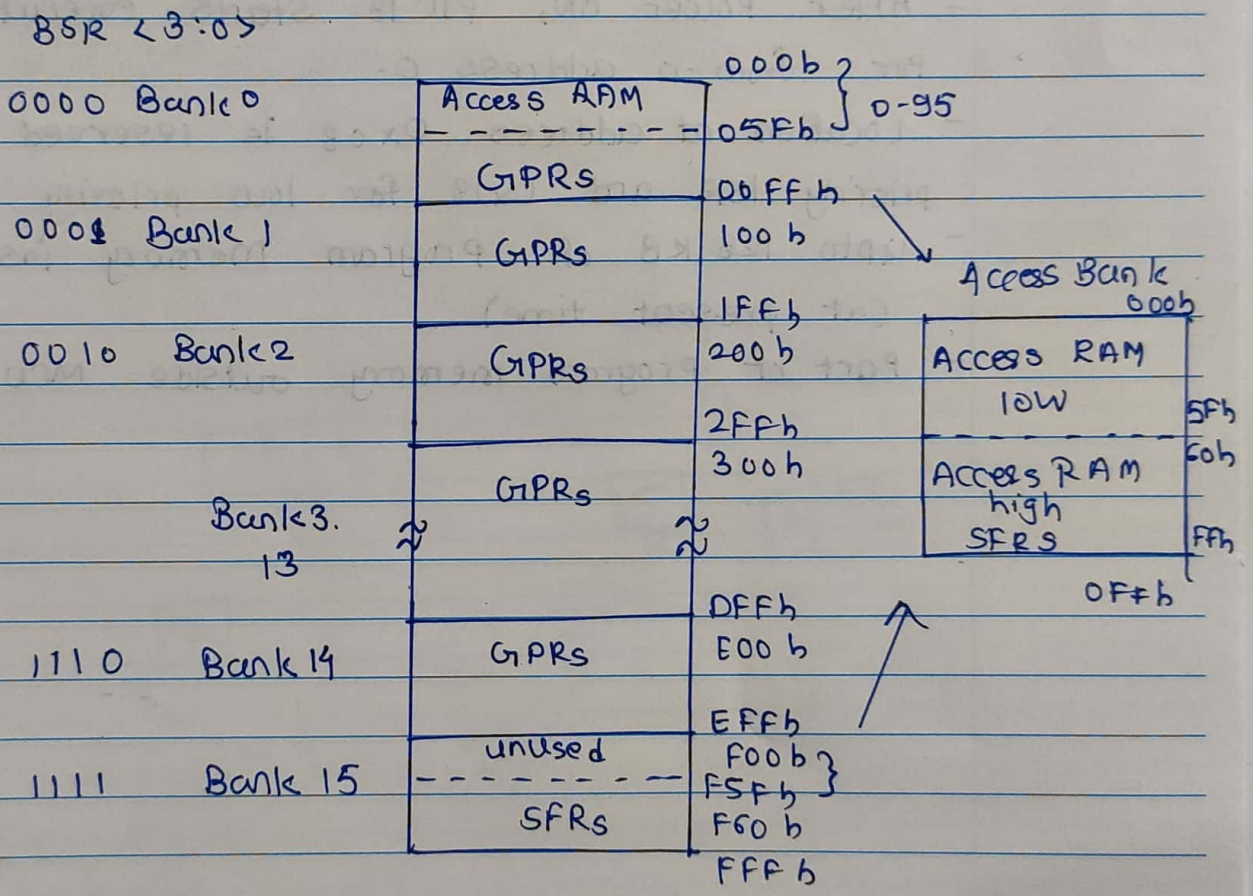
3. Memory features

- 4096 bytes of data memory.
- General purpose registers are used to hold dynamic data.
- Special function registers are used to control operation of peripheral function.

} data registers.

- only one bank is active at a time and is specified by the BSR registers.

- Bank switching is overhead and can be error prone.
- PIC18 implements access bank to reduce problems caused by bank switching.
- Access bank consists of lowest 96 bytes and highest 160 bytes of data memory Space.



- Every Bank is 256 bytes.
- PIC 18 has 2MB Program space.
  1MB ≡ 16 banks.
  Hence, PIC18 has 16 banks.
- 0-56 of first bank : Access RAM (low)
  higher 196 of last bank : Access RAM (high)

- Unused space is for some SFRs that can be added in later versions.
- PC is 21 bit long which enables user program to access upto 2MB of program memory.
- PIC 18 has 31 entry return address stack to return address for subroutine call.
- After Power ON, PIC 18 starts executing instruction for from-0 address 0.
- Location at address 0x08 is reserved for high priority ISR and 0x18 for low priority ISR.
- upto 128 KB of program memory inside MCU chip (at present time).
- Part of program memory outside MCU chip.

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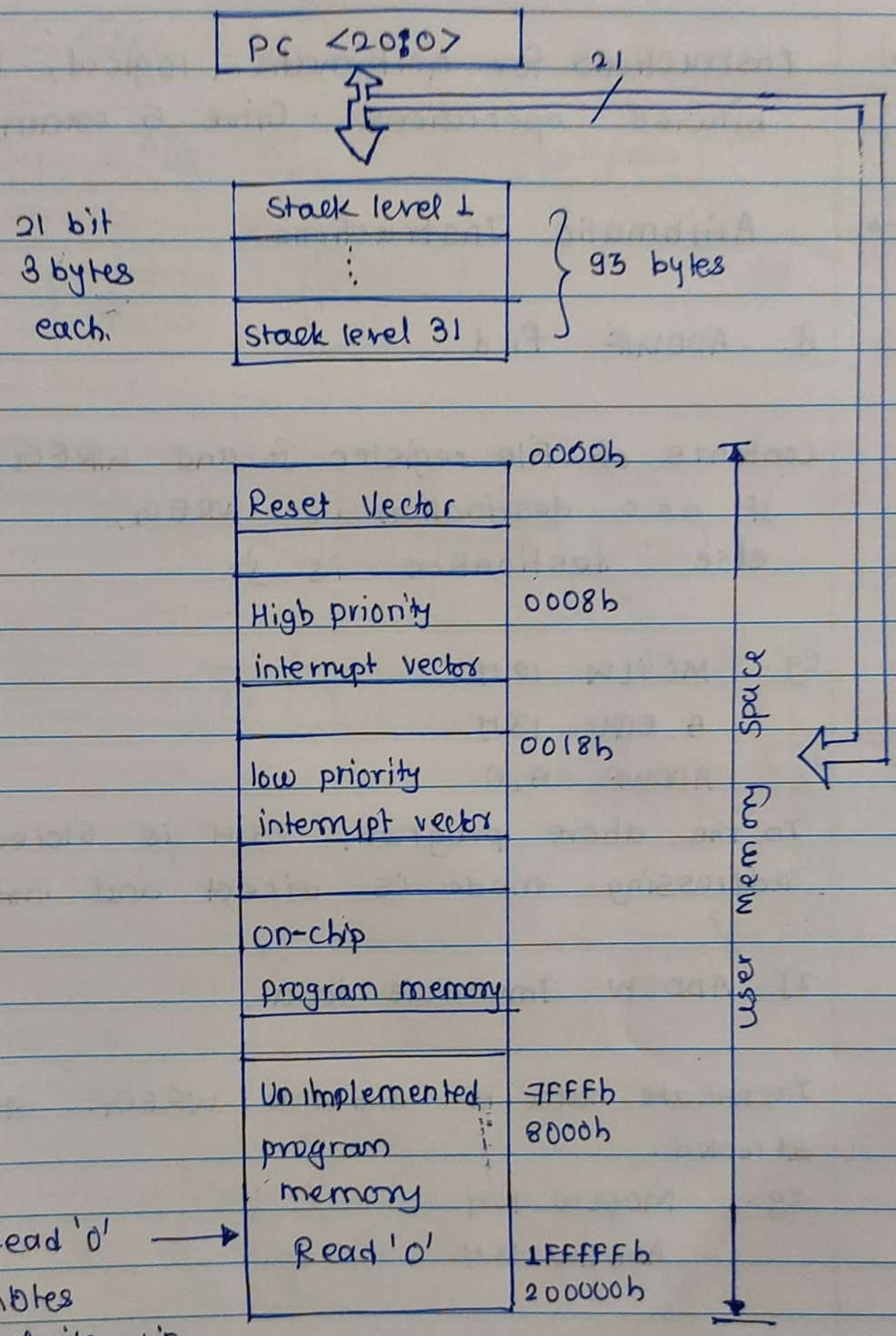

Program Memory Orientation.

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3) Instructions for arithmatic, logical, branch and bitwise operations. Give 5 examples of each type.

→. Arithmatic Instructions

1]. ADDWF f, d

Contents of file register f and WREG are added.
IF d = 0 destination is WREG,
else destination is f.

eg. MOVLW 12H
A EQU 13H
ADDWF A, 0

In the above program, 25H is stored in WREG. The addressing mode is direct and inherent.

2]. ADDLW Immediate data.

Immediate data is added to WREG. status register is affected.

eg. MOVLW 12H
ADDLW 13H

In this program, 25H is stored in WREG.

Addressing mode is inherent and immediate.

3. SUBFW f,d

Contents of WREG are subtracted from the file register f (f - WREG).

if d=0, destination is WREG.

else it is f.

Eg.

```
MOVLW 01H
A EQU 03H
SUBFW A,0
```

In the above program, 02H is stored in WREG. Addressing mode is register and inherent.

4. INC f,d : Increment file register f

eg:
```
A EQU 8H
INC A.
```

9H is stored in A.

Addressing mode is register.

5. DECF f,d ; Decrement file register f

eg:
```
A EQU 8H
DECF A
```

7H is stored in A.

Addressing mode is register.

* Logical Instructions

1. ANDLW Immediate data.

Immediate data and data inside the WREG are 'Anded'.

Eg: MOVLW B' 10001000'.
ANDLW B' 01011000'.

$(0000\ 1000)_2$ is stored in the WREG.
Addressing Mode is immediate and inherent.

2. ANDWF f,d.

The data in file register f is 'anded' with data in the WREG.

Eg:

A EQU B' 00100101'.
MOVLW B' 00000011'.
ANDWF A,0.

$(0000\ 0001)_2$ is stored in WREG.
Addressing mode is register and inherent.

3. ~~IORLW instructions~~

~~Imm~~

3. IORLW Immediate data.

Immediate data and data inside the WREG is 'OR. ed'.
Addressing mode is immediate and inherent.

eg. MOVLW B' 00100101'
IORLW B' 11010001'

$(1111\ 0101)_2$ is stored in the WREG A.

4. IORWF f, ϕ.

Data in File register f is 'OR-ed' with data in WREG.

Eg: A EQU B' 00000001'
MOVLW B' 10000000'
IORWF A,0

$(1000\ 0001)_2$ is stored in the WREG. Addressing mode is inherent and register.

5. XORLW immediate data

Immediate data is 'exclusively OR-ed' with data in the WREG.

eg: MOVLW B' 1111 1111'
XORLW B' 1111 0000'

$(0000\ 1111)_2$ is stored in WREG.
Addressing mode is immediate and inherent.

Branch.

1. GOTO xyz

control goes to xyz

```
Eg:   c   EQU  5H
      loop MOVLW 00H
           ADDLW 06H
           DECFSZ c
           GOTO  loop
```

} Multiply 6 and 5 (Hexadecimal)

2. BNZ address
   Branch if not zero.

3. BZ address.
   Branch if zero.

4. BNC address
   Branch if not carry.

5. BC address
   Branch if carry

. Bitwise

1. BCF f, b

clear bit 'b'.

Eg. A EQU B' 0001 1111'.
BCF A, 4
value in A becomes $(0001\ 0111)_2$

2. BSF f,b : set bit 'b'

eg. A EQU B' 00000000'
BSF A,3
value in A becomes $(0000\ 0100)_2$

3. BTG f,b ; Toggle bit 'b'.

Eg. A EQU B' 0010 0010'
BTG A,2
BTG A,1
value in A becomes $(0010\ 0001)_2$

4. RLCF fid : Rotate left file register through CY.

MSB → CY	00001100	1
CY → LSB	00011001	0

5. RRCF fid : Rotate right file register through CY.

LSB → CY	0000	1100	1
CY → MSB	1000	0110	0