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**#207, Kambipura, Mysore road, Banglore-74**

**Department of Computer Science and Engineering**

**CO QUESTION BANK**

**Module 1**

1. With a neat diagram explain the different processor registers.
2. What are the factors that affect the performance? Explain any 4.
3. What is performance measurement? Explain the overall SPEC rating for a computer in a program suite.
4. Write the difference b/w RISC and CISC processors.
5. Write a note on byte addressability, big-endian and little-endian assignment.
6. Explain the basic operational concepts b/w the processor and the memory.
7. Derive the basic performance equation? Discuss the measures to improve the performance.
8. Explain processor clock and clock rate.
9. What is an addressing mode? Explain any four addressing modes.
10. Explain shift and rotate with examples.
11. Explain subroutine stack frame with example.
12. With a neat block diagram, describe the I/O operation.
13. Write a short notes on Assembly Directives.
14. What is a stack frame? Explain a commonly used layout for information in a subroutine stack frame.
15. Define subroutine. Explain subroutine linkage, using a link register.
16. Write the routine for SAFE PUSH and SAFE POP.
17. What is stack? Explain its role in subroutine nesting.
18. Mention four types of operations to be performed by instructions in a computer. Explain with basic types of instructions formats to carry out C<- [A] +[B].

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# Module 2

1. Define exceptions. Explain two kinds of exceptions.
2. Define bus arbitration. Explain in detail both approach of bus arbitration.
3. What is an interrupt; with example illustrate the concept of interrupts
4. Explain in detail the situation where a number of devices capable of initiating interrupts are connected to the processor? How to resolve the problems?
5. Explain the following terms a) interrupt service routine b) interrupt latency c) interrupt disabling.
6. With a diagram explain daisy chaining technique.
7. Draw the arrangement of a single bus structure and brief about memory mappedI/O.
8. Explain interrupt enabling, interrupt disabling, edge triggering with respect tointerrupts
9. Draw the arrangement for bus arbitrations using a daisy chain and explain inbrief.
10. With neat sketches explain various methods for handling multiple interruptrequests.
11. Define memory mapped I/0 and I/0 mapped I/0 with examples
12. Explain how interrupt request from several I/0 devices can be communicated to a processor through a single INTR line.
13. What are the different methods of DMA. Explain in brief.
14. Explain the important functions of a I/0 interface with a neat blockdiagram
15. What is DMA? Explain the hardware registers that are required in a DMA controller chip. Explain the use of DMA controller in a computer system with a neatdiagram
16. Explain with a block diagram a general 8 bit parallel interface.
17. With the help of a data transfer signals explain how a read operation is performed using PCI bus.
18. Explain briefly bus arbitration phase in SCSI bus.
19. In a computer system why a PCI bus is used? With a neat sketch, explain how the read operation is performed along with the role of IRDY/TRDY on the PCIbus
20. Draw the block diagram of universal bus(USB)structure connected to the hostcomputer
21. Briefly explain all fields of packets that are used for communication between a host and a device connected to an USB port.
22. Draw the hardware components needed for connecting a keyboard to a processor and explain in brief.
23. List the SCSI bus signals with their functionalities.

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# Module 3

* 1. With the block diagram explain the operation of a 16-megabit DRAM chip configured as 2M\*8.
  2. Mention any two differences b/w static and dynamic RAM. Explain the internal organization of a memory chip consisting of 16 words of 8 biteach.
  3. Which are the various factors to be considered in the choice of a memory chip.Explain
  4. Give the organization of a 2M\*32 memory module using 512k\*8 static memorychips
  5. Discuss ,the different types of RAM’s bring out their salient features
  6. Define memory latency and bandwidth of synchronous DRAM memoryunit.
  7. What is virtual memory? Explain how virtual address is translated to physicaladdress.
  8. Explain direct memory mapping technique
  9. Show with diagram the memory hierarchy with respect to speed ,size andcost
  10. Explain different mapping functions used in cache memory.
  11. Define memory latency, memory bandwidth, hit rate and miss penalty.

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# Module 4

* + 1. With neat diagram, explain the virtual memory organization
    2. Design a logic circuit to perform addition or subtraction of two n –bit numbersX&Y
    3. Explain booth algorithm. Apply booth algorithm to multiply the sign numbers+13&-6
    4. Write the logic diagram of 4-bit carry look ahead adder; explain the operation and how it is faster than four bit ripple adder
    5. Perform multiplication for -13&+9 using booth’s algorithm
    6. Write the circuit arrangement for binary division. Perform the restoring division for the given binary number 1000/11, show all cycles
    7. Explain normalization, excess-exponent and special values with respect to IEEE floating point representation
    8. Given A=10101 &B=00100 perform a/b using restoring division algorithm
    9. Explain with figure the design and working of 16 bit carry look ahead adder built from 4 bit adders.
    10. Differentiate between restoring and non restoring division
    11. In a carry look ahead addition, explain the generate Gi and propagate Pi functions for stage i .Using this design 4 bit carry look ahead adder
    12. How do you design FAST ADDERS? Explain a 4 bit carry look aheadadder

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# Module 5

* + - 1. Explain with neat diagram, the basic organization of a micro programmed control,
      2. Describe the three bus organization of the data path and describe indetail.
      3. Write control sequence for the instruction Add R1,R2,R3.
      4. Explain a complete processor with a neat diagram
      5. Write and explain the control sequences for the execution of the following instruction: Add (R3), R1.
      6. Bring out the differences between micro programmed control and hard wired control.
      7. Explain Field coded micro instructions with a neat diagram.
      8. Explain multiple bus organization and its advantages.
      9. Explain the role of cache memory in pipelining.
      10. Explain pipelining performance.