Aditya Wagh

Curriculum Vitae

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Education

2015 - 2019 **B.E. (Hons.) in Electronics and Instrumentation Engineering**.
Birla Institute of Technology and Sciences (BITS), Pilani

2003 - 2015 **Higher Secondary Certificate**.
LVH Arts, Science & Commerce College, Marks: 85.69%

2009 - 2013 **All India Secondary School Examination**.
Symbiosis School, CBSE, GPA: 10/10

Work Experience

Professional

May '17 - Jul '17 **The Ramco Cements Ltd**, *Jaggayapeta, India*.
Software Engineering Intern
Mentor: Mr. Chengal Rao
Focus: Full-stack design of an inventory management web-application

May '18 – Jul '18 **Apras Polymers & Engineering Co.Pvt. Ltd**, *Nashik, India*.
Software Engineering Intern
Supervisor: Mr. Prakash Dhanokar
Focus: Modern and responsive business website design

Academic

Dec '18 - May '19 **CSIR-Central Electronics Engineering Research Institute, Pilani**, *Pilani, India*.
Undergraduate Research Assistant
Mentor: Dr. Sumeet Saurav
Focus: ConvNet models for orientation-aware object detection on aerial images.

Jul '18 - Dec '18 **CSIR-Central Electronics Engineering Research Institute, Pilani**, *Pilani, India*.
Undergraduate Research Intern
Mentor: Dr. Sumeet Saurav
Focus: Instance segmentation models for real-time power-cable fault detection using autonomous drones

Aug '17 - Dec '17 **BITS Pilani**, *Pilani, India*.
Undergraduate Research Assistant
Mentor: Prof. Anu Gupta
Focus: Fault tolerant Static RAM cell design

Projects

2017 **Variable Computation in Recurrent Neural Networks:**

- Modified a RNN model to reduce the amount of required computation by ignoring redundant sequences.
- Implemented a scheduler for the RNN unit which decides the computation required at the current time-step.
- Reduced the number of operations for bit-level language modelling by 50%.

2019 **RISC Processor Design using HDL**

- Designed, programmed and tested 16-bit multi-cycle processor for a given set of instructions and constraints.
- Followed modular approach for programming the processor and its test bench, by dividing it into sub-modules such as memory, register file, ALU and control unit.

2018 **FIR flter design using an adjustable window function.**

- Implemented an adjustable window function based on the combination of Blackman and Lanczos window.
- Achieved a 75% better side-lobe roll off ratio than Lanczos window.

Technical Skills

Languages Python, C/C++, MATLAB, Shell, LaTeX, HTML, CSS, JavaScript

Frameworks Keras, TensorFlow, PyTorch, OpenCV, Bootstrap, Git

Softwares Simulink, LTspice, LabVIEW, EagleCAD, Proteus

Achievements

2015 Amongst the top 1.5% students in the India in Joint Entrance Examination - Mains

2015 Amongst the top 5% students in the India in Joint Entrance Examination - Advanced

2014 Amongst the top 300 students selected for INPhO (Indian National Physics Olympiad)

2019 Elected as the Student Mess Representative for two senior hostels at BITS Pilani.

2017 Elected as the Vice-Chair Person of the IEEE Student Branch at BITS Pilani.

Extracurriculars

Jul '17 - May '18 **Vice-Chairperson**, *IEEE Student Branch, BITS Pilani*, Pilani, India.

- Promoted IEEE Student memberships by 30% in the campus by organising membership drives, workshops and technical events
- Responsible for setting up the IEEE hosted website for the chapter and IEEE Insight, the monthly newsletter of the chapter.
- Revamped the organisational hierarchy of the chapter, introducing various managerial and technical posts.

Aug '18 - July '19 **Governing Council Member**, *Society for Students Mess Services (SSMS), BITS Pilani*, Pilani, India.

- **Mess Representative:** Responsible for sanctioning leaves of the workers, collecting feedback and taking necessary actions.
- **Quality, Health and Safety:** Drafted a QHSE framework for SSMS activities and conducted regular audits every semester.
- **HR:** Responsible for performance appraisals, providing education/medical loans and managing internal worker conflicts.

References

Dr. Syed Zafaruddin, Assistant Professor, BITS Pilani

Dr. Sumeet Saurav, Scientist, Intelligent Systems Group, CEERI Pilani