Aditya Wagh | Curriculum Vitae

+91 74477 93555 • aditya@adityawagh.ml • https://adityawagh.ml

Education

- **Birla Institute of Technology and Sciences (BITS), Pilani** — **Pilani, India**
  Bachelor of Engineering (Hons) in Electronics and Instrumentation Engineering — *2015–2019*
- **LVH Arts, Science & Commerce College** — **Nashik, India**
  Higher Secondary Certificate, MSBSHSE, Marks: 85.69% — *2003–2015*
- **Symbiosis School** — **Nashik, India**
  All India Secondary School Examination, CBSE, GPA: 10/10 — *2009–2013*

Work Experience

Professional

- **The Ramco Cements Ltd** — **Jaggayapeta, India**
  Software Engineering Intern — *May 2017–Jul 2017*

  Designed a petrol bunk inventory management system using Angular.js. Implemented a relational database model for the same using SQLite. The back-end infrastructure was written in Python using Flask.
- **Apras Polymers & Engineering Co.Pvt. Ltd** — **Nashik, India**
  Software Engineering Intern — *May 2018 – Jul 2018*

  Designed a responsive website for the company using Figma. Implemented the front end using React.js, Jekyll and Bootstrap.

Academic

- **CSIR-Central Electronics Engineering Research Institute, Pilani** — **Pilani, India**
  Undergraduate Research Assistant — *Dec 2018 - May 2019*

  Researched convolutional neural network models for orientation-aware object detection on aerial images. Achieved approximately 65 mAP on the DOTA dataset.
- **CSIR-Central Electronics Engineering Research Institute, Pilani** — **Pilani, India**
  Undergraduate Research Intern — *Jul 2018 - Dec 2018*

  Worked on designing instance segmentation models for real-time power-cable fault detection using autonomous drones under Dr. Sumeet Saurav
- **BITS Pilani** — **Pilani, India**
  Undergraduate Research Assistant — *Aug 2017- Dec 2017*

  Worked on fault tolerant Static RAM cell design under Prof. Anu Gupta

Projects

- **Variable Computation in Recurrent Neural Networks:**
  - Modified a RNN model to make it learn to vary the amount of computation according to the sequence that they process.
  - Implemented a scheduler for the RNN unit which decides the computation required at the current time-step.
  - Reduced the number of operations for bit-level language modelling to around 50% compared to normal RNN unit.
- **RISC Processor Design using HDL**
  - Designed, programmed and tested 16-bit multi-cycle processor for a given set of instructions and

constraints.
- Followed modular approach for programming the processor and its test bench, by dividing it into sub-modules such as memory, register file, ALU and control unit.

Technical skills

- **Programming Languages:** Python, C, C++, MATLAB, Shell, LaTeX, HTML, CSS, JavaScript
- **Software Tools, Frameworks & Libraries:** Keras, Tensorflow, PyTorch, OpenCV, Simulink, LTspice, Bootstrap, LabVIEW, Git

Achievements

- Amongst the top 1.5% students in the India in Joint Entrance Examination - Mains, 2015.
- Amongst the top 5% students in the India in Joint Entrance Examination - Advanced, 2015.
- Amongst the top 300 students selected for INPhO (Indian National Physics Olympiad)
- Elected as the Student Mess Representative for two senior hostels at BITS Pilani.
- Elected as the Vice-Chair Person of the IEEE Student Branch at BITS Pilani.

Volunteer Experience

- **IEEE Student Branch, BITS Pilani** **Pilani, India**
  Vice-Chairperson *Jul 2017 - May 2018*
  - Promoted IEEE Student memberships by 30% in the campus by organising membership drives, workshops and technical events
  - Responsible for setting up the IEEE hosted website for the chapter and IEEE Insight, the monthly newsletter of the chapter.
  - Revamped the organisational hierarchy of the chapter, introducing various managerial and technical posts.

- **Society for Students Mess Services (SSMS), BITS Pilani** **Pilani, India**
  Governing Council Member *Aug 2018 - July 2019*
  - **Mess Representative:** Responsible for sanctioning leaves of the workers, collecting feedback and taking necessary actions.
  - **Quality, Health and Safety:** Drafted a QHSE framework for SSMS activities and conducted regular audits every semester.
  - **HR:** Responsible for performance appraisals, providing education/medical loans and managing internal worker conflicts.

References

- Dr. Syed Zafaruddin, Assistant Professor, BITS Pilani
- Dr. Sumeet Saurav, Scientist, Intelligent Systems Group, CEERI Pilani