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School : National Public School, Rajajinagar, Bangalore

***All pictures in the below document are taken from the digital chip design course**

Level 3 :-

Arduino Board – Made up of many components.

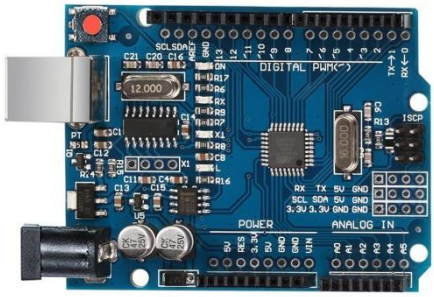
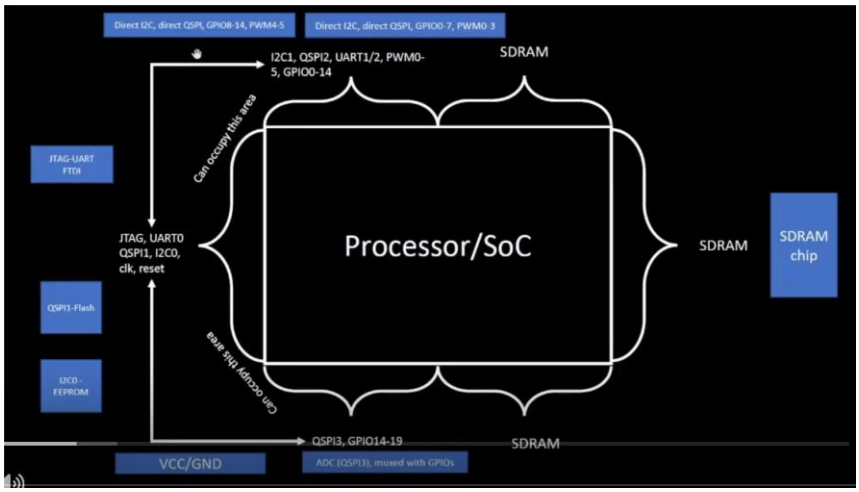


Photo Credit - https://www.ubuy.co.in/product/3V6KZCHAG-arduino-uno-r3-compatible-atmega328p-ch340-usb-microcontroller-board

Below diagram of processor –



Typical requirements for making Arduino board are above.

Zoom in to the main Integrated Circuit –

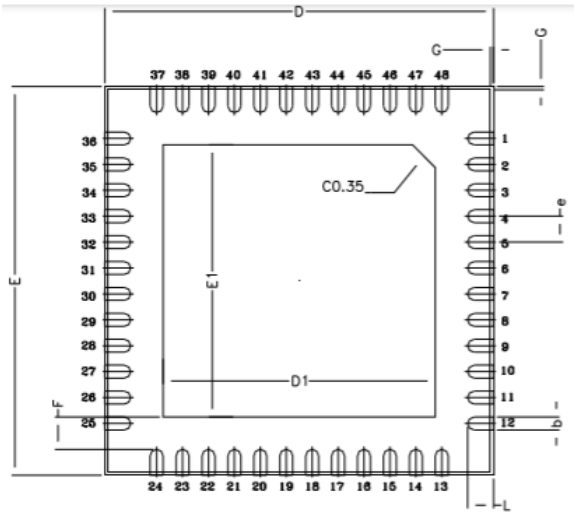
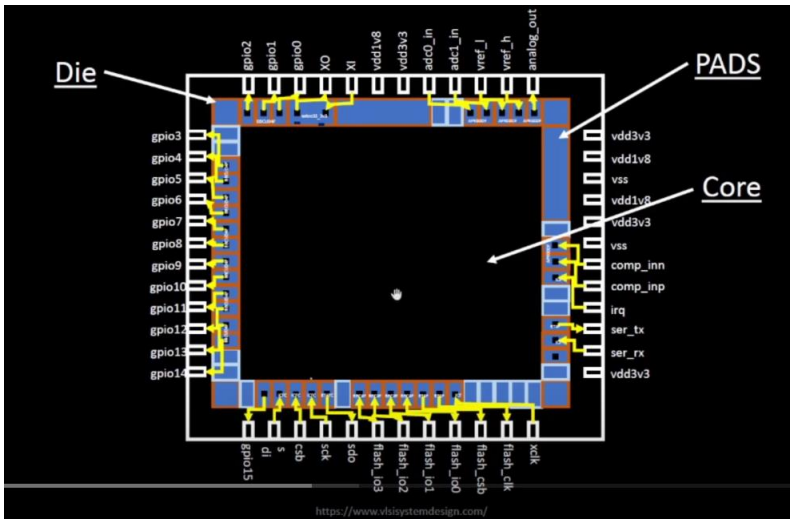


Photo Credits - https://electronics.stackexchange.com/questions/394554/soldering-0-4mm-pitch-qfn-48-chip

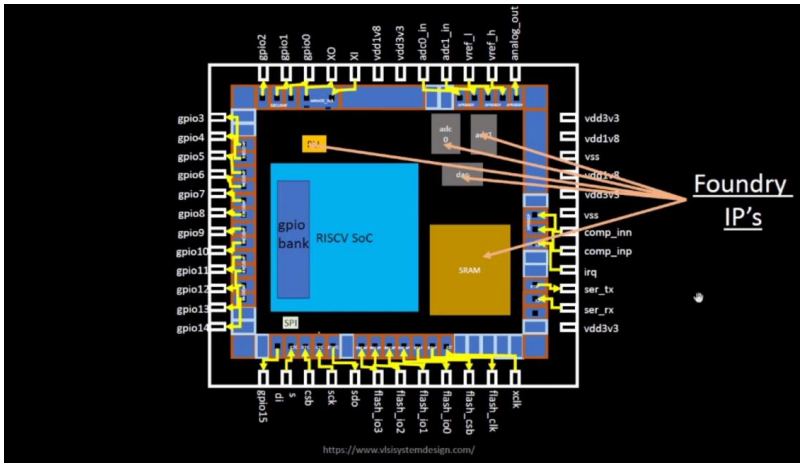
The chip sits at the centre of the package (In the middle of the QFN-48 package)

Wire bonds connected to the chip are able to transfer all the signal coming from the outside world to the integers of the chip.



Many parts in a chip –

1. Pads – Through pads you can send the signal inside the chip and vice versa
2. Core – The core is where all the digital logic sits. The AND Gate, OR Gate etc are found in the core
3. Die – Size of the entire chip



Foundry – A factory where chips get manufactured.

IP – Intellectual Property.

Reason why the Foundry IPs are called like that as they need intelligence to be made.

The RISCV SOC and the SPI are macros.

They are called macros as they are put digital logic.

To manufacture chips, there needs to be communication with Foundry.

RISC-V Architecture

If you have a C Program and you need it to run on a computer, then you need to pass it through hardware to make it binary to get the required output.

Another interface is required to be present between the flow and the RISC-V architecture that is the hardware description language.

You need to implement this RISC – V specifications using some RTL Ex : Picorv32 cpu core

This rtl implements these specifications of the architecture to make the layout.

Software applications to Hardware.

The application software first enters into the system software which then converts the application into a binary language.

The majors system softwares are the OS, Compiler and the Assembler.

OS – Handles IO Operations, Allocates memory and does the low level system functions. The other function is to make sure that it turns into a binary language.

Compiler – Converts the program code into a set of instructions

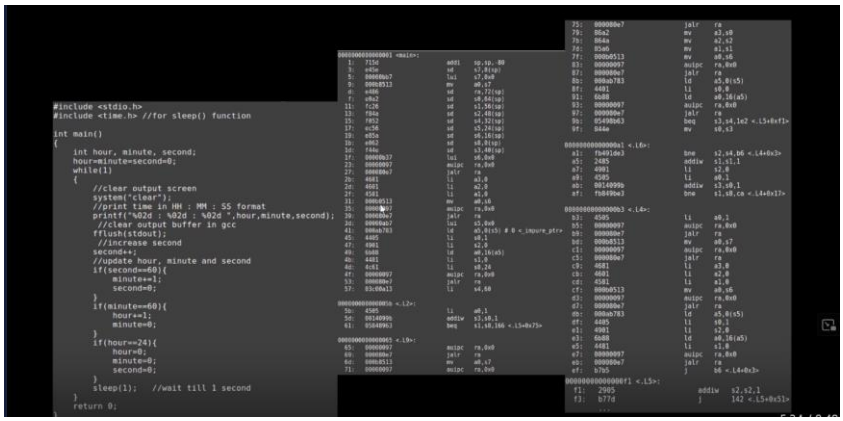
The compiler turns it into a set of instructions which is dependent on the hardware

Then the job of the assembler is to make the instructions into a binary language.

Then the hardware receives the code and does the function specified.

Ex : Stopwatch –

The functions, which is written in a specific language, is put into a compiler, and if the hardware is a RISCV, then the output of the compiler will be a set of RISCV instructions, which then enter the chip layout to perform the functions



Input and Output of Compiler

Instructions act as an abstract interface between the C and the Hardware.

The hardware only understands the HDL, so if you give it a set of 1s and 0s, it understands it needs to do something with that.

The instructions are put into the assembler which turn it into a binary language.

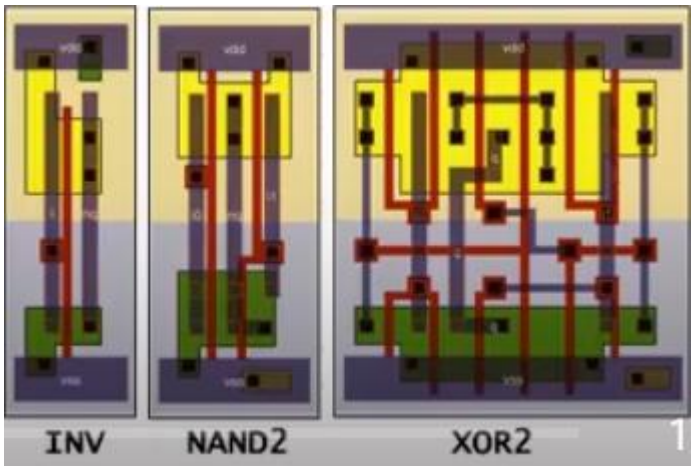
SoC design and OpenLANE –

RTL to GDSII Flow –

Synthesis, Clock Tree Synthesis, Floor/Power Planning, Routing, Placement, Sign Off.

Synthesis – Converts RTL to a circuit out of components from the standard cell library.

The standard cells have regular layouts.



Chip Floor Planning – Partition the chip die between system building blocks and then the I/O pads will be placed.

Macro Floor Planning – The macro dimensions are defined, The rows and routing tracks are defined

Power Planning – Has power pads, power straps and power rings.

Placement – We place the Gate-2 steopsLevel Netlist cells on the floorplan rows, aligned with the site.

2 steps – Global and Detailed

Global placement tries to find the optimal placement for all the cells. Such positions are not correct, so they may overlap

Detailed Placement are minimally altered to be legal

CTS – Clock distribution network.

To deliver the clock to all sequential elements.

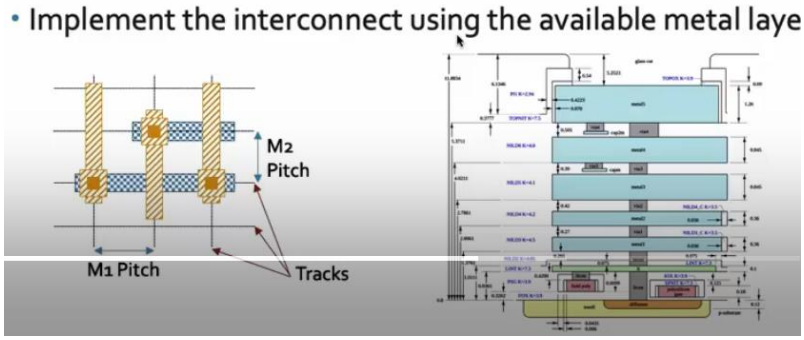
With minimum skew

Usually a tree.

Synthesized to level of clock.

Certain structures are used, such as H , X Tree etc

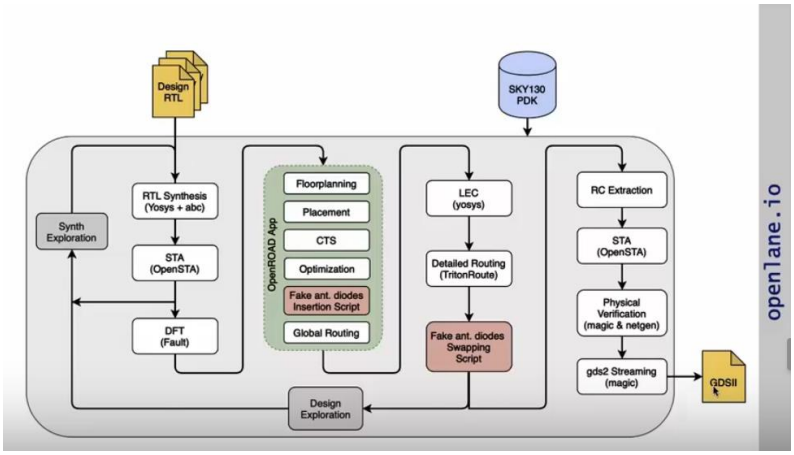
Route –



To implement the interconnect using available metal layers

The local layers are all aluminium.

OpenLANE ASIC Flow –



Starts with RTL Synthesis

Can be used to generate a report

Based on this we can make a best strategy to continue

OpenLANE has design exploration Uitility

Then the physical implementation

PnR (Place and Route) –

Floor and Power planning

End decoupling Capacitors and Tap cells insertion

Placement : Global and Deatailed

Next step in process in Yosys –

Verification must be performed.

Modification of netlist

Used to confirm that what we ended up with was not what we started with.

Fake ant. Diodes insertion script –

When a metal wire segment is made, it can act as antenna.

Preventive approach – Add fake antenna diode, run antenna checker and if the checker reports violation, replace it with a real one.

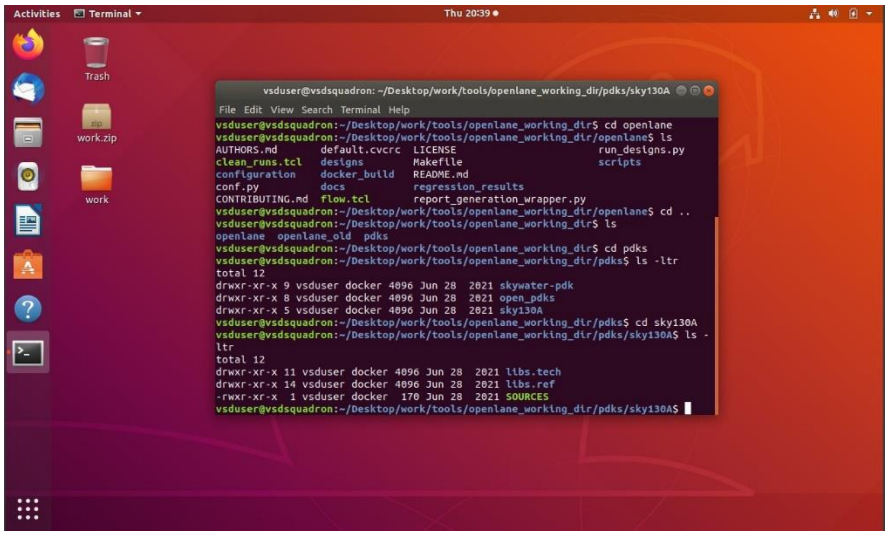
Static Timing Analysis – Involves RC Extraction from routed layout.

Then physical verification.

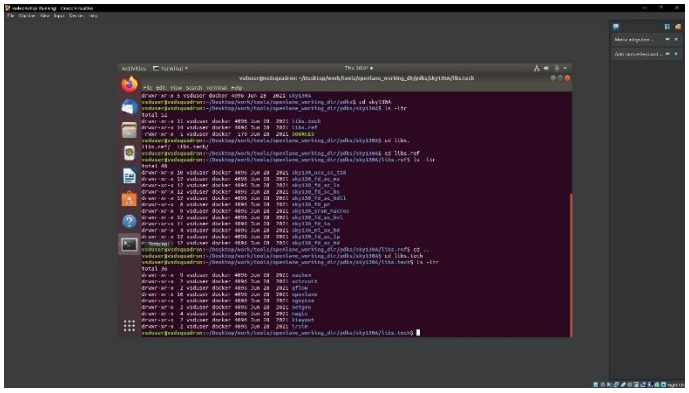
Open Source EDA Tools –

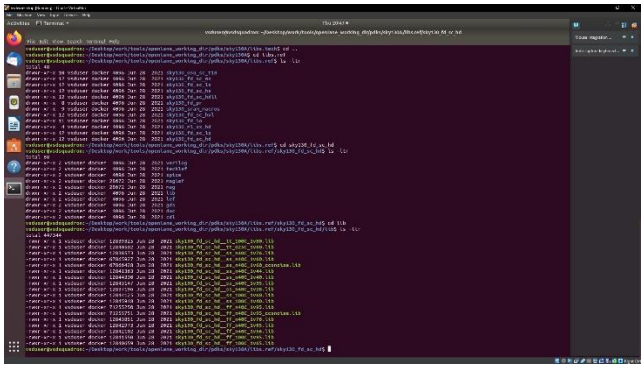
SKY130_D1_SK3 - Get familiar to open-source EDA tools

Screenshot of the virtual Ubuntu box running the open source EDA tools

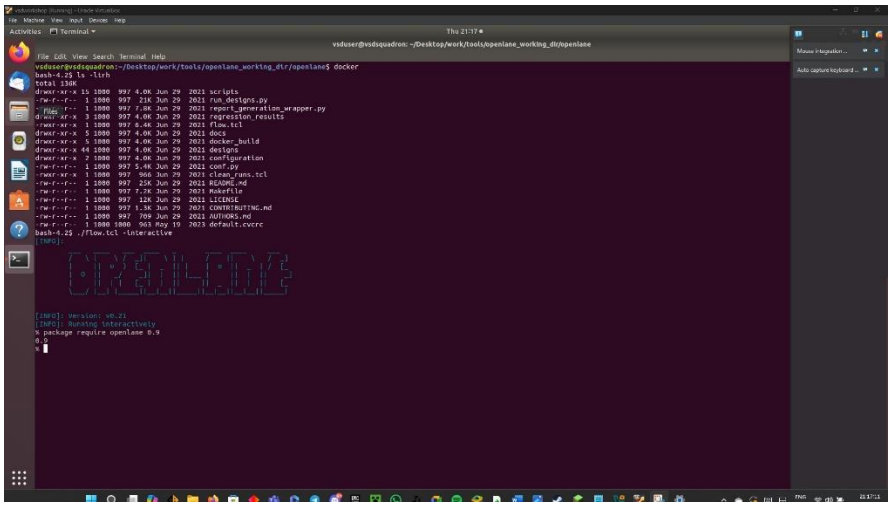


Screenshots of some of the files and directory structure of the open source EDA tool.

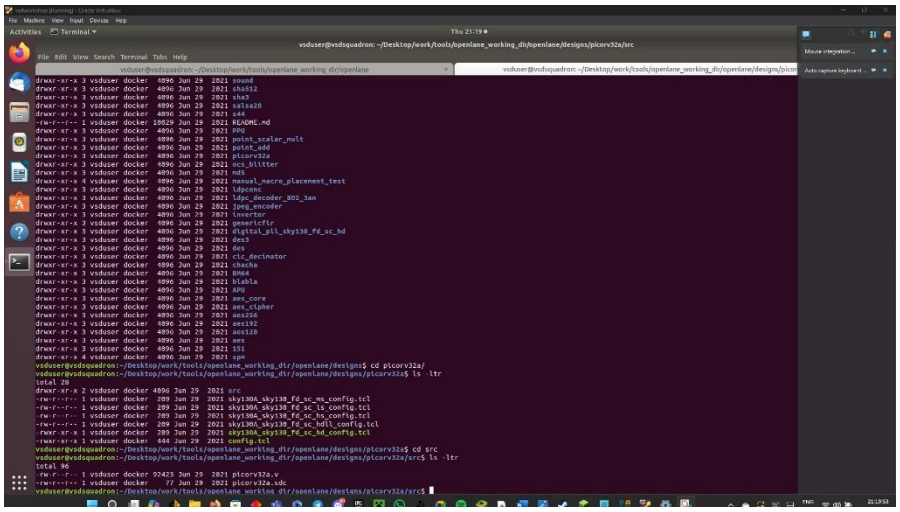


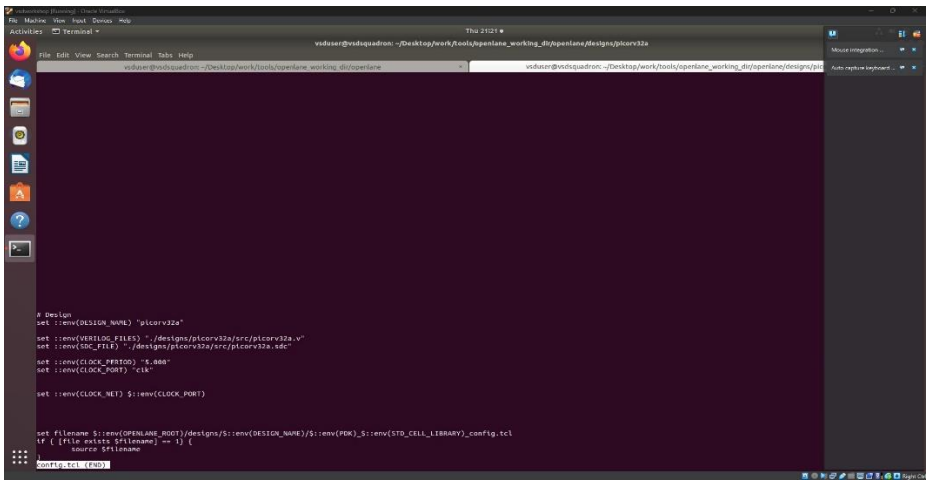


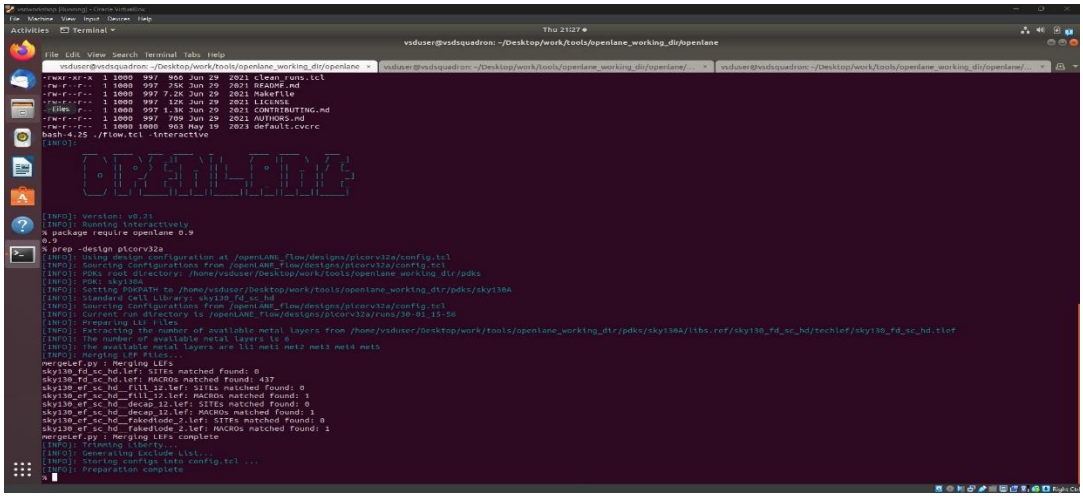
Screenshot on opening OpenLANE



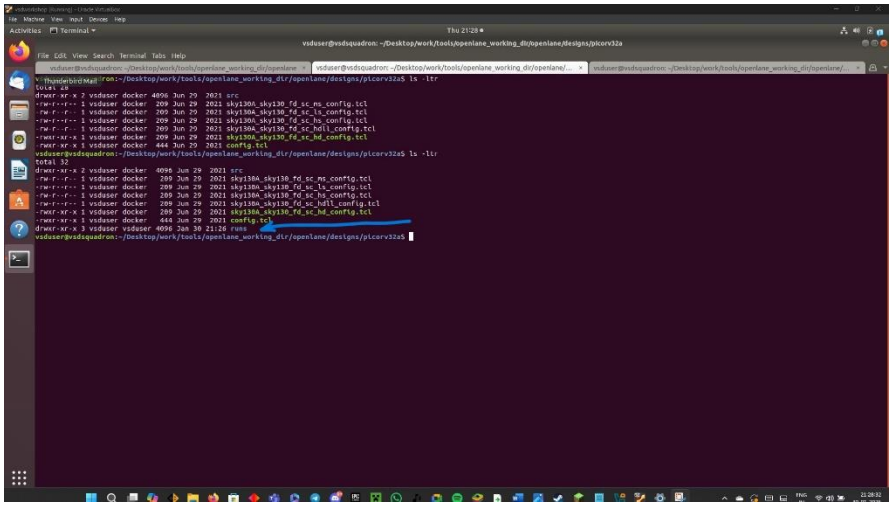
Design preparation steps - screenshots

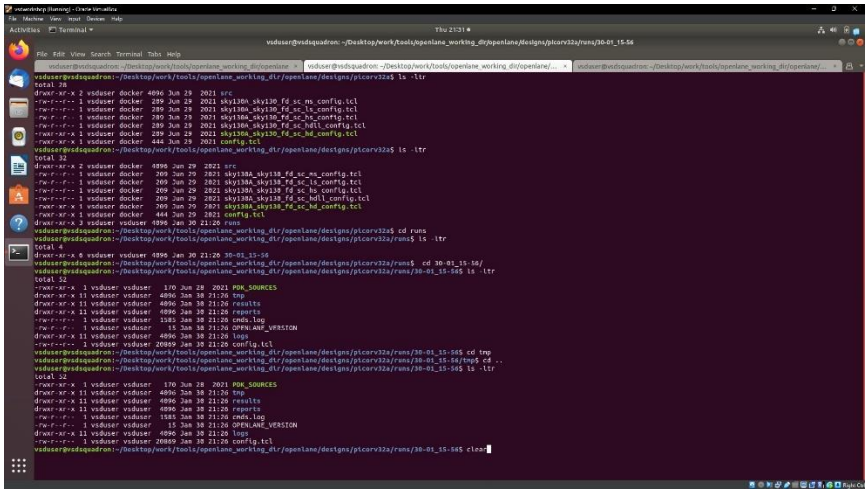




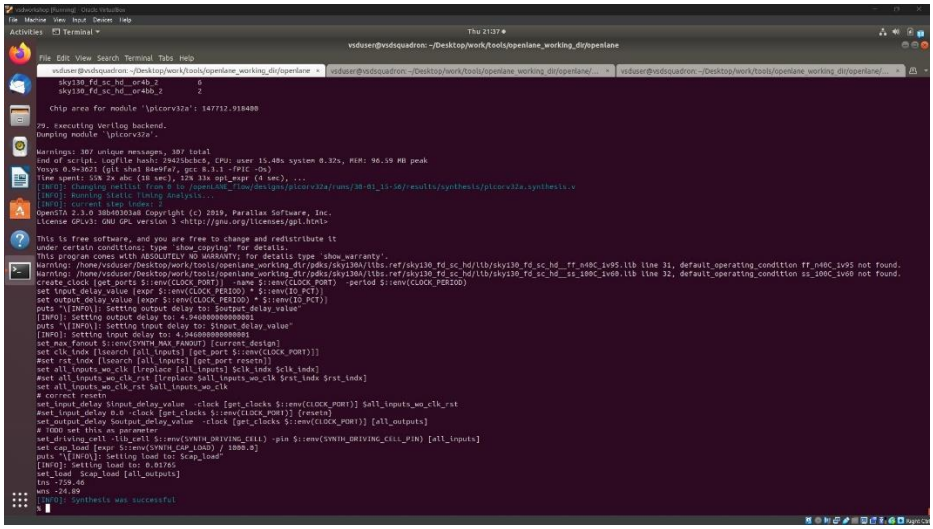


Once the preparation is completed successfully, the runs directory with the current date is created as shown in the screenshot below.





Output of the run_synthesis command



Steps to Characterize Synthesis Results

After synthesis calculate flip-flop ratio as below.

Flip flop ratio = no of DFFs / No of cells * 100

= 1613/14876*100 = 10.84%