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Grade : 8th grade

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*All pictures in the below document are taken from the digital chip design course

Level 3 Day 2 –

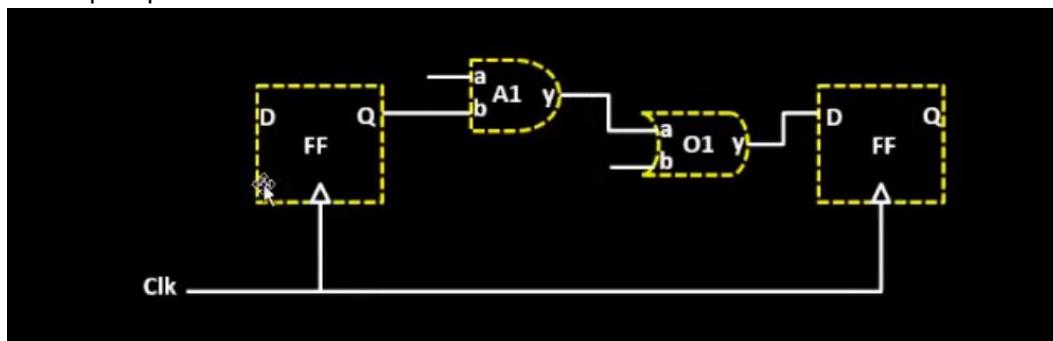
Define width and height of Core and die

Netlist – Defines the connectivity between all components.

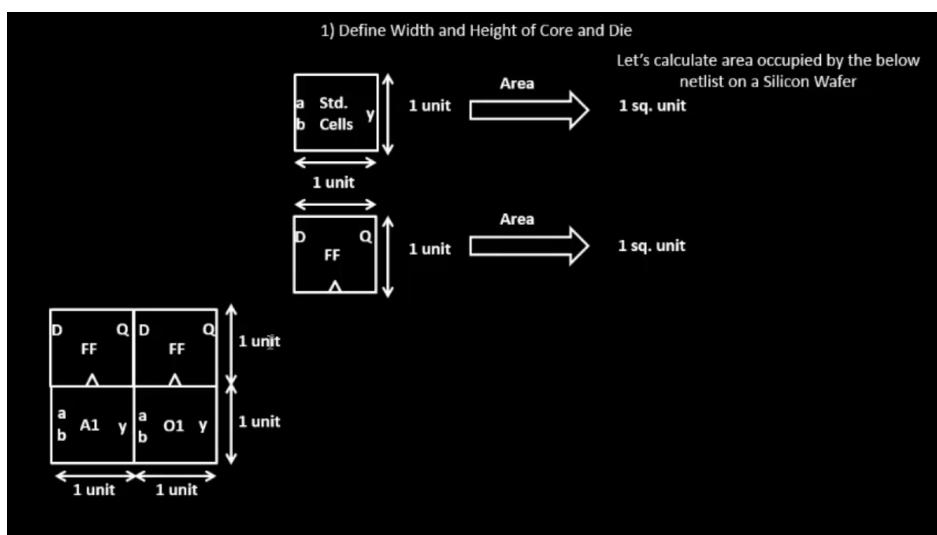
Example of a Netlist –

A1, 01 – AND Gate and OR Gate

FF – Flip Flops



Then we give the AND Gate and OR Gate dimensions such that the length and breadth is 1 unit each, so the area is 1 sq. unit. Let us also assume the same for the Flip Flops.

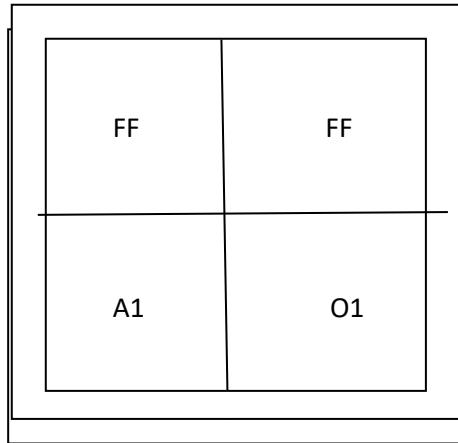


Calculating the area of the FF's and the Gates, let us club them into one singular area, such that the total area is 4 sq. unit

On a silicone wafer, we have many cells, which are made up of core and die. The core is the inner part where all the logic gates are found, while the die encapsulates the core.

If you place the above netlist inside a core, then it uses all parts of it, making it 100% utilized.

As seen in the below diagram, the core is 100% utilized.



$$\text{Utilization Factor} = \frac{\text{Area occupied by netlist}}{\text{Total Area of the Core}} = \frac{4 \times 1 \text{ sq. unit}}{2 \text{ unit} \times 2 \text{ unit}} = \frac{4 \text{ sq unit}}{4 \text{ sq unit}} = 1$$

If the utilization factor is 1, then the core is 100% utilized, ideally there is 50 to 60 % utilization

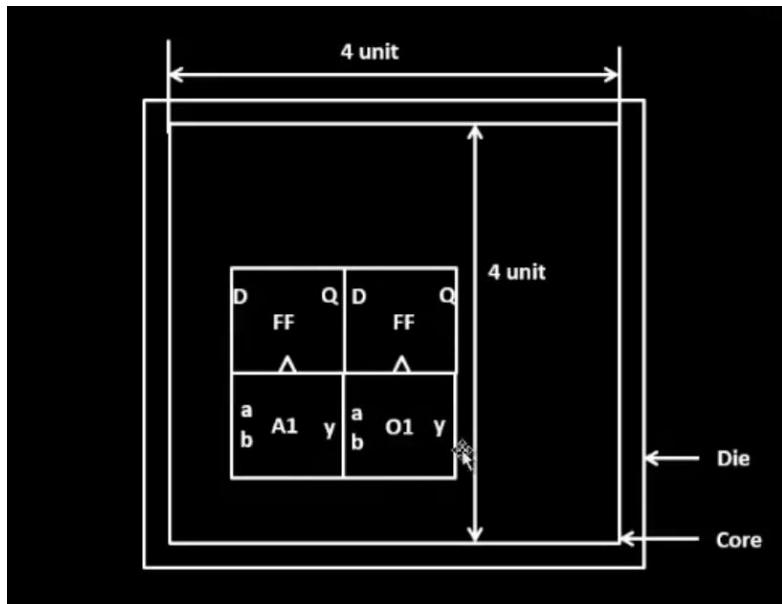
$$\text{Aspect Ratio} = \frac{\text{Height}}{\text{Width}} = \frac{2}{2} = 1$$

Whenever Aspect Ratio is 1, it signifies the chip is a square chip, if it is other than 1, then it is a rectangle.

If the core is a rectangle, then Utilization Factor = $\frac{2 \times 2}{4 \times 2} = \frac{4}{8} = 0.5$ Utilization Factor, which signifies a rectangle shape.

Aspect Ratio – 2 divided by 4 = 0.5 Aspect Ratio

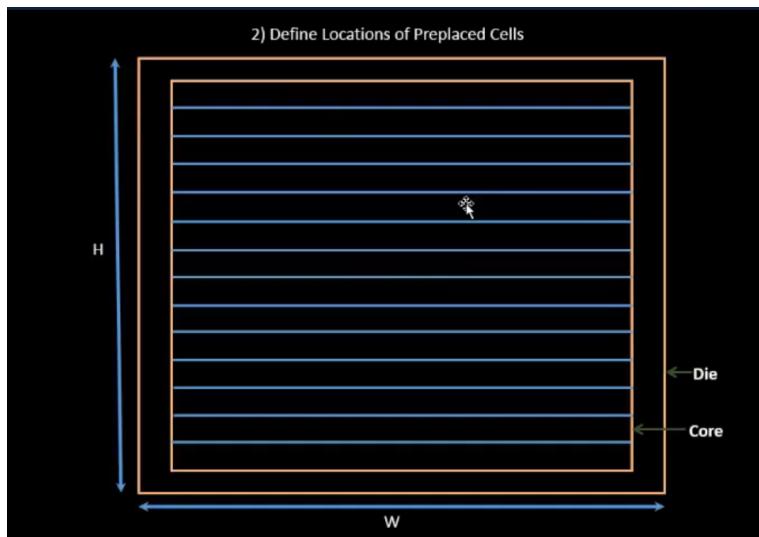
If core is a square with 4 unit length and breadth –



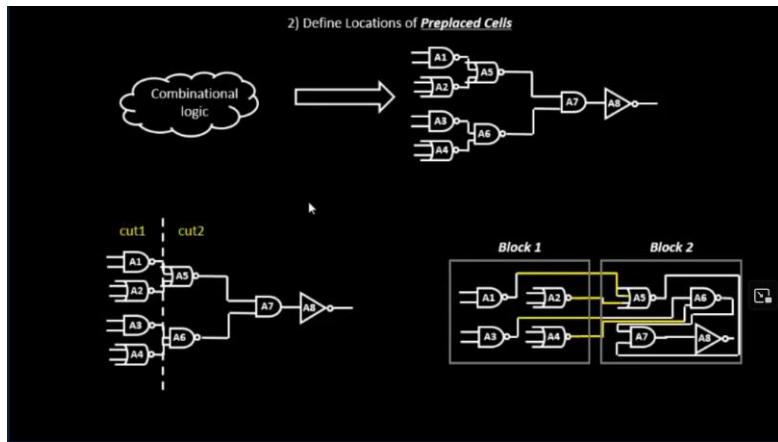
Then Utilization Factor = $\frac{4}{16} = 0.25$, which signifies that 75% of the core is available for optimization

Aspect Ratio = $\frac{4}{4} = 1$, which signifies that it is a square.

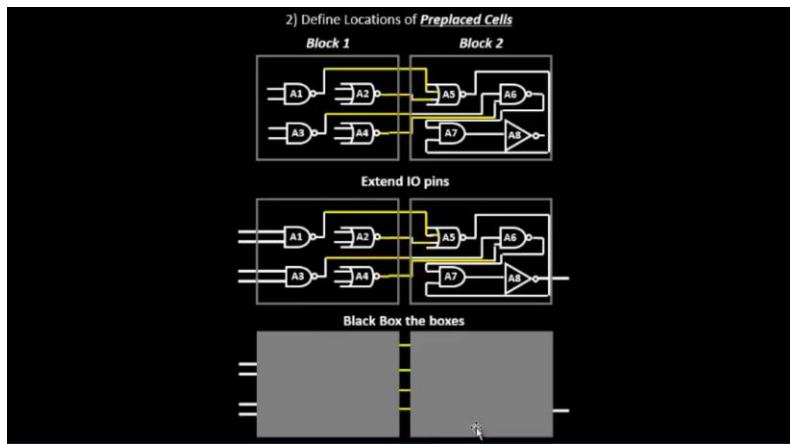
Next step is to define the location of preplaced cells.



To define the location, we must first have the combinational logic –

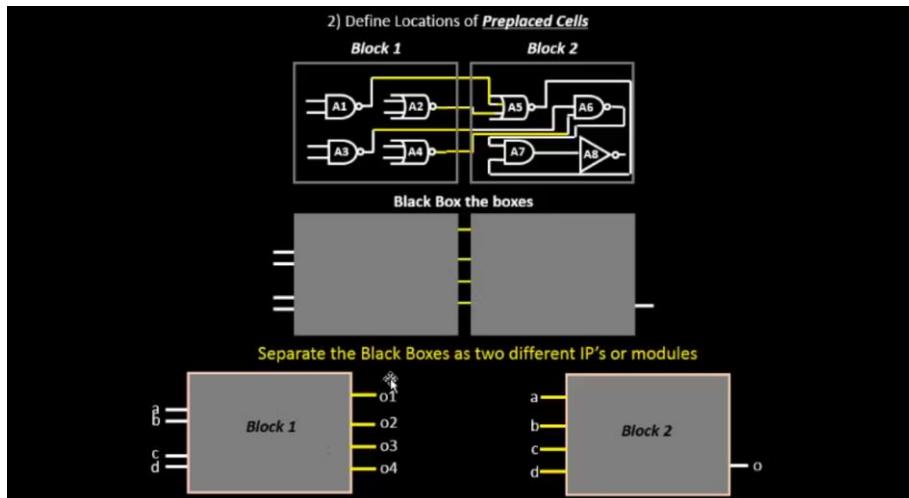


We then can define block 1 and 2 separating them –



We then can extend the input and output pins and then black box them, such that only the input and output pins are seen.

We then can separate the black boxes as 2 different IP's or modules.

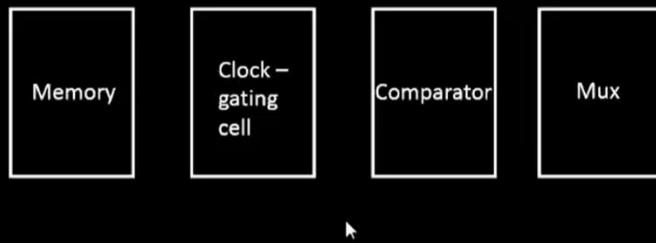


Then the 2 blocks can be implemented separately

These IPs as shown below need to be implemented only once and can be reused. Since they are implemented only once before automated placement and routing , they are called pre-placed cells.

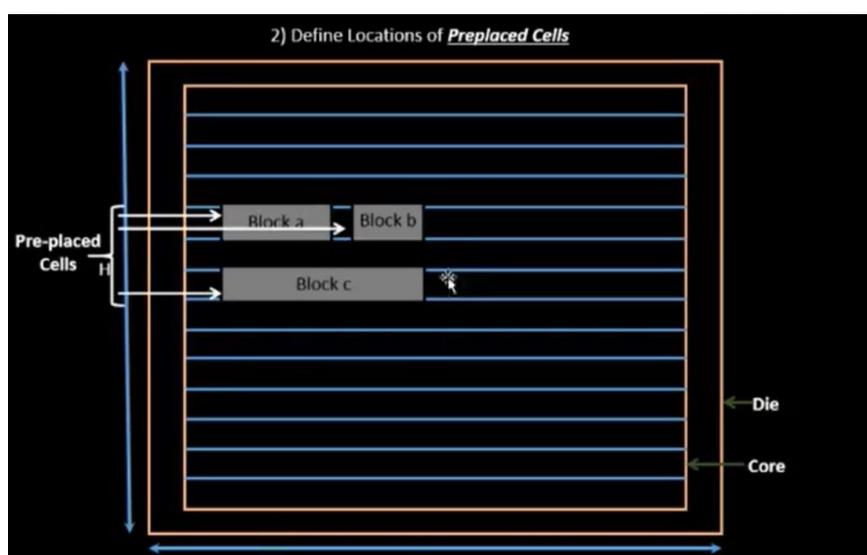
Their locations re fixed and are not moved in the floor plan

- Similarly, there are other IP's also available, for eg.



- The arrangement of these IP's in a chip is referred as Floorplanning
- These IP's/blocks have user-defined locations, and hence are placed in chip before automated placement-and-routing and are called as *pre-placed cells*.
- Automated placement and routing tools places the remaining logical cells in the design onto chip

The blocks are the memories which in case of a particular design interact with the input side so they are placed close to the input pins which is as per some designs to the left of the core. Locations of the pre-placed cells can't be moved.



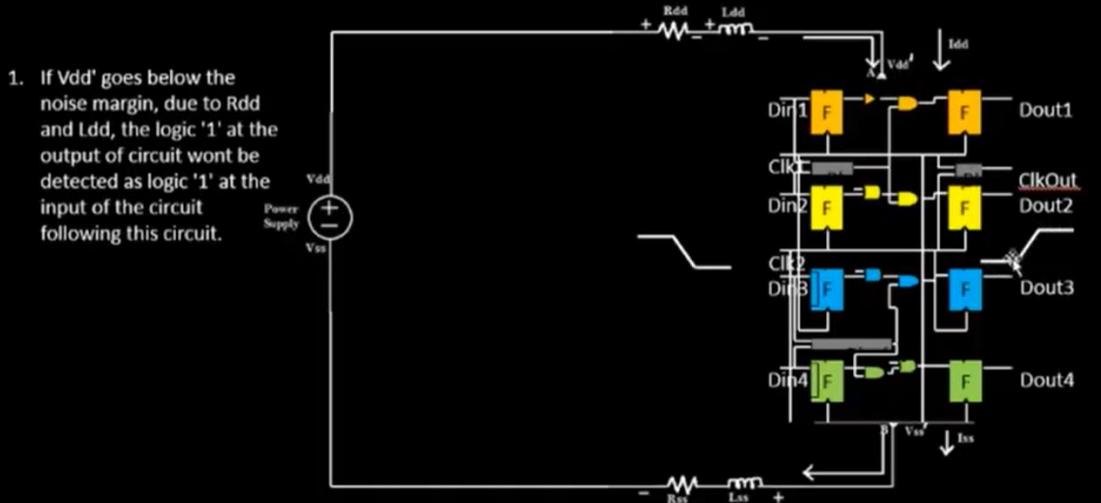
De-coupling capacitors

Resistance and inductance are found on the physical wires there are multiple voltage drops

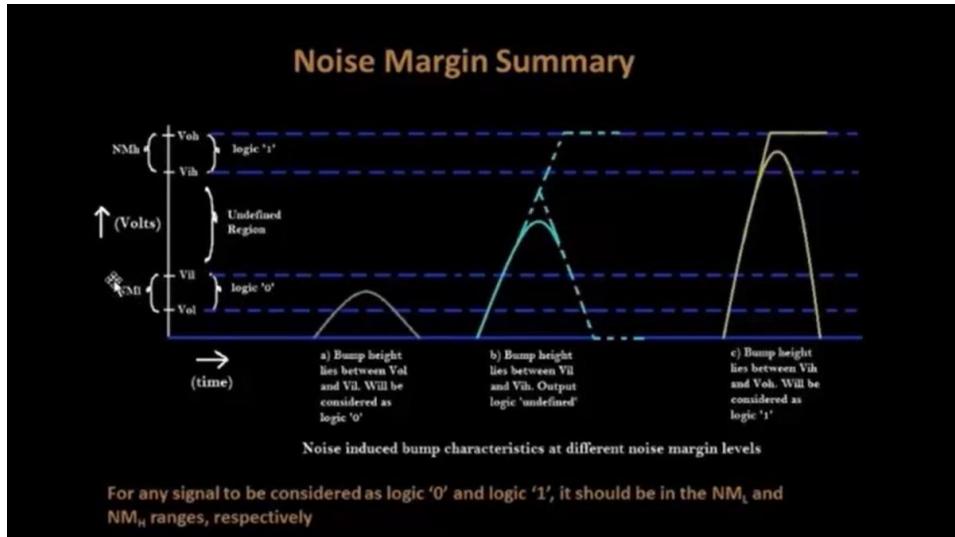
If V_{dd} is the source voltage, when it flows , $V_{dd'}$ is less than V_{dd}

If V_{dd} is 1 V and $V_{dd'}$ is 0.7 V , for a logic 1 to be deducted , should be within the noise margin

Consider the amount of the switching current required
for a complex circuit something like below

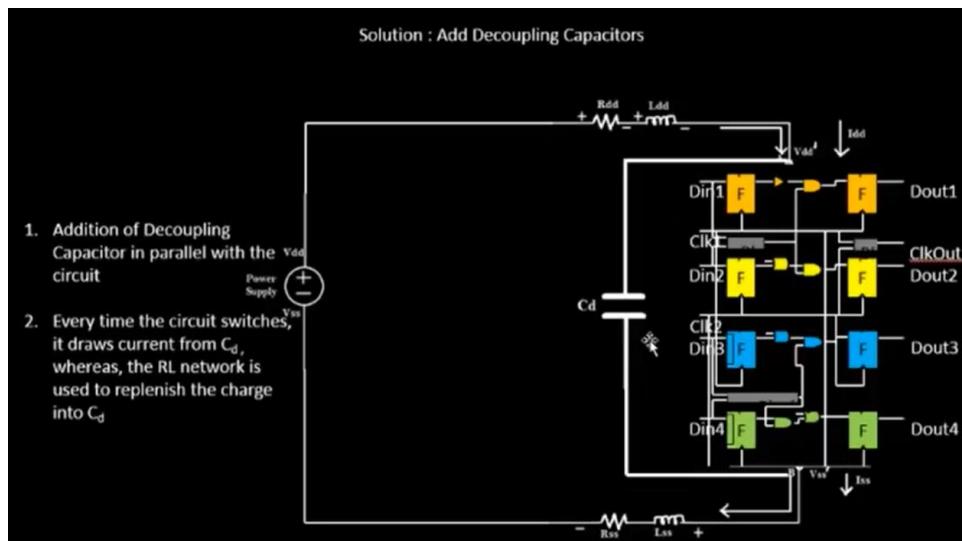


Noise margin waveforms are as below



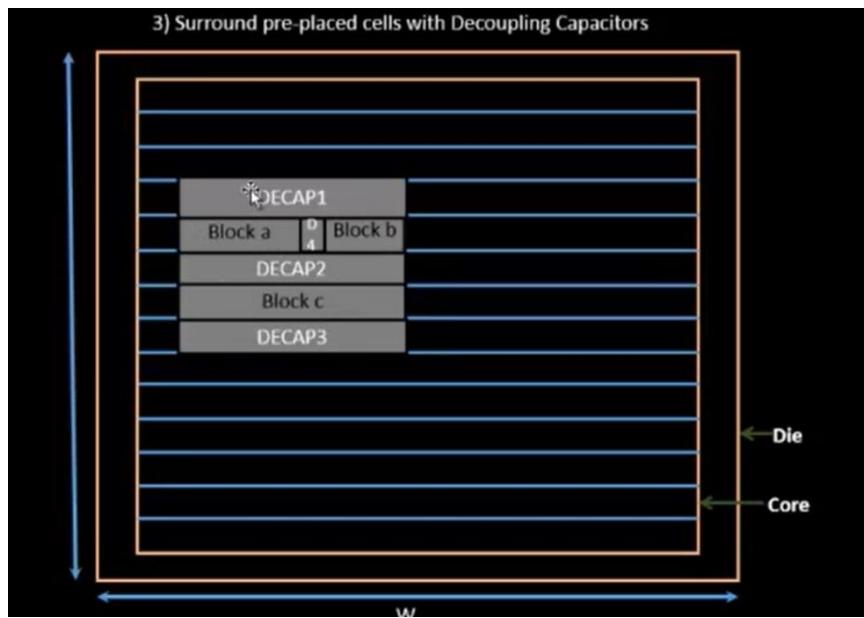
The problem of the voltage falling in the noise region which leads to undefined value can be solved with the help of decoupling capacitors - In case of input voltage drop, it provides adequate power to a cell to maintain the voltage level. It decouples the power from the main power supply. They are placed close to the blocks physically.

Solution : Add Decoupling Capacitors



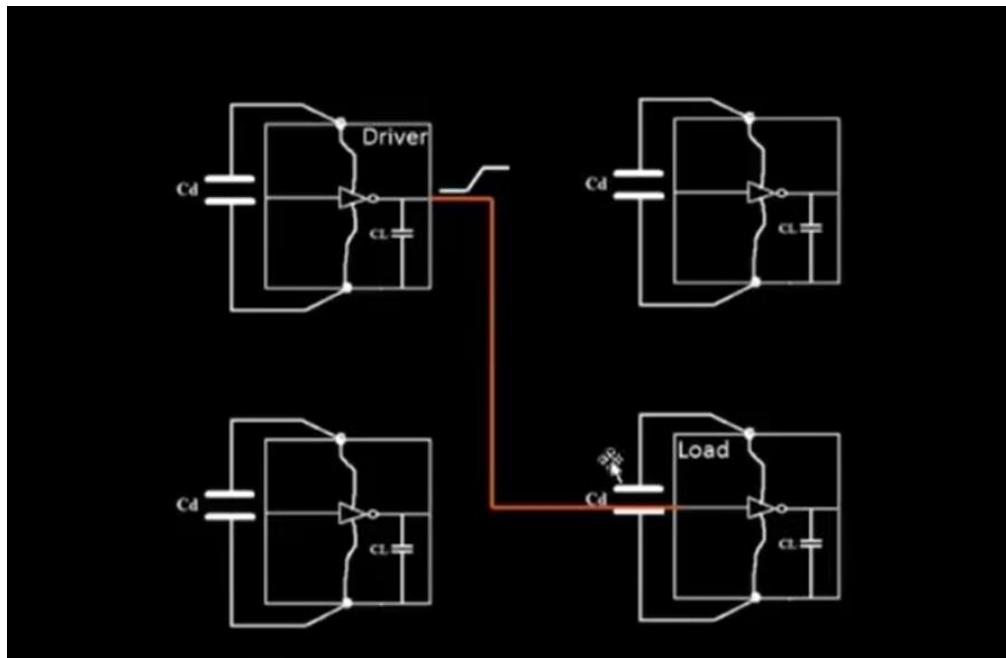
When there is a switching activity, the Capacitor loses charges to the circuit and when there is no switching activity , it charges again.

Placement of the decoupling capacitors are as below. The pre-paced cells get their charges from the decoupling capacitors.

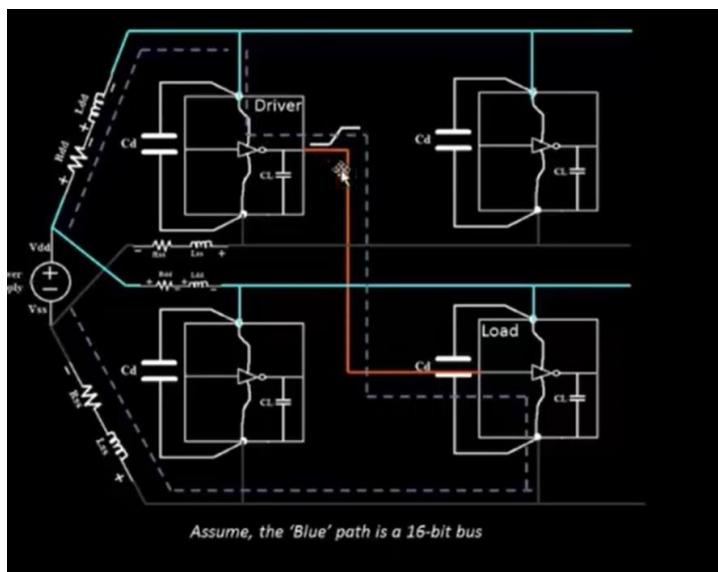


Power planning

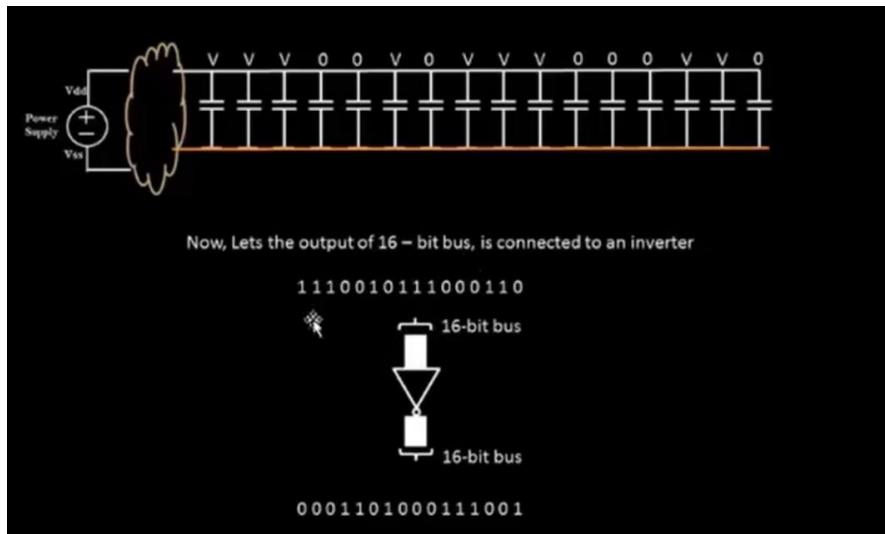
The macros are as shown and each of them require power. In the below image, there is a driver and a load and a signal is being sent from driver to the load. Signal is logic 0 to logic 1



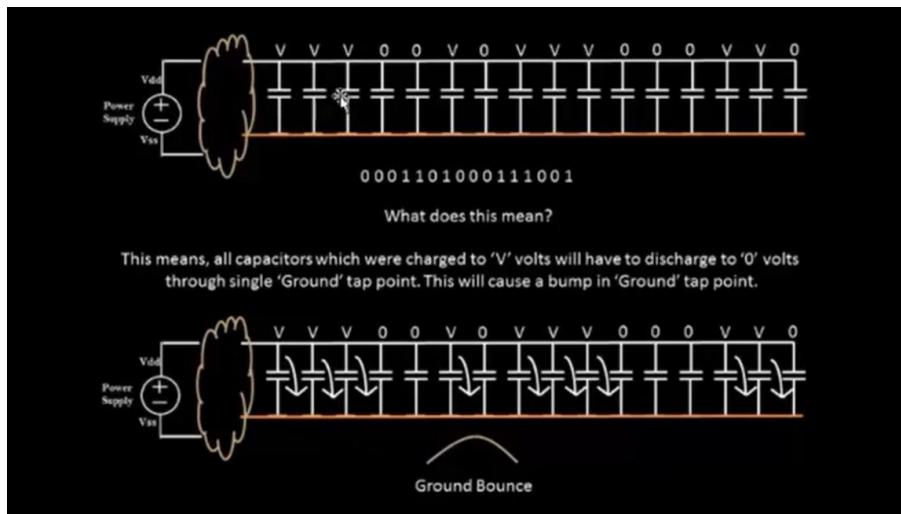
On connecting the power supply, the logic 1 from driver to load has to be retained as more decoupling capacitors cannot be added.



Whenever there is logic 1 , the capacitors are charged to Vdd and when it is logic 0 , the capacitors are discharged to ground. On passing through an inverter, the capacitors which were at 1 will discharge to 0 and visa versa.

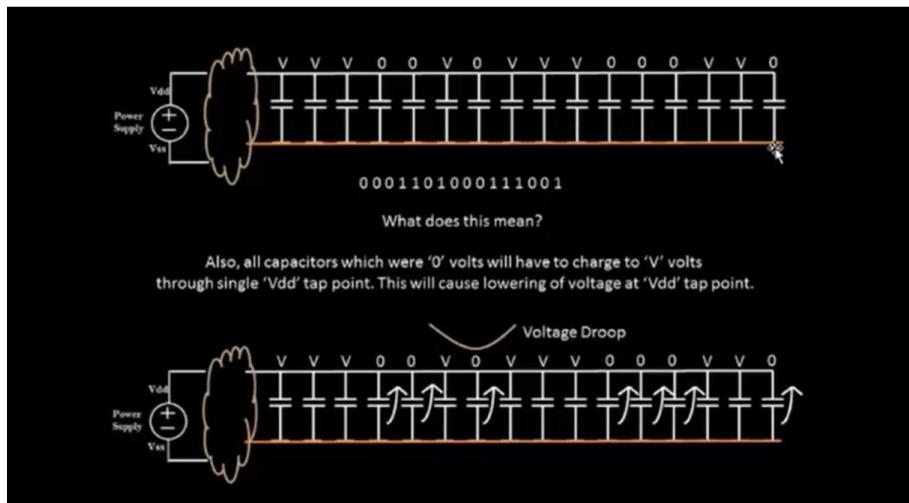


Scenario where there could be a problem called ground bounce

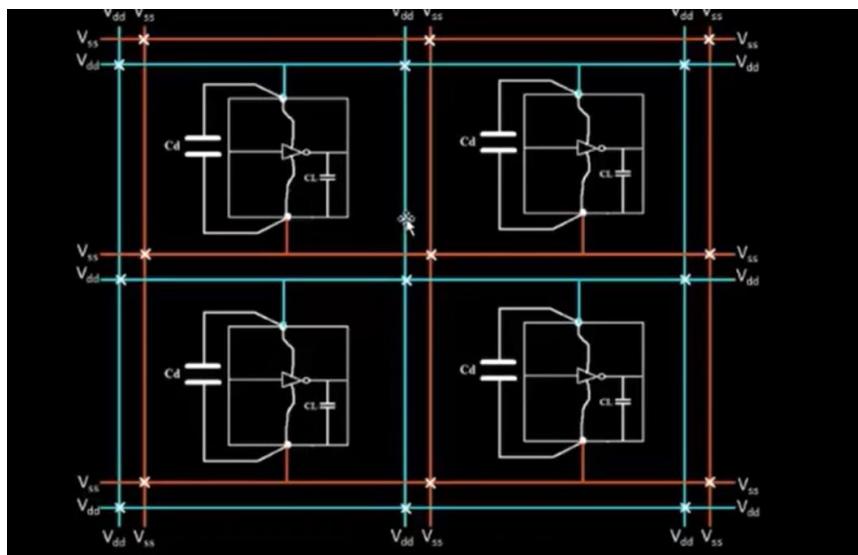


There are chances of a ground bounce and if this is more than the noise level, it could lead to undefined values.

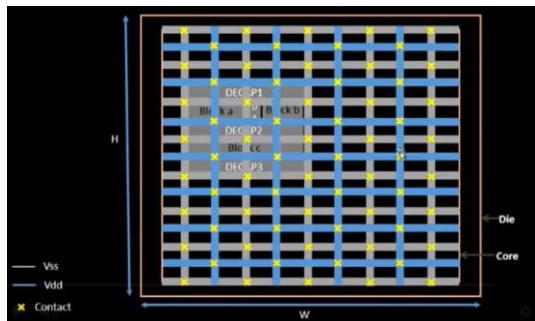
When the capacitances then charge, there is a voltage droop as all capacitors are demanding power from the same power supply. If this voltage droop is above the noise margin, it is ok else the values goes to undefined stage.



This problem of ground bounce and voltage droop can be solved using multiple Voltage sources. This is called a mesh

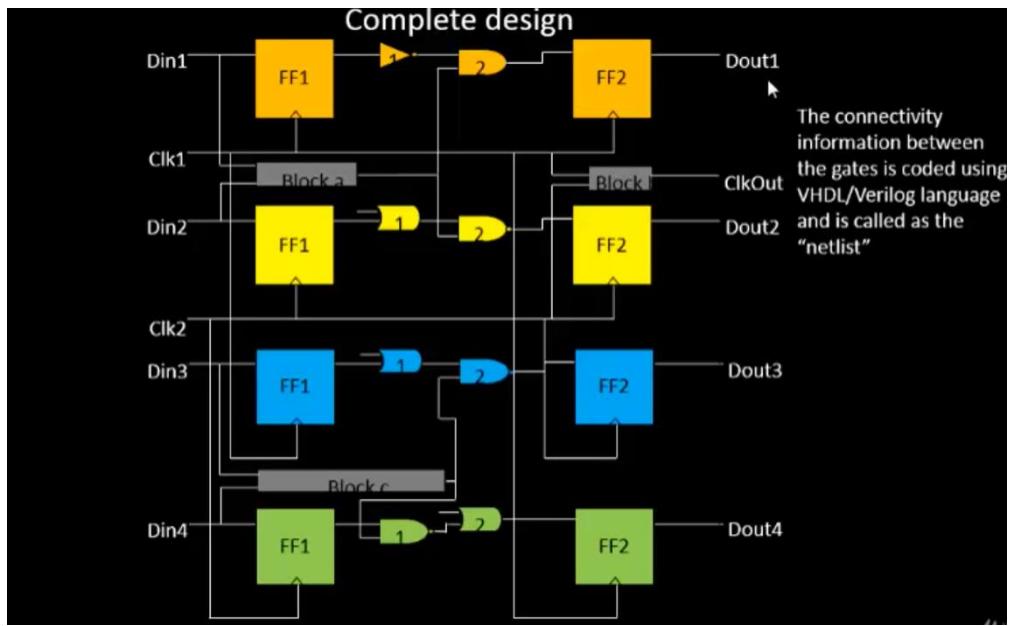


How it looks in a chip design. Any logic will use the nearest power supply and dump to the nearest ground.



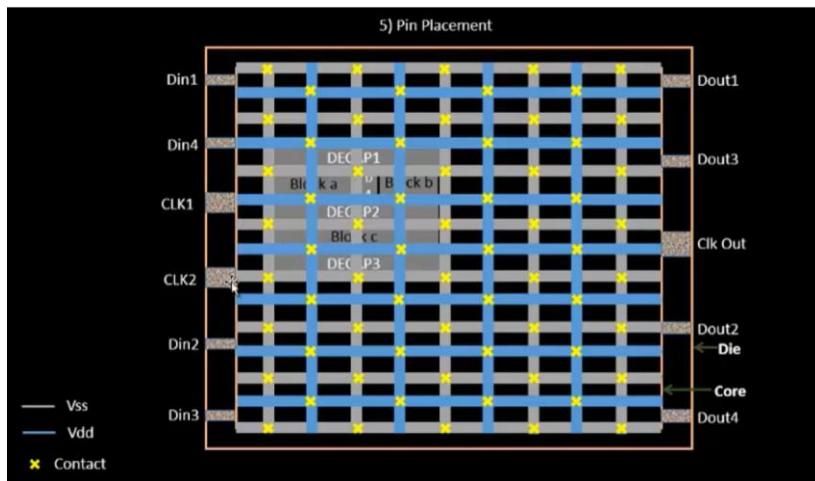
Pin placement

Example circuit with pre-placed cells

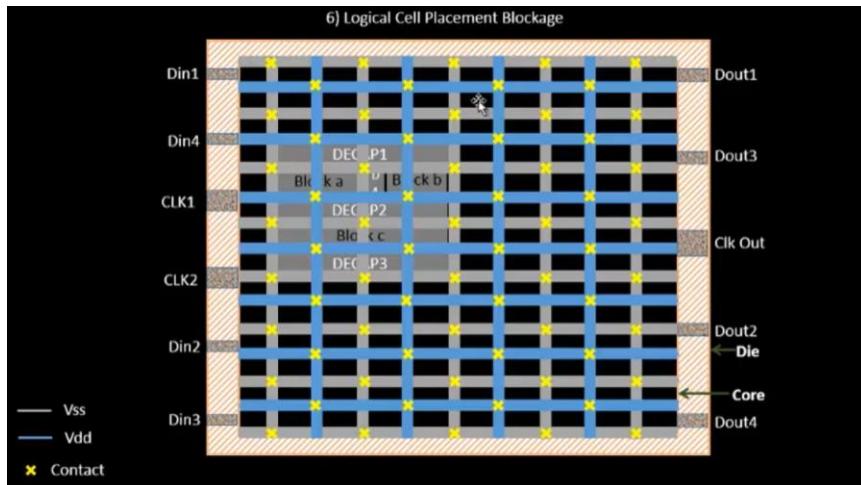


Netlist is the connectivity information of the various gates. Defined using the Verilog language

The input pins are to the left of the core and output pins to the right of the core. The clocks drive the entire chip



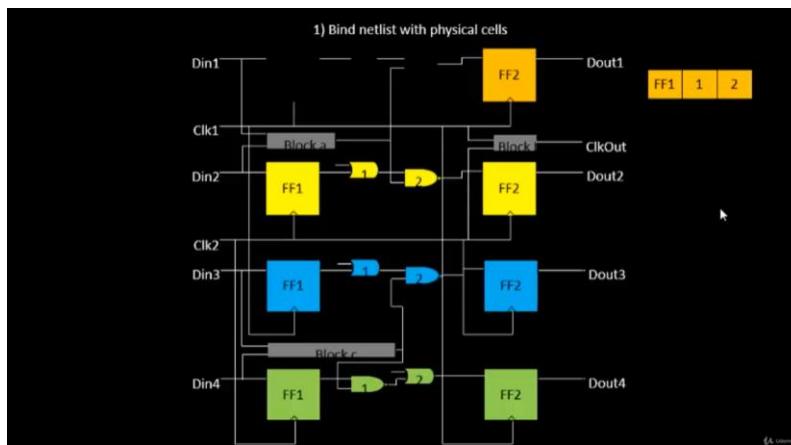
The area between core and die is blocked using a logical blockage so that the automated routing and placement tool does not place in that area as it is reserved for the pin locations.



Sky130 Day 2 - Good floorplan vs bad floorplan and introduction to library cells

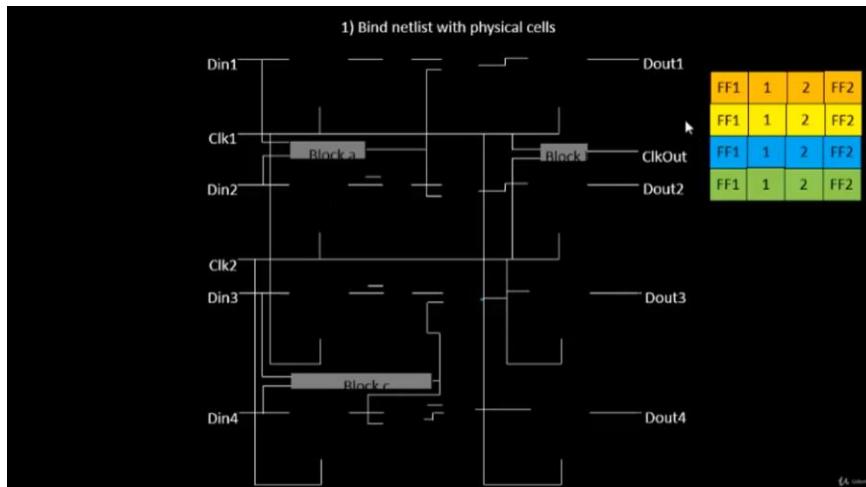
SKY130_D2_SK2 - Library Binding and Placement

SKY_L1 - Netlist binding and initial place design

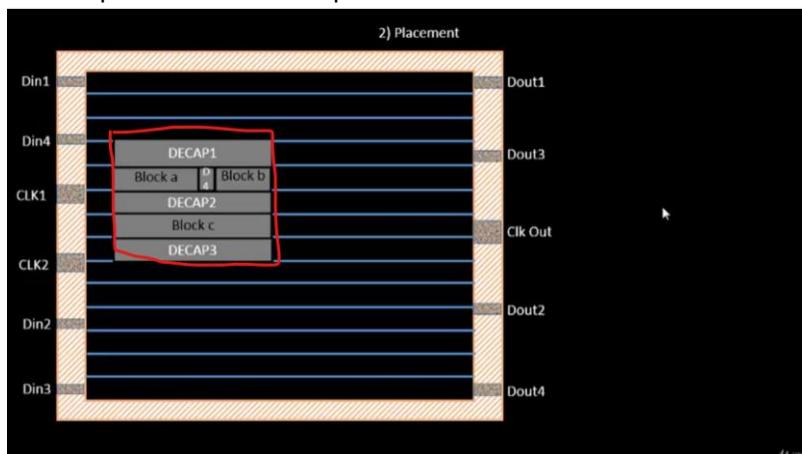


The Flip Flop 1 and 2 , AND and OR gates have a square shape box – a physical dimension as seen in the real world.

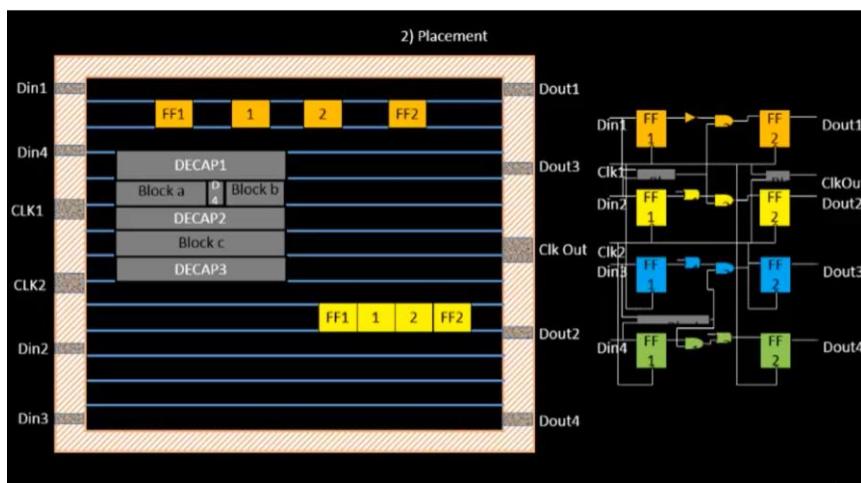
Each component in the netlist is given a proper shape like a square or a rectangle



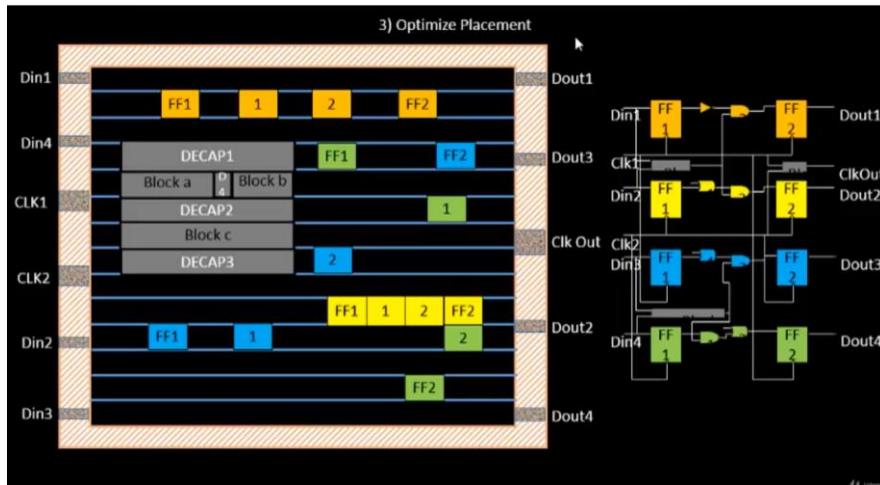
No components should be placed in the area marked in red



Placement of the components are done close to the Din and Dout where FF and the combinational logic gates take the minimum time to communicate as shown below.



The remaining flip flops and logic gates in blue and green color as placed as below with the consideration of their respective Din and Dout as close to it as possible.

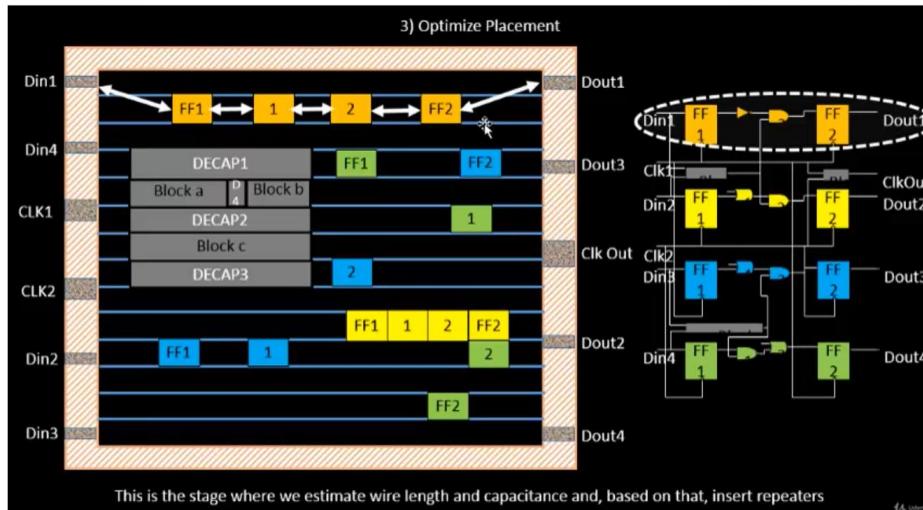


SKY_L2 - Optimize placement using estimated wire-length and capacitance

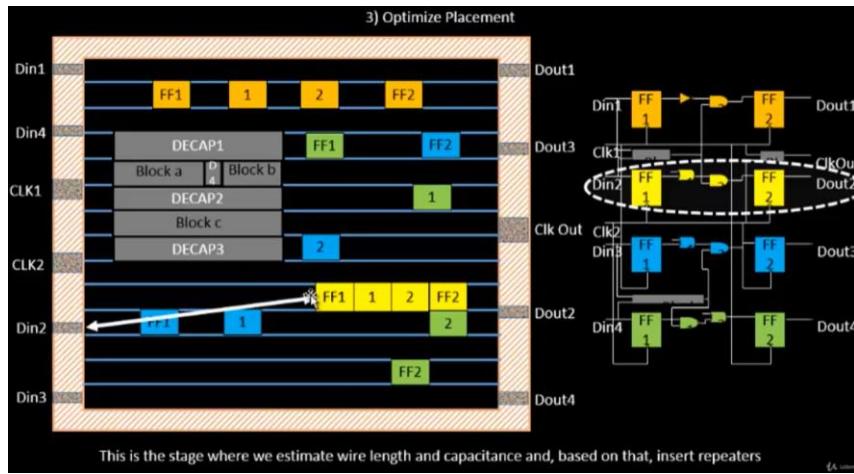
Next stage is optimizations

Signal integrity is maintained by adding repeaters or buffers but more the number of buffers added , more area will be occupied on the floor plan.

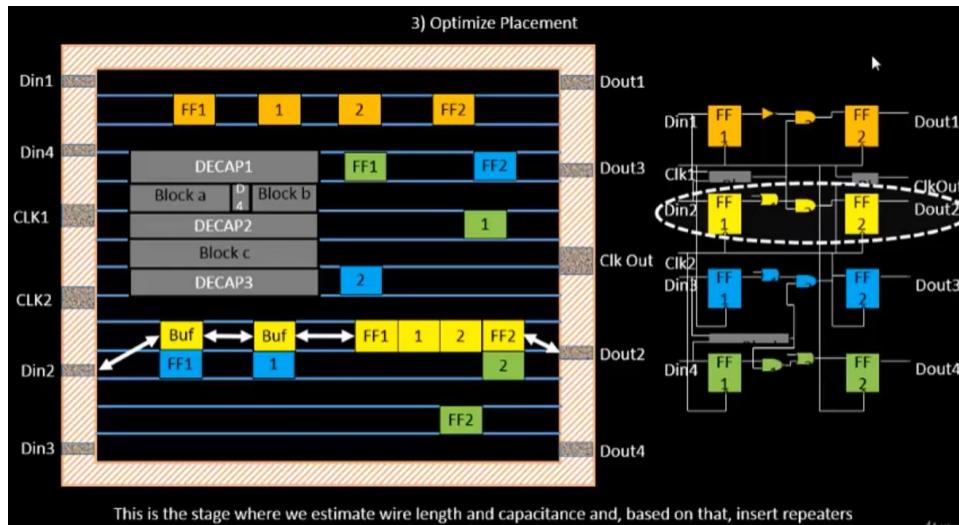
Signal integrity is maintained is the first set of FF and gates and its input and output.



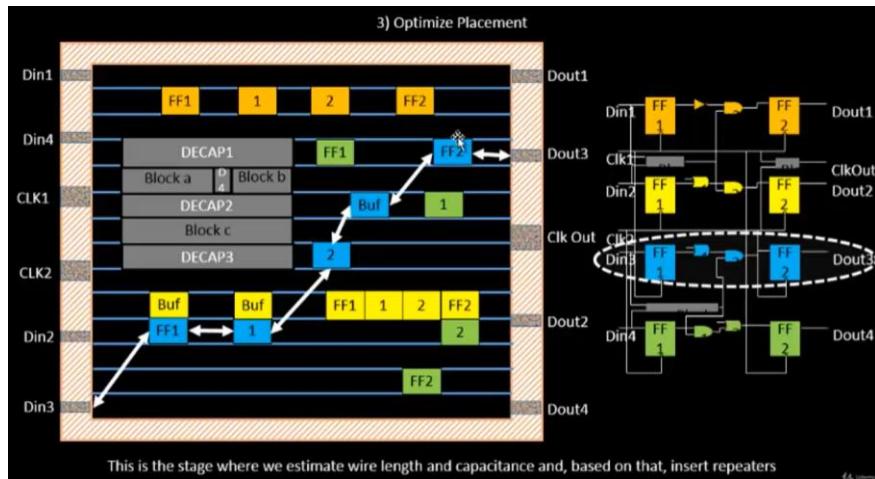
For the Yellow colour circuit , FF1 is far from Din2



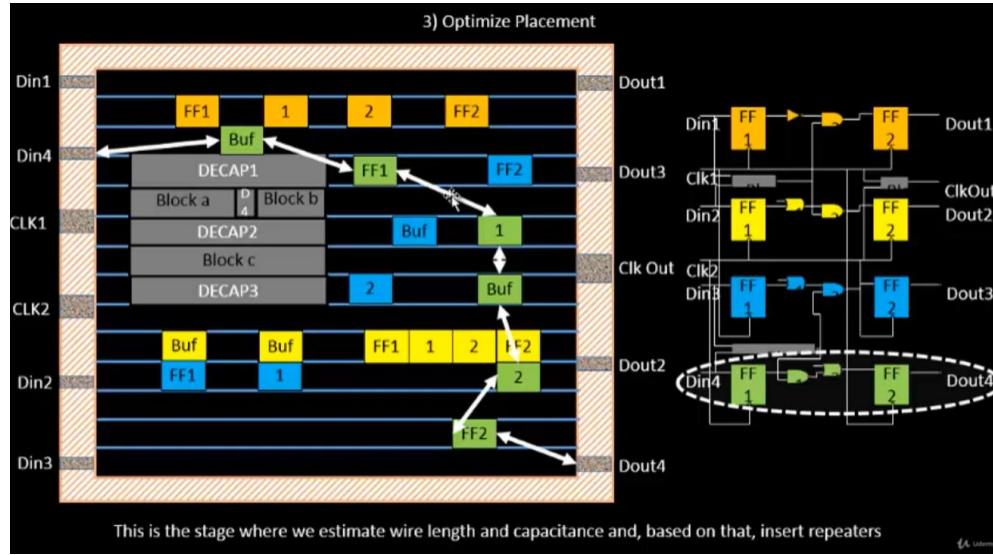
You add buffers or repeaters to reduce the length of the wire and maintain signal integrity as shown below. FF1, 1, 2, FF2 are abutted to each other and is seen as a classic example of high frequency circuit.



For the blue colour circuit, there is a buffer required for logic circuit 2 to FF2 as all other distances are optimal.



For the Green colour circuit, the buffers are placed as below. The routing will be done such that the crisscross areas, the wires will be in different layers.



SKY_L4 - Need for libraries and characterization

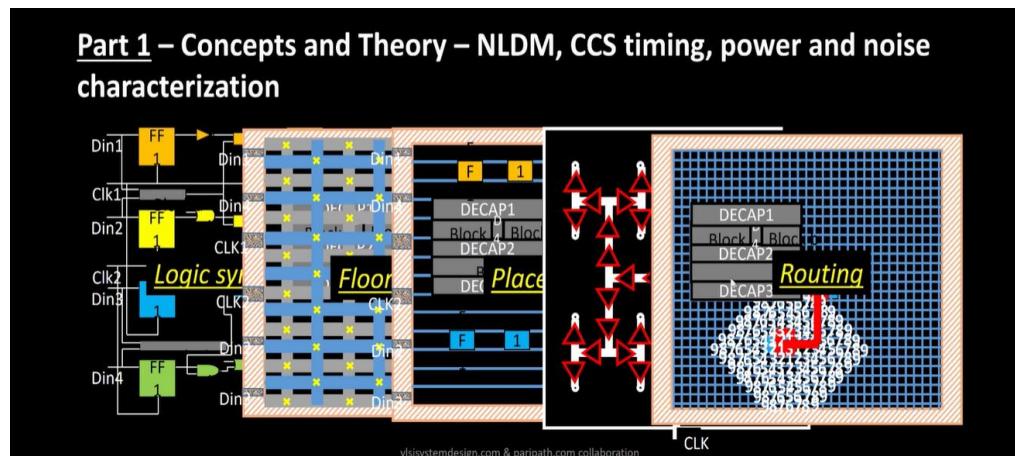
Logic synthesis is a process in which a program is used to automatically convert a high-level textual representation of a design (specified using an HDL at the register transfer level (RTL) of abstraction) into equivalent registers and Boolean equations.

Output of the Logic synthesis is the floor planning where the size(width and height) of core and die is done depending of the sizes of the flip-flops and gates in the logic sysnthesis.

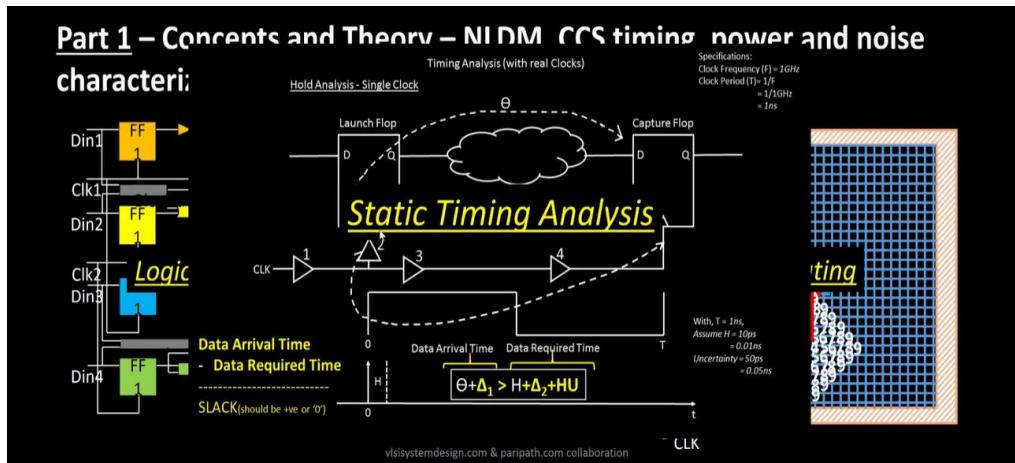
Next is placement where the logic gates are placed on the floor plan such that the distances of the FF and logic gates are close to its inputs and outputs.

Then there is Clock Tree Synthesis (CTS) so that there is zero skew and all Flip flops receive the clock signal at the same time. The buffer clocks also are made sure have the same rise and fall of the clock signals.

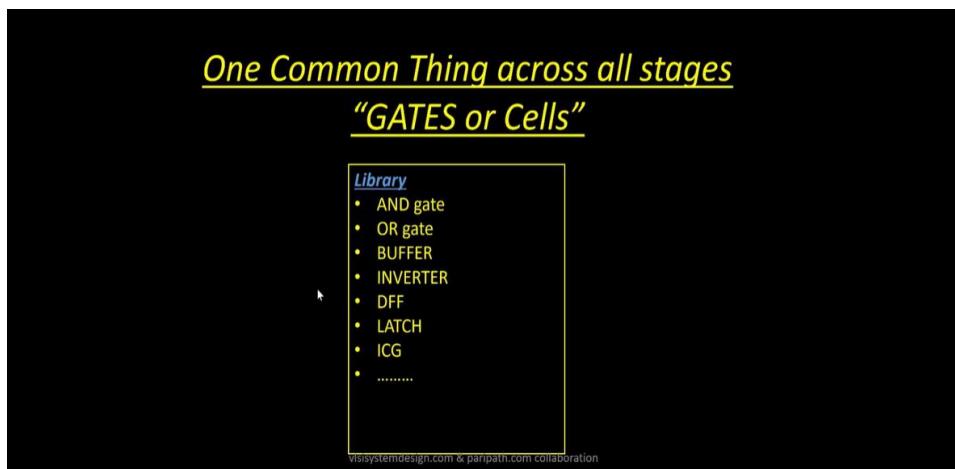
Finally there is routing, where the connections between cells have to go through a certain flow.



Static timing analysis (STA) is a way of evaluating a design's timing performance by testing for timing violations along all conceivable paths. This is the last stage and is called signoff stage



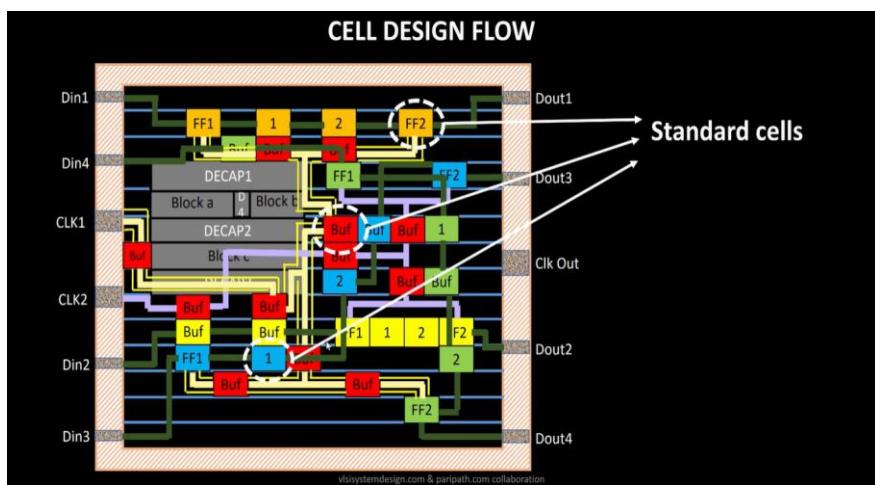
Common for all stages of characterization is the cells or gates



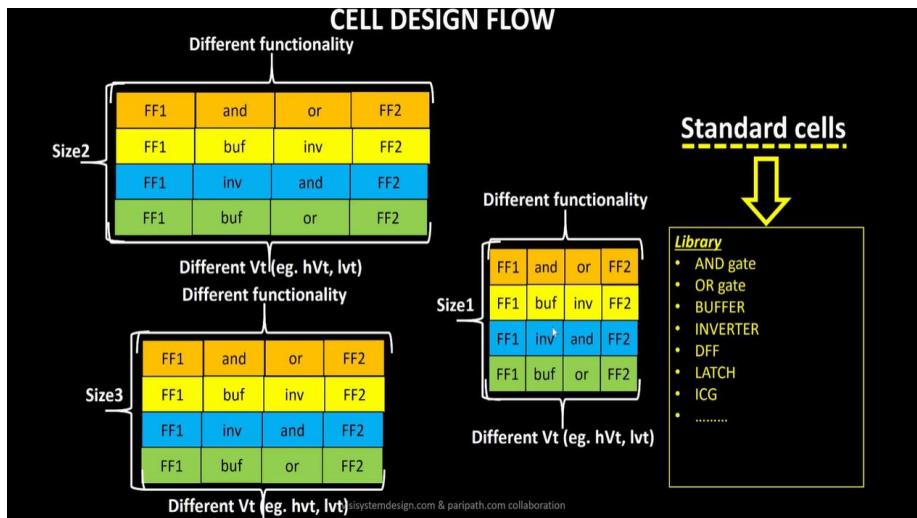
These cells have to be modelled so that the EDA tools understand them.

SKY130_D2_SK3 - Cell design and characterization flows

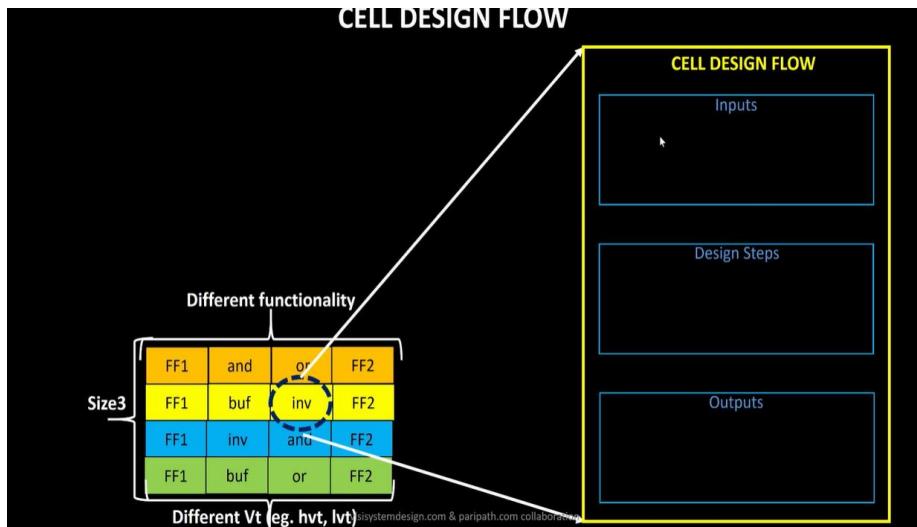
Typical placement and routed cells, the cells or gates are called standard cells



Library has a set of standard cells which of different sizes and shapes and different threshold voltages.

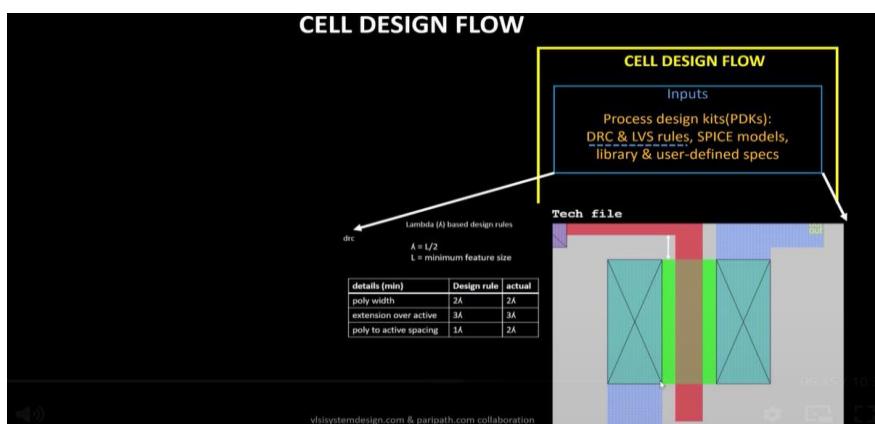


Each cell like for example an inverter needs to be designed using the cell design flow

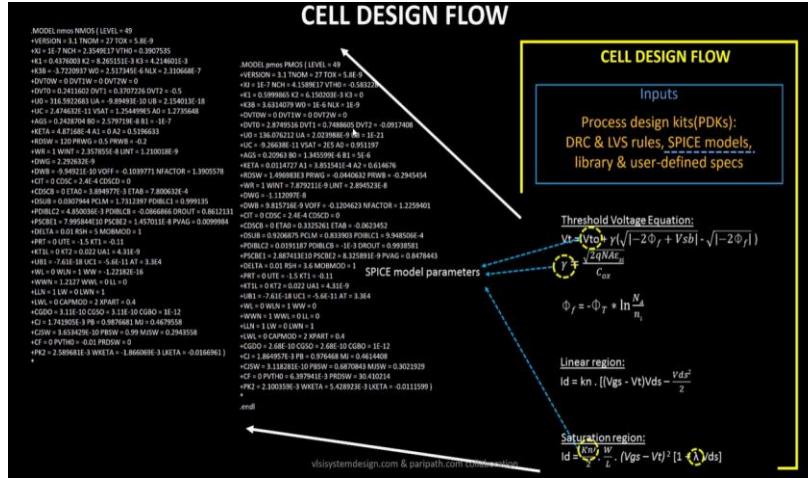


The inputs for the cell design flow are process design kits (PDKs), DRC & LVS rules, SPICE models, library and user defined specs which are given by the foundry.

Design Rule Checks (DRC) ensure that the chip's physical layout adheres to the specified design rules. Layout vs. Schematic (LVS) checks verify that the actual layout matches the intended schematic. Think of it as a quality control process, verifying that what was planned is what's being built.



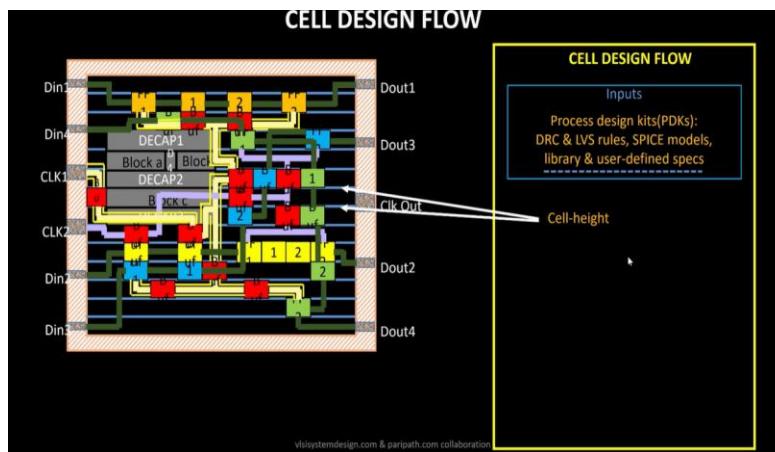
SPICE models - SPICE Simulation Program with Integrated Circuit Emphasis (SPICE) SPICE is a computer simulation and modelling program used by engineers to mathematically predict the behavior of electronics circuits.



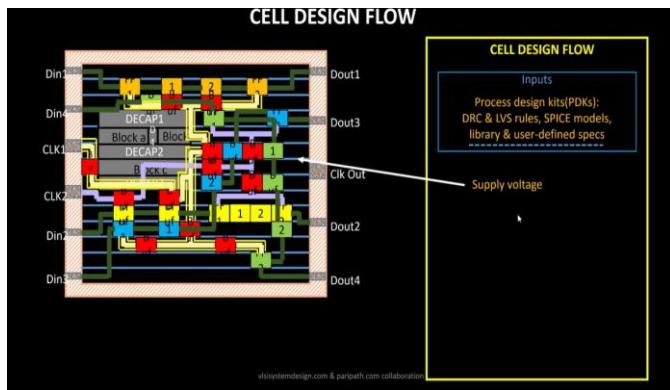
User defined specs and library

Cell height is defined as the separation between the power and the ground.

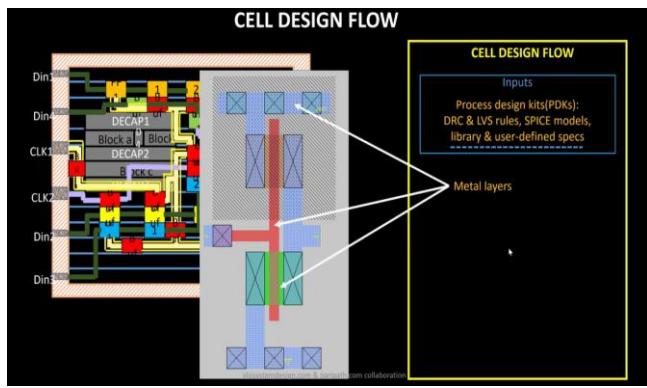
Drive strength decides the cell width.



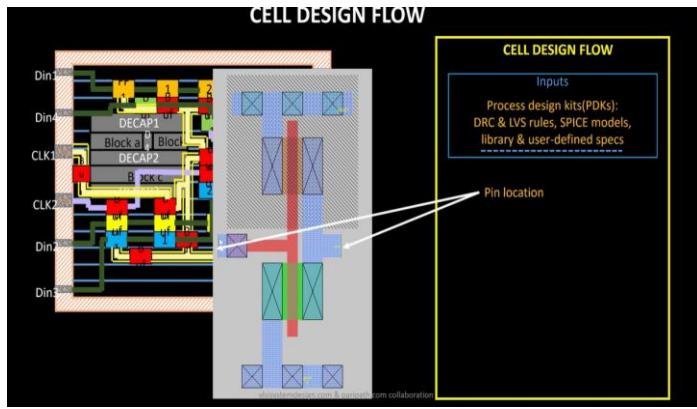
Supply voltage



Metal layers



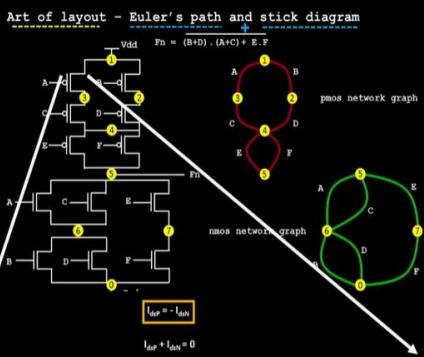
Pin locations



Design stage has circuit design, layout design and characterization.

Circuit design

CELL DESIGN FLOW



$$k_p \cdot \{[(V_m - V_{dd} - V_t), V_{dsatp}] - \frac{V_{dsatp}}{2}\} + k_n \cdot \{[(V_m - V_t), V_{dsatn}] - \frac{V_{dsatn}}{2}\} = 0$$

Alternatively, the required ratio of PMOS v/s NMOS transistor size can be derived, such that V_m is set

$$\frac{(W_p)}{(W_n)} = \frac{K_{nF} \cdot V_{dsatn} \cdot [(V_m - V_t)] - \frac{V_{dsatn}}{2}}{K_{pF} \cdot V_{dsatp} \cdot [-(V_m + V_{dd} + V_t)] + \frac{V_{dsatp}}{2}}$$

$V_m \sim 0.98v$

V_m is the point where $V_{in} = V_{out}$

$V_m \sim 1.2v$

vlsisystemdesign.com & paripath.com collaboration

CELL DESIGN FLOW

Inputs

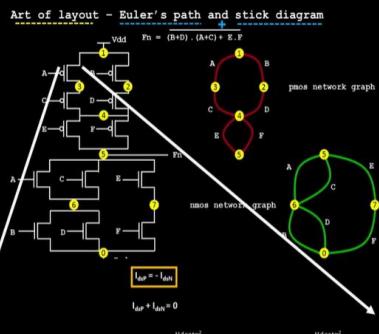
Process design kits(PDKs):
DRC & LVS rules, SPICE models,
library & user-defined specs

Design Steps

Circuit design, layout design,
characterization

Output of the circuit design is the CDL – Circuit Design Language

CELL DESIGN FLOW



$$k_p \cdot \{[(V_m - V_{dd} - V_t), V_{dsatp}] - \frac{V_{dsatp}}{2}\} + k_n \cdot \{[(V_m - V_t), V_{dsatn}] - \frac{V_{dsatn}}{2}\} = 0$$

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CELL DESIGN FLOW

Inputs

Process design kits(PDKs):
DRC & LVS rules, SPICE models,
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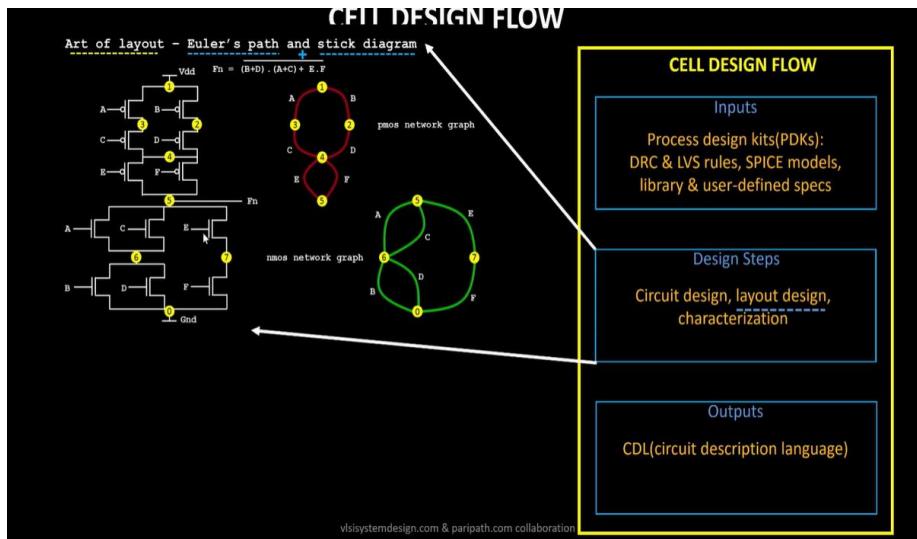
Design Steps

Circuit design, layout design,
characterization

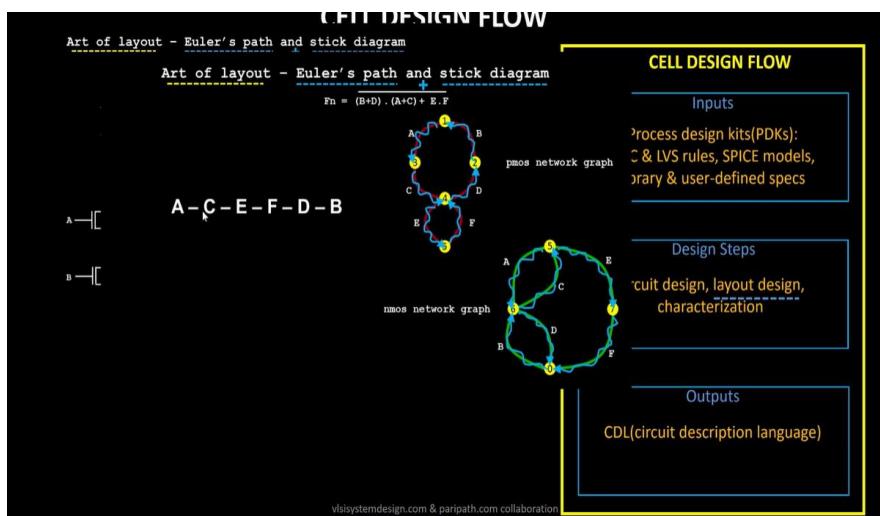
Outputs

CDL(circuit description language)

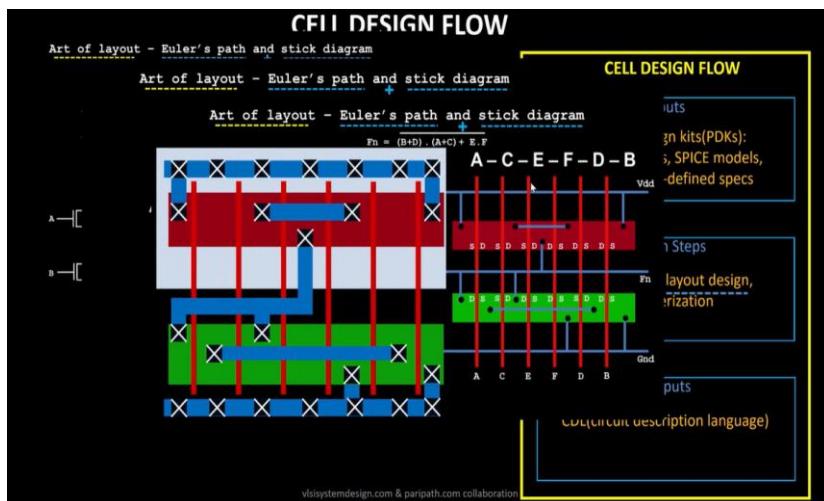
Layout design is to get the pmos and nmos network graphs



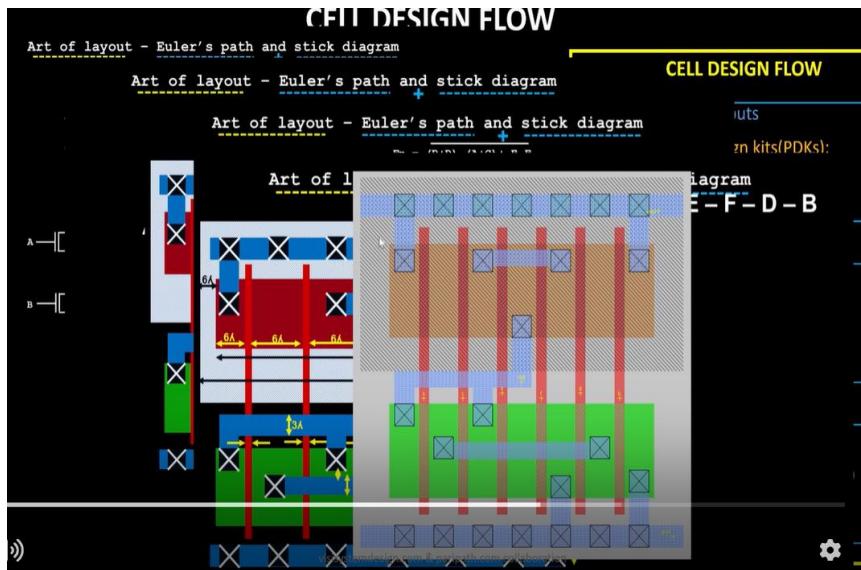
Next is to get the Euler's path - A Euler path is a path that uses every edge of a graph exactly once. A Euler circuit is a circuit that uses every edge of a graph exactly once.



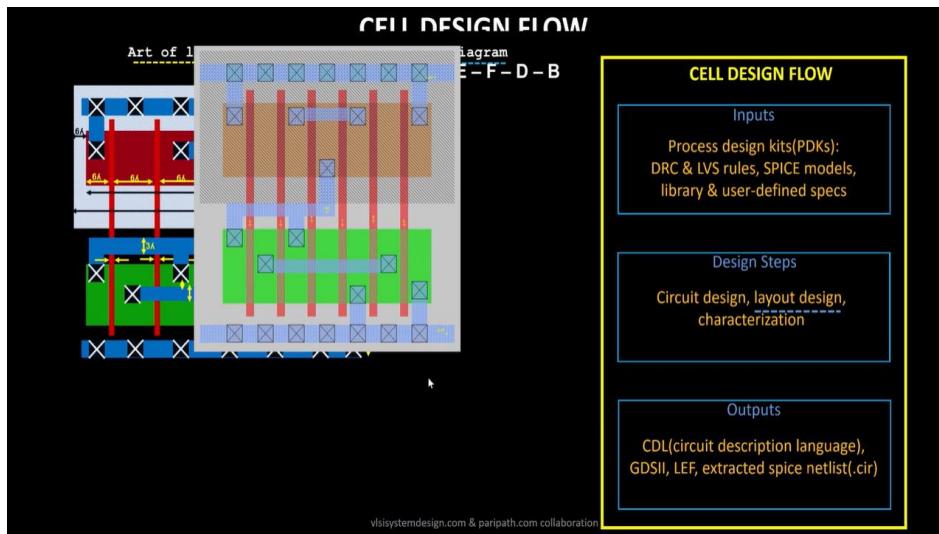
After this a stick diagram is to be drawn



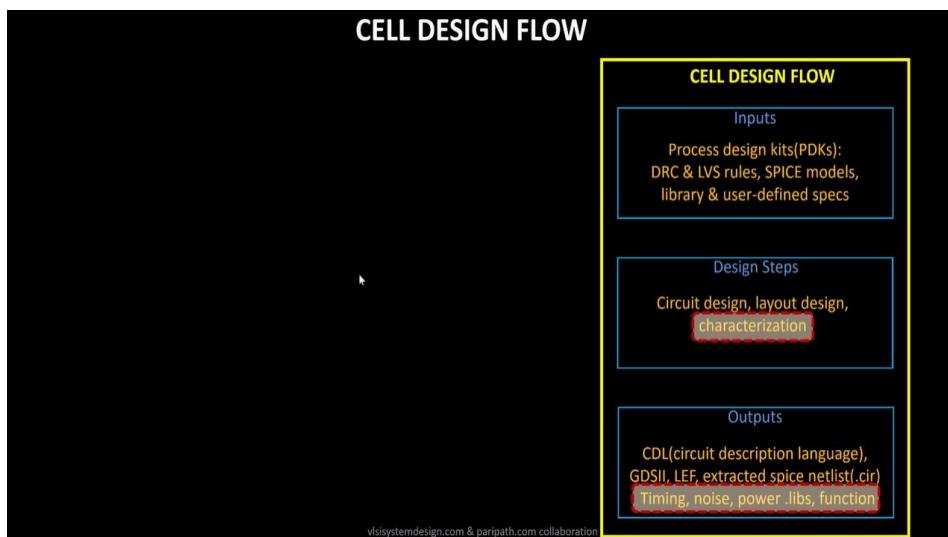
Typical layout using magic EDA tool



Output of the Layout design is GDSII, LEF, extracted spice netlist (.cir)

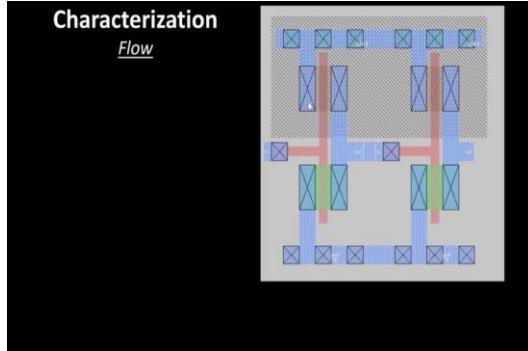


Output of characterization is timing, noise, power, libs and function

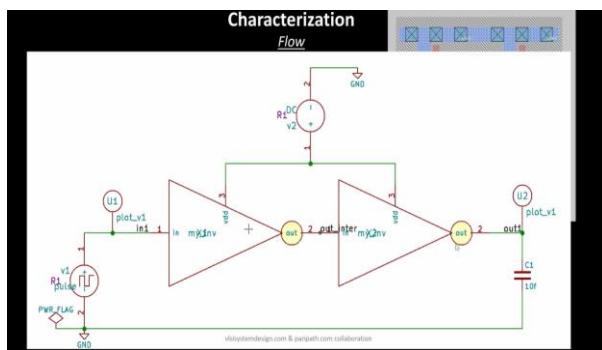


Typical characterization flow for an inverter

Layout of a buffer



Circuit design



Extracted Spice netlist of a buffer and PMOS and NMOS models

```

Characterization
Flow
.v1 inl v1 pulse 1.0 10p 10p 1n 2n
* u1 inl plot v1
* u2 outl plot v1
v2 net_x1-pad3_gnd_dc 1.8
x1 inl net_x1-pad2_net_x1-pad3_my_inv
c1 outl gnd 10f
x2 net_x1-pad2_outl net_x1-pad3_my_inv
.tran 10e-12 4e-09 0e-00
* Control Statements
.control
run

.model CMOS NMOS (LEVEL=8 VERSION=3.2 TNOM=27 TOX=4.1E-9 XJ=1E-7 NCH=2.3549E17 VTH0=0.3823463 K1=0.5810697
K2=4.774618E-3 K3=0.0431669 K3B=1.14983E6 W0=1E-7 NLX=1.910552E-7 DVT0W=0 DVT1W=0 DVT2W=0
D1T0=1.2894824 DVT1=0.3622063 DVT2=0.013729 UI=280.633249 IA=-1.208537E-9 UB=2.158625E-18
UC=5.342807E-11 VSAT=9.366802E4 A0=1.593146 AGS=0.3939741 BO=-6.413949E-9 BI=-1E-7 KETA=-5.180424E-4
A1=0.12E-1 RD5W=195.5517558 PRWG=0.1998781 WR=1 WINT=7.984732E-10 LINT=1.571424E-8 XL=0
XW=-1E-8 DWG=1.297221E-9 DWB=1.4794E-9 VOFF=-0.0955434 NFACTOR=2.4358891 CIT=0 CDS=2.4E-4 CDS0=0
CD5CB=0 ETA=0.104851E-3 ETAB=2.5121384E-5 DSUB=0.0167075 PCLM=0.8073191 PDIBLC1=0.166161 PDIBLC2=3.112892E-3
PDIBLCB=0.1 DROUT=0.7875618 PSCE=0.181053CE-9 213635E-10 PVAG=3.85243E-3 DELTA=0.01 RSH=6.7 MOBNOD=1
PRT=0 UTE=-1.5 KTI=0 KT2=0.622 UAI=4.31E-9 UBI=-7.61E-18 UCI=-5.6E-11 AT=3.3E4 WL=0 WLN=1
WW=0 WWL=1 WNL=0 LL=0 LLN=1 LW=0 LWN=1 CAPMOD=2 XPART=0.5 CGD=7.08E-10 CGS=7.08E-10 CGBO=1E-12
CJ=9.68858E-4 PB=0.8 M=0.38E4582 CJ5W=2.512138E-10 PBSW=0.809284 MJSW=0.1066414 CJ5WG=3.3E-10 PBSW=0.809286
MJ5WG=0.1066414 CF=0 PVTH0=0.192722E-3 PROSW=5 PK2=6.450505E-5 WKETA=-4.27294E-4 LKETA=-0.0104078
PU=6.3268729 PUA=2.226552E-11 PUB=0 PVSAT=969.1480157 PETA0=1E-4 PKETA=-1.049509E-3)

.model CMOSP PMOS (LEVEL=8 VERSION=3.2 TNOM=4.1E-9 XJ=1E-7 NCH=4.1589E17 VTH0=0.3938813 K1=0.5479015
K2=0.3606586 K3=0.0993095 K3B=1.798622 W0=1E-6 NLX=1.313191E-7 DVT0W=0 DVT1W=0 DVT2W=0
DVT1=0.2227356 DVT2=0.1 U=115.6852975 UA=1.505832E-9 UB=1E-7 UC=1E-10 VSAT=1.329694E5 A0=1.7596478
AGS=0.3641621 B0=3.427126E-7 B1=1.062928E-9 KETA=0.0134667 A1=0.6859506 A2=0.35667788 RDSW=168.5705677
PRWG=0.4987371 WR=1 WINT=0.028832E-8 XL=0 XW=-1E-8 DWG=-2.349633E-9 OWB=-7.152486E-9
VOFF=-0.0994037 NFACTOR=1.9424315 CIT=0 CDS=2.4E-4 CDS0=0 CD5CB=0 ETA=0.0608072 ETAB=-0.0426148
DSUB=0.7343015 PCLM=3.2579974 PDIBLC1=7.229527E-6 PDIBLC2=0.02538E-6 PDIBLCB=1E-3 DROUT=0 PSCE=1.45478E10
PSCE=2.4292027E-9 PVAG=15 DELTA=0.01 RSH=7.8 MOBNOD=1 PRT=0 UTE=-1.5 KTI=0.11 KT1L=0 KT2=0.022 UAI=4.31E-9
CGD=6.32E-10 CGS=6.32E-10 CGBO=1E-12 CJ=1.172138E-3 PB=0.8421173 MJ=0.4109788 CJ5W=2.242669E-10 PBSW=0.8
MJ5W=0.3752089 CJ5WG=4.22E-10 PBSW=0.8 MJ5WG=0.3752089 CF=0 PVTH0=1.888482E-3 PROSW=11.5315407 PK2=1.559399E-3
WKETA=0.0319301 LKETA=2.955547E-3 PU=0.11065313 PUA=4.62102E-11 PUB=1E-21 PVSAT=50 PETA0=1E-4 PKETA=-4.346368E-3)

```

Steps of the characterization flow, Steps 1 to 8

Characterization

Flow

```

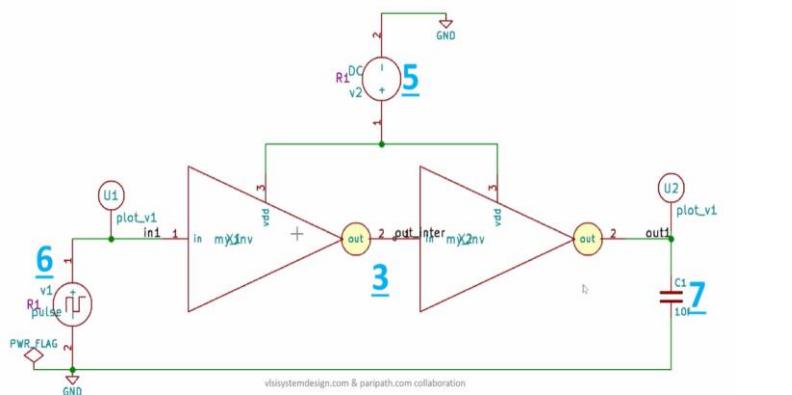
include my_inv.sub
v1 inl my_inv.v 1.8 0 10p 10p in 2n
* u1 inl plot_v1
* u2 outl plot_v1
x1 inl net_x1-pad3_gnd_dc 1.8
x1 inl net_x1-pad2_net_x1-pad3_my_inv
c1 outl gnd 10f
x2 net_x1-pad2_outl net_x1-pad3_my_inv
.xtran 10e-12 4e-09 0e-00
* Control Statements
.control
run

```

```

.model CMOS NMOS (LEVEL=8 VERSION=3.2 TNOM=27 TOX=4.7e-9 Xj=1e-7 NCh=2.3549E17 VTH0=0.3823463 K1=0.5810697
K2=4.774618E-3 K3=0.0431669 K3B=1.498376 W0=1e-7 NLX=1.910552E-7 DVT0W=0 DVT1W=0 DVT2W=0
D/T0=1.2894824 DVT1=0.3622063 DVT2=0.0 13729 U0=280.633249 UA=-1.208537E-9 UB=2.158625E-18
UC=5.342807E-11 VSAT=9.366802E4 A0=1.593146 AGS=3939741 B0=-6.413949E-9 Bl=-1e-7 KETA=-5.180424E-4
A1=0 A2=1 RDSTW=105.5517558 PRWG=0.5 RWB=-0.1998871 WR=1 WINT=7.904732E-10 LINT=1.571424E-8 XL=0
XW=-1E-8 DWG=1.97221E-9 DWB=1.47941E-9 CDS=2.4358891 CIT=0.4538891 CDS2C=2.4E-4 CDS0D=0
CDSCB=0.1 DROUT=0.8775510 PSCBE=0.213635E-9 PVAG=3.85243E-3 DELTA=0.01 RSH=6.7 MOBW=0.112892E-3
PRT=0 UTE=-1.5 KT1=0.11 KT2=0.022 UA1=4.31E-9 UB1=-7.61E-18 UC1=-5.6E-11 AT=3.3E4 WL=0 CGSD=7.08E-10 CGBO=1E-12
Ww=0 WWN=1 Wwl=0 LL=0 LLN=1 LW=0 LN=1 LWL=0 CAPMOD=2 XPART=0.5 CGD=0.32E-10 CGSO=0.32E-10 CGBO=1E-12 Cj=1.172138E-3 PB=0.8421173 Mj=0.4109788 CJSw=2.242609E-10 PBSW=0.8
MJSW=0.3752089 CJSSW=4.22E-10 PBSW=0.8 MJSW=0.3752089 CF=0 PVTH0=1.888482E-3 PRDSW=11.5315407 PK2=1.559399E-3
WKETA=0.0319301 LKETA=2.955547E-3 PU0=1.1105313 PU1=4.62162E-11 PUB=1E-21 PVSAT=50 PETAO=IE-4 PKETA=-4.346368E-3
PU0=6.3268729 PU1=2.265527E-11 PUB=0 PVSAT=969.1480157 PETAO=IE-4 PKETA=-1.049599E-3)

```



Characterization

Flow

```

include my_inv.sub
v1 inl my_inv.v 1.8 0 10p 10p in 2n
* u1 inl plot_v1
* u2 outl plot_v1
x1 inl net_x1-pad3_gnd_dc 1.8
x1 inl net_x1-pad2_net_x1-pad3_my_inv
c1 outl gnd 10f
x2 net_x1-pad2_outl net_x1-pad3_my_inv
.xtran 10e-12 4e-09 0e-00
* Control Statements
.control
run

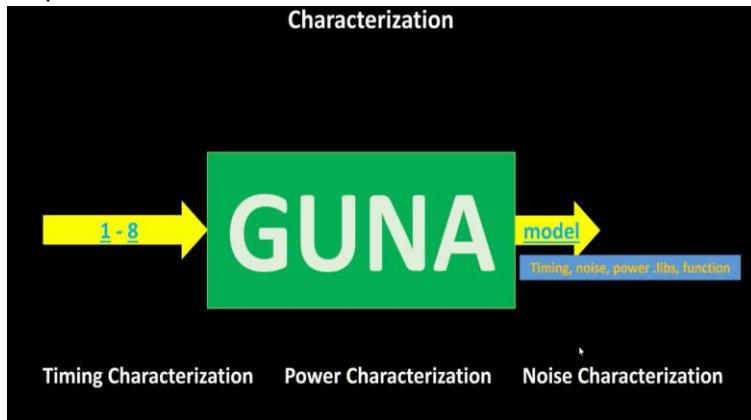
```

```

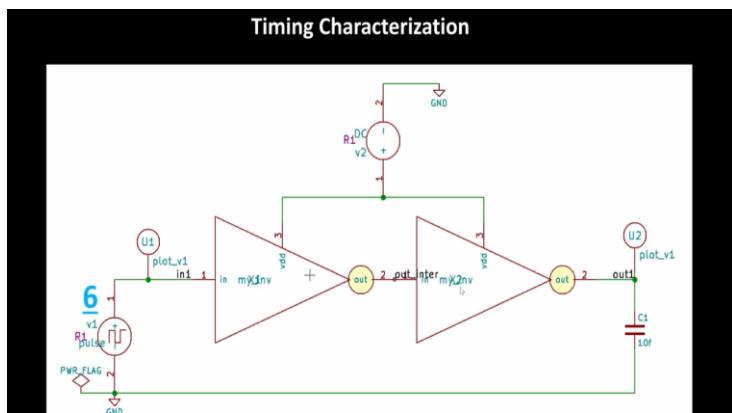
.model CMOS NMOS (LEVEL=8 VERSION=3.2 TNOM=27 TOX=4.7e-9 Xj=1e-7 NCh=2.3549E17 VTH0=0.3823463 K1=0.5810697
K2=4.774618E-3 K3=0.0431669 K3B=1.498376 W0=1e-7 NLX=1.910552E-7 DVT0W=0 DVT1W=0 DVT2W=0
D/T0=1.2894824 DVT1=0.3622063 DVT2=0.0 13729 U0=280.633249 UA=-1.208537E-9 UB=2.158625E-18
UC=5.342807E-11 VSAT=9.366802E4 A0=1.593146 AGS=3939741 B0=-6.413949E-9 Bl=-1e-7 KETA=-5.180424E-4
A1=0 A2=1 RDSTW=105.5517558 PRWG=0.5 RWB=-0.1998871 WR=1 WINT=7.904732E-10 LINT=1.571424E-8 XL=0
XW=-1E-8 DWG=1.97221E-9 DWB=1.47941E-9 CDS=2.4358891 CIT=0.4538891 CDS2C=2.4E-4 CDS0D=0
CDSCB=0.1 DROUT=0.8775510 PSCBE=0.213635E-9 PVAG=3.85243E-3 DELTA=0.01 RSH=6.7 MOBW=0.112892E-3
PRT=0 UTE=-1.5 KT1=0.11 KT2=0.022 UA1=4.31E-9 UB1=-7.61E-18 UC1=-5.6E-11 AT=3.3E4 WL=0 CGSD=7.08E-10 CGBO=1E-12
Ww=0 WWN=1 Wwl=0 LL=0 LLN=1 LW=0 LN=1 LWL=0 CAPMOD=2 XPART=0.5 CGD=0.32E-10 CGSO=0.32E-10 CGBO=1E-12 Cj=1.172138E-3 PB=0.8421173 Mj=0.4109788 CJSw=2.242609E-10 PBSW=0.8
MJSW=0.3752089 CJSSW=4.22E-10 PBSW=0.8 MJSW=0.3752089 CF=0 PVTH0=1.888482E-3 PRDSW=11.5315407 PK2=1.559399E-3
WKETA=0.0319301 LKETA=2.955547E-3 PU0=1.1105313 PU1=4.62162E-11 PUB=1E-21 PVSAT=50 PETAO=IE-4 PKETA=-4.346368E-3
PU0=6.3268729 PU1=2.265527E-11 PUB=0 PVSAT=969.1480157 PETAO=IE-4 PKETA=-1.049599E-3)

```

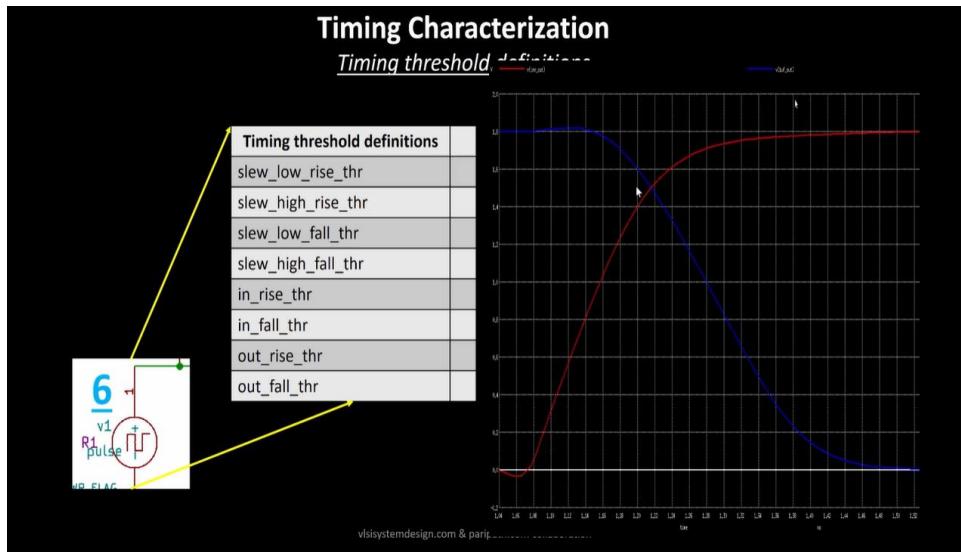
Steps 1 to 8 are feed into a tool called GUNA



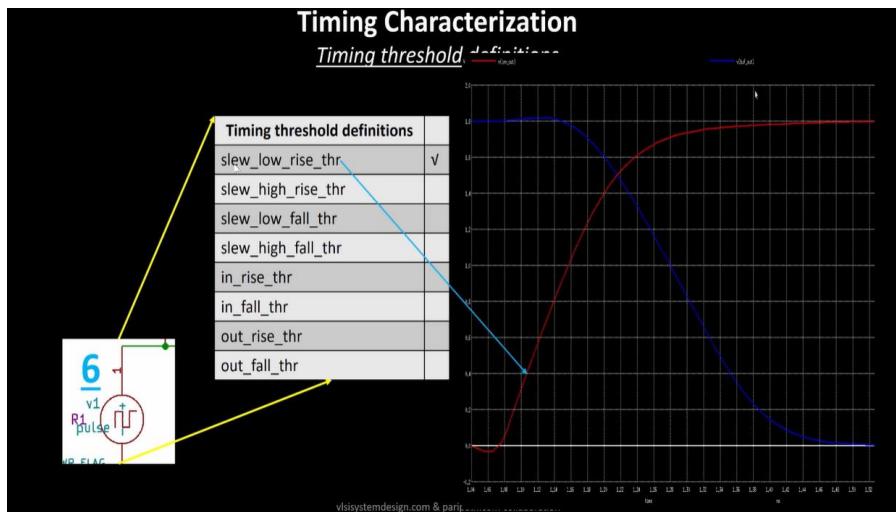
SKY130_D2_SK4 - General timing characterization parameters



Variables related to any waveform seen and the input and output of the 2 invertors and the buffer output



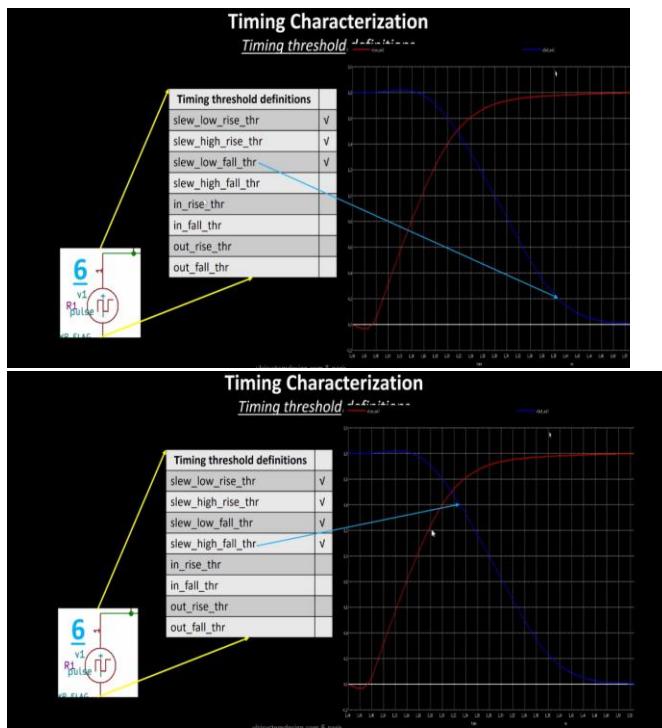
Slew low rise threshold is the lower 20 % or 30 % of the bottom of the power supply as shown in the figure below



Slew high rise threshold is 20% from top of the power supply .

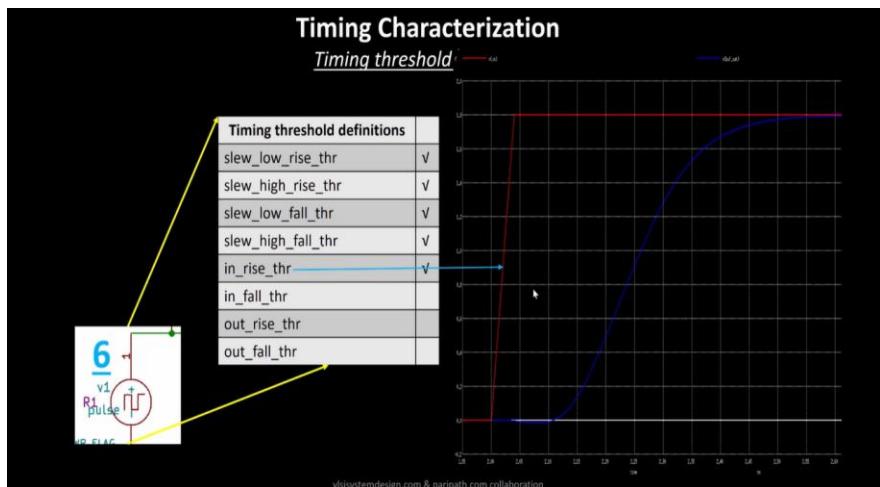
Slew rise of the waveform is calculated as the time difference between slew low rise threshold and slew high rise threshold.

Similarly the Slew fall of the waveform is calculated as the time difference between slew low fall threshold and slew high fall threshold.

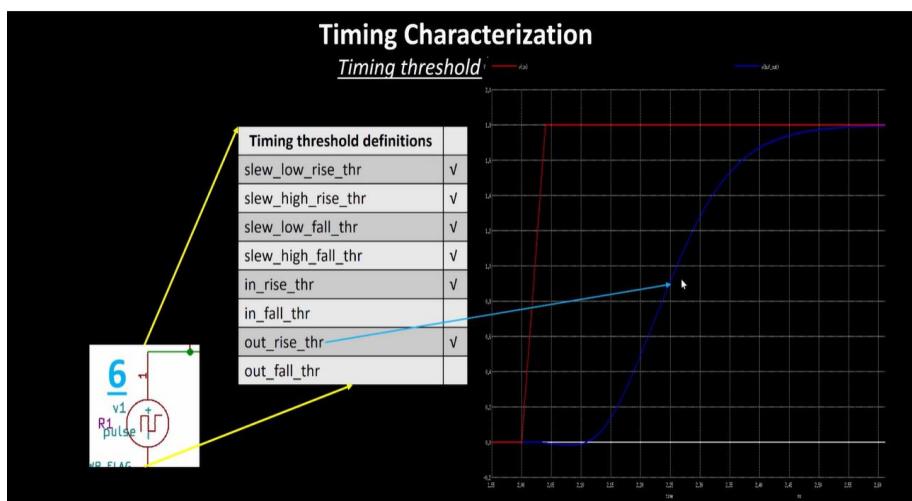


Delay of the particular inverter

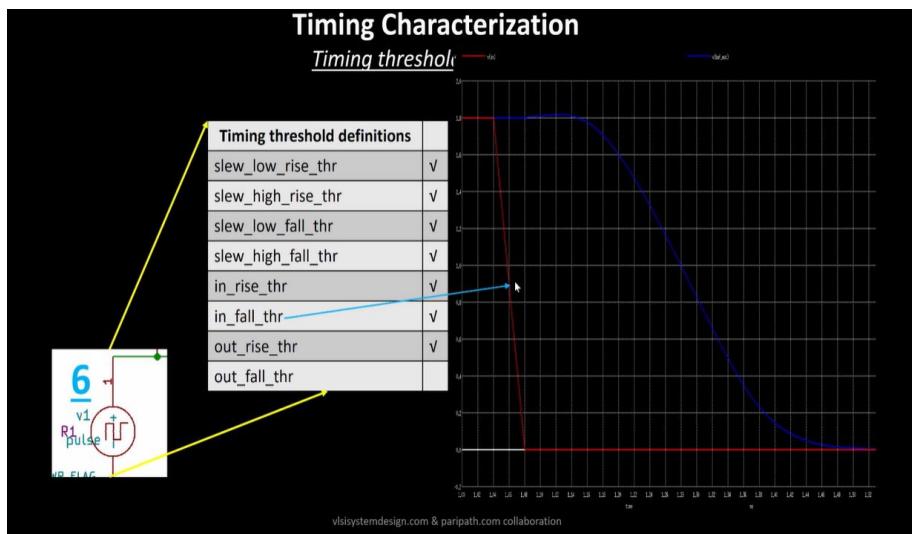
In_rise_threshold - 50% of the rise of the input waveform

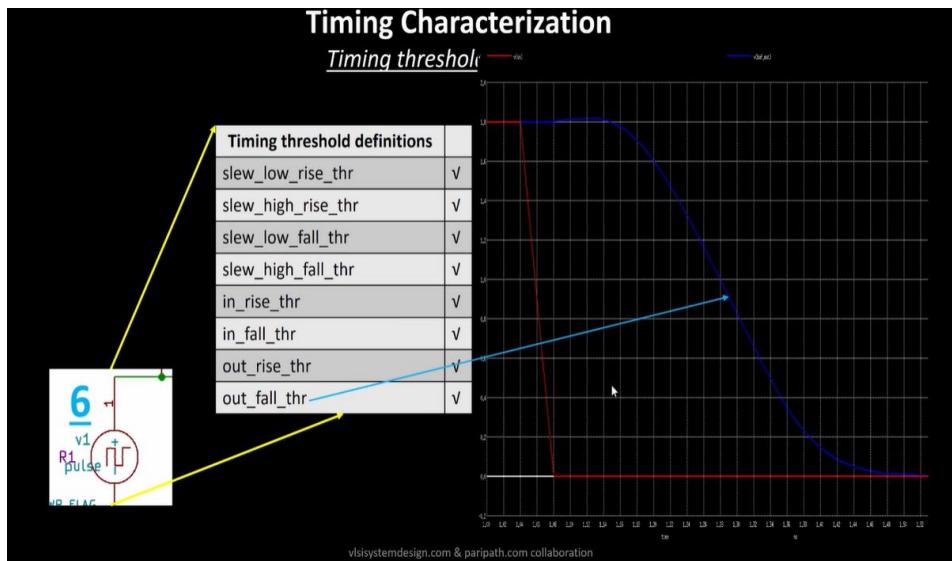


out_rise_threshold - 50% of the rise of the output waveform

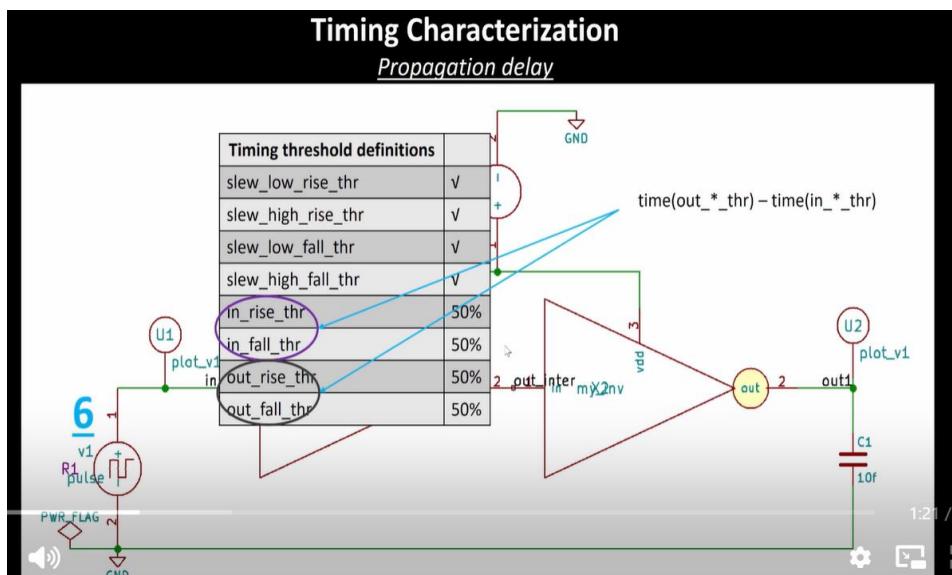


Similarly for the fall threshold – 50%

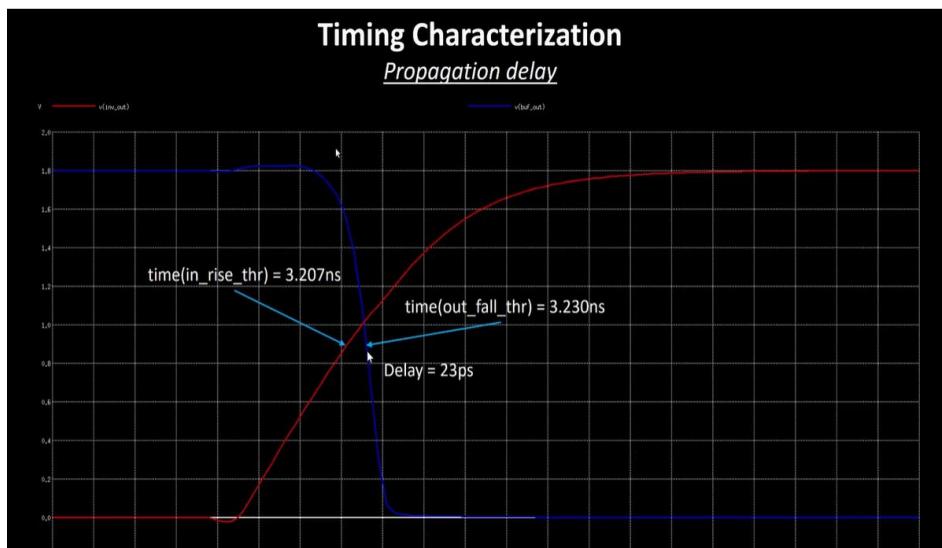




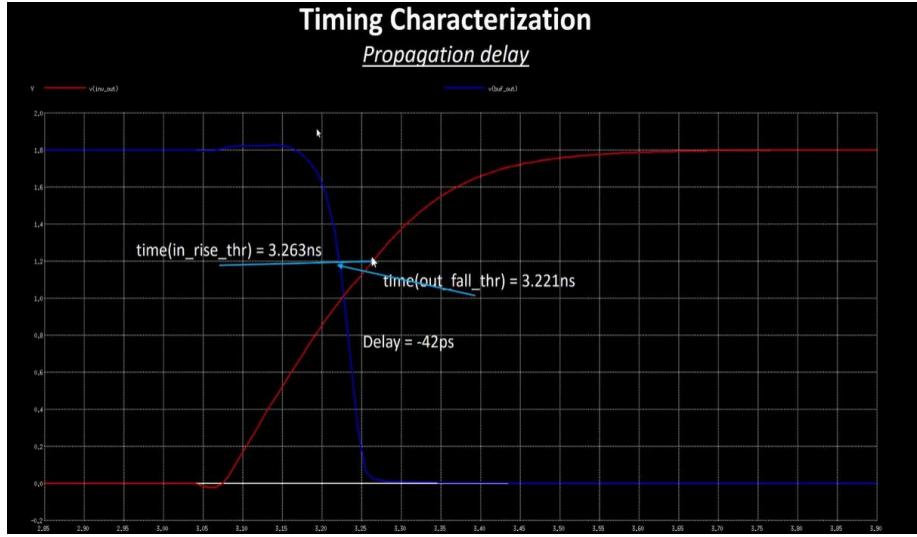
Propogation Delay - Out – In thresholds.



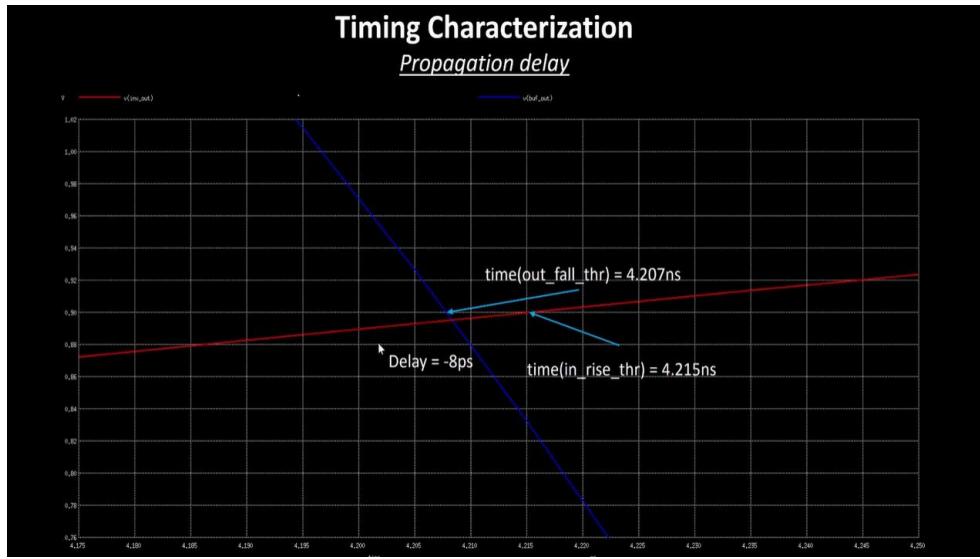
Calculation of the thresholds



If there is movement of the thresholds, it causes a negative value – Output comes before the input which is not correct and only positive delays are expected. This results due to poor choice of threshold points.



If the 2 invertors are very far from each other, it cause the above issue as seen in the waveforms below



Transition time

Time difference between the slew high rise and slew low rise thresholds

And also the difference between slew high fall and slew low fall thresholds.

Timing Characterization

Transition time

Timing threshold definitions	
slew_low_rise_thr	✓
slew_high_rise_thr	✓
slew_low_fall_thr	✓
slew_high_fall_thr	✓
in_rise_thr	50%
in_fall_thr	50%
out_rise_thr	50%
out_fall_thr	50%

time(slew_high_rise_thr) – time(slew_low_rise_thr)

Timing Characterization

Transition time

Timing threshold definitions	
slew_low_rise_thr	✓
slew_high_rise_thr	✓
slew_low_fall_thr	✓
slew_high_fall_thr	✓
in_rise_thr	50%
in_fall_thr	50%
out_rise_thr	50%
out_fall_thr	50%

time(slew_high_fall_thr) – time(slew_low_fall_thr)

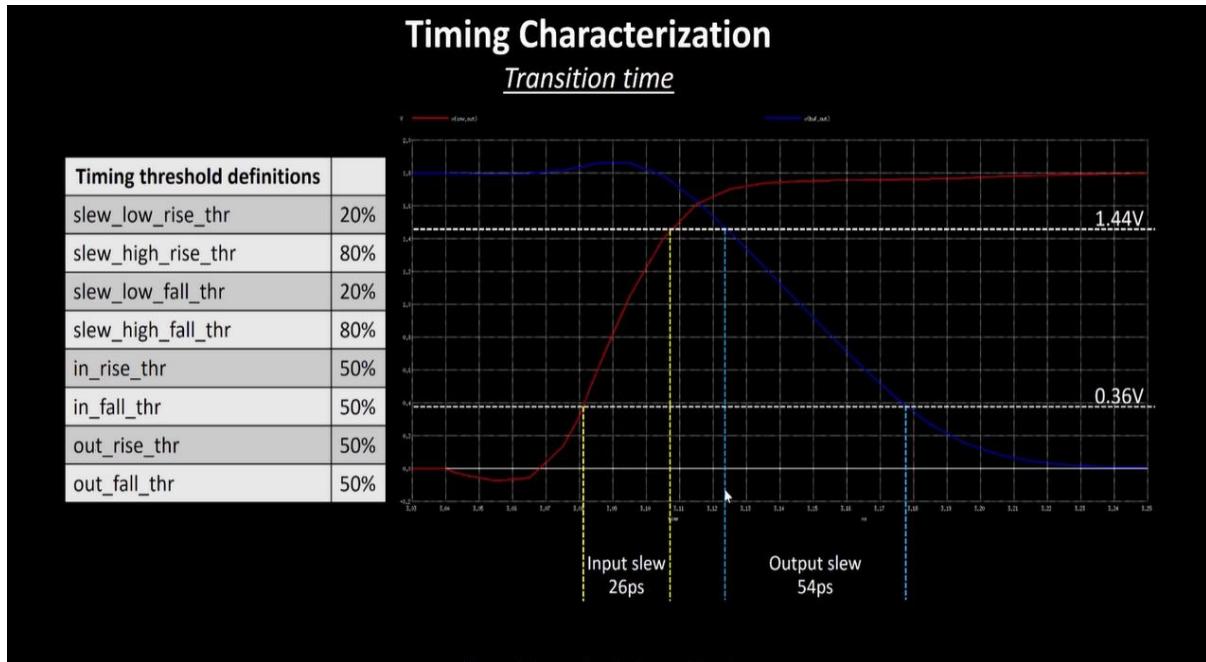
5.06

Timing Characterization

Transition time

Timing threshold definitions	
slew_low_rise_thr	20%
slew_high_rise_thr	80%
slew_low_fall_thr	20%
slew_high_fall_thr	80%
in_rise_thr	50%
in_fall_thr	50%
out_rise_thr	50%
out_fall_thr	50%

Transitions are calculated as given in the below example



LABS –

Floorplan labs – (SKY130_D2_SK1 - Chip Floor planning considerations SKY_L6 - Steps to run floorplan using OpenLANE, SKY130_D2_SK1 - Chip Floor planning considerations SKY_L7 - Review floorplan files and steps to view floorplan, SKY130_D2_SK1 - Chip Floor planning considerations SKY_L8 - Review floorplan layout in Magic)

```

Activities Terminal ▾
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/configuration
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane × vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlan...
Variable | Description
| 'FP_CORE_UTIL' | The core utilization percentage. <br> (Default: '50' percent)
| 'FP_ASPECT_RATIO' | The core's aspect ratio (height / width). <br> (Default: '1')
| 'FP_SIZING' | Whether to use relative sizing by making use of 'FP_CORE_UTIL' or absolute one using 'DIE_AREA'. <br> (Default: "relative" - accepts "absolute" as well)
| 'DIE_AREA' | Specific die area to be used in floorplanning. Specified as a 4-corner rectangle. Units in mm <br> (Default: unset)
| 'FP_IO_HMETAL' | The metal layer on which to place the io pins horizontally (top and bottom of the die). <br> (Default: '4')
| 'FP_IO_VMETAL' | The metal layer on which to place the io pins vertically (sides of the die) <br> (Default: '3')
| 'FP_IO_MODE' | Decides the mode of the random IO placement option. 0=matching mode, 1=random equidistant mode <br> (Default: '1')
| 'FP_WELLTAP_CELL' | The name of the welltap cell during welltap insertion. |
| 'FP_ENDCAP_CELL' | The name of the endcap cell during endcap insertion. |
| 'FP_PDN_VOFFSET' | The offset of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: '16.32') |
| 'FP_PDN_VPITCH' | The pitch of the vertical power stripes on the metal layer 4 in the power distribution network <br> (Default: '1 53.6') |
| 'FP_PDN_HOFFSET' | The offset of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '16.65') |
| 'FP_PDN_HPITCH' | The pitch of the horizontal power stripes on the metal layer 5 in the power distribution network <br> (Default: '153.18') |
| 'FP_PDN_AUTO_ADJUST' | Decides whether or not the flow should attempt to re-adjust the power grid, in order for it to fit inside the core area of the design, if needed. <br> 1=enabled, 0 =disabled (Default: '1') |
| 'FP_TAPCELL_DIST' | The horizontal distance between two tapcell columns <br> (Default: '14') |
| 'FP_IO_VEXTEND' | Extends the vertical to pins outside of the die by the specified units:<br> (Default: '-1' Disabled) |
| 'FP_IO_HEXTEND' | Extends the horizontal to pins outside of the die by the specified units:<br> (Default: '-1' Disabled) |
| 'FP_IO_VLENGTH' | The length of the vertical IOs in microns. <br> (Default: '4') |
| 'FP_IO_HLENGTH' | The length of the horizontal IOs in microns. <br> (Default: '4') |
| 'FP_IO_VTHICKNESS_MULT' | A multiplier for vertical pin thickness. Base thickness is the pins layer minwidth <br> (Default: '2') |
| 'FP_IO_HTHICKNESS_MULT' | A multiplier for horizontal pin thickness. Base thickness is the pins layer minwidth <br> (Default: '2') |
| 'BOTTOM_MARGIN_MULT' | The core margin, in multiples of site heights, from the bottom boundary. <br> (Default: '4') |
| 'TOP_MARGIN_MULT' | The core margin, in multiples of site heights, from the top boundary. <br> (Default: '4') |
| 'LEFT_MARGIN_MULT' | The core margin, in multiples of site widths, from the left boundary. <br> (Default: '12') |
| 'RIGHT_MARGIN_MULT' | The core margin, in multiples of site widths, from the right boundary. <br> (Default: '12') |
| 'FP_PDN_CORE_RING' | Enables adding a core ring around the design. More details on the control variables in the pdk configurations

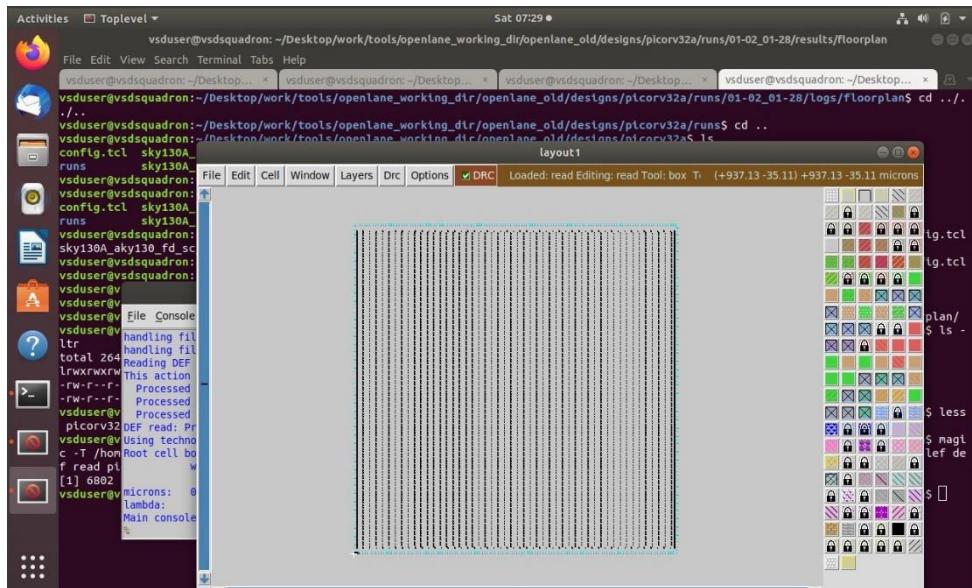
```

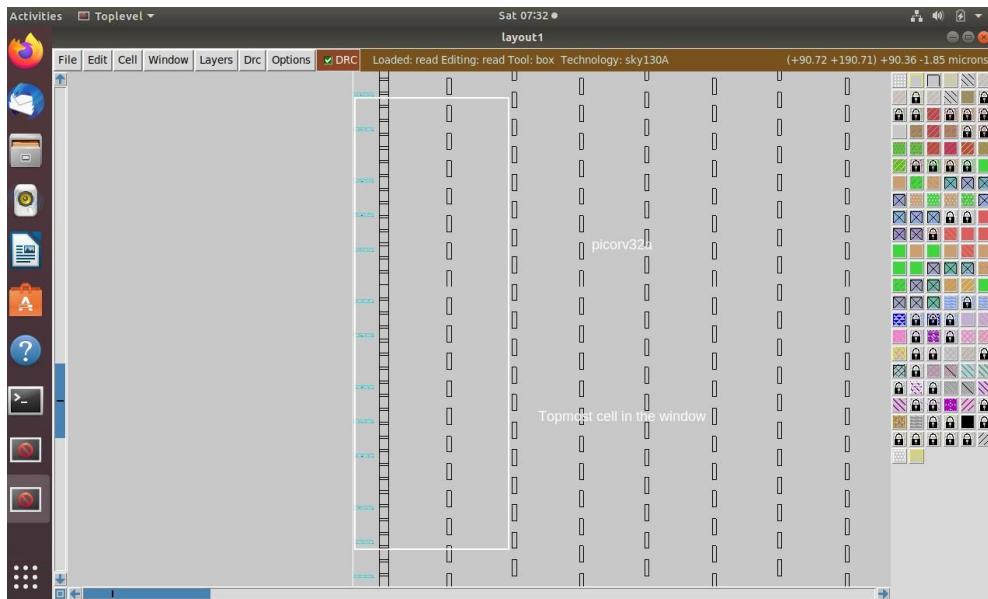
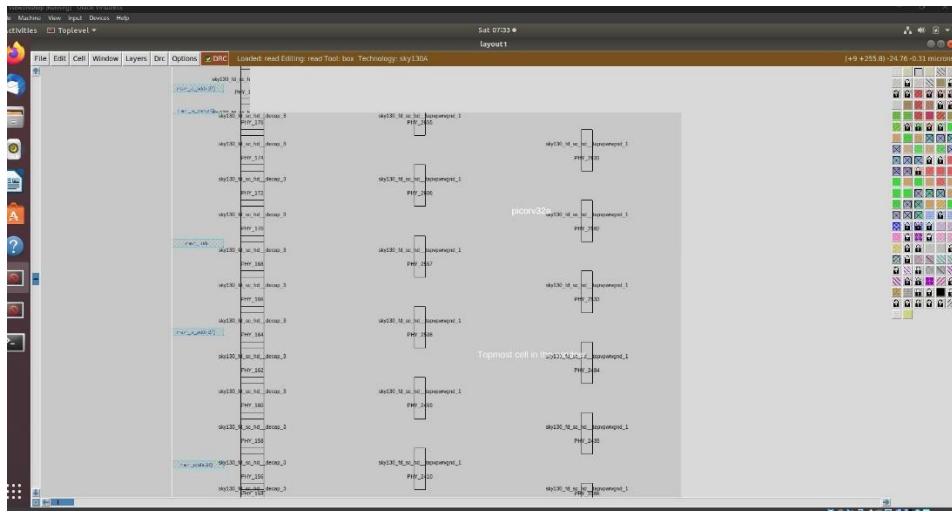
Fri 21:56 •

```
vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
File Edit View Search Terminal Tabs Help
[WARNING PSM-0030] Vsrc location at (565.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (705.520um, 10.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 103.880um).
[WARNING PSM-0030] Vsrc location at (285.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 103.880um).
[WARNING PSM-0030] Vsrc location at (425.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 103.880um).
[WARNING PSM-0030] Vsrc location at (705.520um, 150.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 103.880um).
[WARNING PSM-0030] Vsrc location at (565.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 257.060um).
[WARNING PSM-0030] Vsrc location at (705.520um, 290.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 257.060um).
[WARNING PSM-0030] Vsrc location at (5.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (5.400um, 410.240um).
[WARNING PSM-0030] Vsrc location at (145.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (145.800um, 410.240um).
[WARNING PSM-0030] Vsrc location at (285.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (286.200um, 410.240um).
[WARNING PSM-0030] Vsrc location at (425.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (426.600um, 410.240um).
[WARNING PSM-0030] Vsrc location at (565.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (567.000um, 410.240um).
[WARNING PSM-0030] Vsrc location at (705.520um, 430.880um) and size =10.000um, is not located on a power stripe. Moving to closest stripe at (707.400um, 410.240um).
[INFO PSM-0031] Number of nodes on net VGND = 19578.
[INFO PSM-0037] G matrix created successfully.
[INFO PSM-0040] Connection between all PDN nodes established in net VGND.
[INFO]: PDN generation was successful.
[INFO]: Changing layout from /openLANE_flow/designs/picorv32a/runs/31-01_16-24/results/floorplan/picorv32a.floorplan.def to /openLANE_flow/designs/picorv32a/runs/31-01_16-24/tmp/floorplan/7-pdn.def
1 %

```

Screenshots from the VM





Above 3 screenshots are of running the floorplan in magic.