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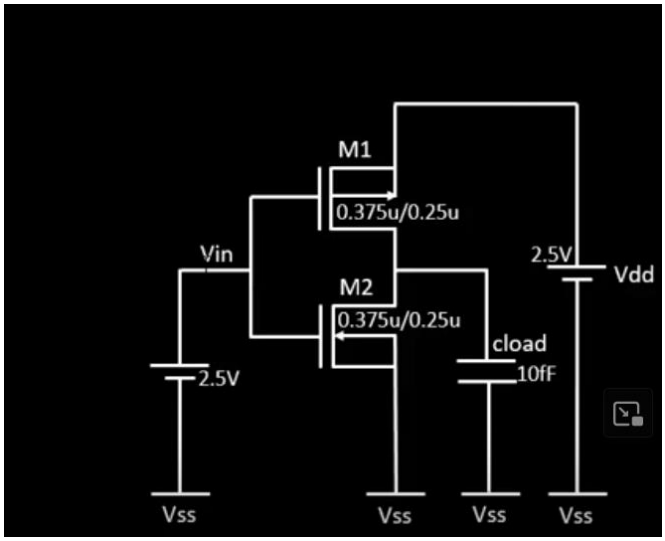
Grade : 8th grade

School : National Public School, Rajajinagar, Bangalore

***All pictures in the below document are taken from the digital chip design course**

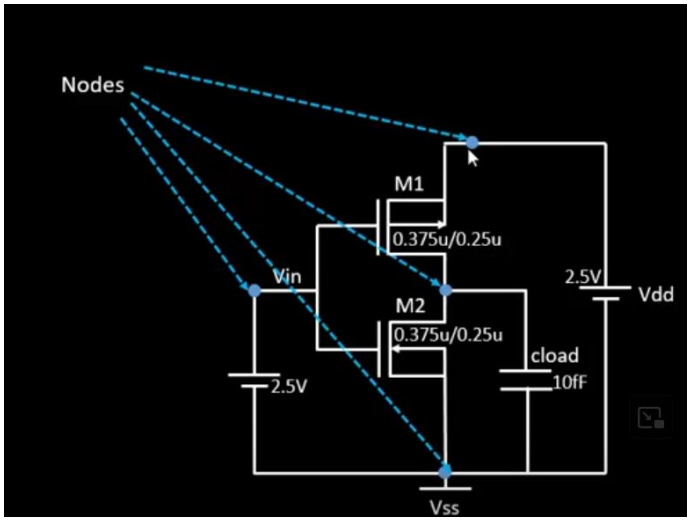
Level 3 Day 3 –

SPICE Deck for CMOS Inverter

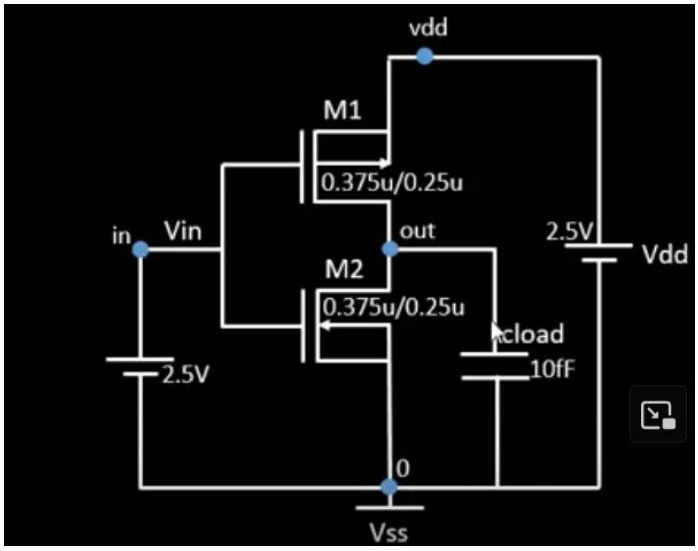


Usually PMOS is 3 times the size of the NMOS.

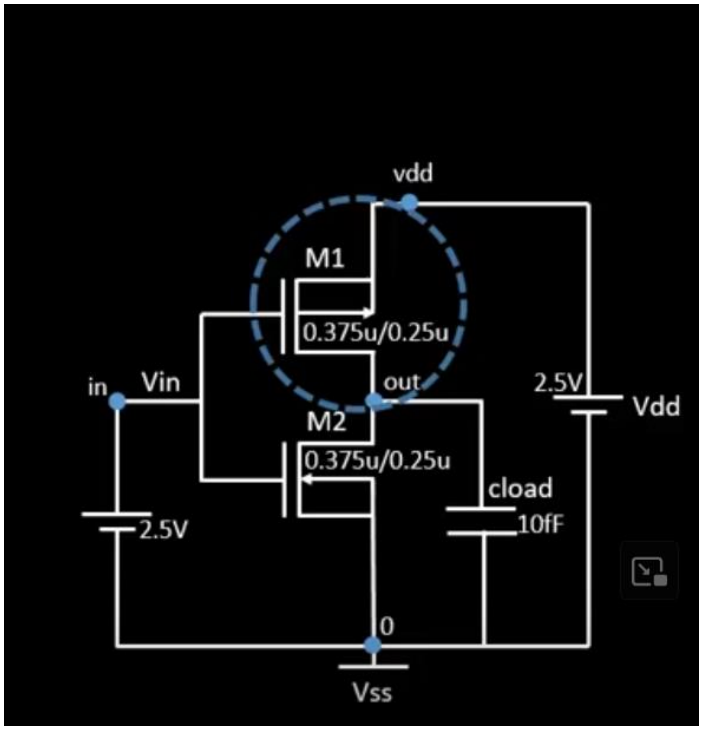
For something to be called a node, there has to be one component between them.



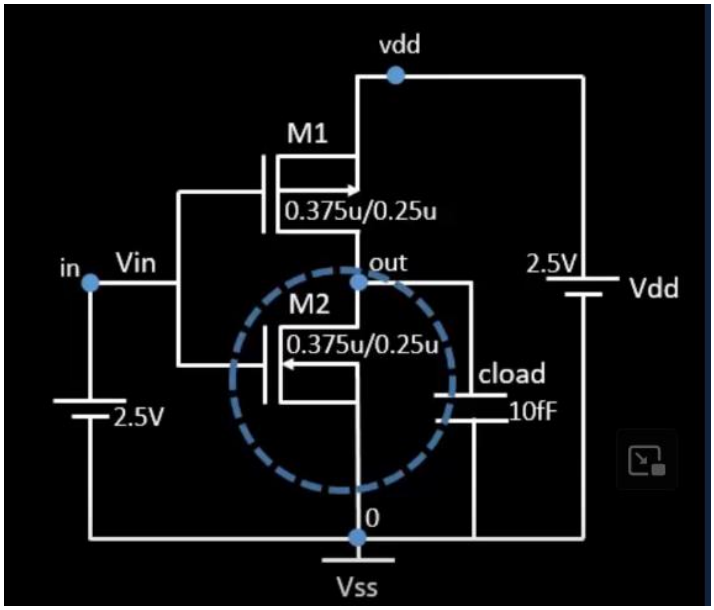
For naming the nodes



Notes –



M1 out in vdd vdd pmos W=0.375u L=0.25u



M2 out in 0 0 nmos W=0.375u L=0.25u

cload out 0 10f

Vdd vdd 0 2,5

Vin in 0 2.5

Simulation Commands –

.op

.dc Vin 0 2.5 0.05

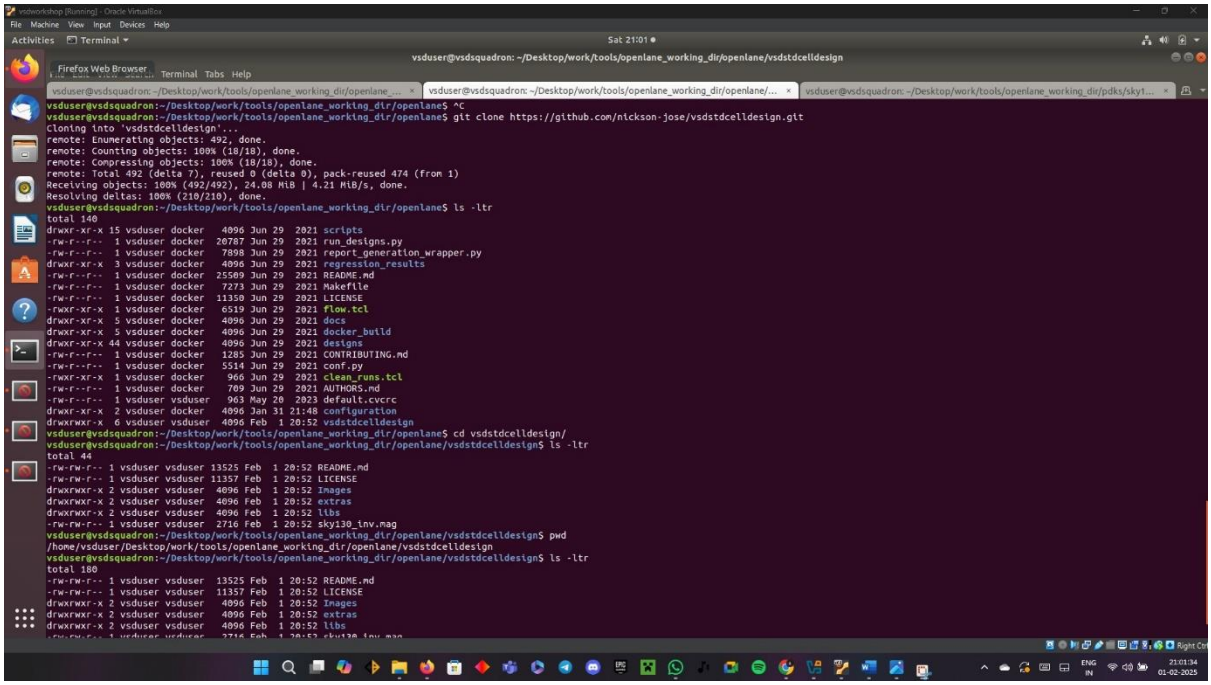
.include tsmc_025um_model.mod –

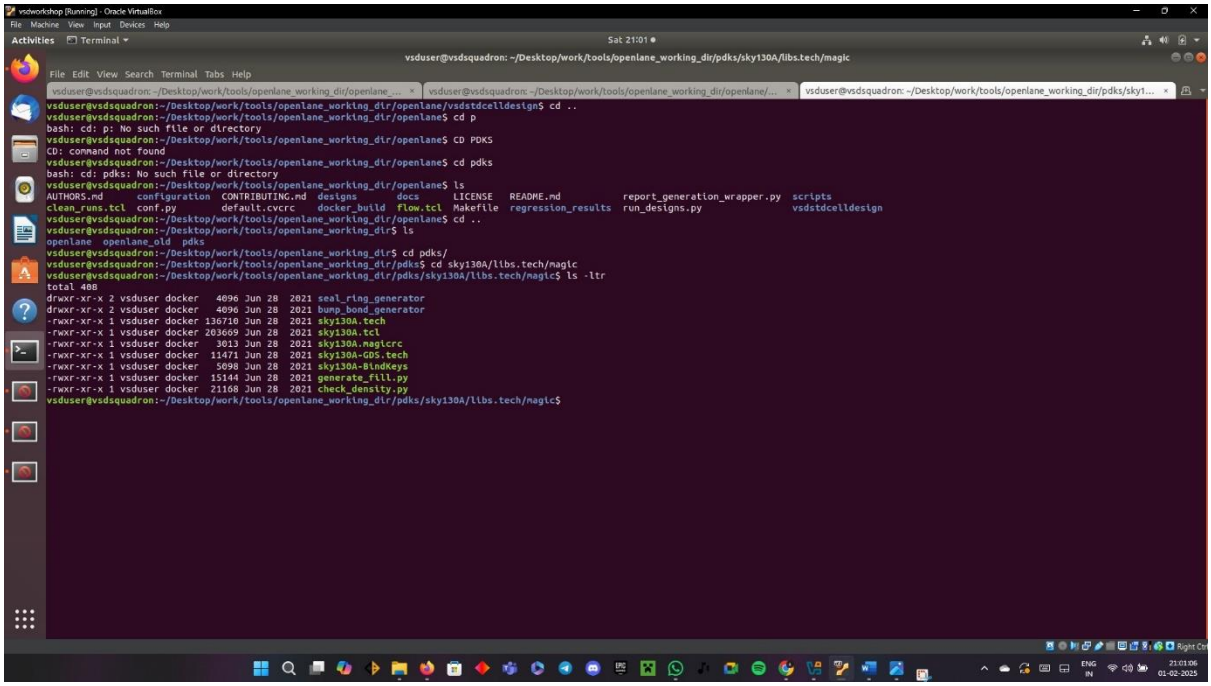
.LIB “tsmc_025um_model.mod” CMOS_MODELS

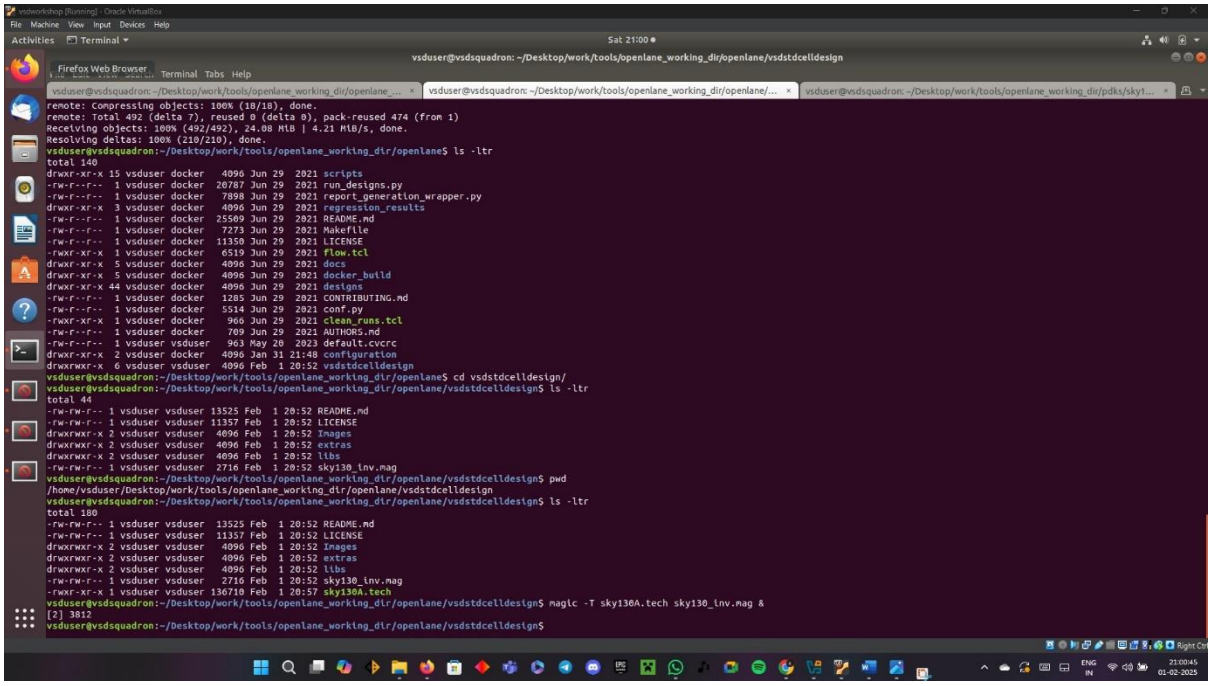
.end

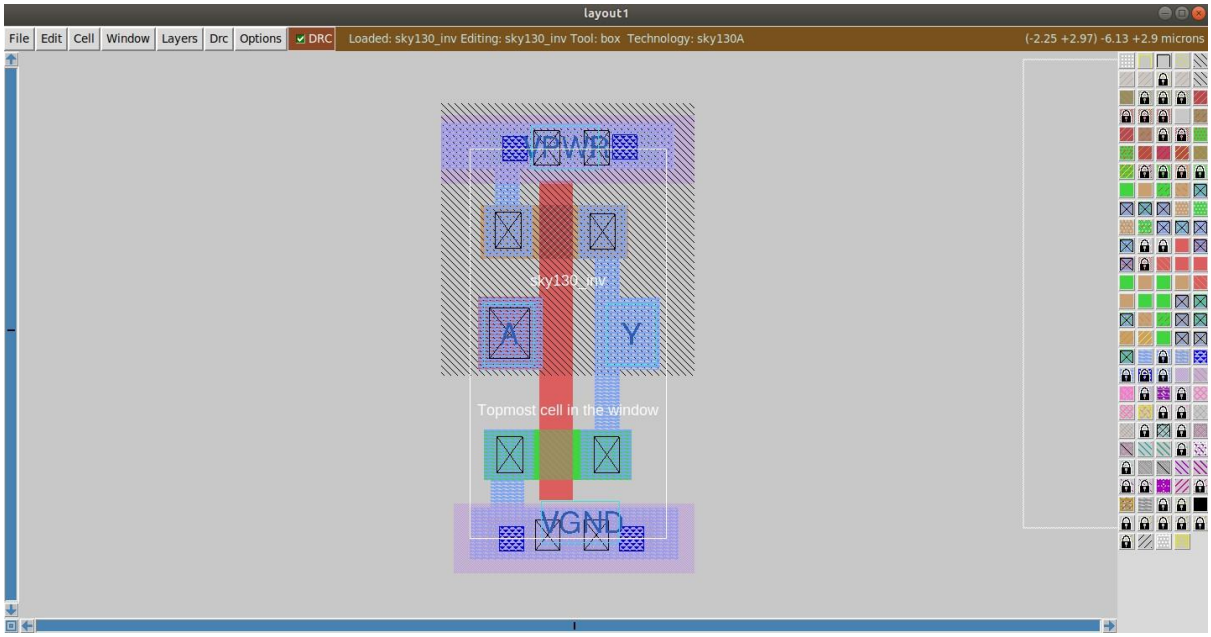
SPICE Waveform : Wn=Wp=0.375u, Ln,p=0.25u device (Wn/Ln=Wp/Lp = 1.5)

Labs –


vsdworkshop [Running] - Oracle VirtualBox
File Machine View Input Devices Help
Activities
Terminal
Sat 21:01
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
Firefox Web Browser
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/...
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/pdks/sky1...
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ^C
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ git clone https://github.com/nickson-jose/vsdstdcelldesign.git
Cloning into 'vsdstdcelldesign'...
remote: Enumerating objects: 492, done.
remote: Counting objects: 100% (18/18), done.
remote: Compressing objects: 100% (18/18), done.
remote: Total 492 (delta 7), reused 0 (delta 0), pack-reused 474 (from 1)
Receiving objects: 100% (492/492), 24.08 MiB | 4.21 MiB/s, done.
Resolving deltas: 100% (210/210), done.
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls -ltr
total 140
drwxr-xr-x 15 vsduser docker   4096 Jun 29 2021 scripts
-rw-r--r-- 1 vsduser docker 20787 Jun 29 2021 run_designs.py
-rw-r--r-- 1 vsduser docker   7898 Jun 29 2021 report_generation_wrapper.py
drwxr-xr-x 3 vsduser docker   4096 Jun 29 2021 regression_results
-rw-r--r-- 1 vsduser docker 25589 Jun 29 2021 README.md
-rw-r--r-- 1 vsduser docker   7273 Jun 29 2021 Makefile
-rw-r--r-- 1 vsduser docker 11350 Jun 29 2021 LICENSE
-rwxr-xr-x 1 vsduser docker   6519 Jun 29 2021 flow.tcl
drwxr-xr-x 5 vsduser docker   4096 Jun 29 2021 docs
drwxr-xr-x 5 vsduser docker   4096 Jun 29 2021 docker_build
drwxr-xr-x 44 vsduser docker   4096 Jun 29 2021 designs
-rw-r--r-- 1 vsduser docker   1285 Jun 29 2021 CONTRIBUTING.md
-rw-r--r-- 1 vsduser docker   5514 Jun 29 2021 conf.py
-rwxr-xr-x 1 vsduser docker   966 Jun 29 2021 clean_runs.tcl
-rw-r--r-- 1 vsduser docker   709 Jun 29 2021 AUTHORS.md
-rw-r--r-- 1 vsduser vsduser   963 May 20 2023 default.cvcrc
drwxr-xr-x 2 vsduser docker   4096 Jan 31 21:48 configuration
drwxrwxr-x 6 vsduser vsduser 4096 Feb 1 20:52 vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd vsdstdcelldesign/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 44
-rw-rw-r-- 1 vsduser vsduser 13525 Feb 1 20:52 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Feb 1 20:52 LICENSE
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 20:52 Images
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 20:52 extras
drwxrwxr-x 2 vsduser vsduser 4096 Feb 1 20:52 libs
-rw-rw-r-- 1 vsduser vsduser 2716 Feb 1 20:52 sky130_inv.mag
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ pwd
/home/vsduser/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 180
-rw-rw-r-- 1 vsduser vsduser 13525 Feb 1 20:52 README.md
-rw-rw-r-- 1 vsduser vsduser 11357 Feb 1 20:52 LICENSE
drwxrwxr-x 2 vsduser vsduser   4096 Feb 1 20:52 Images
drwxrwxr-x 2 vsduser vsduser   4096 Feb 1 20:52 extras
drwxrwxr-x 2 vsduser vsduser   4096 Feb 1 20:52 libs
ENG
IN
21:01:34
01-02-2025

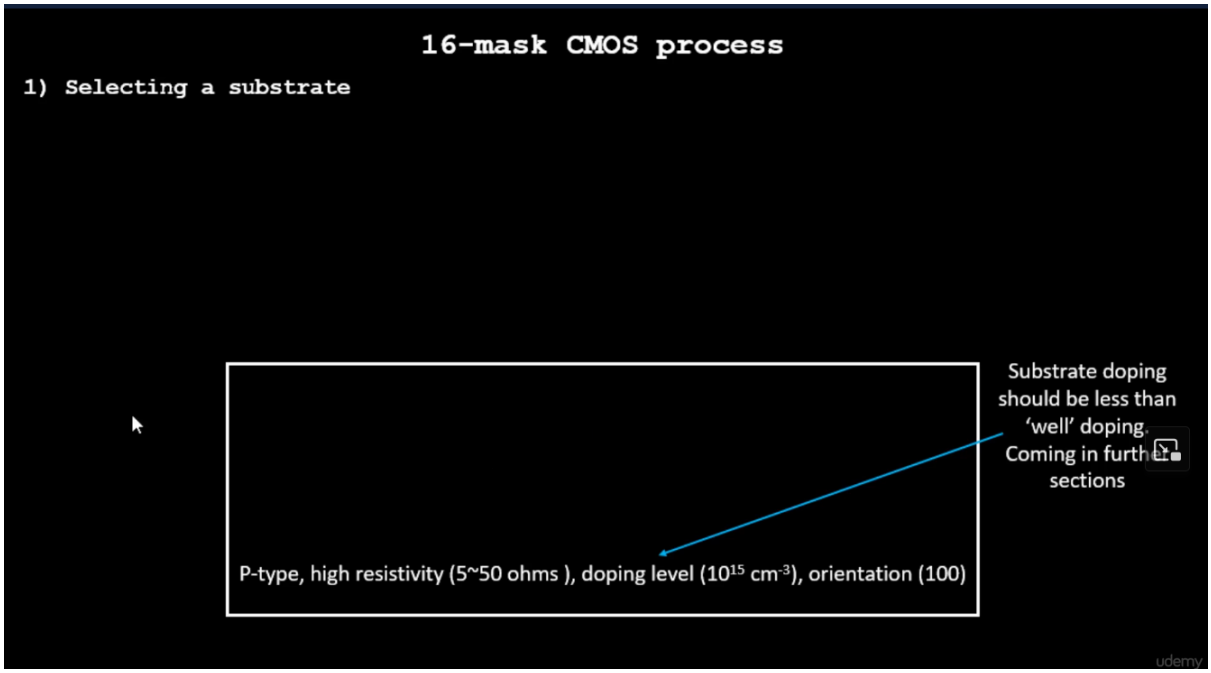

vsdworkshop [Running] - Oracle VirtualBox
File Machine View Input Devices Help
Activities
Terminal
Sat 21:01
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic
File Edit View Search Terminal Tabs Help
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/...
vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/pdks/sky1...
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ cd ..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd p
bash: cd: p: No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ CD PDKS
CD: command not found
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd pdks
bash: cd: pdks: No such file or directory
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ ls
AUTHORS.md   configuration CONTRIBUTING.md designs   docs   LICENSE   README.md   report_generation_wrapper.py scripts
clean_runs.tcl conf.py   default.cvcrc   docker_build flow.tcl Makefile regression_results run_designs.py   vsdstdcelldesign
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane$ cd ..
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ ls
openlane openlane_old pdks
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir$ cd pdks/
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks$ cd sky130A/libs.tech/magic
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$ ls -ltr
total 408
drwxr-xr-x 2 vsduser docker   4096 Jun 28 2021 seal_ring_generator
drwxr-xr-x 2 vsduser docker   4096 Jun 28 2021 bump_bond_generator
-rwxr-xr-x 1 vsduser docker 136710 Jun 28 2021 sky130A.tech
-rwxr-xr-x 1 vsduser docker 203609 Jun 28 2021 sky130A.tcl
-rwxr-xr-x 1 vsduser docker   3013 Jun 28 2021 sky130A.magicrc
-rwxr-xr-x 1 vsduser docker 11471 Jun 28 2021 sky130A-GDS.tech
-rwxr-xr-x 1 vsduser docker   5098 Jun 28 2021 sky130A-BindKeys
-rwxr-xr-x 1 vsduser docker 15144 Jun 28 2021 generate_fill.py
-rwxr-xr-x 1 vsduser docker 21168 Jun 28 2021 check_density.py
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/pdks/sky130A/libs.tech/magic$
ENG
IN
21:01:06
01-02-2025



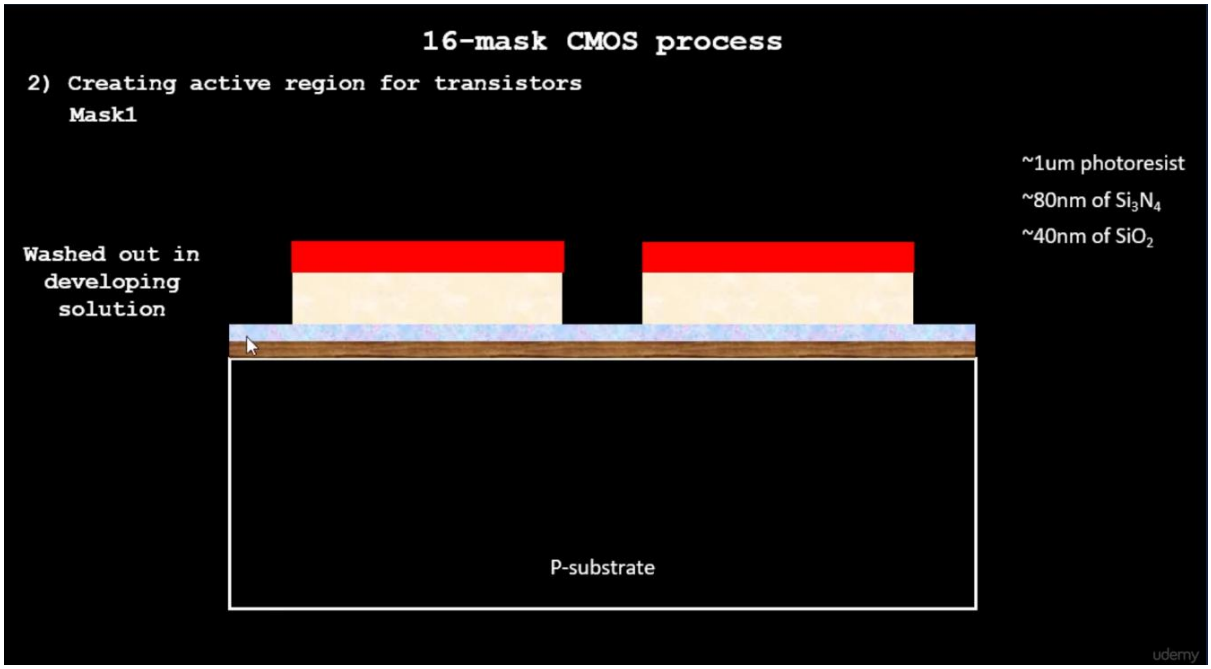


Inception of Layout Â CMOS fabrication process –

Selecting a process



Creating active region for transistors



16-mask CMOS process

2) Creating active region for transistors

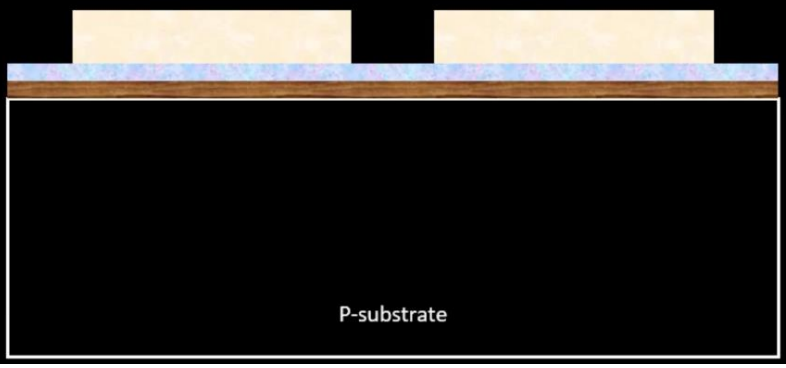
Mask1

~1um photoresist

~80nm of Si_3N_4

~40nm of SiO_2

Washed out in developing solution



16-mask CMOS process

2) Creating active region for transistors

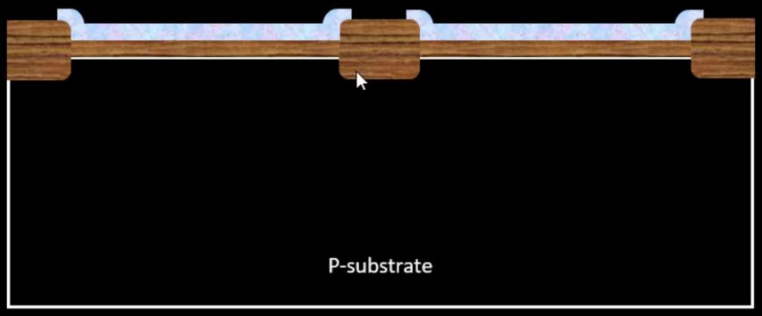
Mask1

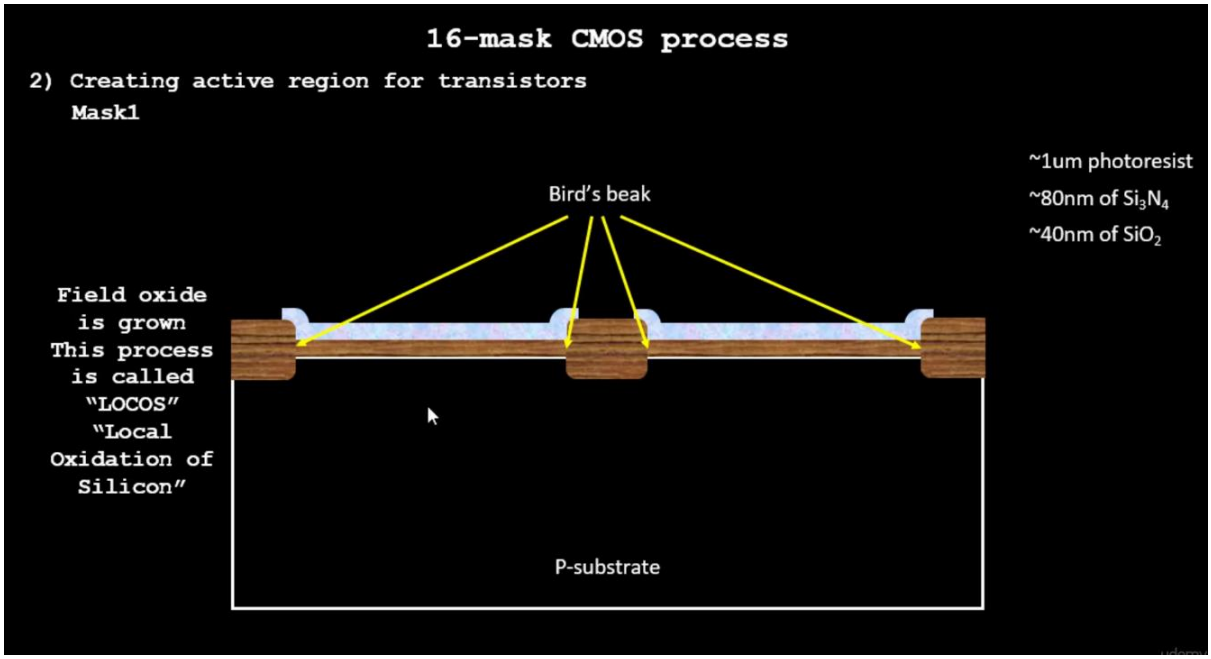
~1um photoresist

~80nm of Si_3N_4

~40nm of SiO_2

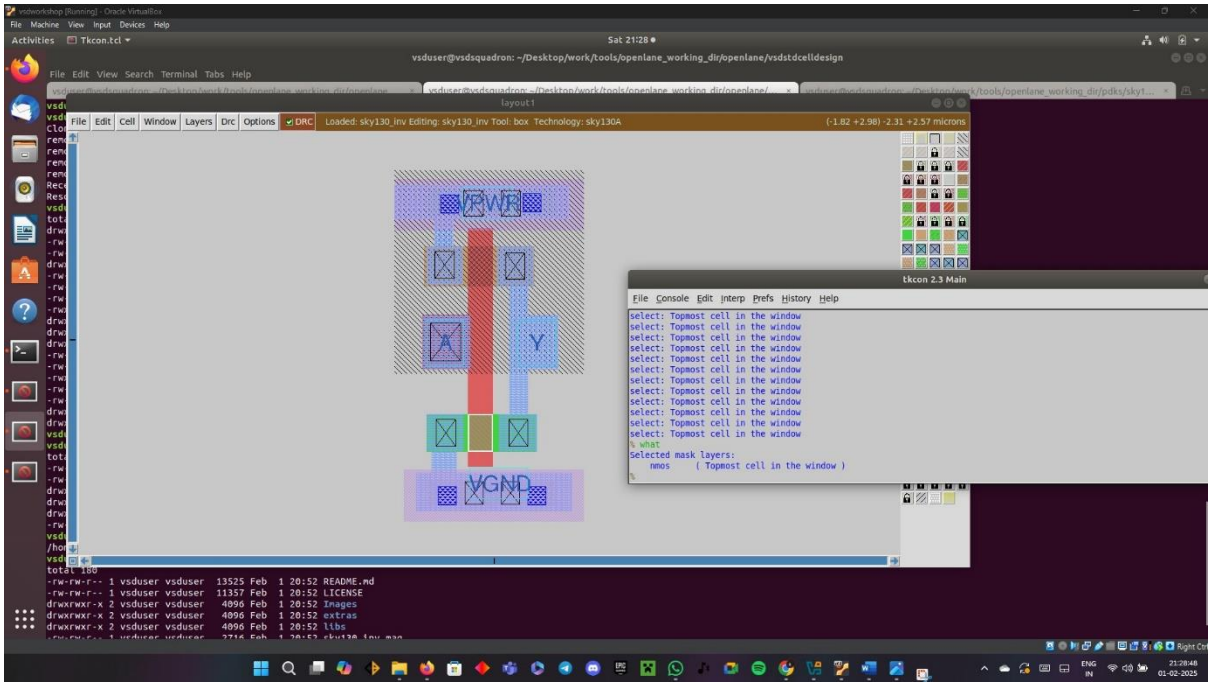
Placed in oxidation furnace



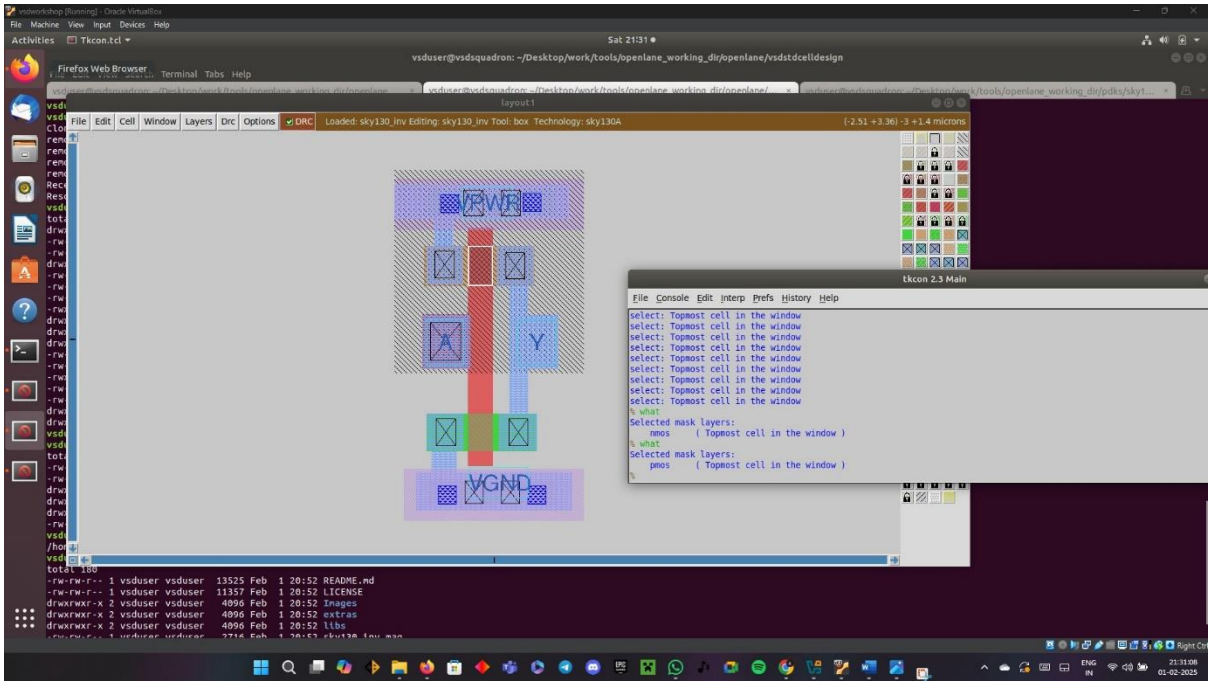


Labs –

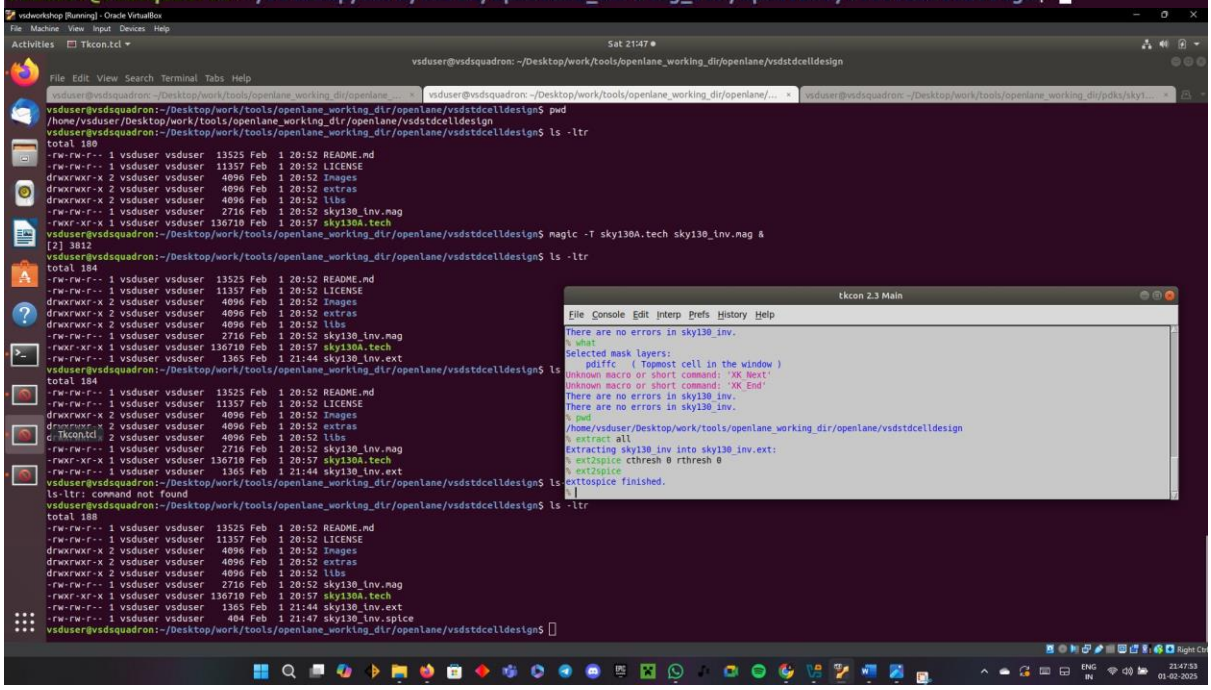
The highlighted is explained by the command "what" in the tkcon.tcl



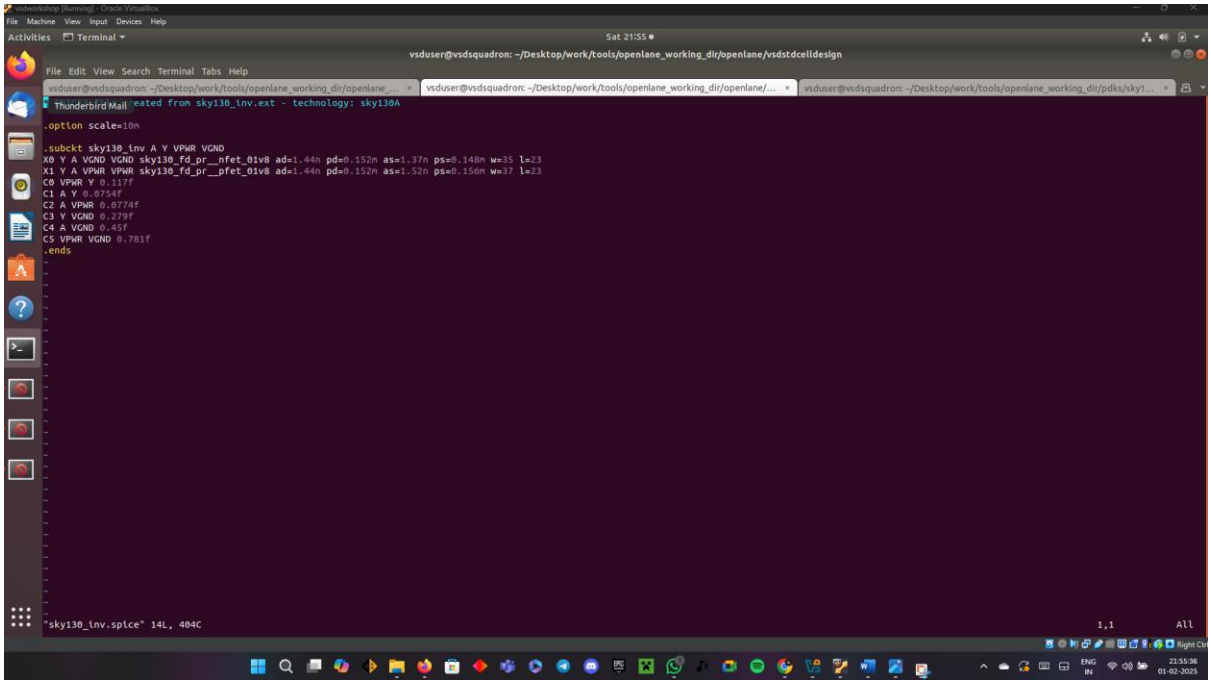
Same as above, instead it's for pmos




```
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$ ls -ltr
total 184
-rw-rw-r-- 1 vsduser vsduser  13525 Feb  1 20:52 README.md
-rw-rw-r-- 1 vsduser vsduser  11357 Feb  1 20:52 LICENSE
drwxrwxr-x 2 vsduser vsduser   4096 Feb  1 20:52 Images
drwxrwxr-x 2 vsduser vsduser   4096 Feb  1 20:52 extras
drwxrwxr-x 2 vsduser vsduser   4096 Feb  1 20:52 libs
-rw-rw-r-- 1 vsduser vsduser   2716 Feb  1 20:52 sky130_inv.mag
-rwxr-xr-x 1 vsduser vsduser 136710 Feb  1 20:57 sky130A.tech
-rw-rw-r-- 1 vsduser vsduser   1365 Feb  1 21:44 sky130_inv.ext
vsduser@vsdsquadron:~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign$
```



Spice file


vsduser@vsdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane/vsdstdcelldesign
eated from sky130_inv.ext - technology: sky130A
.option scale=10m
.subckt sky130_inv A Y VPWR VGND
X0 Y A VGND VGND sky130_fd_pr__nfet_01v8 ad=1.44n pd=0.152m as=1.37n ps=0.148m w=35 l=23
X1 Y A VPWR VPWR sky130_fd_pr__pfet_01v8 ad=1.44n pd=0.152m as=1.52n ps=0.156m w=37 l=23
C0 VPWR Y 0.117f
C1 A Y 0.0754f
C2 A VPWR 0.0774f
C3 Y VGND 0.279f
C4 A VGND 0.45f
C5 VPWR VGND 0.781f
.ends
"sky130_inv.spice" 14L, 404C
1,1
All