

Name : Aditya Narayanan Raghavan

Grade : 8th grade

School : National Public School, Rajajinagar, Bangalore

***All pictures in the below document are taken from the digital chip design course**

Level 3 :-

Arduino Board – Made up of many components.

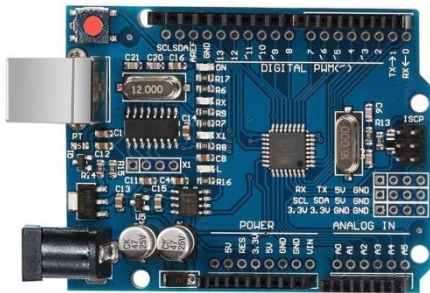
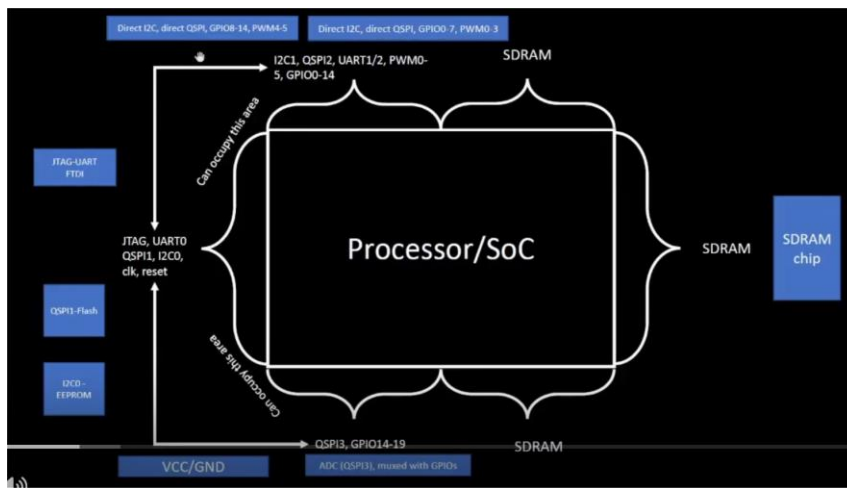


Photo Credit - <https://www.ubuy.co.in/product/3V6KZCHAG-arduino-uno-r3-compatible-atmega328p-ch340-usb-microcontroller-board>

Below diagram of processor –



Typical requirements for making Arduino board are above.

Zoom in to the main Integrated Circuit –

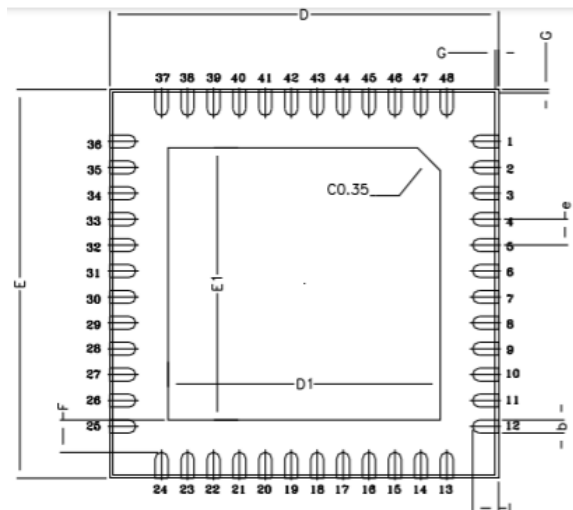
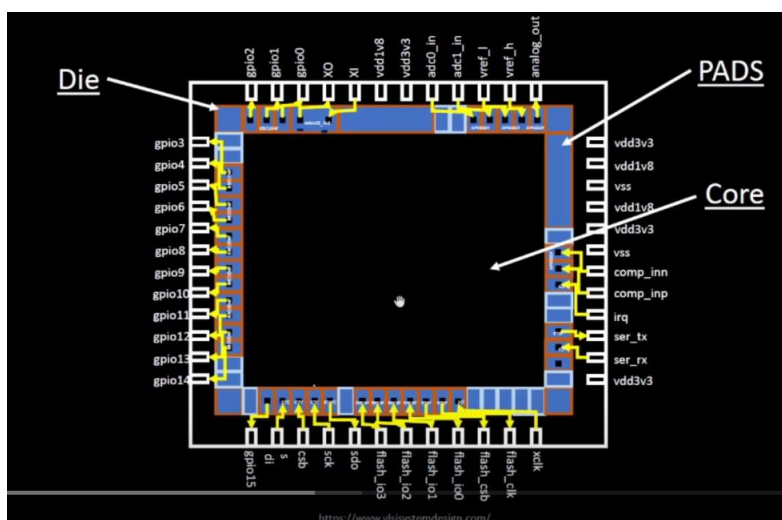


Photo Credits - <https://electronics.stackexchange.com/questions/394554/soldering-0-4mm-pitch-qfn-48-chip>

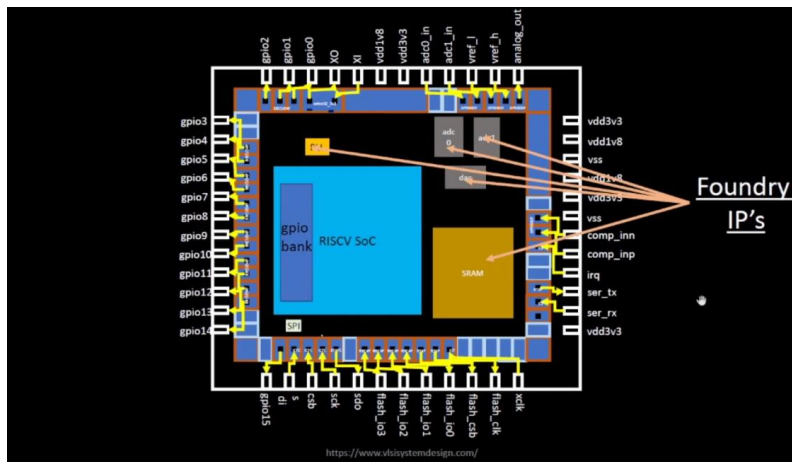
The chip sits at the centre of the package (In the middle of the QFN-48 package)

Wire bonds connected to the chip are able to transfer all the signal coming from the outside world to the integers of the chip.



Many parts in a chip –

1. Pads – Through pads you can send the signal inside the chip and vice versa
2. Core – The core is where all the digital logic sits. The AND Gate, OR Gate etc are found in the core
3. Die – Size of the entire chip



Foundry – A factory where chips get manufactured.

IP – Intellectual Property.

Reason why the Foundry IPs are called like that as they need intelligence to be made.

The RISC-V SOC and the SPI are macros.

They are called macros as they are put digital logic.

To manufacture chips, there needs to be communication with Foundry.

RISC-V Architecture

If you have a C Program and you need it to run on a computer, then you need to pass it through hardware to make it binary to get the required output.

Another interface is required to be present between the flow and the RISC-V architecture that is the hardware description language.

You need to implement this RISC – V specifications using some RTL Ex : Picorv32 cpu core

This rtl implements these specifications of the architecture to make the layout.

Software applications to Hardware.

The application software first enters into the system software which then converts the application into a binary language.

The majors system softwares are the OS, Compiler and the Assembler.

OS – Handles IO Operations, Allocates memory and does the low level system functions. The other function is to make sure that it turns into a binary language.

Compiler – Converts the program code into a set of instructions

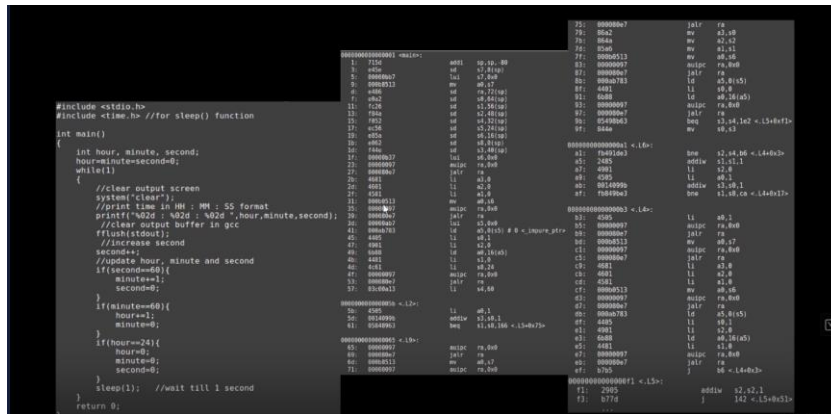
The compiler turns it into a set of instructions which is dependent on the hardware

Then the job of the assembler is to make the instructions into a binary language.

Then the hardware receives the code and does the function specified.

Ex : Stopwatch –

The functions, which is written in a specific language, is put into a compiler, and if the hardware is a RISCv, then the output of the compiler will be a set of RISCv instructions, which then enter the chip layout to perform the functions



Input and Output of Compiler

Instructions act as an abstract interface between the C and the Hardware.

The hardware only understands the HDL, so if you give it a set of 1s and 0s, it understands it needs to do something with that.

The instructions are put into the assembler which turn it into a binary language.

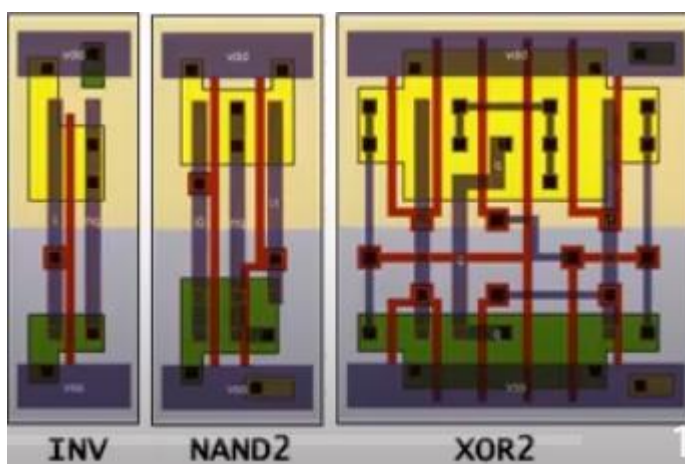
SoC design and OpenLANE –

RTL to GDSII Flow –

Synthesis, Clock Tree Synthesis, Floor/Power Planning, Routing, Placement, Sign Off.

Synthesis – Converts RTL to a circuit out of components from the standard cell library.

The standard cells have regular layouts.



Chip Floor Planning – Partition the chip die between system building blocks and then the I/O pads will be placed.

Macro Floor Planning – The macro dimensions are defined, The rows and routing tracks are defined

Power Planning – Has power pads, power straps and power rings.

Placement – We place the Gate-2 steepsLevel Netlist cells on the floorplan rows, aligned with the site.

2 steps – Global and Detailed

Global placement tries to find the optimal placement for all the cells. Such positions are not correct, so they may overlap

Detailed Placement are minimally altered to be legal

CTS – Clock distribution network.

To deliver the clock to all sequential elements.

With minimum skew

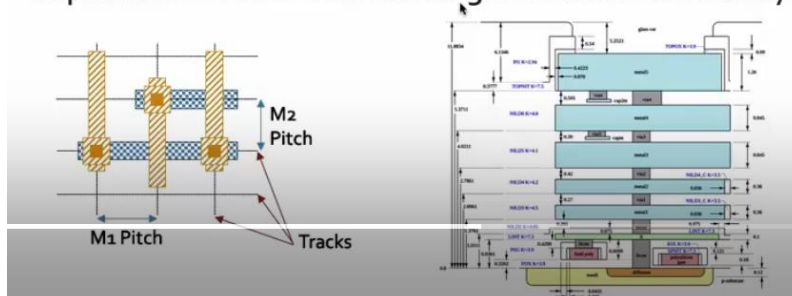
Usually a tree.

Synthesized to level of clock.

Certain structures are used, such as H , X Tree etc

Route –

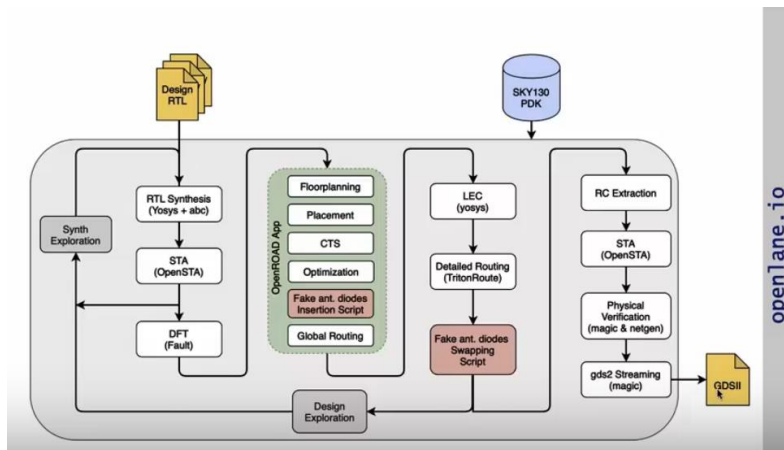
- Implement the interconnect using the available metal laye



To implement the interconnect using available metal layers

The local layers are all aluminium.

OpenLANE ASIC Flow –



Starts with RTL Synthesis

Can be used to generate a report

Based on this we can make a best strategy to continue

OpenLANE has design exploration Utility

Then the physical implementation

PnR (Place and Route) –

Floor and Power planning

End decoupling Capacitors and Tap cells insertion

Placement : Global and Detailed

Next step in process in Yosys –

Verification must be performed.

Modification of netlist

Used to confirm that what we ended up with was not what we started with.

Fake ant. Diodes insertion script –

When a metal wire segment is made, it can act as antenna.

Preventive approach – Add fake antenna diode, run antenna checker and if the checker reports violation, replace it with a real one.

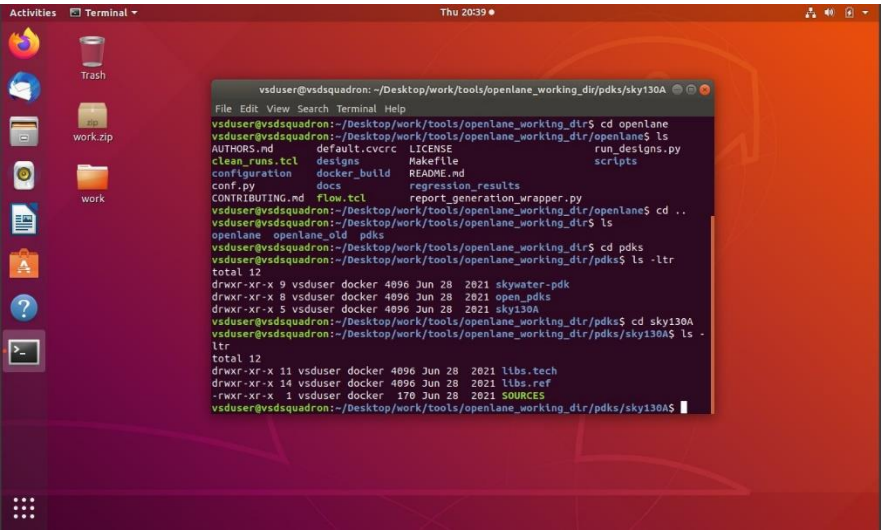
Static Timing Analysis – Involves RC Extraction from routed layout.

Then physical verification.

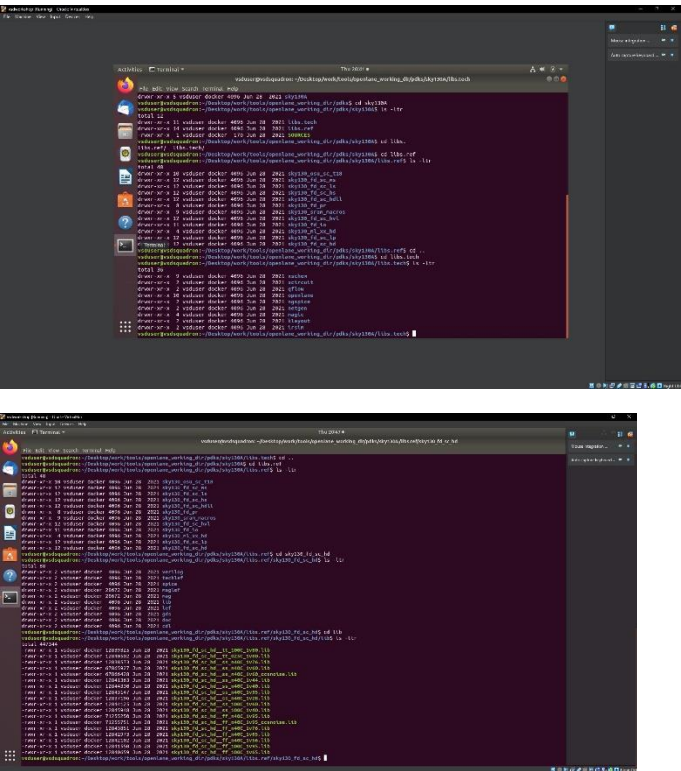
Open Source EDA Tools –

SKY130_D1_SK3 - Get familiar to open-source EDA tools

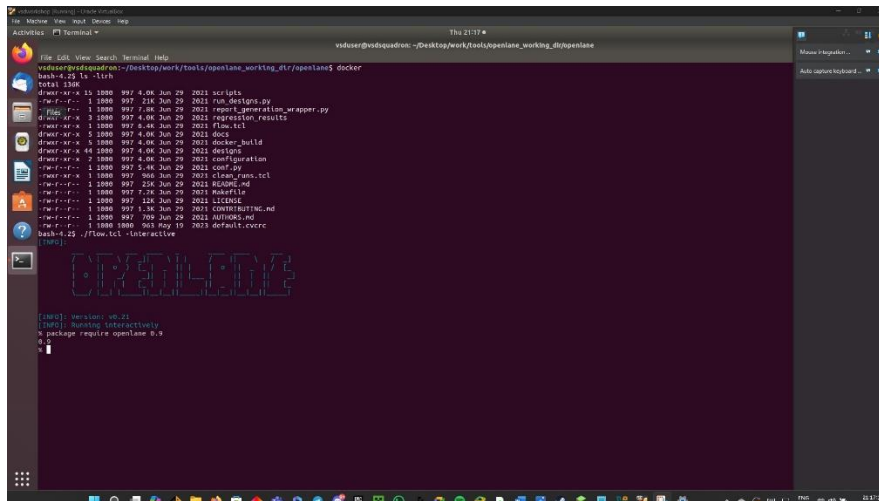
Screenshot of the virtual Ubuntu box running the open source EDA tools



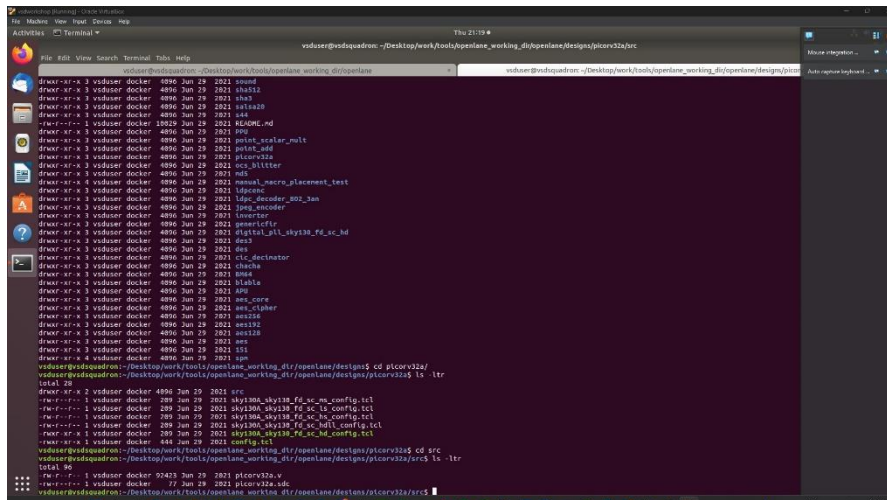
Screenshots of some of the files and directory structure of the open source EDA tool.



Screenshot on opening OpenLANE



Design preparation steps - screenshots




```

vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
$ ./sky130_fd_sc_hd_40b_2
Chip area for module 'picorv32a': 147712.918400
79. executing Verilog backend.
Dumping module 'picorv32a'.
Warnings: 107 unfiled messages, 107 total
End of script. Logfile hash: 8483b6c6. CPU: user 15.48s system 0.32s, MEM: 96.59 MB peak
Yosys 0.9+1621 (git sha1 84e5ef, gcc 8.3.1 -fPIC -O3)
Time spent: 303.7s abc (clk_wgt), 575.31s gpi_wgt (4 sec), ...
[INFO] Changing celllist from 0 to openlane_flow/Design/picorv32a/run/08-d1-16/results/synthesis/picorv32a.synthesis.v
[INFO] Running static timing analysis...
[INFO] Current time index: 0
Questa 2.2.0 304002048 Copyright (c) 2019, Parallax Software, Inc.
License GPLv3: GNU GPL version 3 <http://gnu.org/licenses/gpl.html>
This is free software, and you are free to change and redistribute it
under certain conditions; type 'show copying' for details.
This program comes with ABSOLUTELY NO WARRANTY; for details type 'show warranty'.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pd/sky130a/lib/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_ff_n40c_lv95.lib line 31, default_operating_condition ff_n40c_lv95 not found.
Warning: /home/vsduser/Desktop/work/tools/openlane_working_dir/pd/sky130a/lib/sky130_fd_sc_hd/lib/sky130_fd_sc_hd_is_180c_lv95.lib line 32, default_operating_condition is_180c_lv95 not found.
create_clock [get_ports $:env(CLOCK_PORT)] -name $:env(CLOCK_PORT) -period $:env(CLOCK_PERIOD)
set input_delay_value [expr $:env(CLOCK_PERIOD) * $:env(ID_PCT)]
set output_delay_value [expr $:env(CLOCK_PERIOD) * $:env(OD_PCT)]
puts "[INFO]: Setting output delay to $:env(OUT_DELAY)"
[INFO]: Setting output delay to: 4.9400000000000001
[INFO]: Setting input delay to: $:env(OUT_DELAY)
[INFO]: Setting input delay to: 4.9400000000000001
set_max_fanout $:env(SVNM_MAX_FANOUT) [current design]
set_clk_idx [search [all_inputs] [get_ports $:env(CLOCK_PORT)]]
set rst_idx [search [all_inputs] [get_ports resetn]]
set all_inputs_w_clk [replace [all_inputs] $clk_idx $rst_idx]
set all_inputs_w_rst [replace [all_inputs_w_clk] $rst_idx $rst_idx]
set all_inputs_w_clk_rst [replace [all_inputs_w_rst] $rst_idx $rst_idx]
# correct resetn
set input_delay_value [clock [get_clocks $:env(CLOCK_PORT)]] $all_inputs_w_clk_rst
set input_delay 0.0 -clock [get_clocks $:env(CLOCK_PORT)] [resetn]
set output_delay [set_output_delay -clock [get_clocks $:env(CLOCK_PORT)]] [all_outputs]
# 1000 set this as parameter
set_cap_load [expr $:env(SVNM_DRIVING_CELL) * pin $:env(SVNM_DRIVING_CELL_PIN) [all_inputs]]
set cap_load [expr $:env(SVNM_CAP_LOAD) / 1000.0]
puts "[INFO]: Setting load to $cap_load"
[INFO]: Setting load to 0.0705
set_load $cap_load [all_outputs]
tss -728.68
wms -24.89
[INFO]: Synthesis was successful

```

Steps to Characterize Synthesis Results

After synthesis calculate flip-flop ratio as below.

Flip flop ratio = no of DFFs / No of cells * 100

$$= 1613/14876 * 100 = 10.84\%$$

```

vsduser@vdsquadron: ~/Desktop/work/tools/openlane_working_dir/openlane
$ ./sky130_fd_sc_hd_40b_2
Number of memories: 0
Number of memory 3151: 0
Number of processors: 0
Number of cells: 14876
sky130_fd_sc_hd_a21110_2 1
sky130_fd_sc_hd_a21110_2 35
sky130_fd_sc_hd_a21101_2 60
sky130_fd_sc_hd_a21101_2 140
sky130_fd_sc_hd_a21101_2 0
sky130_fd_sc_hd_a21101_2 37
sky130_fd_sc_hd_a2101_2 244
sky130_fd_sc_hd_a2101_2 80
sky130_fd_sc_hd_a2101_2 1913
sky130_fd_sc_hd_a20020_2 1760
sky130_fd_sc_hd_a20001_2 41
sky130_fd_sc_hd_a3111_2 2
sky130_fd_sc_hd_a310_2 0
sky130_fd_sc_hd_a3101_2 7
sky130_fd_sc_hd_a310_2 0
sky130_fd_sc_hd_a410_2 1
sky130_fd_sc_hd_a410_2 157
sky130_fd_sc_hd_a410_2 148
sky130_fd_sc_hd_a410_2 345
sky130_fd_sc_hd_a400_2 1
sky130_fd_sc_hd_a400_2 1810
sky130_fd_sc_hd_a400_2 0
sky130_fd_sc_hd_a400_2 42
sky130_fd_sc_hd_a400_2 1613
sky130_fd_sc_hd_a400_2 1813
sky130_fd_sc_hd_a400_2 1224
sky130_fd_sc_hd_a400_2 221
sky130_fd_sc_hd_a400_2 79
sky130_fd_sc_hd_a400_2 524
sky130_fd_sc_hd_a400_2 1
sky130_fd_sc_hd_a400_2 42
sky130_fd_sc_hd_a400_2 1
sky130_fd_sc_hd_a400_2 0
sky130_fd_sc_hd_a400_2 69
sky130_fd_sc_hd_a400_2 6
sky130_fd_sc_hd_a400_2 54
sky130_fd_sc_hd_a400_2 141
sky130_fd_sc_hd_a400_2 209
sky130_fd_sc_hd_a400_2 1
sky130_fd_sc_hd_a400_2 264
sky130_fd_sc_hd_a400_2 9
sky130_fd_sc_hd_a400_2 1312
sky130_fd_sc_hd_a400_2 99
sky130_fd_sc_hd_a400_2 119
sky130_fd_sc_hd_a400_2 92

```

Calculator

Standard

10.84296853993009

% C C C C

% x² √

7 8 9 ×

4 5 6 -

1 2 3 +

% 0 .