Report for Assignment 4, 5, 6

After completing these three assignments, we have come up with our own CPU design, thoroughly implemented and tested on FPGA board.
In assignment 4, we designed the preliminary circuit for the CPU able to execute an instruction subset. In assignment 5, we improved our design by observing the errors we encountered in simulation which further helped us in implementing the display interface and FSM on the hardware

The features of the design

- A display interface to observe register file, instruction loaded, address to program memory, address to data memory, data coming from and to data memory, i_decode_state and instr_class.
- An FSM to control the execution of the loaded program step by step or at one go using push buttons.
- Controlling the start program using the initial address given using slide switches.

Please find the reports in the same folder.