

EXPERIMENT MANUAL

FOR

DIGITAL ELECTRONICS LAB

EXPERIMENT No: 01



DEPARTMENT OF APPLIED PHYSICS
DELHI TECHNOLOGICAL UNIVERSITY
SHAHBAD DAULATPUR, MAIN BAWANA ROAD
DELHI- 110042

EXPERIMENT No. 1

AIM: Study & verification of truth tables of TTL Gates: - AND, OR, NOT, NAND, NOR.

APPARATUS: Logic Gate Circuit Trainer, IC used 7400, 7402, 7404, 7408, 7432, 7486, connecting wires.

THEORY:

The digital circuit which either allows a signal to pass through or stop it is called gate. Gates which allow a signal to pass through only when some logical conditions are satisfied are called logic gate. Logic gates usually combine one or more logic variables input to produce an output. All of the possible combinations of the input variables and the corresponding outputs are normally listed in a table called a truth table.

The simple logic gates are: (i) AND (ii) OR (iii) NOT.

The compound (Universal) logic gates are (i) NAND (NOT-AND) (ii) NOR (NOT-OR)

AND GATE USING 7408: A circuit which performs an AND operation. It has N Inputs (N=2) and one output. Digital signals applied at the input terminals marked A, B. The o/p is obtained at the o/p terminal marked Y.



| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

TRUTH TABLE

In case of this basic gate output is present only when all the inputs are present.

Its logical expression is given by $Y = A \cdot B$

OR GATE USING 7432: It allows the signal to pass through when even anyone of the logical conditions is satisfied.



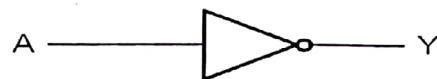
| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

TRUTH TABLE

The GATE in which output is 1 if and only one or more inputs are 1.

Its logical equation is given by $Y = A + B$

NOT GATE USING 7404: It allows the signal to pass through when the only logical condition is not satisfied it.



| Input | Output |
|-------|--------|
| A | Y |
| 0 | 1 |
| 1 | 0 |

TRUTH TABLE

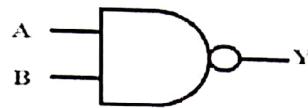
It is also known as inverter. It has one input (A) and one output (Y).

Its logical equation is $Y = \bar{A}$

NAND GATE USING 7400: It combines characteristics of a NOT and an AND gate.

The NOT-AND operation is known as NAND operation. A bubble on the output side of NAND gate represents NOT operation, inversion or complementation.

Its logical equation is $Y = \overline{A \cdot B}$

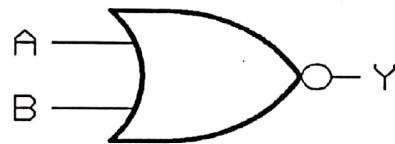


| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

TRUTH TABLE

A NAND gate is a universal gate. It serves as a building block for AND, OR and NOT gates.

NOR GATE USING 7401: It combines characteristics of a NOT and on OR gate. The NOT-OR operation is known as NOR operation.



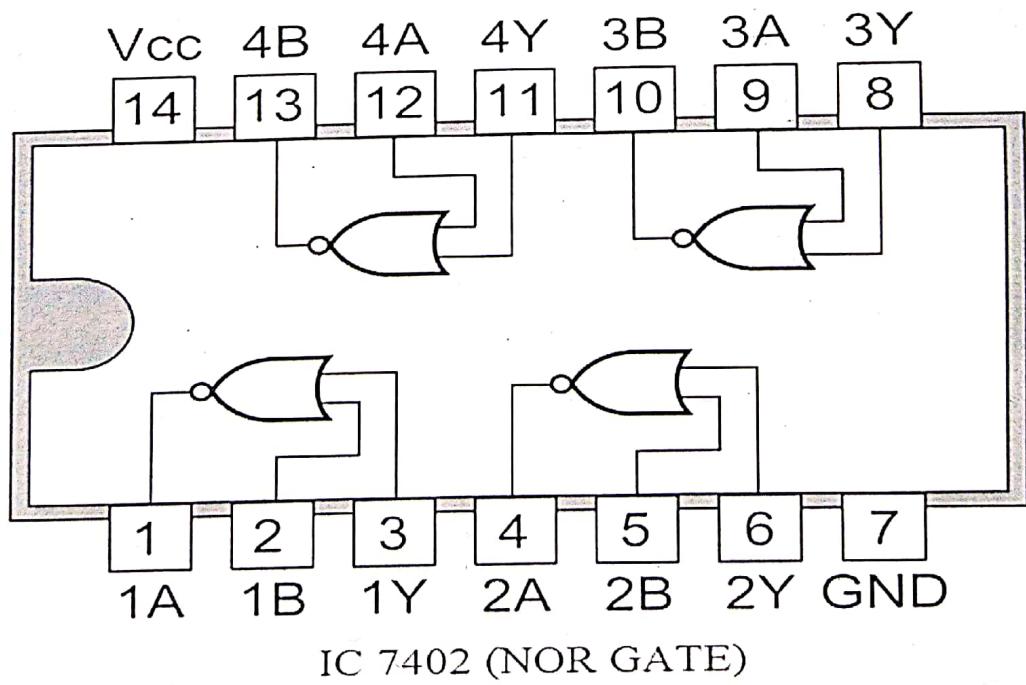
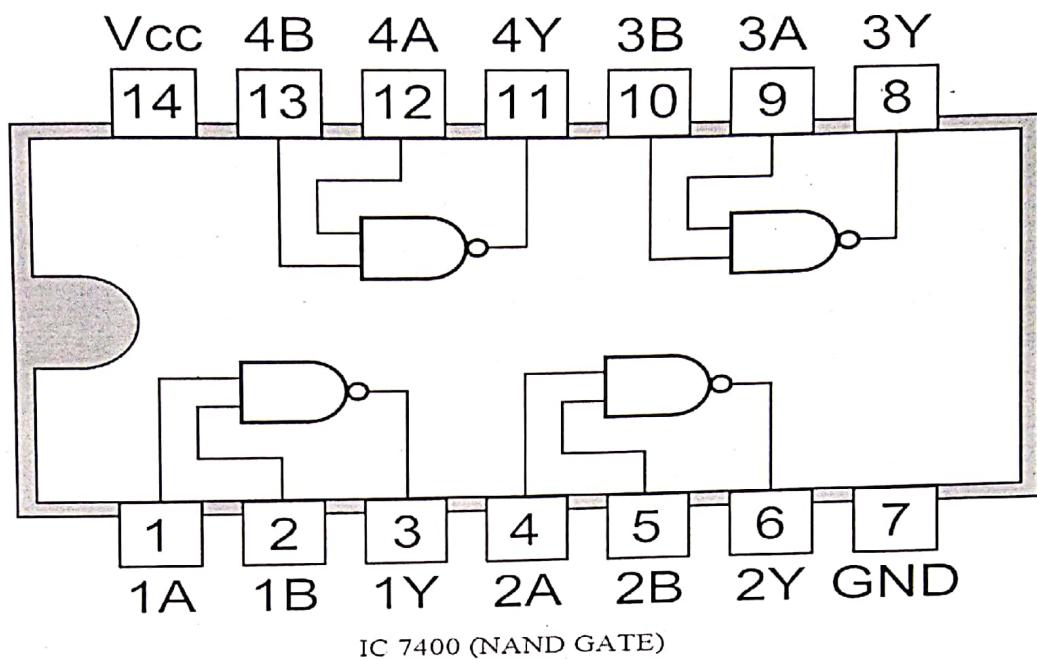
| Inputs | | Outputs |
|--------|---|---------|
| A | B | Y |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

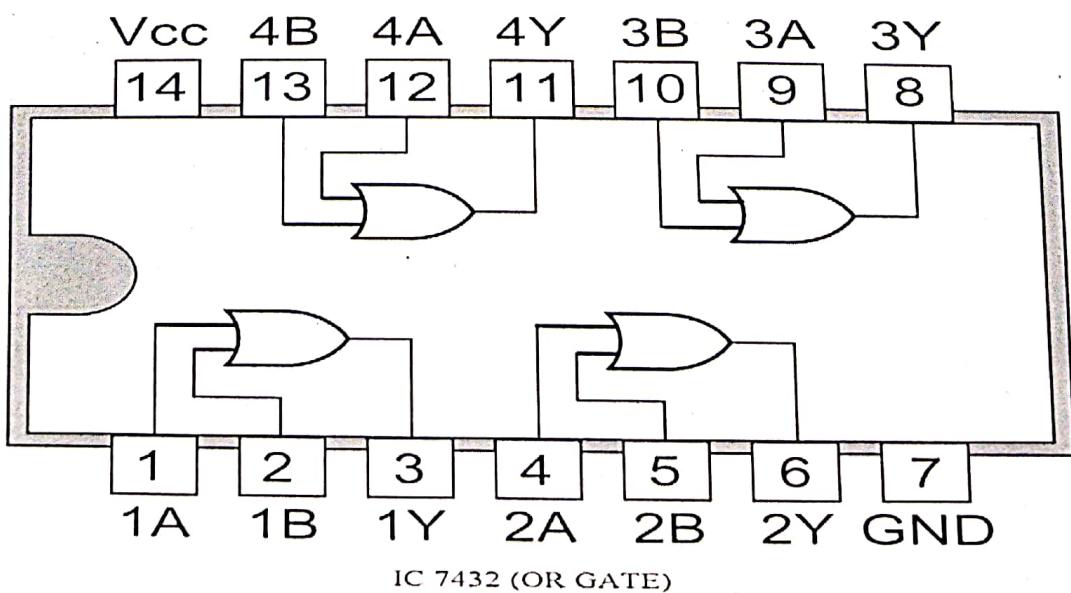
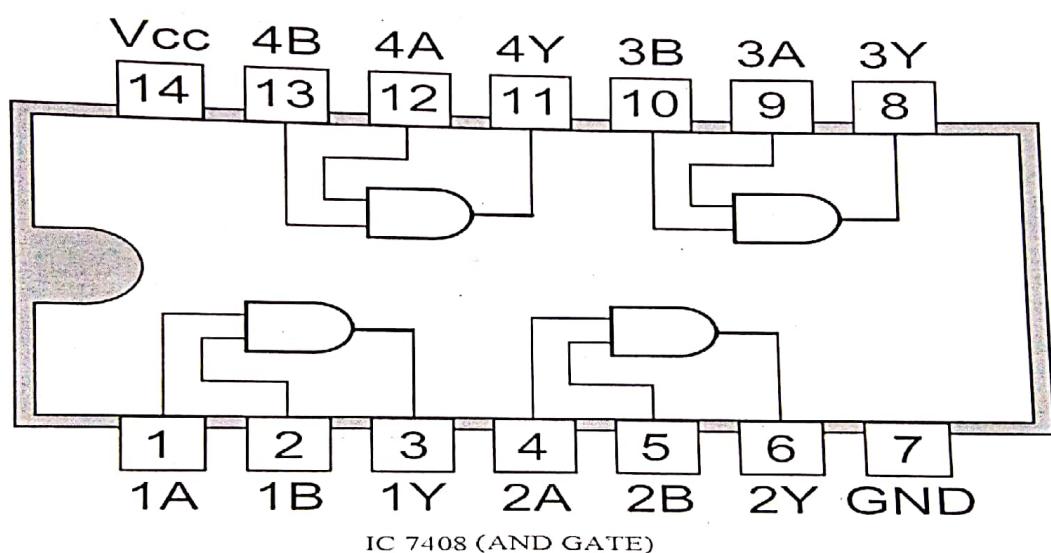
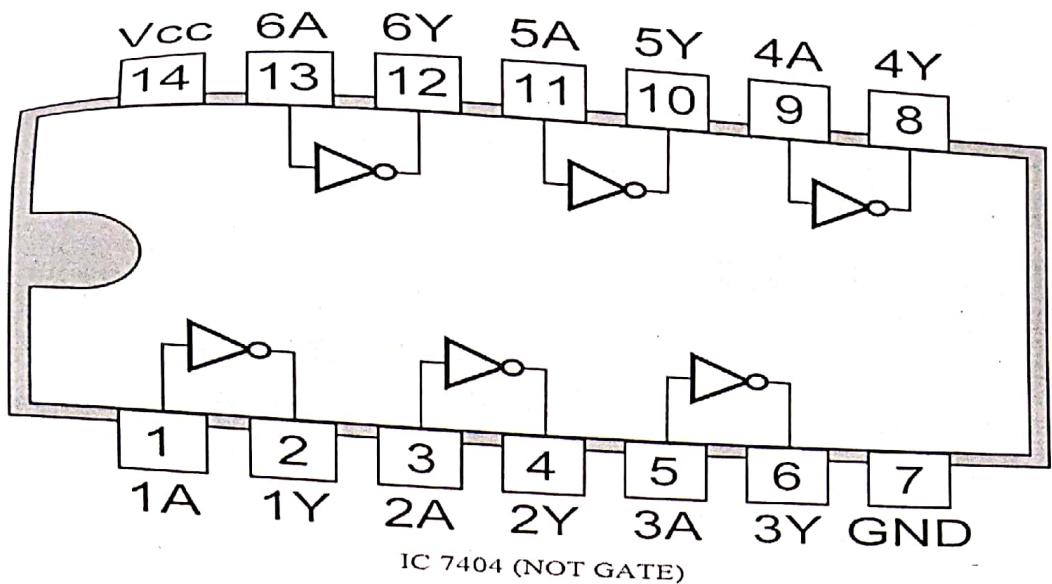
TRUTH TABLE

Similar to NAND gate, a bubble on the output side of the NOR gate represents the NOT operation.

The logic equation is $Y = \overline{A + B}$

Pin Description:





PROCEDURE:

1. Take the IC's numbered 7408, 7432, 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

EXPERIMENT MANUAL
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EXPERIMENT No: 02



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EXPERIMENT No. 2

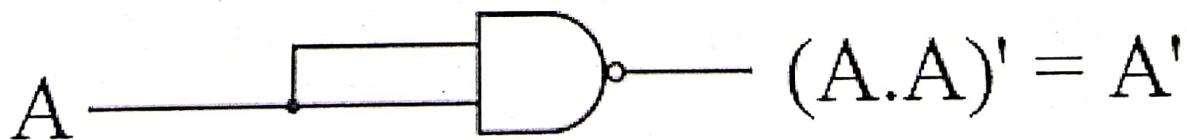
AIM: To implement all Logic gates using Universal gate IC -7400 (NAND Gate IC) and IC-7402 (NOR Gate IC).

APPARATUS: Digital trainer kit, Logic gate IC 7400, Logic gate IC 7402, Connecting wires.

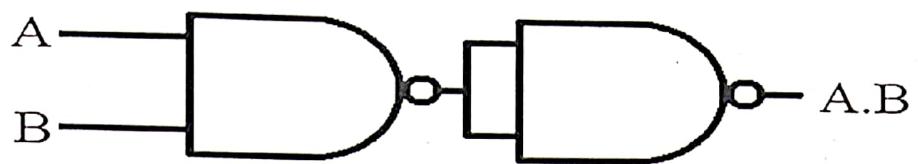
THEORY:

Since NAND gate is a universal gate, all other logic gates can be implemented using it. Implementation using NAND gate:

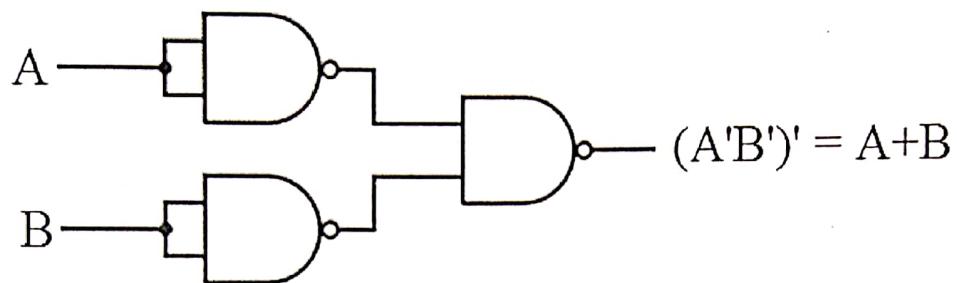
1. **NOT Gate:** The input is given into short circuited pins of two inputs NAND gate and the output is inversion of input as shown in fig.
2. **AND Gate:** Two NAND gates are required. Inputs given to one NAND gate produce an output which acts as input for second NAND gate and the final output is same as AND gate output.
3. **OR Gate:** Three NAND gates are required. Two inputs are given to two different NAND gates the outputs of these are given as input to third NAND gate. Final output is same as of OR gate output.
4. **XOR Gate:** Four NAND gates are required. The connections are made as per the given circuit diagram, the final output is same as XOR gate output.
5. **XNOR Gate:** Five NAND gates are required. So we use two 7400 ICs. The final output of XOR gate (Four gates) is given as input to fifth NAND gate and the output is same as XNOR gate i.e. XNOR is inversion of XOR.



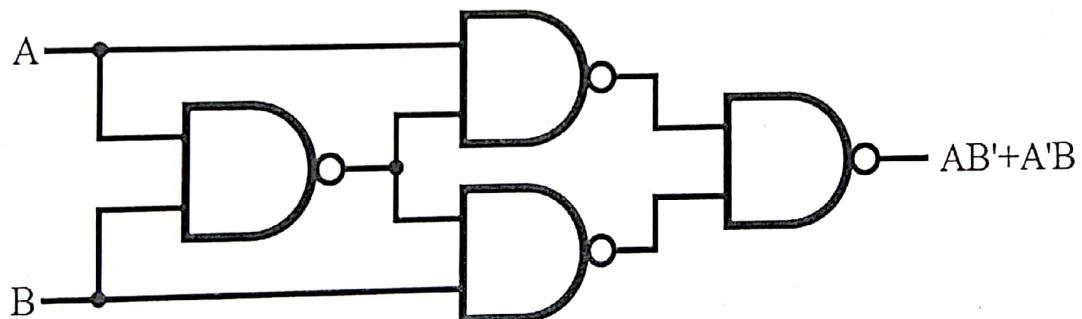
NOT GATE USING NAND GATE



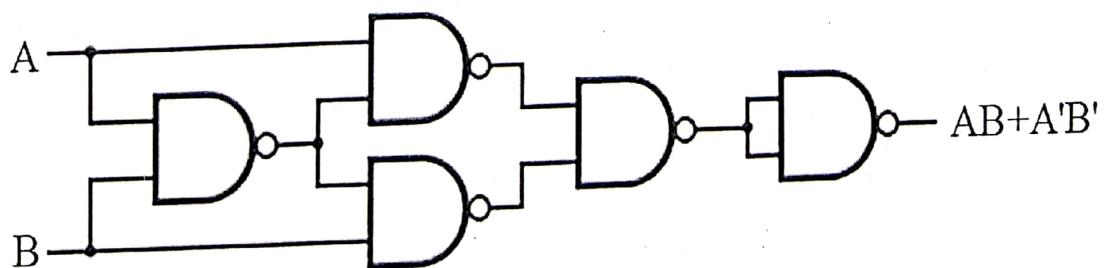
AND GATE USING NAND GATE



OR GATE USING NAND GATE

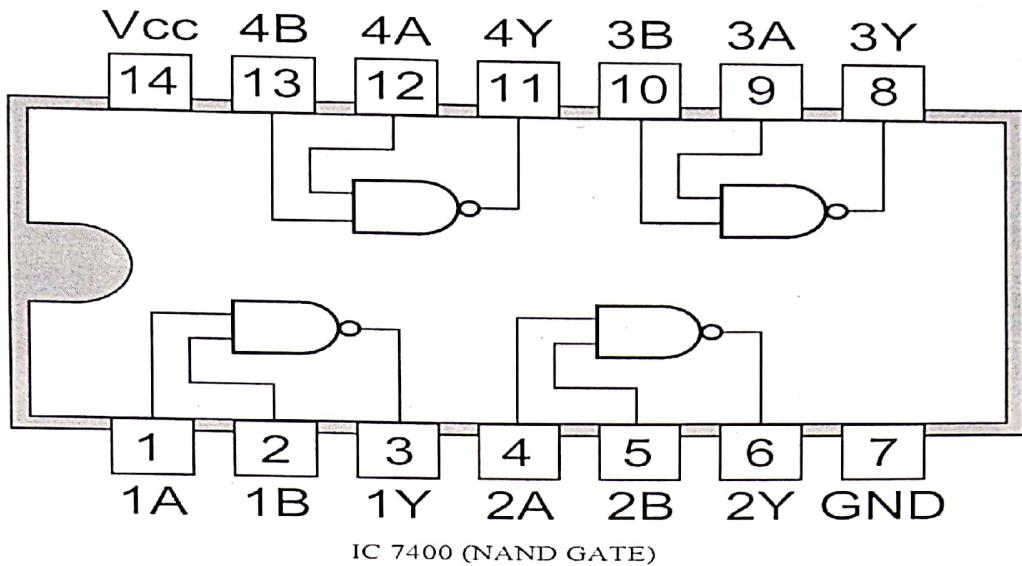


EX-OR GATE USING NAND GATE



EX-NOR GATE USING NAND GATE

PIN DESCRIPTION:



PROCEDURE:

1. Take a 14 pin NAND gate IC, a trainer kit which must be switched off and some wires.
2. Insert the IC into the 14 pin IC slot in the trainer kit.
3. Now make the connection one by one as given circuit diagrams and pin description.
4. Make ground connection and V_{CC} connection for voltage supply.
5. In the kit LEDs are attached with the input toggle switches and output. At low value (0) of switch LED do not glow or LED glow Green, while at high value (1) switch LED glow Red.
6. By changing inputs using toggle switches verify truth tables for all circuits.

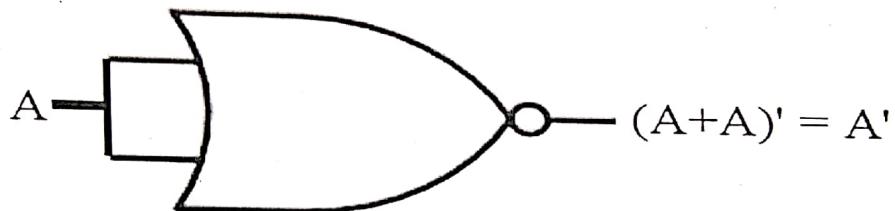
PART-II

THEORY:

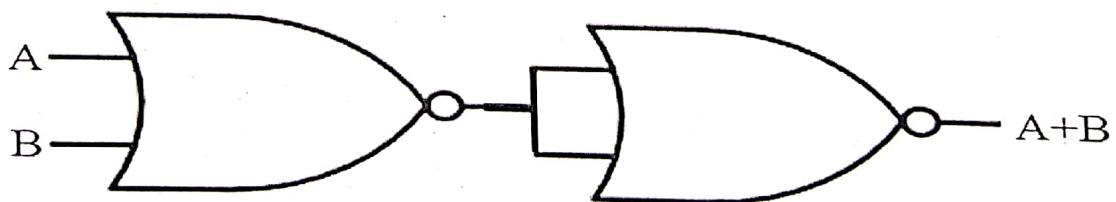
Since NOR gate is a universal gate, all other logic gates can be implemented using it. Implementation using NOR gate:

1. **NOT Gate:** The input is given into short circuited pins of two inputs NOR gate and the output is inversion of input as shown in fig.

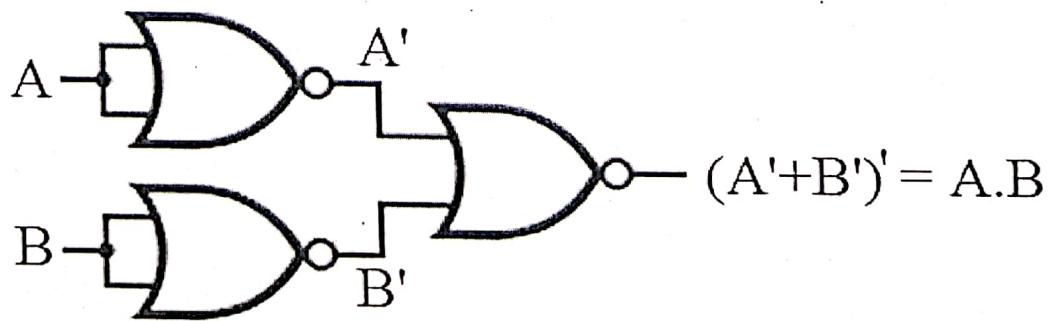
2. **AND Gate:** Two NOR gates are required. Inputs given to one NOR gate produce an output which acts as input for second NOR gate and the final output is same as AND gate output.
3. **OR Gate:** Three NOR gates are required. Two inputs are given to two different NOR gates the outputs of these are given as input to third NOR gate. Final output is same as of OR gate output.
4. **XOR Gate:** Four NOR gates are required. The connections are made as per the given circuit diagram, the final output is same as XOR gate output.
5. **XNOR Gate:** Five NOR gates are required. So we use two 7402 ICs. The final output of XOR gate (Four gates) is given as input to fifth NOR gate and the output is same as XNOR gate i.e. XNOR is inversion of XOR.



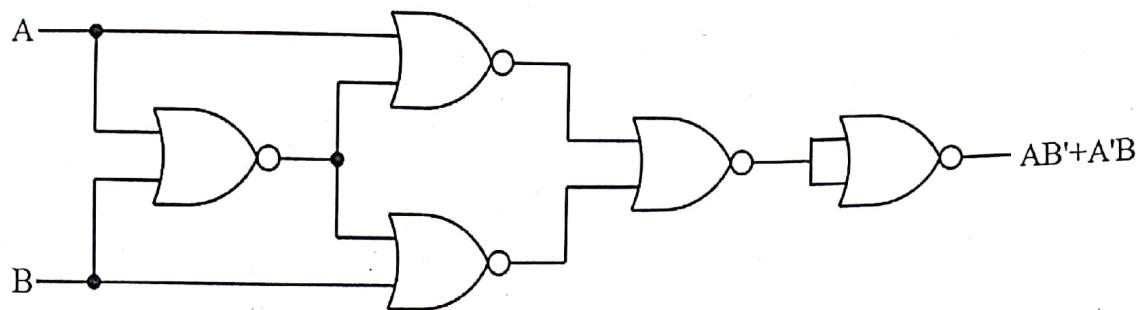
NOT GATE USING NOR GATE



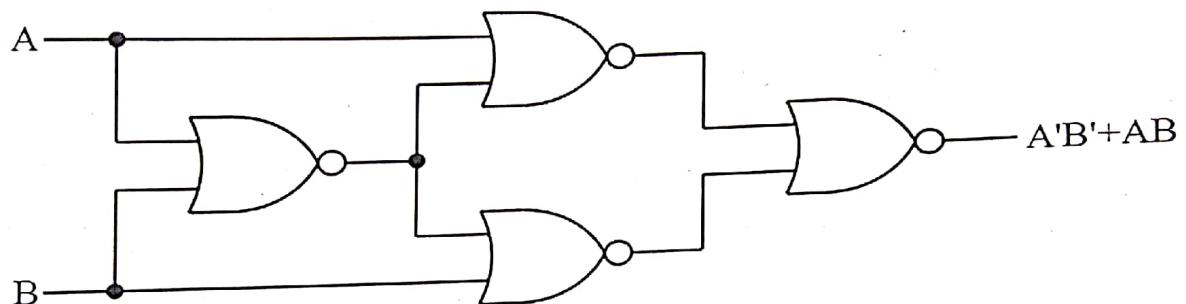
OR GATE USING NOR GATE



AND GATE USING NOR GATE

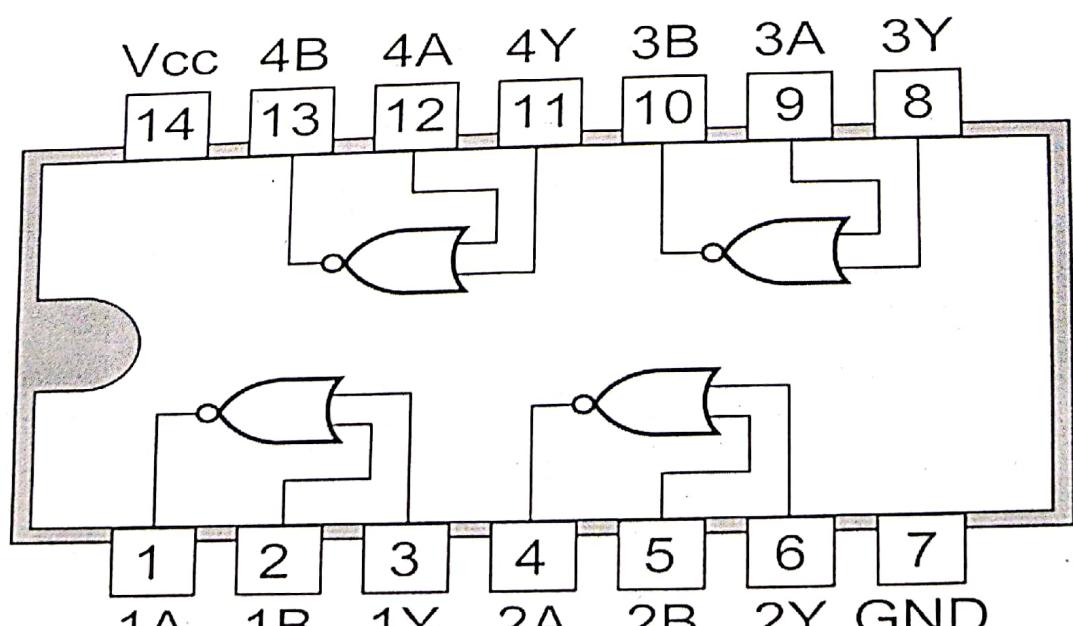


EX-OR GATE USING NOR GATE



EX-NOR GATE USING NOR GATE

PIN DESCRIPTION:



IC 7402 (NOR GATE)

PROCEDURE:

1. Take a 14 pin NOR gate IC, a trainer kit which must be switched off and some wires.
2. Insert the IC into the 14 pin IC slot in the trainer kit.
3. Now make the connection one by one as given circuit diagrams and pin description.
4. Make ground connection and Vcc connection for voltage supply.
5. In the kit LEDs are attached with the input toggle switches and output. At low value (0) of switch LED do not glow or LED glow Green, while at high value (1) switch LED glow Red.
6. By changing inputs using toggle switches verify truth tables for all circuits.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 03



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EXPERIMENT No. 3

AIM: To design Half Adder and Full Adder circuits using Logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7408, 7432, 7486, connecting wires.

THEORY:

HALF ADDER: A half adder is a MSI circuit that adds two binary digits, giving a SUM bit and a CARRY bit as in the logic truth table. If A and B are the two input bits then SUM is the XOR of A & B:

$$\text{Sum} = A\bar{B} + \bar{A}B$$

Similarly CARRY is the AND of A & B:

$$\text{Carry} = A \cdot B$$

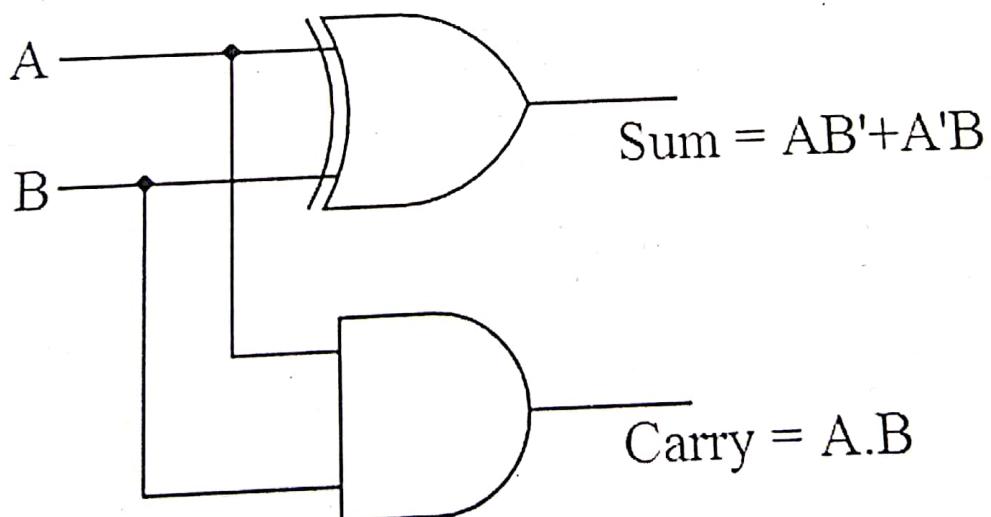


Fig: Half Adder

| INPUTS | | OUTPUTS | |
|--------|---|---------|-------|
| A | B | SUM | CARRY |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

TRUTH TABLE (HALF ADDER)

FULL ADDER: Full adder is a MSI circuit that adds two input bits and carry from the previous stage and out a SUM bit and CARRY OUT bit. A and B are the main bits, C is the carry from the previous stage. SUM produced is:

$$\text{Sum} = \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$$

CARRY is the output carry bit and is:

$$\text{Carry} = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

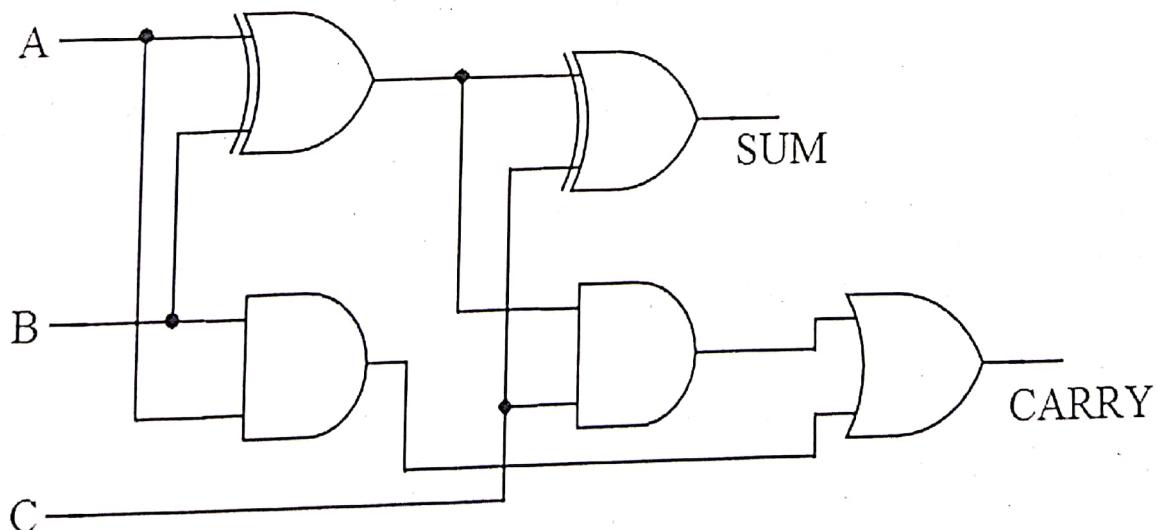


Fig: Full Adder

| INPUTS | | | OUTPUTS | |
|--------|---|---|---------|-------|
| A | B | C | SUM | CARRY |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

TRUTH TABLE (FULL ADDER)

PROCEDURE:

1. Take the IC's numbered 7408, 7432, 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 04



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EXPERIMENT No. 4

AIM: To design Half Subtractor and Full Subtractor circuits using Logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7404, 7408, 7432, and 7486, connecting wires.

THEORY:

HALF SUBTRACTOR: A half subtractor circuit subtracts two binary digits using XOR, NOT and AND gates giving output of difference bit and borrow bit.

$$D = X\bar{Y} + \bar{X}Y$$

$$B = \bar{X}Y$$

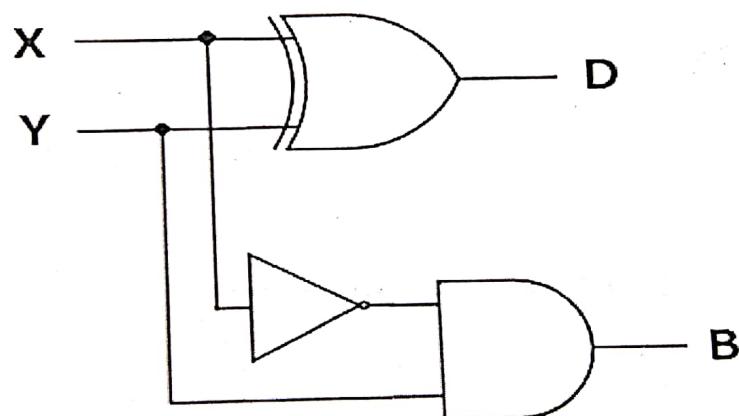


Fig: Half Subtractor

TRUTH TABLE (HALF SUBTRACTOR)

| INPUTS | | OUTPUTS | |
|--------|---|---------|---|
| X | Y | D | B |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

FULL SUBTRACTOR: A full subtractor is an arithmetic circuit that subtracts two bits and a borrow and difference bit is generated as output.

$$D = \bar{X}\bar{Y}Z + \bar{X}YZ + X\bar{Y}\bar{Z} + XYZ$$

$$B = \bar{X}Y + \bar{X}Z + YZ$$

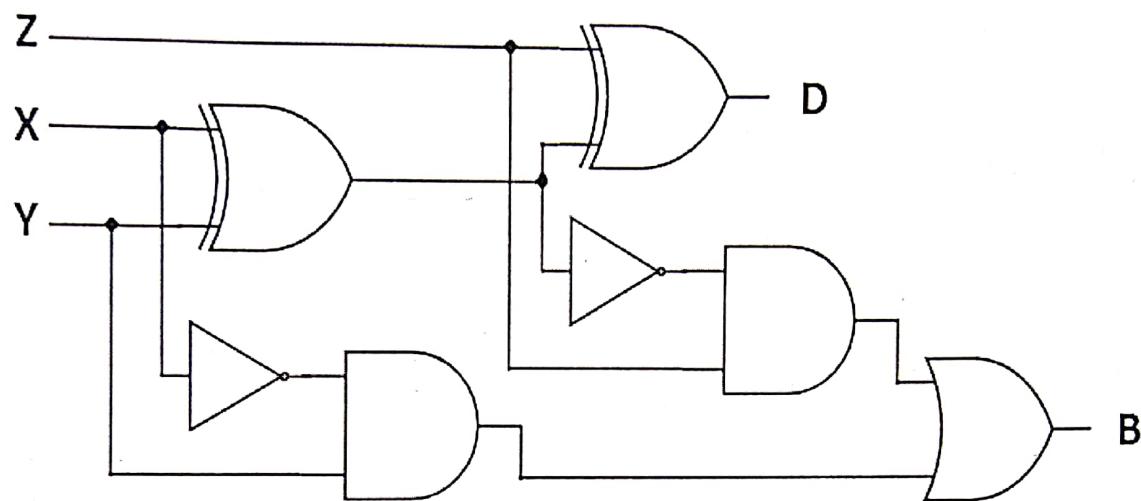


Fig: Full Subtractor

TRUTH TABLE (FULL SUBTRACTOR)

| INPUTS | | | OUTPUTS | |
|--------|---|---|---------|---|
| X | Y | Z | D | B |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

PROCEDURE:

1. Take the IC's numbered 7408, 7432, 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
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EXPERIMENT No: 05



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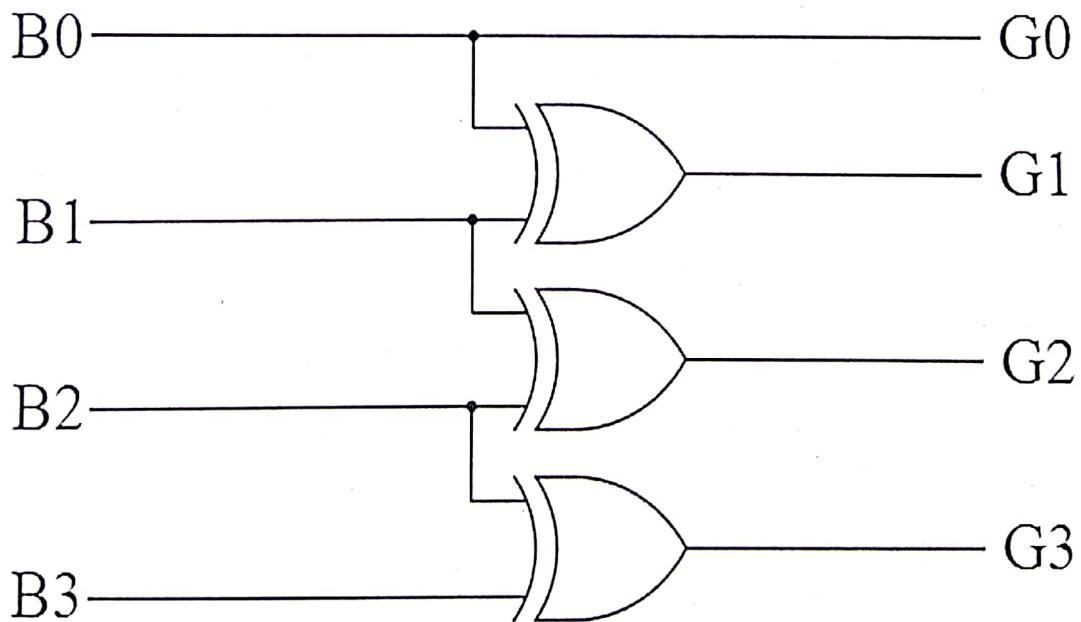
EXPERIMENT No. 5

AIM: To design Binary to Gray and Gray to Binary code converters using Logic gates.

APPARATUS: Digital trainer kits, Logic gate IC 7486 (XOR Gate), Connecting wires.

THEORY:

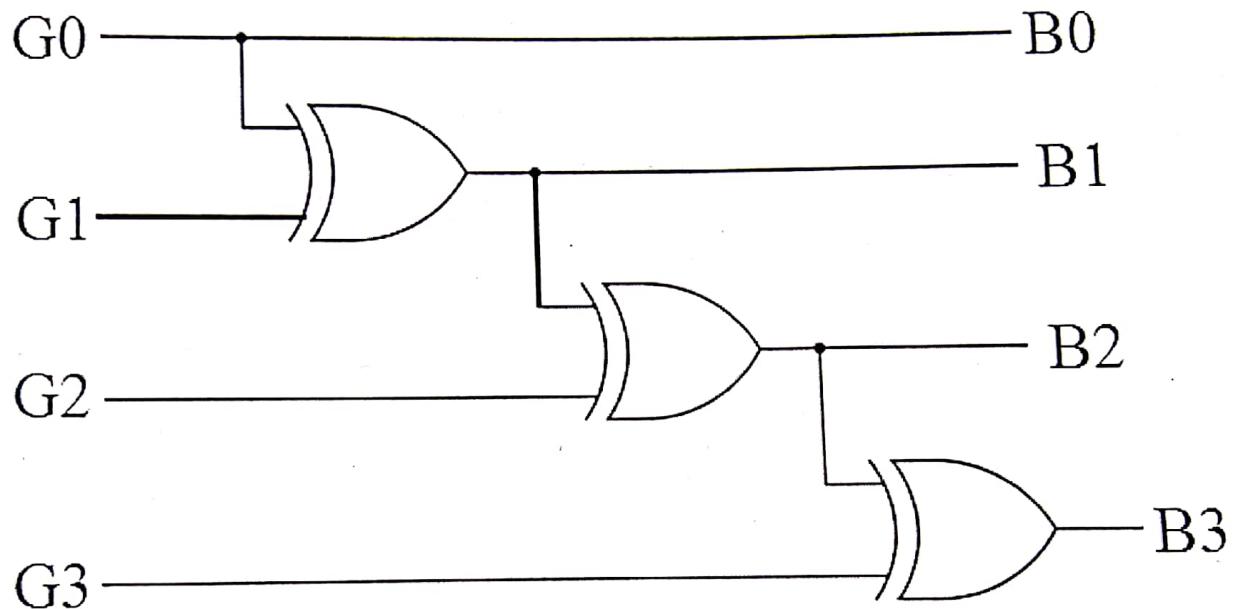
Binary to Gray Code Converter: Consider Binary code bits B₀, B₁, B₂, and B₃ as inputs and Gray code bits G₀, G₁, G₂, and G₃ as outputs. For converting binary to gray code, the MSB is noted. This MSB is added to the bit in next position. The sums are recorded and carry if any generated is discarded. This procedure is repeated till last bit of binary number is reached. The Karnaugh maps will be used for Gray code outputs (G₀, G₁, G₂, and G₃) value calculation. So find minimal expressions for G₀, G₁, G₂, and G₃ and realize these using logic gates.



Binary to Gray Code Converter

Gray to Binary Code Converter: Consider Gray code bits G₀, G₁, G₂, and G₃ as inputs and Binary code bits B₀, B₁, B₂, and B₃ as outputs. For converting gray to binary

code, the MSB is noted. This MSB is added to the bit in next position. The sums are recorded and carry if any generated is discarded. This sum is further added to the bit in next position and sums are recorded and carry if any generated is discarded procedure is repeated till last bit of gray code is reached. The Karnaugh maps will be used for Binary code outputs (B_0 , B_1 , B_2 , and B_3) value calculation. So find minimal expressions for B_0 , B_1 , B_2 , and B_3 and realize these using logic gates.



Gray to Binary Code Converter

| Sr No. | BINARY CODE | | | | GRAY CODE | | | |
|--------|-------------|----|----|----|-----------|----|----|----|
| | B0 | B1 | B2 | B3 | G0 | G1 | G2 | G3 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 6 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 7 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 11 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 12 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 13 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 14 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 15 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

PROCEDURE:

1. Take the IC's numbered 7486.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

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EXPERIMENT MANUAL
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EXPERIMENT No: 06



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EXPERIMENT No. 6

AIM: Multiplexer and Demultiplexer: Truth-table verification and realization using logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7404, 7408, and 7432, connecting wires.

THEORY:

MULTIPLEXER: The multiplexer is a digital circuit which has many input lines and one output line. The function of the multiplexer is to select one of the input lines and connect it to the output.

Four Input Multiplexer: A four input multiplexer is shown in figure. There are four inputs I_0, I_1, I_2 and I_3 which are selectively transmitted to output Y depending on select input combinations. Here two select inputs are required as $2^N = 4$ where N is number of select inputs i.e. $N = 2$. Each data input is routed to output Y depending upon select input combination. When $S_1S_0 = 0, 0$ the input reaches output Y. The logic diagram for 4:1 multiplexer is given in figure.

The Boolean expression for output is:

$$Y = \overline{S_1} \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

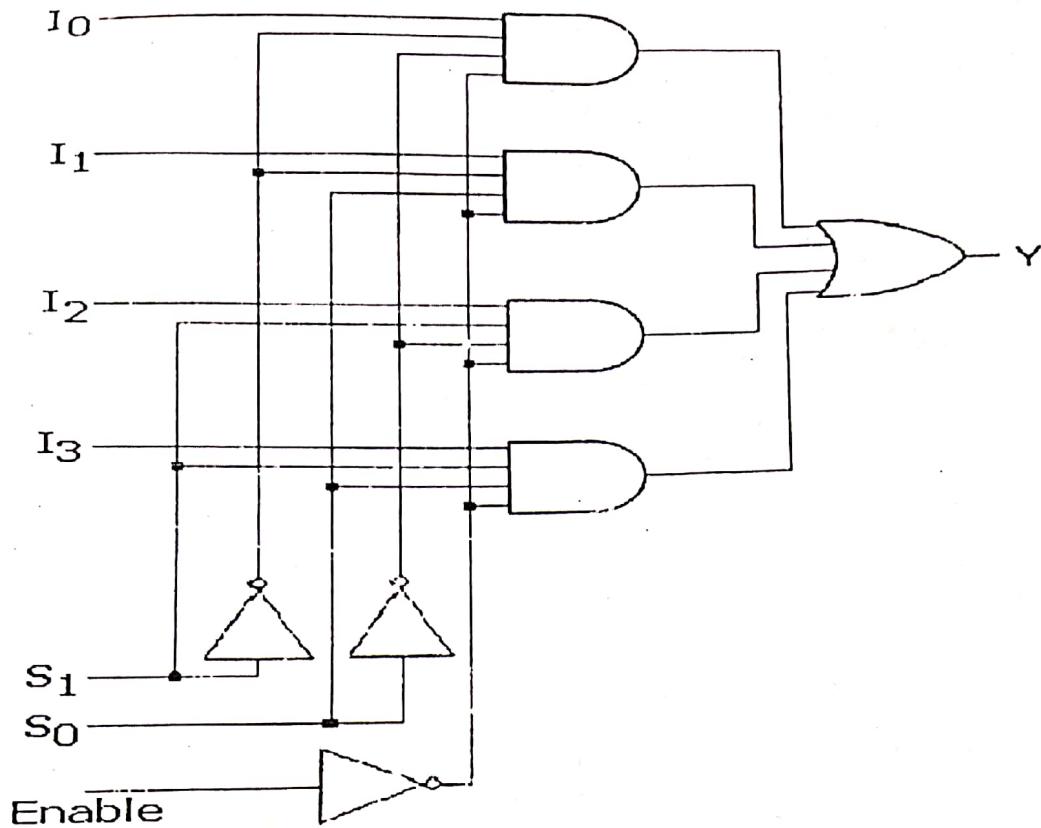


Fig: 4:1 MULTIPLEXER

TRUTH TABLE FOR 4:1 MULTIPLEXER

| Enable | Select Inputs | | Output Selected Y |
|--------|----------------|----------------|----------------------|
| | S ₀ | S ₁ | |
| 0 | 0 | 0 | I ₀ |
| 0 | 0 | 1 | I ₁ |
| 0 | 1 | 0 | I ₂ |
| 0 | 1 | 1 | I ₃ |

DEMULTIPLEXER: The demultiplexer is a digital circuit which has one input and many output lines. In other words the demultiplexer takes one input data source and selectively distributes it to N output channels. The number of select lines is S where $N = 2^S$.

1:4 Demultiplexer: Figure shows logic diagram for a demultiplexer that distributes one line (input) to four output lines. The single data input lines are connected to all AND gates. But only one of these lines will be enabled by select lines S_0, S_1 , e.g. $S_0S_1=0\ 0$, the D_0 will be available.

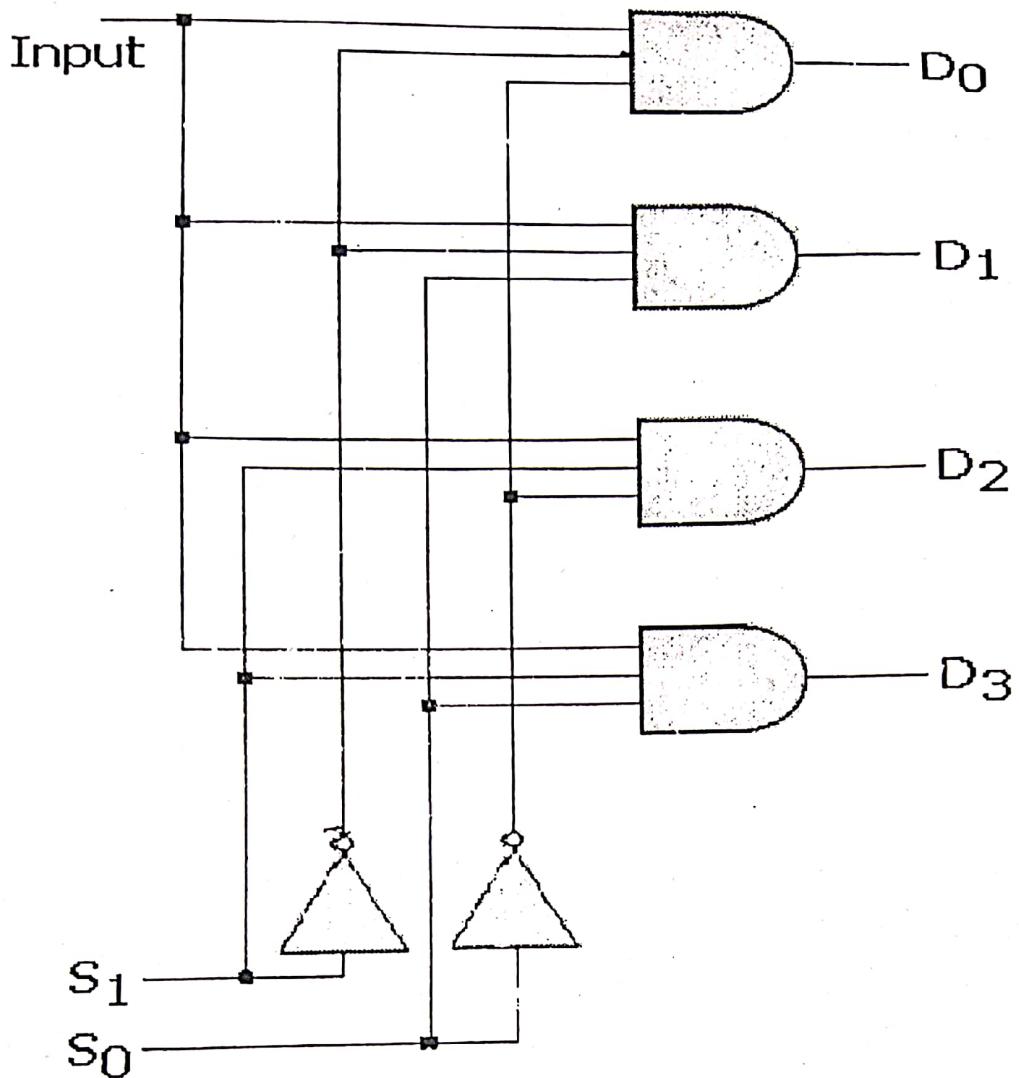


Fig: 1:4 DEMULTIPLEXER

TRUTH TABLE FOR 1:4 DEMULTIPLEXER

| Select Inputs | | | Outputs | | |
|----------------|----------------|----------------|----------------|----------------|----------------|
| S ₁ | S ₀ | D ₃ | D ₂ | D ₁ | D ₀ |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

PROCEDURE:

1. Take the IC's numbered 7404, 7408, 7432.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

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EXPERIMENT No: 07



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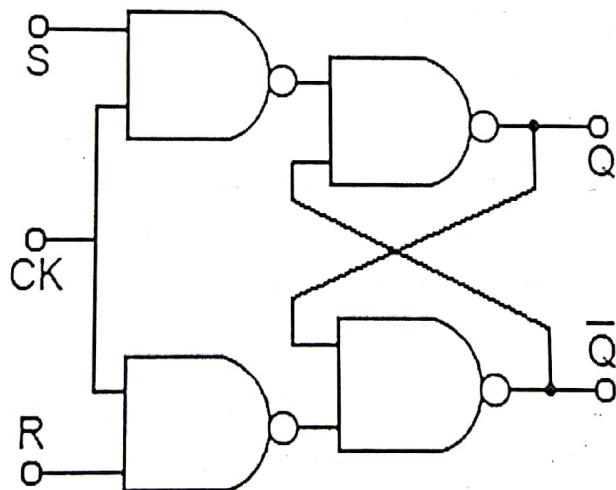
EXPERIMENT No. 7

AIM: Flip Flops: Truth -table verification and realization of SR, JK, T-type and D-type Flip -Flop using logic gates.

APPARATUS: Digital trainer kits, Logic gate IC's 7400, 7402, 7404, and 7408, connecting wires.

THEORY:

- S-R Flip flop:** It is required to set or reset the memory cell in synchronism with a train of pulses known as clock. Such circuit is referred to as a clocked set reset (S -R) FLIP FLOP. Also the circuit responds to the input signal only if the clock is present.



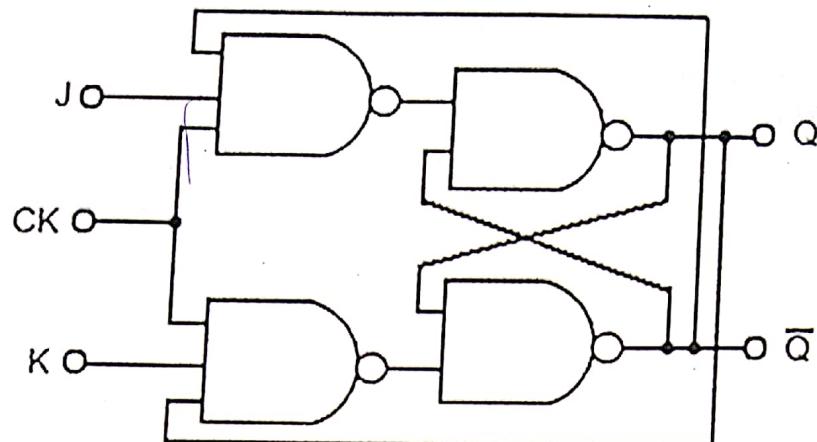
SR-FLIP FLOP

TRUTH TABLE OF SR-FLIP FLOP

| S | R | CLK | Outputs Q_{n+1} |
|---|---|-----|-------------------|
| 0 | 0 | ↑ | Q_n (No Change) |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | Ambiguous |

If $S_n = R_n = 0$ and CK is applied, the o/p at the end of the clock pulse is same as o/p before the clock pulse i.e. $Q_{n+1} = Q_n$.

2. **J-K Flip flop:** The uncertainty in the state of an S-R flip flop when $S_n = R_n = 1$ can be eliminated by converting it into a J-K flip flop.

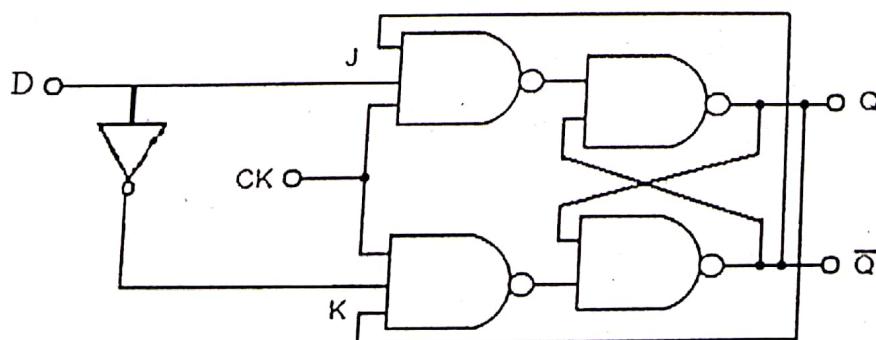


J-K FLIP FLOP

TRUTH TABLE OF J-K FLIP FLOP

| J | K | CLK | Outputs Q_{n+1} |
|---|---|-----|-------------------|
| 0 | 0 | ↑ | Q_n (No Change) |
| 0 | 1 | ↑ | 0 |
| 1 | 0 | ↑ | 1 |
| 1 | 1 | ↑ | Q_n (Toggles) |

3. **D-Type Flip flop:** The circuit diagram of D type flip flop shows that it has only one i/p reference to as D-input or data input. Its truth table shows that the output Q_{n+1} at the end of the clock pulse equal the input D_n before the clock pulse.



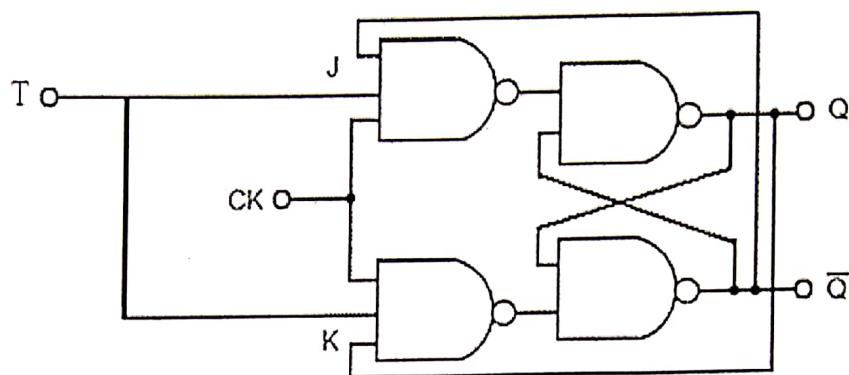
D-FLIP FLOP

TRUTH TABLE OF D-FLIP FLOP

| D | CLK | Outputs Q_{n+1} |
|---|-----|-------------------|
|---|-----|-------------------|

| | | |
|---|---|---|
| 1 | ↑ | 1 |
| 0 | ↑ | 0 |

4. **T-Type Flip flop:** In a J-K flip-flop, if $J = K$, the resulting flip flop is referred to as a T-type flip flop. It has only one input referred to as T-input. A truth table shows that if $T=1$ it acts as a toggle switch. For every clock pulse, the output Q changes.



T-FLIP FLOP

TRUTH TABLE OF T-FLIP FLOP

| T | CLK | Outputs Q_{n+1} |
|---|-----|-------------------|
| 1 | ↑ | Q_n |
| 0 | ↑ | \bar{Q}_n |

PROCEDURE:

1. Take the IC's numbered 7404, 7408, 7432.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 08



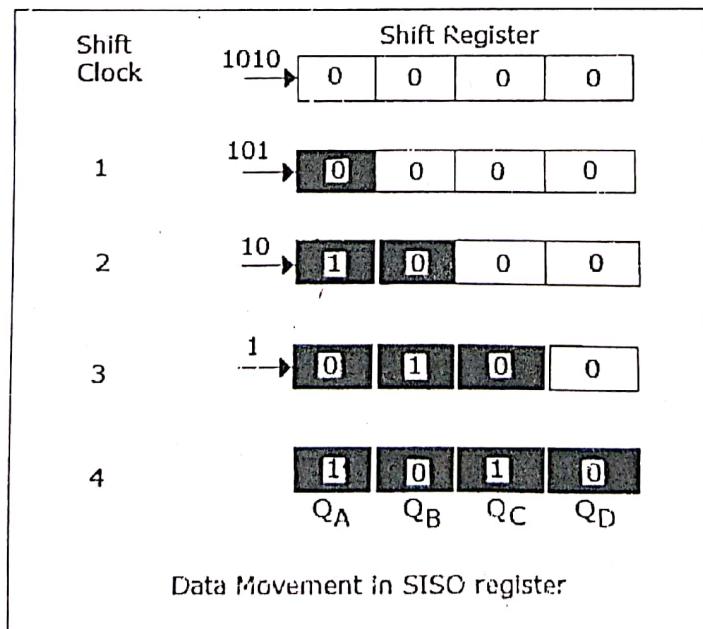
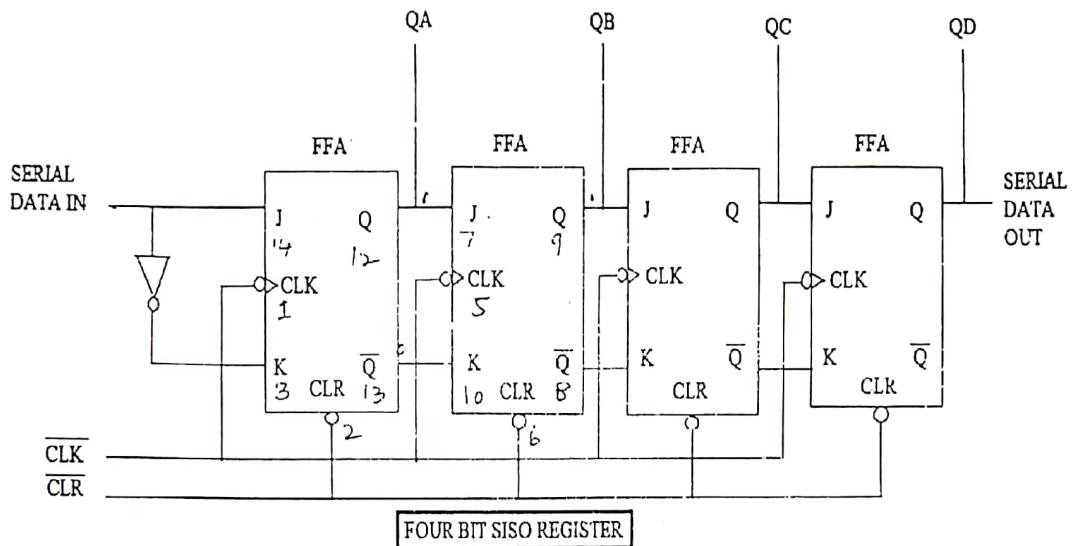
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EXPERIMENT No. 8

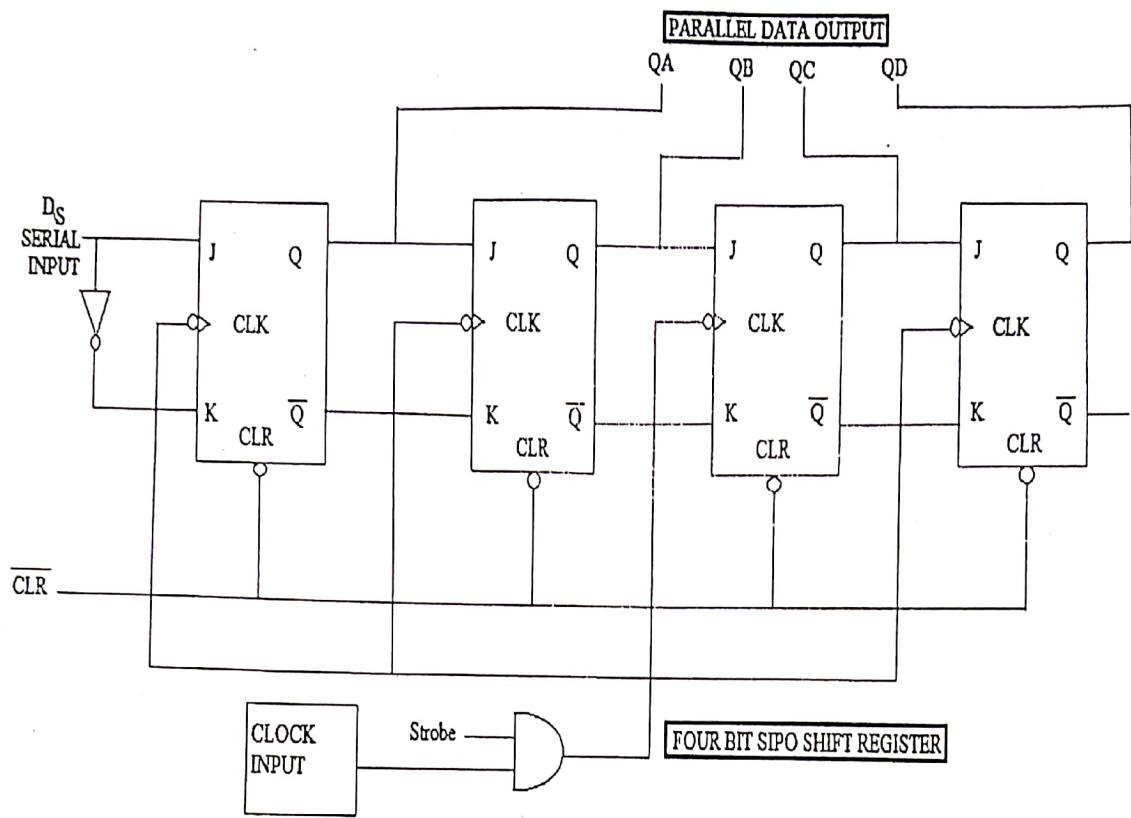
AIM: To design & verify operation of SISO; SIPO; and PISO, PIPO Shift Registers using JK flip flop and logic gates.

APPARATUS: Digital trainer kits, Logic gate & F/F IC's., Connecting wires.

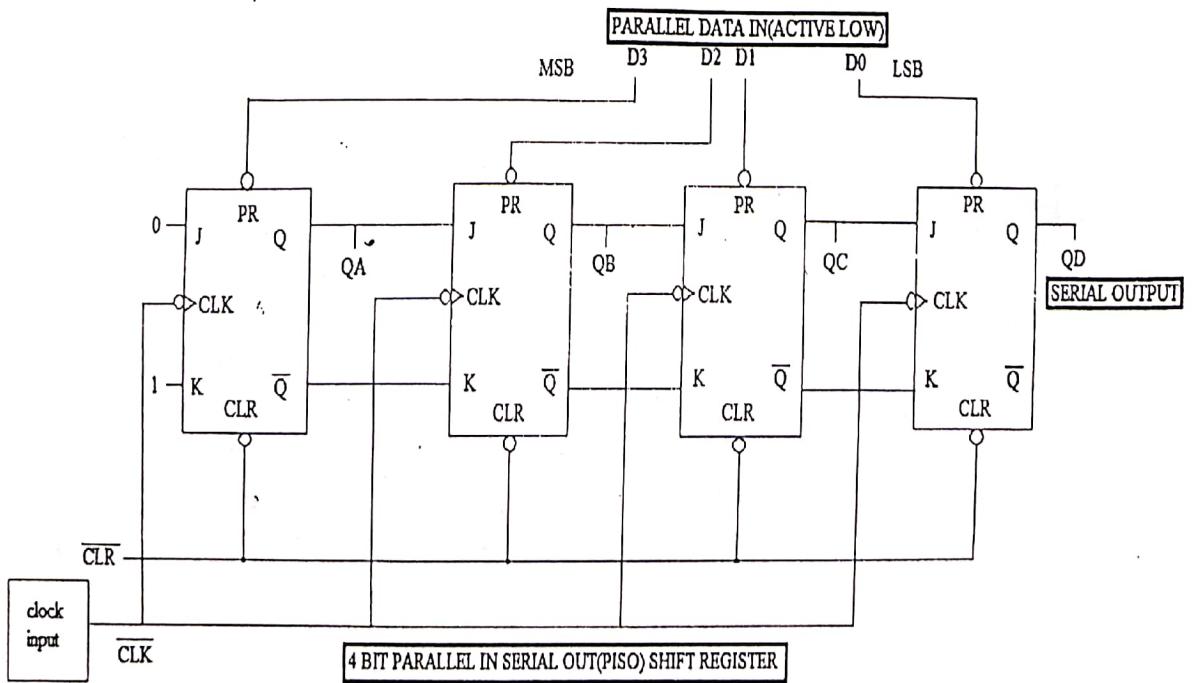
Four Bit SISO Register:



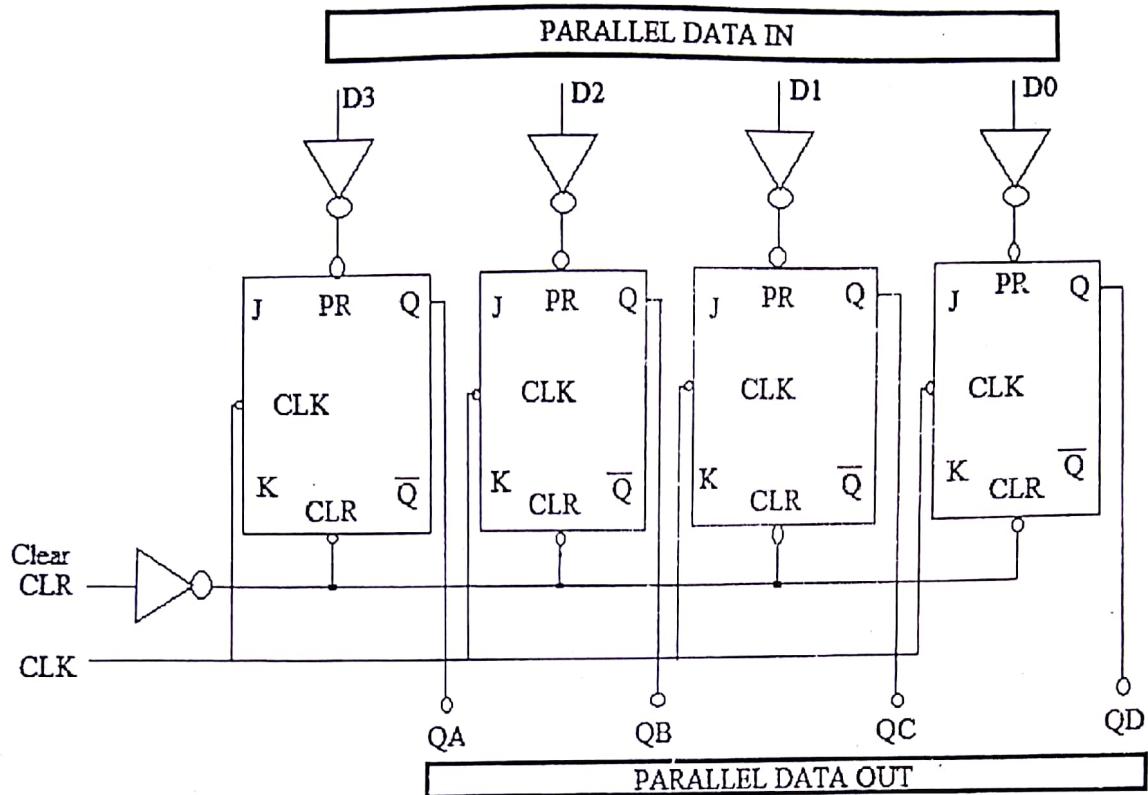
Four Bit SIPO shift register:



4 Bit Parallel in Serial out (PISO) shift register:



PIPO shift register:



PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 09



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EXPERIMENT No. 9

AIM: To design and implement the operation of Ring Counter and Johnson Counter using D-FFs.

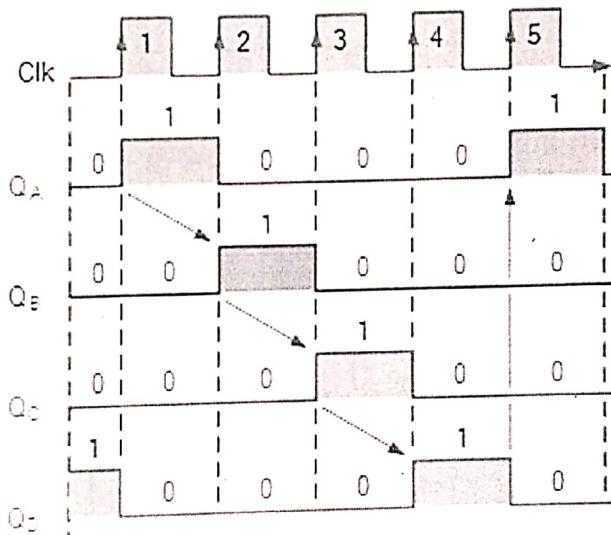
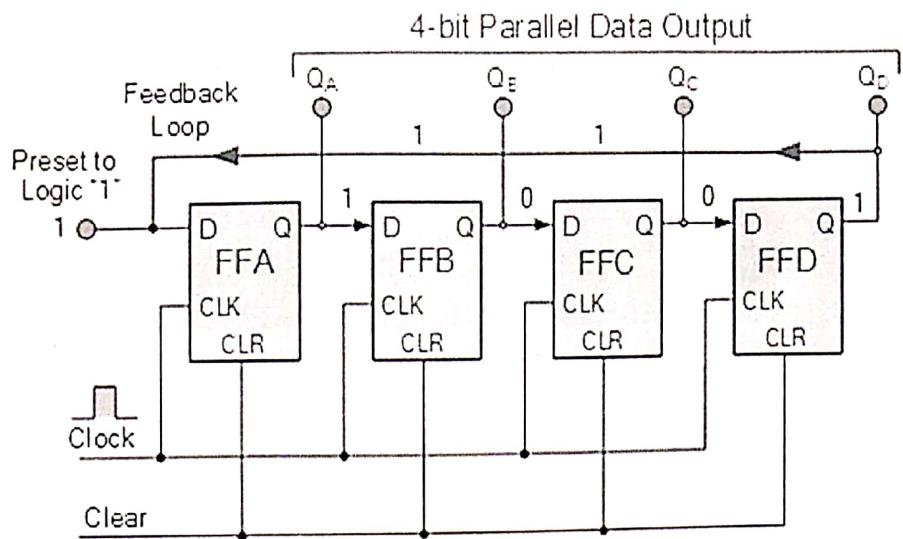
APPARATUS: Logic Trainer kit, IC 7474, Connecting leads.

THEORY:-

A Ring counter is a type of counter composed of flip-flops connected into a shift register, with the output of the last flip-flop fed to the input of the first, making a "circular" or "ring" structure. The synchronous Ring Counter, is preset so that exactly one data bit in the register is set to logic "1" with all the other bits reset to "0". To achieve this, a "CLEAR" signal is firstly applied to all the flip-flops together in order to "RESET" their outputs to a logic "0" level and then a "PRESET" pulse is applied to the input of the first flip-flop (FFA) before the clock pulses are applied. This then places a single logic "1" value into the circuit of the ring counter.

CIRCUIT AND TIMING DIAGRAM:

On each successive clock pulse, the counter circulates the same data bit between the four flip-flops over and over again around the "ring" every fourth clock cycle. But in order to cycle the data correctly around the counter we must first "load" the counter with a suitable data pattern as all logic "0's" or all logic "1's" outputted at each clock cycle would make the ring counter invalid. This type of data movement is called "rotation", and like the previous shift register, the effect of the movement of the data bit from left to right through a ring counter can be presented graphically as follows along with its timing diagram:



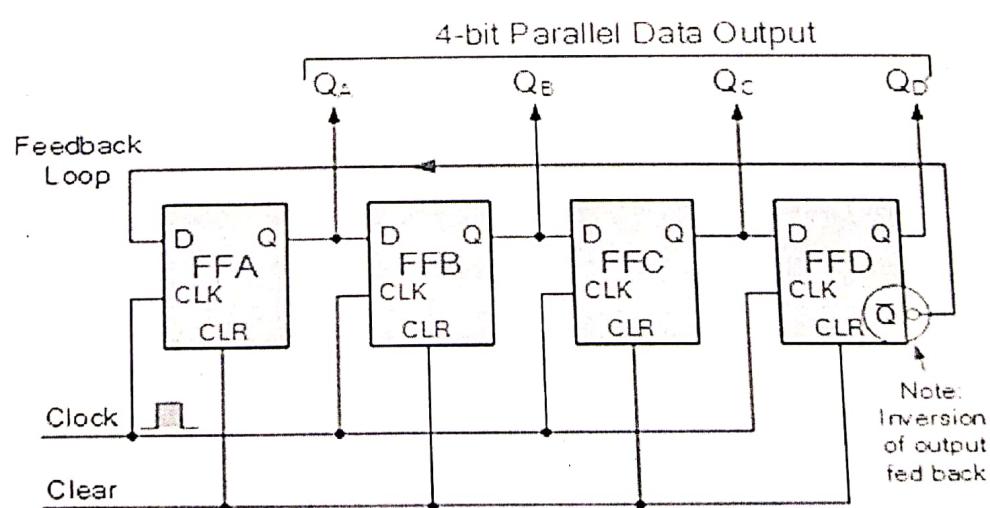
A binary counter can represent 2^N states, where N is the number of bits in the code, whereas a straight ring counter can represent only N states and a Johnson counter can represent only $2N$ states. This may be an important consideration in hardware implementations where registers are more expensive than combinational logic.

Johnson Ring Counter

The Johnson Ring Counter or "Twisted Ring Counter", is another shift register with feedback exactly the same as the standard Ring Counter above, except that this time the inverted output Q of the last flip-flop is now connected back to the input D of the first flip-flop as shown below.

The main advantage of this type of ring counter is that it only needs half the number of flip-flops compared to the standard ring counter then its modulo number is halved. So a “n-stage” Johnson counter will circulate a single data bit giving sequence of 2^n different states and can therefore be considered as a “mod- 2^n counter”.

| Clock Pulse No | FFA | FFB | FFC | FFD |
|----------------|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 0 |
| 3 | 1 | 1 | 1 | 0 |
| 4 | 1 | 1 | 1 | 1 |
| 5 | 0 | 1 | 1 | 1 |
| 6 | 0 | 0 | 1 | 1 |
| 7 | 0 | 0 | 0 | 1 |



Truth Table for a 4-bit Johnson Ring Counter

PROCEDURE:

1. Make the connection as shown in the figure.
2. Switch on the power supply,
3. Verify the Truth Table for Ring Counter and Johnson Ring Counter

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 11

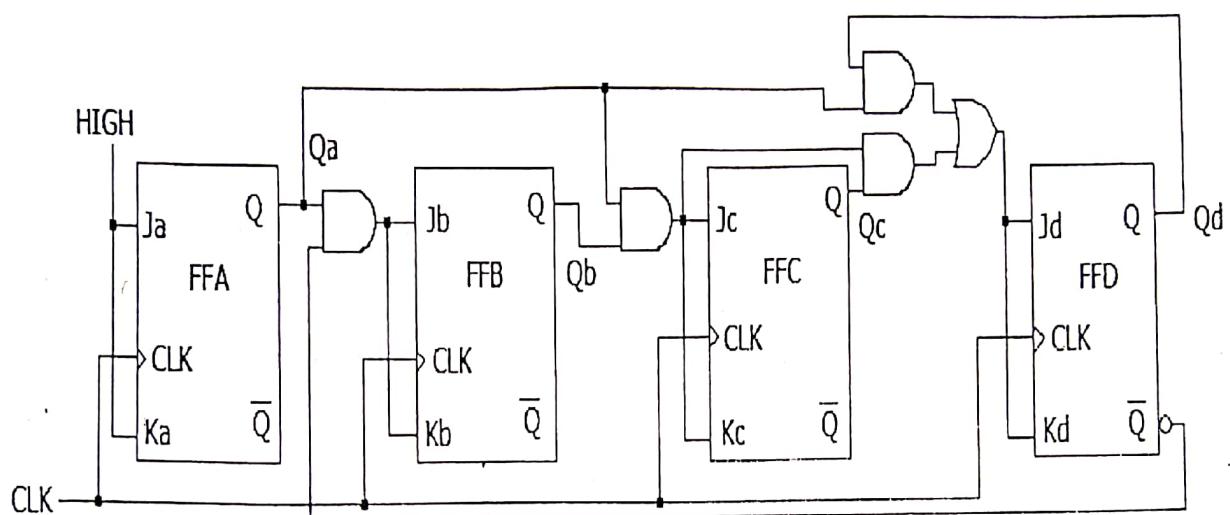


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EXPERIMENT No. 11

AIM: To design & verify operation of Synchronous BCD Decade counter using J-K flip flop.

APPARATUS: Digital trainer kits, Logic gate & F/F IC's., Connecting wires.
Synchronous BCD Decade counter:



Synchronous BCD Decade Counter

Table: Sequence of states for BCD Counter

| Clock Pulse | Q _D | Q _C | Q _B | Q _A |
|-------------|----------------|----------------|----------------|----------------|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

PROCEDURE:

1. Take the IC's mentioned in apparatus required.
2. Place them properly on their respective places.
3. Make the connections as per the circuit diagram.
4. The circuit can be verified using various values of inputs and then testing the values of output as per truth table.

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.

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EXPERIMENT No: 12



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EXPERIMENT No. 12

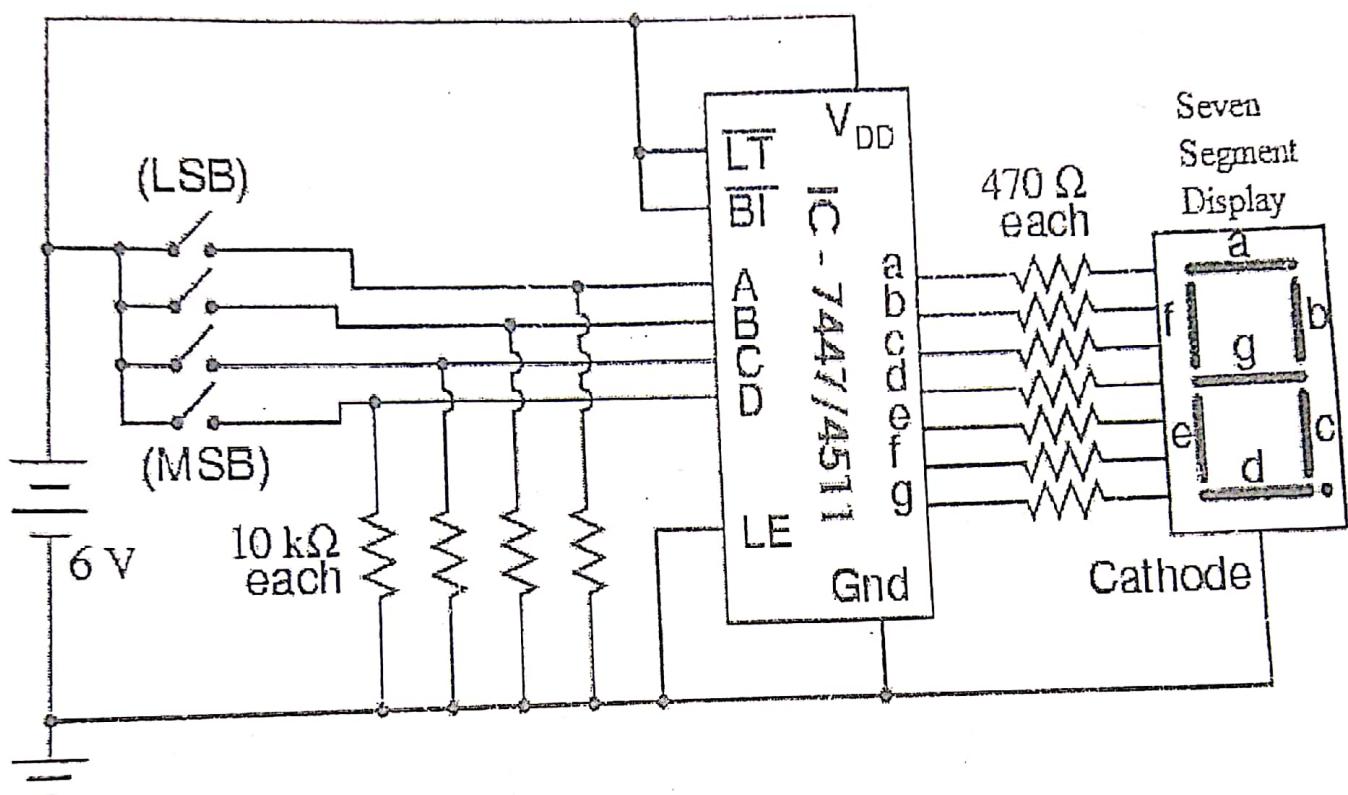
AIM: To Design BCD to Seven Segment Display driver circuit using IC 7447.

APPARATUS: Logic Trainer kit, IC 7447/4511, 7 segment display (Common cathode), Connecting leads.

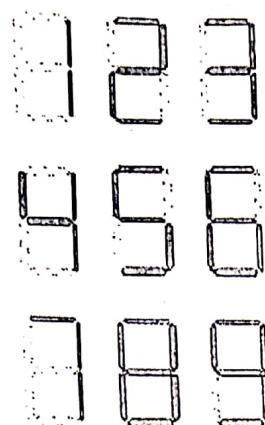
THEORY:-

A BCD to 7-segment decoder/driver is used as a 4-bit BCD input and provides the outputs that will pass current through the appropriate segment to display the decimal digit. For display numerical digit, a 7-segment configuration is used to form the decimal character 0 to 9 and sometimes the hex character A through F. One common arrangement uses light emitting diode (LED'S) for each segment, by controlling the current through each LED. Some segment will pass light through and other will dark so that the desired character pattern will be generated.

CIRCUIT DIAGRAM:

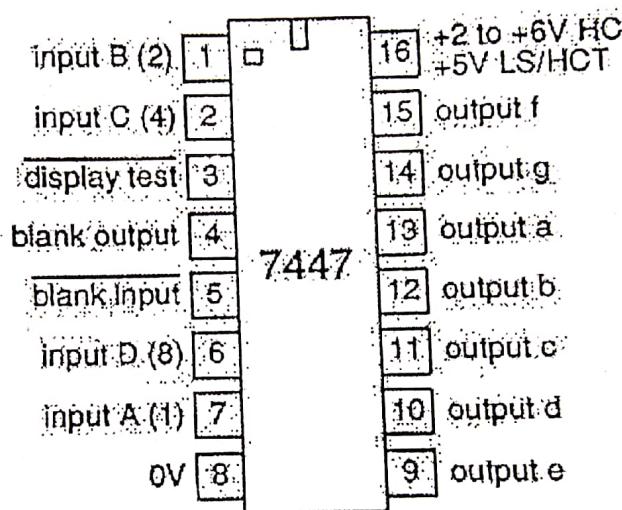


TRUTH TABLE:



| Digit Shown | Illuminated Segment (1 = illumination) | | | | | | |
|----------------|--|---|---|---|---|---|---|
| | a | b | c | d | e | f | g |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 9 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

PIN DESCRIPTION:



PROCEDURE:

1. Make the connection as shown in the figure.
2. Switch on the power supply,
3. Verify the Truth Table for BCD to seven segment display
4. If the LED glows, output is at logic "1" otherwise at logic "0".

PRECAUTIONS:

1. Circuit should be properly connected.
2. Do not short circuit in the trainer kit during operation.
3. Wires should be held by their heads while being removed else they may get damage.