

01

Thursday

September  
2011

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1. Subject Code: EP 207 Course Title: Digital Electronics (Engineering Analysis and Design)  
 2. Contact Hours: L: 3 T: 0 P: 2  
 3. Examination Duration (Hrs.) Theory: 3 Practical: 0  
 4. Relative Weight: CWS: 15 PRS: 15 MTE: 30 ETE: 40 PRE: 0  
 5. Credits: 4  
 6. Semester: ODD  
 7. Subject Area: DCC  
 8. Pre-requisite: NIL  
 9. Objective: To familiarize the student with the concept of Boolean algebra, logic gates, sequential and combinational circuits, counters and RAMs.  
 10. Details of Course:

S. No.	Contents	Contact Hours
1.	Minimization Techniques: Boolean postulates and laws – De-Morgan's Theorem-Principle of Duality	3
2.	Boolean expression - Minimization of Boolean expressions — Minterm – Maxterm	1
3.	Sum of Products (SOP) – Product of Sums (POS) – Karnaugh map Minimization, Don't care conditions	3
4.	Implementation of Logic Functions using gates, NAND-NAND and NOR-NOR implementations.	2
5.	BCD and XS3 Addition, Gray Codes	1
6.	1's complement and 2's complement subtraction.	3
7.	Introduction to the circuits for Arithmetic UNIT: Design procedure – Half adder – Full Adder – Half subtractor – Full subtractor	1
8.	Parallel binary Adder/Subtractor –Serial Adder/Subtractor - BCD adder - 2's complement adder/subtractor	3
9.	Multiplexer, Demultiplexer, Decoder, Encoder,	2
10.	Latches, Flip-flops - SR, JK, D, T, and Master-Slave – Characteristic table and equation – Edge triggering – Level Triggering	2
11.	Realization of one flip flop using other flip flops.	2
12.	Registers – shift registers - Bidirectional shift registers, serial and parallel configurations.	1
13.	Shift register counters – Ring counter, Johnson counter, Asynchronous Ripple or serial counter	3
14.	Asynchronous Up/Down counter - Synchronous counters – Synchronous Up/Down counters – Programmable counters	1
15.	Design of Synchronous counters: state diagram- State table –State minimization –State assignment - Excitation table and Circuit implementation	2
16.	Modulo-n counter,– Non-Sequential Counter Design using JK, D and T-design.	2
17.	Introduction to VHDL-Behavioural Modeling, Dataflow Modeling, Structural Modeling, Application in Digital System Designs.	2
18.	Digital to analog converter: Binary Weighted Resistors, Analog to digital converter-Successive Approximation Method,	1
19.	Logic gates, DTL, TTL, ECL, I <sup>2</sup> L, CMOS Gates and their parameters and comparisons.	2
20.	Classification of memories – ROM - ROM organization - PROM – EPROM – EEPROM – EEPROM	2
21.	RAM – RAM organization – Write operation – Read operation, memory expansion	2
22.	Static RAM Cell-Bipolar RAM cell – MOSFET RAM cell – Dynamic RAM cell	1

Intelligence without ambition is a bird without wings.

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### Topic I

#### Boolean's Law

$$\begin{array}{l} 1. \quad \overline{0} = 1 \\ 2. \quad \overline{1} = 0 \\ 3. \quad \overline{A} = A \\ 4. \quad \overline{A} = 0 \\ 5. \quad \overline{\overline{A}} = A \end{array}$$

} NOT Law

$$\begin{array}{l} 6. \quad A \cdot 0 = 0 \\ 7. \quad A \cdot 1 = A \\ 8. \quad A \cdot A = A \\ 9. \quad A \cdot \overline{A} = 0 \end{array}$$

} AND Law

$$\begin{array}{l} 10. \quad A + 0 = A \\ 11. \quad A + 1 = 1 \\ 12. \quad A + A = A \\ 13. \quad A + \overline{A} = 1 \end{array}$$

} OR Law.

$$\begin{array}{l} 14. \quad A + B = B + A \\ 15. \quad A \cdot B = B \cdot A \end{array} \quad \left. \right\} \text{Commutative Law.}$$

$$\begin{array}{l} 16. \quad A + (B + C) = (A + B) + C \\ 17. \quad A \cdot (B \cdot C) = (A \cdot B) \cdot C \end{array} \quad \left. \right\} \text{Associative Law.}$$

$$\begin{array}{l} 18. \quad A \cdot (B + C) = (A \cdot B) + (A \cdot C) \\ 19. \quad A + (\overline{A} \cdot B) = A + B \\ 20. \quad A + (B \cdot C) = (A + B) \cdot (A + C) \end{array} \quad \left. \right\} \text{Distributive Law.}$$

$$\begin{array}{l} 21. \quad \overline{A + B + C + \dots + N} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \dots \cdot \overline{N} \\ 22. \quad \overline{A \cdot B \cdot C \cdot \dots \cdot N} = \overline{A} + \overline{B} + \overline{C} + \dots + \overline{N} \end{array} \quad \left. \right\} \text{De-Morgan's Theorem.}$$

Kindle not a fire that you cannot extinguish.

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Theorem of Duality → we can convert to other Boolean expression.

#### Boolean Relation

$$A + B = B + A$$

$$A + (B + C) = (A + B) + C$$

$$A \cdot (B + C) = A \cdot B + A \cdot C$$

$$A + 0 = A$$

$$A + 1 = 1$$

$$A \cdot A = A$$

$$A \cdot \overline{A} = 0$$

$$\overline{A} = A$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$A + AB = A$$

$$A + \overline{A}B = A + B$$

#### Dual

$$AB = BA$$

$$A(BC) = (AC)B$$

$$A + BC = (A + B)(A + C)$$

$$A \cdot 1 = A$$

$$A \cdot 0 = 0$$

$$A \cdot A = A$$

$$A \cdot \overline{A} = 0$$

$$\overline{A} = A$$

$$\overline{AB} = \overline{A} + \overline{B}$$

$$A(A + B) = A$$

$$A \cdot (\overline{A} + B) = AB$$

#### Topic 2

#### Minterms / Maxterms for 3 Variables

##### Variable

$$A \ B \ C$$

$$0 \ 0 \ 0$$

$$0 \ 0 \ 1$$

$$0 \ 1 \ 0$$

$$0 \ 1 \ 1$$

$$1 \ 0 \ 0$$

$$1 \ 0 \ 1$$

$$1 \ 1 \ 0$$

$$1 \ 1 \ 1$$

##### Minterms

$$m_0$$

$$\overline{A} \overline{B} \overline{C}$$

$$\overline{A} \overline{B} C$$

$$\overline{A} B \overline{C}$$

$$A \overline{B} \overline{C}$$

$$A \overline{B} C$$

$$A B \overline{C}$$

$$A B C$$

##### Maxterm

$$M_0$$

$$A + B + C$$

$$A + B + \overline{C}$$

$$A + \overline{B} + C$$

$$A + \overline{B} + \overline{C}$$

$$A + B + \overline{C}$$

$$A + B + C$$

$$\overline{A} + B + C$$

$$\overline{A} + B + \overline{C}$$

Many talk like philosophers and live like fools.

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TOPIC - 3

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$$\text{Q } Y(A, B, C, D) = \Sigma(0, 2, 3, 5, 7, 8, 9, 10, 13, 15)$$

SOP

	A	B	C	D	
	AB	AC	AD	CD	
	CD	BD	BC	BCD	
	BD	BD	BD	BD	
	CD	CD	CD	CD	
	BD	BD	BD	BD	
	CD	CD	CD	CD	
	BD	BD	BD	BD	

$$Y = BD + AC\bar{D} + \bar{A}C\bar{D}$$

	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	
	AB	CD	CD	CD	

$$Y = BD + \bar{A}\bar{B}C + A\bar{B}\bar{C} + \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}D$$

$$Y = BD + A\bar{B}C + A\bar{B}\bar{C} + B\bar{D}(C + \bar{C})$$

$$Y = BD + \bar{B}\bar{D} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$$

Notes

He who goes a borrowing goes a sorrowing.

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POS

$$Y(A, B, C, D) = \Sigma(3, 4, 5, 7, 9, 13, 14, 15)$$

	CD	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD
	AB	CD	CD	CD	CD

$$Y = (\bar{A}\bar{B}\bar{C}) + (\bar{C}\bar{D}\bar{A}) + (A\bar{C}\bar{D}) + (\bar{A}\bar{B}C)$$

$$Y = (A+B+C) \cdot (A+\bar{C}+D) \cdot (\bar{A}+C+D) \cdot (\bar{A}+B+\bar{C})$$

→ The don't care conditions

Two variable truth table.

A	B	F
0	0	Φ
0	1	f <sub>1</sub>
1	0	f <sub>2</sub>
1	1	Φ

He is a good physician who cures himself.

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For SOP, the don't care conditions are taken as one.

For POS, the don't care conditions are taken as zero.

$$Y(A, B, C, D) = \sum(1, 3, 5, 8, 9, 13) + \sum_d(0, 7, 12, 14)$$

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AB	CD	CD	CD	CD
$\bar{A}B$	$\phi$	0	1	1
$\bar{A}B$	0	1	1	$\phi$
AB	$\phi$	1	1	1
AB	1	0	1	$\phi$

$$\text{SOP } Y = AC + \bar{A}D + \bar{C}D$$

$$\text{POS } Y = (\bar{A}+C) \cdot (A+\bar{D}) \cdot (\bar{C}+\bar{D})$$

AB	CD	CD	CD	CD
$\bar{A}B$	$\phi$	0	1	1
$\bar{A}B$	0	1	1	$\phi$
AB	$\phi$	1	1	1
AB	1	0	1	$\phi$

$$Y = AC + \bar{A}D + \bar{C}D$$

$$\text{POS } Y = (\bar{A}+C) \cdot (A+\bar{D}) \cdot (\bar{C}+\bar{D})$$

How can one pole build a great house?

0	0	0	0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	0
5	0	1	1
6	0	1	0
7	0	1	1
8	1	0	0
9	1	0	1

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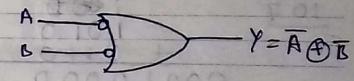
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### Topic 34

\* Implementation of Logic functions using gates

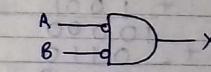
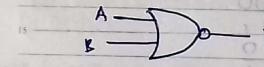
⇒ NAND.

$$\bar{A}\bar{B} = \bar{A} + \bar{B}$$



⇒ NOR.

$$A+B = \bar{A} \cdot \bar{B}$$



### Topic 5

#### BCD Addition

(Binary coded decimal)

$$8421 \\ 2^3 2^2 2^1 2^0$$

Rules of addition.

⇒ If the sum is obtained is less than or equal to 9, then it is a valid BCD result.

⇒ Sum > 9 → invalid

To make valid add 6 decimal number (0110)

If you act like a worm, why blame others for stepping on you.

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<u>eg 1</u>	77	0 111	0 100	0 0000
	23	<u>0 810</u>	<u>0011</u>	0 0001
	97	<u>1 800</u>	<u>0111</u>	0 0100
<u>eg 2</u>	77	11	0 100	0 100
	33	<u>0 111</u>	<u>0011</u>	0 101
	107	<u>00101</u>	<u>0111</u>	0 110
		1010		0 111
12		+ 0110		1 000
			0111	1 001
		0001 0000		

$$\begin{array}{r}
 \text{15} \\
 \text{173} \\
 \frac{17}{\underline{94}} \\
 \text{171}
 \end{array}
 \quad
 \begin{array}{r}
 \text{16} \\
 \text{00010111} \\
 + 00010111 \\
 \hline
 \text{00010111}
 \end{array}
 \quad
 \begin{array}{r}
 \text{17} \\
 \text{0111} \\
 + 0100 \\
 \hline
 \text{1011}
 \end{array}
 \quad
 \begin{array}{r}
 \text{16} \\
 \text{0110} \\
 + 0111 \\
 \hline
 \text{0001}
 \end{array}$$

## For Subtraction

\* Case 1:  
If :- 1<sup>st</sup> no > 2<sup>nd</sup> no

① Takes 2's complement of 2<sup>nd</sup> no. and add to 1<sup>st</sup> no.

(ii) While adding if any four-bit group does not produce a carry, or if the result obtained is greater than  $q$ , then subtract  $b$  from that 4-bit result by the 2's complement method. During this operation, if a carry is produced, neglect the carry.

"If a man does his best, what else is there?"

For more information about the study, please contact Dr. Michael J. Hwang at (319) 356-4000 or email at [mhwang@uiowa.edu](mailto:mhwang@uiowa.edu).

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eg 1) Sub 0111 1000 1000 - 0011 1000 0010

→ 2's complement of 2nd no

$$\begin{array}{r}
 \text{Add 1} \\
 \hline
 1100.0111 .1110
 \end{array}$$

→ Add 1'st no & 2's complement.

$$\begin{array}{r}
 & 1100 & 0111 & 1110 \\
 & + 0111 & \hline
 10100 & 0000 & 0110
 \end{array}$$

neglect  $\rightarrow$

$\star$  Case 2:  $\rightarrow$  If  $2^{\text{nd}}$  no.  $> 1^{\text{st}}$  no.

① Takes 2's complement of 2<sup>nd</sup> no and add to 1<sup>st</sup> no and then take 2's complement.

⑪ While adding, if any four-bit group produces a carry or if the result obtained is greater than 9, then take the 2's complement of the result and subtract 6 from that four-bit group which produced a carry by the 2's complement method. During this operation, if a carry is produced by a four-bit group, neglect the carry.

(iii) Write the result with a minus sign.

If you speak insults, you will hear them.

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Eg 1) Sub  $(0111\ 1001) - (1000\ 0001)$

2's complement :-

1000 0001	As it produces carry
0111 1110	so
Add 1	2's comp - 1000
↓ 1st no +	1st comp 0111
1111 1001	Add 1 ↓ 1
2's complement $\Rightarrow$ 0000 0111	2's comp 1010
= 0000 0111	Add 6 0010
(000000010)	0010

Eg 2) Sub  $(0111\ 0110 \cdot 0010\ 0110) - (1000\ 0001 \cdot 0101\ 0111)$

2's complement :-

1000 0001 · 0101 0111	→ 2's comp 1100
0111 1110 · 1010 1000	+ 1
↓ 1st no +	0111 0110 · 0011 0011
1111 0100 · 1100 1111	→ 2's comp 1010
2's Comp :	2's comp - 0000 1011 · 0011 0000
Add 1	+ 1
0000 1011 · 0011 0001	As it produces carry 1010
So add 2's comp of 6	(00000101 · 00110001)

If the devil finds a man idle, he'll set him to work.

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X3 additionRules of addition

⇒ Add 3 (digit तीन) then obtain 4-bit binary equivalent  
→ to both numbers.

⇒ If carry produced then add 0011 to no produce carry.

⇒ If carry not produced then subtract 0011 from that group.

Eg 1) Add 123 and 536

123	536
333	333
456	869
→ 0100 0101 0100	
+ 1000 0110 1001	
1101 1011 1111	
- 0011 0011 0011	
1001 1000 1100	

$$\begin{array}{r} 1-0=1 \\ 10-1=1 \\ 0-0=0 \\ 1-1=0 \end{array}$$

For subtraction

\* Case 1 : → 2nd no < 1st no.

① Add 3 to each digit. Obtain 4-bit binary.

② Perform sub by 2's complement.

③ If carry produced add 0011 to group  
If carry not produced sub 0011 from the group

If there is a way to do it better... find it.

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Tue 1 9 15 22 29  
Wed 2 12 18 25  
Thu 3 13 20 27  
Fri 4 14 21 28  
Sat 5 15 22 29  
Sun 6 16 23 30Eg Sub 536 and 123.

$$\begin{array}{r} 536 \\ 333 \\ 869 \\ \hline 456 \end{array}$$

$$\begin{array}{r} 1000 0110 1001 \\ +011 1010 1010 \\ \hline \end{array}$$

$$1000 0110 1001 - \cancel{0110} 0101010$$

$$\begin{array}{l} 2^{\text{nd}} \text{ comp of } 2^{\text{nd}} \text{ no} = 0100 01010110 \\ 1^{\text{st}} \text{ comp} = 1001 1010 1001 \end{array}$$

$$\begin{array}{r} +1 \\ \hline 1001 1010 1010 \end{array}$$

$$\begin{array}{l} \text{Now Add } 1^{\text{st}} \text{ no} \\ \text{2nd} \quad \begin{array}{r} 1000 0110 1001 \\ +1011 1010 1010 \\ \hline 0110 0001 0011 \\ +0011 0011 0011 \\ \hline 0111 0100 0110 \end{array} \end{array}$$

$$\underline{\text{Ans}} = 0111 0100 0110$$

(Case II) 1<sup>st</sup> no < 2<sup>nd</sup> no.

- (I) Add 3 to each digit both no. Obtain 4-bit binary.
- (II) Invert Sub by 2<sup>nd</sup> comp.
- (III) If carry produced - Sub 0011 from 2<sup>nd</sup> comp of result.

He is a good friend that speaks well of us behind our backs.

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(IV) If carry not produced, add 0011 to the 2's comp of the result

Eg Sub 123 and 536

$$\begin{array}{r} 123 \\ +333 \\ \hline 456 \end{array}$$

$$\begin{array}{r} 456 - 0100 0101 0110 \\ 869 - 1000 0110 1001 \end{array}$$

$$\begin{array}{l} 2^{\text{nd}} \text{ comp} \\ 1^{\text{st}} \text{ comp} \\ \text{Add 1} \end{array} \begin{array}{r} 0111 1001 0110 \\ +0111 1001 0111 \\ \hline 0111 1001 0111 \end{array}$$

$$\begin{array}{l} \text{Add 1st no} \\ 2^{\text{nd}} \text{ comp} \\ 2^{\text{nd}} \text{ comp} \\ \text{Add 1} \end{array} \begin{array}{r} 0100 0101 0110 \\ +0111 1001 0111 \\ 1011 1110 1101 \\ 0100 0001 0010 \\ +1 \\ 0110 0001 0011 \\ -0011 -0011 -0011 \\ 0000 0010 0000 \\ 0111 0100 0110 \end{array}$$

Ans

\* Carry Code → There is Only one bit change since go from one number to the next in sequence. We first start with all zeroes and then produce it by carrying the LSB to bring the new state.

Hold fast to dreams, for if dreams die, life is a broken bird that cannot fly.

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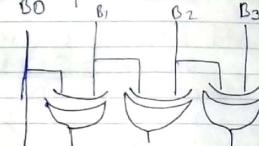
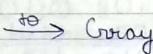
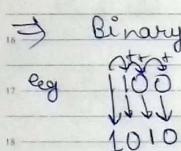
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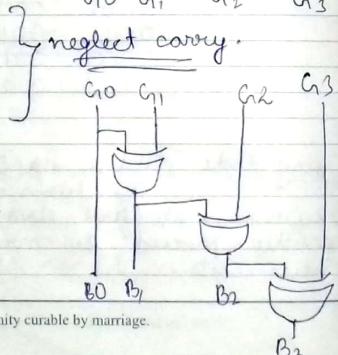
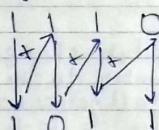
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Thu	10 17 24
Fri	11 18 25
Sat	12 19 26
Sun	13 20 27

Decimal no	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	01 <u>11</u> 11	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010



$\Rightarrow$  Convert to Binary



Love is a temporary insanity curable by marriage

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Topic 6

- (i) Take the 1's comp. of 2nd no.
- (ii) Add to the 1st no.
- (iii) If there is a carry add to the result.
- (iv) If no carry take 1's complement. Write the answer with negative sign.

$$\text{eg. } \begin{array}{r} 11 \\ - 11001101 \\ \hline 11110000 \end{array}$$

12 1's comp:  $\begin{array}{r} 11001101 \\ \downarrow \\ 00110010 \end{array}$

$$\begin{array}{r}
 \text{Add both no :-} \quad 1111\ 0000 \\
 + \quad 0011\ 0010 \\
 \hline
 1001\ 0001\ 0 \\
 \downarrow \qquad \qquad \qquad \downarrow \\
 \text{Carry } 0010001
 \end{array}$$

Eg 2 Sub 1100 1101 - 1111 0000  
                  1111 0000

18 J's comp 0000 1111

$$\begin{array}{r} \text{Add both no:-} \\ \begin{array}{r} 11001101 \\ + 00001111 \\ \hline 11011100 \end{array} \end{array}$$

No carry.

$$\begin{array}{r} \text{1st comp of result} \\ -0010001 \\ \hline 11011100 \end{array}$$

*Journal of Health Politics, Policy and Law*, Vol. 35, No. 4, December 2010  
DOI 10.1215/03616878-35-4 © 2010 by The University of Chicago

09

October

2011

Sunday

Wk-41 • 282-083

(15)

October		2011	
Mon	3	10	17
Tue	4	11	18
Wed	5	12	19
Thu	6	13	20
Fri	7	14	21
Sat	8	15	22
Sun	9	16	23

### \* 2's complement Subtraction

① Takes 2's comp of 2nd no.

② Add to the 1st no.

③ If carry neglect it.

④ If no carry, take 2's comp of result and write ans with -ve sign.

Ex 1) Sub  $11110000 - 11001101$

2's comp of 2nd no.

$$\begin{array}{r} 11001101 \\ 1's \text{ comp} : - 00110010 \\ \text{Add } 1 \\ \hline 2's \text{ comp} : \rightarrow 00110011 \end{array}$$

Add both nos

$$\begin{array}{r} 11110000 \\ + 00110011 \\ \hline 100100011 \end{array}$$

↑  
Carry (neglect)

$$\text{Ans} = 00100011$$

Ex 2) Sub  $11110000$  from  $11001101$

2's comp of 2nd no.

$$\begin{array}{r} 11110000 \\ 1's \text{ comp} : 00001111 \\ \text{Add } 1 \\ \hline 00010000 \end{array}$$

Add 1's no & 2's comp.

A sleeping fox counts hens in his dreams.

November		2011	
Mon	7	14	21
Tue	8	15	22
Wed	9	16	23
Thu	10	17	24
Fri	11	18	25
Sat	12	19	26
Sun	13	20	27

(16)

October

2011

Wk-42 • 283-083

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Monday

$$\begin{array}{r} 11001101 \\ 00010000 \\ \hline 11011101 \end{array}$$

(no carry)

Take 2's comp

$$\begin{array}{r} 11011101 \\ 1's \text{ comp} : 00100010 \\ \text{Add } 1 \\ \hline 00100011 \end{array}$$

$$\text{Ans} = -00100011$$

### Topic 7

\* Half Adder : → It is a combinational circuit that can add only two binary bits together. The circuit have 2 input

#### Half adder - truth table

	Input A	Input B	Output Sum(S)	Carry(Cout)
Notes	0	0	0	0
	0	1	1	0
Notes	1	0	1	0
	1	1	0	1

A lean compromise is better than a fat lawsuit.

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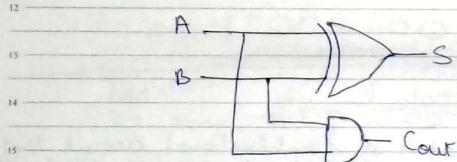
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2011  
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		<u>Sum</u>		<u>Carry</u>	
A	B	$\bar{A}$	$\bar{B}$	$\bar{A}$	$\bar{B}$
0	0	1	1	0	0
1	0	0	1	0	1

$S = A'B + AB'$        $Cout = AB$

Full Adder

→ It is a MSI circuit that adds two input bits and carry from the previous stage and out a sum-bit and carry out bit.

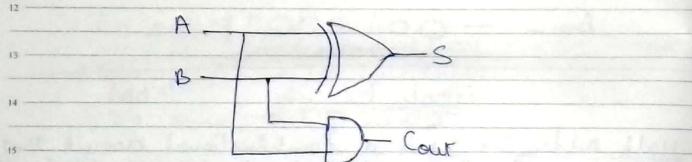
		<u>Truth table</u>		Sum	Cout
A	B	Cin			
0	0	0	0	0	0
1	0	1	0	1	0
2	0	1	1	0	0
3	1	0	0	1	1
4	1	0	1	0	0
5	1	1	0	0	1
6	A great man shows his greatness by the way he treats little men.		1	1	
7	1	1	1	1	1

October 2011  
Mon 3 10 17 24  
Tue 4 11 18 25  
Wed 5 12 19 26  
Thu 6 13 20 27  
Fri 7 14 21 28  
Sat 8 15 22 29  
Sun 9 16 23 30November 2011  
Mon 7 14 21 28  
Tue 8 15 22 29  
Wed 9 16 23 30  
Thu 10 17 24 31  
Fri 11 18 25 32  
Sat 12 19 26 33  
Sun 13 20 27 34

(18)

October  
2011  
Wk-42 • 285-080Wednesday  
12

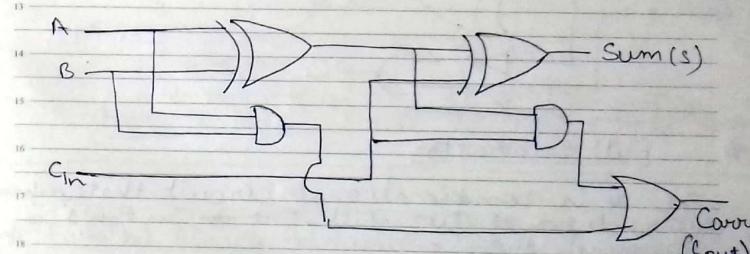
		<u>Sum</u>		<u>Carry</u>	
A	B	$\bar{A}$	$\bar{B}$	$\bar{A}$	$\bar{B}$
0	0	1	1	0	0
1	0	0	1	0	1



		<u>Sum</u>		<u>Carry</u>	
A	B	$\bar{A}$	$\bar{B}$	$\bar{A}$	$\bar{B}$
0	0	1	1	0	0
1	0	0	1	0	1

$$\text{Sum} = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC$$

$$\text{Cout} = BC + AC + AB$$

Half Subtractor

It can subtract only 1 bit binary to digit from another to give difference output and a borrow output.

INPUT		OUTPUT	
A	B	difference	Borrow
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

Notes: A hypocrite is a man who pays his taxes with a smile.

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October  
2011

Wk-42 • Difference

	A	B	D
8	0	1	1
9	1	0	0

$$D = \bar{A}B + A\bar{B}$$

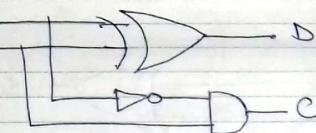
19

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Borrow

	A	B	D
8	0	0	1
9	0	0	0

$$BC = \bar{A}B$$



### \* Full Subtractor

It is a combinational circuit that performs subtraction of two bits. One bit is borrowed from previous.

Input

Output

Notes	A	B	C	Diff	Borrow
0	0	0	0	0	0
1	0	0	1	1	1
2	0	1	0	1	1
3	0	1	1	0	0
4	1	0	0	0	0
5	1	0	1	0	0
6	1	1	0	0	0
7	1	1	1	1	1

A liar needs a good memory.

October 2011

Diff

	A	B	C	BC	BC	BC	BC
8	0	1	0	1	0	1	0
9	1	0	1	0	1	0	1

October 2011

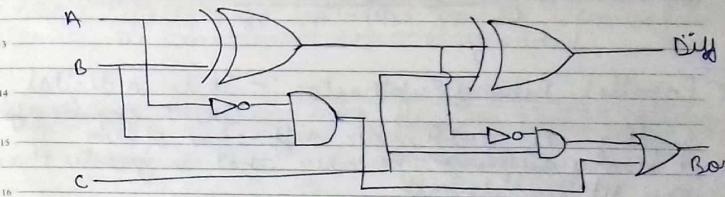
Wk-42 • 287-07K

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Friday

	A	B	C	BC	BC	BC	BC
8	0	1	0	1	0	1	0
9	1	0	1	0	1	0	1

$$D = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$C = \bar{A}C + \bar{A}B + BC$$



### Topic 8

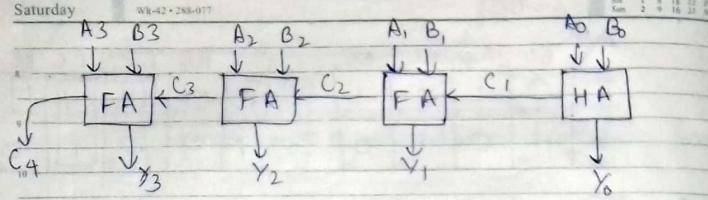
\* Parallel Binary Adder: → It is a combinational circuit consisting of various full adders in parallel structure so that when more than 1-bit numbers are to be added, then there can be full adder for every column for the addition. If 4-bit numbers are to be added then there will be 4-full adder in the parallel binary adder.

A sleeping fox counts hens in his dreams.

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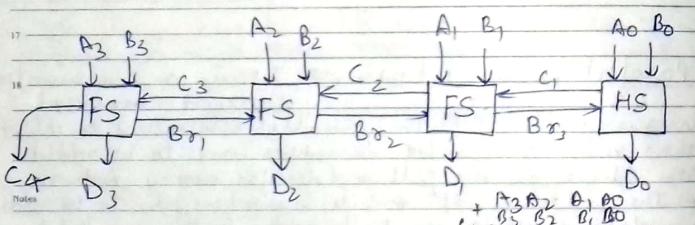
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2011  
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$$\begin{array}{r} A_3 \quad A_2 \quad A_1 \quad A_0 \\ B_3 \quad B_2 \quad B_1 \quad B_0 \\ \hline C_4 \quad Y_3 \quad Y_2 \quad Y_1 \quad Y_0 \end{array}$$

\* Parallel Binary Subtractor: → It is a digital circuit capable of finding the arithmetic difference of two binary numbers that is greater than one bit in length.

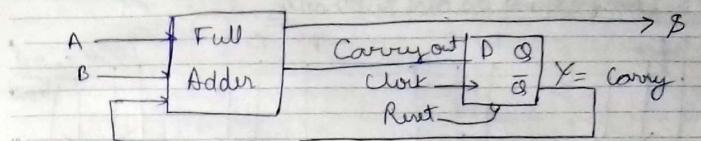


\* Serial binary adder: → It is a digital circuit that performs binary addition bit by bit. The serial full adder has three single-bit inputs for the numbers to be added and the carry in.

Learning makes a good man better and an ill man worse.

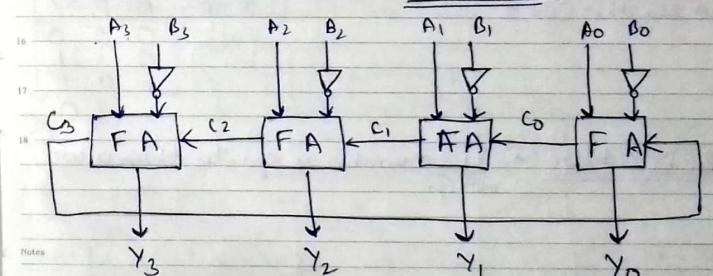
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2011  
Wk-42 • 288-07816  
Sunday

\* Serial binary subtractor: → It operates the same as the serial binary adder, except the subtracted number is converted to its 2's complement before being added.

\* 2's complement adder: → Parallel 4-bit 1's complement subtractor



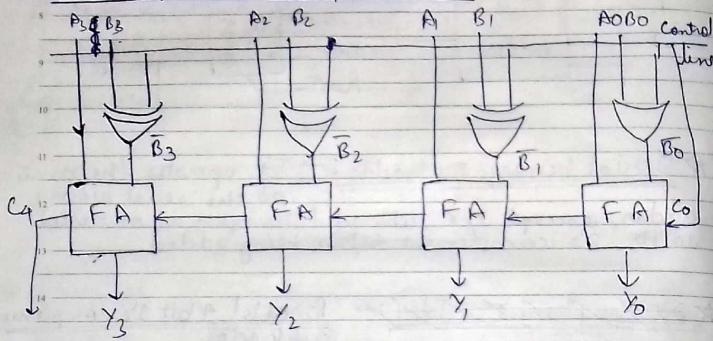
Adversity is the first path to truth.

17  
Monday

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2011  
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(23)

★ 2's Complement adder/ Subtractor



Let say that  $C_1 = 1$

XOR	A	B	$\sim$
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1

★ BCD adder : If number is greater than 9, add 6.

Observation, not old age, brings wisdom.

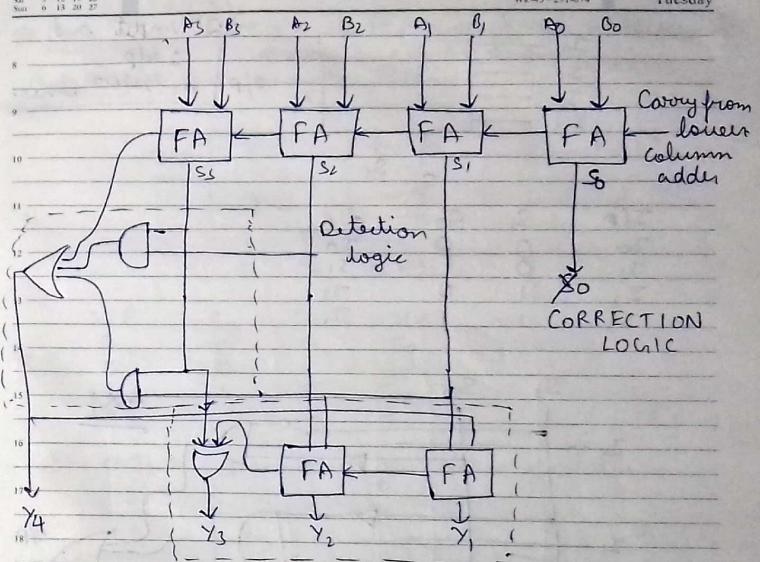
October 2011  
Mon 31 3 10 17 24  
Tue 1 4 11 18 25  
Wed 2 5 12 19 26  
Thu 3 6 13 20 27  
Fri 4 7 14 21 28  
Sat 5 8 15 22 29  
Sun 6 9 16 23 30

November 2011  
Mon 7 14 21 28  
Tue 1 8 15 22 29  
Wed 2 9 16 23 30  
Thu 3 10 17 24 31  
Fri 4 11 18 25  
Sat 5 12 19 26  
Sun 6 13 20 27

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October  
2011  
Wk-43 • 291-074

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Tuesday



Topic 9

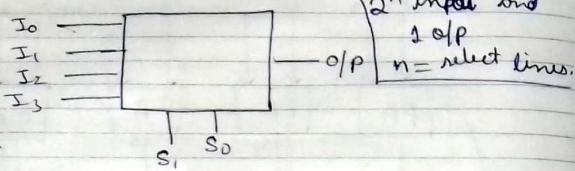
★ Multiplexer : It is a digital switch which selects one of the many inputs to a single output.

You may be disappointed if you fail but you are doomed if you don't try.

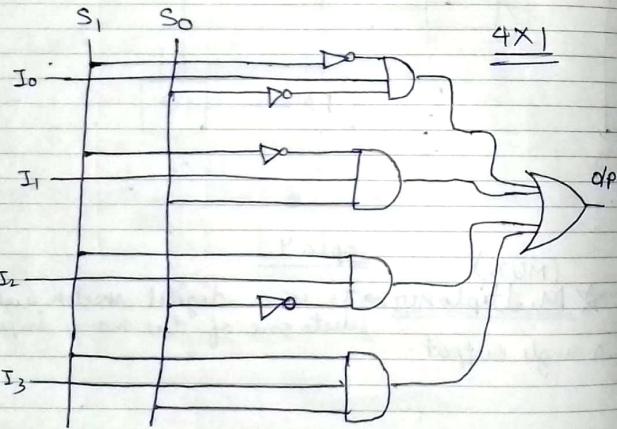
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Wednesday

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2011  
Wk-43 • 292-073

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I/P	S <sub>1</sub>	S <sub>0</sub>	O/P
I <sub>0</sub>	0	0	I <sub>0</sub>
I <sub>1</sub>	0	1	I <sub>1</sub>
I <sub>2</sub>	1	0	I <sub>2</sub>
I <sub>3</sub>	1	1	I <sub>3</sub>



To be successful, the first thing to do is fall in love with your work.

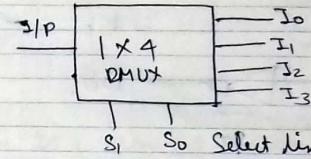
October 2011  
Monday

November 2011  
Tuesday

$2^n$  input and 1 O/P  
 $n = \text{select lines.}$

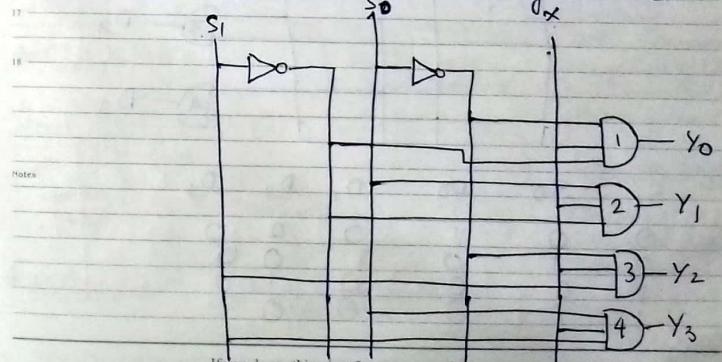
(DMUX)

\* Demultiplexer: → It is the opposite of a multiplexer.  
Many inputs but one output.  
One input and many outputs.



I/P	S <sub>0</sub>	S <sub>1</sub>	O/P
A	0	0	I <sub>0</sub>
0	0	1	I <sub>1</sub>
1	1	0	I <sub>2</sub>
A	1	1	I <sub>3</sub>

The output appears based on states of select lines.



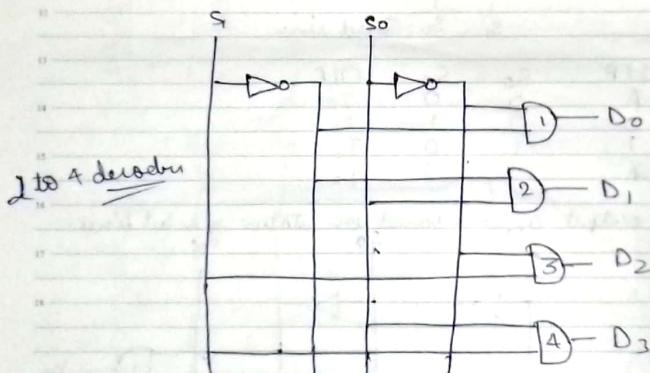
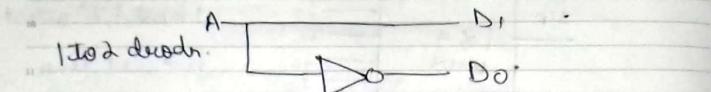
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Wk-43 • 394-071

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\* Decoder: → A decoder is a circuit that changes a code into a set of signals. A decoder takes an  $n$  digit binary number and decodes it into  $2^n$  data lines.



S <sub>1</sub>	S <sub>0</sub>	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

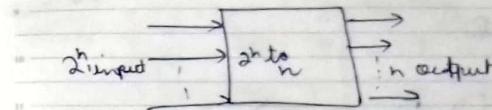
Be nice to people on your way up because you meet them on your way down.

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2011  
Wk-43 • 394-071

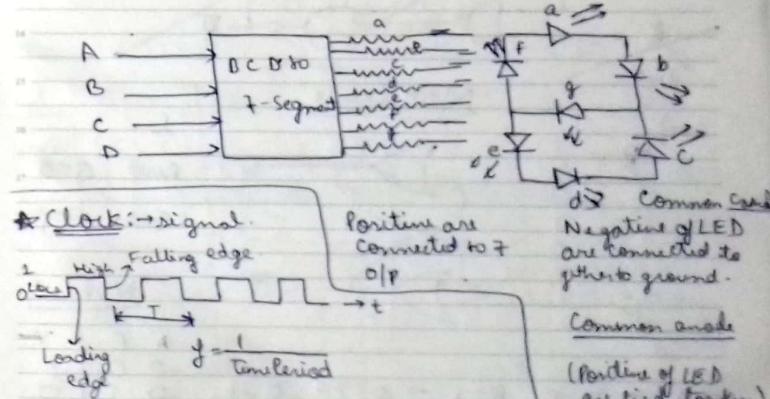
28

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2011  
Wk-43 • 395-07022  
Saturday

\* Encoder: → It is a circuit that changes a set of signals into a code.



\* Binary to 7-segment display



\* Duty cycle: →  $\frac{\text{Ratio of time signal}}{\text{Total time}}$

$$\frac{t}{T} = \frac{1}{2}$$

"I can write better than anybody who can write faster, and I can write faster than anybody who can write better."

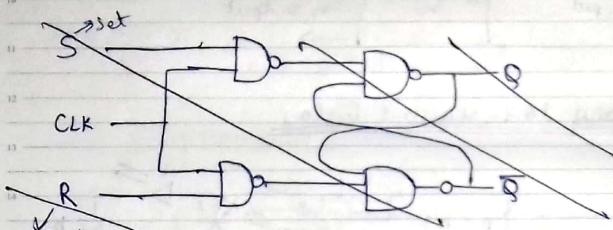
23

October  
2011  
Wk-41 • 296-066

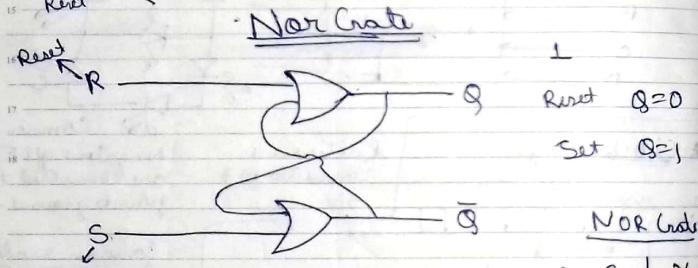
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Topic 10

\* Flip-flop : Kind of multivibrator also called latches or toggles.

(1) S-R Flip flop

NOR Gate



NOR Gate

Case I :  $\rightarrow S=0, R=1 \rightarrow Q=0, \bar{Q}=1$

$$S=0, R=0 \rightarrow Q=0, \bar{Q}=1$$

Memory

Don't stay in bed, until you can make money in bed.

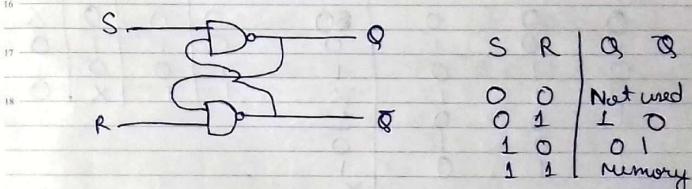
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Case II)  $S=1, R=0 \rightarrow Q=1, \bar{Q}=0$   
 $S=0, R=0 \rightarrow Q=0, \bar{Q}=0$  Memory

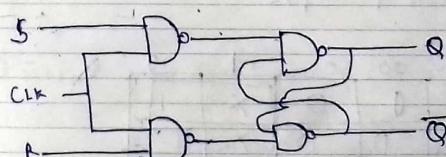
Case III)  $S=1, R=1 \rightarrow Q=0, \bar{Q}=0$   
 $S=0, R=0 \rightarrow Q=0/1, \bar{Q}=1/0$  Not used

S	R	Q	$\bar{Q}$
0	0	0	1
0	1	0	1
1	0	1	0
1	1	Not used	Not used

Nand Gate



S	R	Q	$\bar{Q}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1



He who spits at Heaven gets it back on his face.

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October  
Tuesday  
Wk-44 • 298-067

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$$S^* = \overline{S} \cdot \overline{\text{Clk}} = \overline{S} + \overline{\text{Clk}}$$

$$R^* = \overline{R} \cdot \overline{\text{Clk}} = \overline{R} + \overline{\text{Clk}}$$

Truth Table

Clk	S	R	$Q$	$\bar{Q}$	$Q_{n+1}$
0	X	X			
1	0	0	Memory	Memory	$Q_n$
1	0	1	0	1	$Q_n$
1	1	0	1	0	1
1	1	1			Not used

Characteristic Table :-      Excitation Table

$Q_n$	S	R	$Q_{n+1}$	$Q_n Q_{n+1}$	S	R
0	0	0	0	00	0	X
0	0	1	0	01	0	0
0	1	0	1	10	1	0
0	1	1	X	11	X	0
1	0	0	1	00	0	0
1	0	1	0	01	0	1
1	1	0	1	10	1	0
1	1	1	X	11	X	1

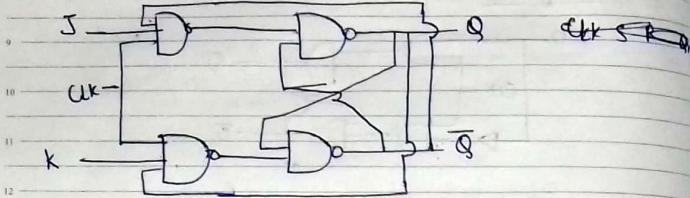
$Q_n$	00	01	10	11	$Q_{n+1} = S + Q_n$
0	0	0	X	1	
1	D	0	X	1	

The achievement of your goal is assured the moment you commit yourself.

 $Q_{n+1} = S + Q_n$ 

&lt;/div

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October  
2011  
Wk-44 • 300-065JK Flip flop

$\text{clk} = 0 \quad \text{Memory}$   
 $\text{clk} = 1 \quad J=1 \quad K=0, \quad Q = 1, \quad \bar{Q} = 0$   
 $J=0 \quad K=1, \quad Q = 0, \quad \bar{Q} = 1$   
 $J=1 \quad K=1, \quad Q = 0, \quad \bar{Q} = 1$   
 $Q = 0, 1, 0, 1 \dots \quad Q_{n+1} = 0$   
 $\bar{Q} = 1, 0, 1, 0 \dots \quad \bar{Q}_{n+1} = 1$

Truth table

clk	J	K	Q <sub>n+1</sub>
0	X	X	Q <sub>n</sub>
1	0	0	Q <sub>n</sub>
1	0	1	Q <sub>n</sub>
1	1	0	Q <sub>n</sub>
1	1	1	Q <sub>n</sub>

{ Memory }  
 { (Toggle) }

Trust not him that hath once broken faith.

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October  
2011  
Wk-44 • 300-065November  
2011  
Wk-44 • 301-064Characteristic table

Q <sub>n</sub>	J	K	Q <sub>n+1</sub>
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Excitation table

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	0

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	0	1
1	0	1	0

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	1	X
1	0	X	0

$$J = Q_{n+1}$$

$$K = \bar{Q}_{n+1}$$

Q <sub>n</sub>	J	K	J	K
0	0	0	1	1
1	0	0	1	1

$$Q_{n+1} = \bar{Q}_n J + Q_n K$$

Q <sub>n</sub>	J	K	J	K
1	0	0	1	0
1	0	0	1	0

It is better to have a permanent income than to be fascinating.

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2011  
Wk-44 • 301-064

Friday

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Wk-44 • 301-064November  
2011  
Wk-44 • 302-065Characteristic table

Q <sub>n</sub>	J	K	Q <sub>n+1</sub>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	0

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	0	1
1	0	1	0

Q <sub>n</sub>	Q <sub>n+1</sub>	J	K
0	0	1	X
1	0	X	0

Q <sub>n</sub>	J	K	J	K
0	0	0	1	1
1	0	0	1	1

$$J = Q_{n+1}$$

$$K = \bar{Q}_{n+1}$$

Q <sub>n</sub>	J	K	J	K
1	0	0	1	0
1	0	0	1	0

Q <sub>n</sub>	J	K	J	K
----------------	---	---	---	---

$$Q_{n+1} = \bar{Q}_n J + Q_n K$$

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Saturday

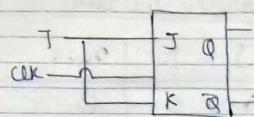
October  
2011

Wk-44 • 502-063

(35)

★ T flip flop :

Toggle



Truth Table

Clk	T	Q <sub>n+1</sub>
0	X	Q <sub>n</sub> (Memory)
1	0	Q <sub>n</sub> (Memory)
1	1	Q <sub>n</sub> (Toggling)

Characteristics table

→ Excitation table

Q <sub>n</sub>	T	Q <sub>n+1</sub>
0	0	0
0	1	1
1	0	1
1	1	0

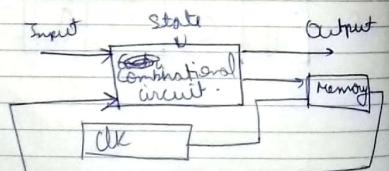
⇒ odd 1's detected

for

$$Q_{n+1} = Q_n \oplus T$$

Notes

★ Edge triggering



It is not the thief who is hanged, but one who was caught stealing.

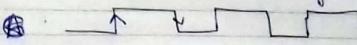
October  
2011

November  
2011

October  
2011

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Sunday

Flip flop conversion

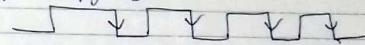


① +ve edge



when goes from low to high then there will be change.

② -ve edge triggering



when goes from high to low then there will be change.

★ Level edge triggering



Whenever the clock is at high there is a change which is called level triggering.

A proverb is a short sentence based on long experience.

FEBRUARY						
M	T	W	T	F	S	S
				1	2	3
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

2018

DE

Days 001-364

01

January  
Monday

Wk.-01

## Topic 11

### ★ Conversion of 1 Flip-flop to other.

#### ① Step:-

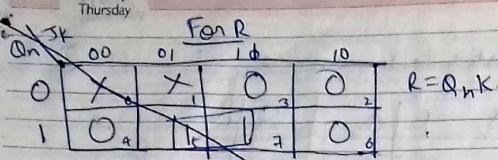
- ① Identify available and required flip flop.
- ② Make characteristic table for required flip flop.
- ③ Make excitation table for available flip flop.
- ④ Write boolean expression for available ff.
- ⑤ Draw the circuit

Wk-01  
04  
January Thursday

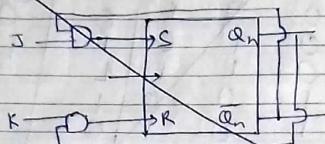
Days 004-361

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				



(V)



### I S-R to JK Flip flop

i Available flip flop = SR  
Required flip flop = JK

### ii Characteristic table of JK

$Q_n$	J	K	$Q_{n+1}$	S	R
0	0	0	0	0	X
0	0	1	0	0	X
0	1	0	1	1	0
0	1	1	1	0	0
1	0	0	1	X	0
1	0	1	0	0	1
1	1	0	1	X	0
1	1	1	0	0	1

Wk-01  
05  
January Friday

Days 005-360

2018

### iii Excitation table of S-R

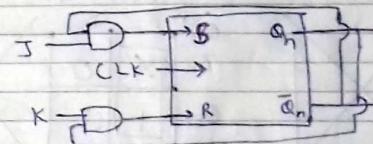
$Q_n$	$Q_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

### IV For S

$Q_n$	$\bar{Q}_n$	$\bar{S}$	$\bar{K}$	$\bar{J}$	$\bar{K}$	$\bar{J}$	$\bar{S}$	$\bar{R}$
0	0	1	1	1	1	1	X	00
X	0	0	0	X	0	0	0	110

$$S = \bar{Q}_n J$$

$$R = Q_n K$$



### II S-R to D flip flop

i Available flip flop = SR  
Required flip flop = D

Wk-01  
06  
January Saturday

Days 006-359

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

JANUARY

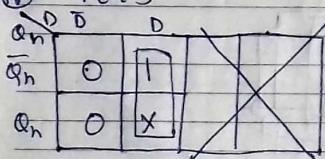
(ii) Characteristic table for D.

$Q_n$	D	$Q_{n+1}$	S	R
0	0	0	0	X
0	1	1	0	0
1	0	0	0	1
1	1	1	X	0

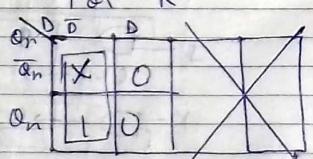
(iii) Excitation for SR.

$Q_n$	$Q_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

(iv) For S



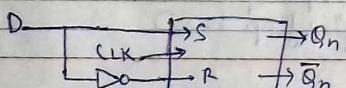
For R



Sunday 07

$S = D$

(v)



M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

2018

Days 008-357

08  
January Monday

WL-02

(iii) SR-to-T Flip flop

- i Available flip flop = SR
- ii Required flip flop = T.

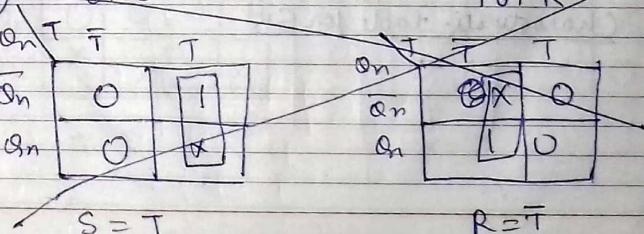
(ii) Characteristic table for T.

$Q_n$	T	$Q_{n+1}$	S	R
0	0	0	0	X
0	1	1	1	0
1	0	1	X	0
1	1	0	0	1

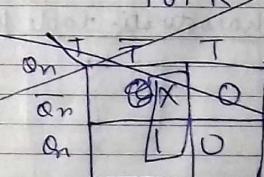
(iii) Excitation table for SR.

$Q_n$	$Q_{n+1}$	S	R
0	0	0	X
0	1	1	0
1	0	X	0
1	1	0	1

(iv) For S



For R



$S = T$

$R = \bar{T}$

09

Wk-02 Days 009-356

January Tuesday

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

(IV)

For S

$Q_n$	T	T
0	1	
x	0	

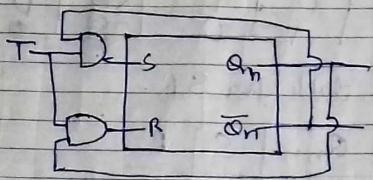
$$S = \bar{Q}_n T$$

For R

$Q_n$	T	T
0	x	0
0	0	1

$$R = Q_n T$$

(V)



(IV) Convert JK to SR flip flop

i) Available flip flop = JK  
Required flip flop = SR.

ii) Characteristic table for SR

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

2018

FEBRUARY

Days 010-355

10

January Wednesday

Wk-02

$Q_n$	S	R	$Q_{n+1}$	J	K
0	0	0	0	0	x
0	0	1	0	0	x
0	1	0	1	1	x
0	1	1	x	x	x
1	0	0	1	x	x
1	0	1	0	x	0
1	1	0	1	x	0
1	1	1	x	x	x

iii) Excitation table for JK

$Q_n$	$Q_{n+1}$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

(IV) For S

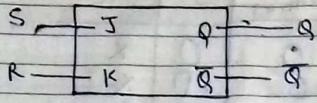
$Q_n$	SR	SR	SR	SR
0	0	0	x	1
x	x	x	x	x

$$J = S$$

$Q_n$	SR	$\bar{S}R$	$S\bar{R}$	SR
x	x	x	x	x
0	0	1	x	0

$$K = R$$

Wk-02	11	January Thursday	Days 011-354	2018	JANUARY
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#### V JK to D flip flop

- i) Available flip flop:  $\rightarrow$  JK flip flop.  
ii) Required flip flop:  $\rightarrow$  D flip flop.

ii) Characteristic table of D.

$Q_n$	D	$Q_{n+1}$	J	K
0	0	0	0	x
0	1	1	1	x
1	0	0	x	1
1	1	1	x	0

iii) Excitation table for JK.

$Q_n$	$Q_{n+1}$	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

M	T	W	T	F	S	S
6	7	8	9	10	11	
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

Days 012-353

12

January Friday

Wk-02

④ For J

$Q_n$	D	D
$Q_n$	0	1
$Q_n$	x	x

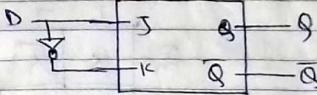
$$J = D$$

For K

$Q_n$	D	D
$Q_n$	x	x
$Q_n$	1	0

$$K = \overline{D}$$

V



#### VI JK to T flip flop

- i) Available flip flop:  $\rightarrow$  JK flip flop  
ii) Required flip flop:  $\rightarrow$  T

ii) Characteristic table for T

$Q_n$	T	$Q_{n+1}$	J	K
0	0	0	0	x
0	1	1	1	x
1	0	1	x	0
1	1	0	x	1

Wk-02  
13  
January Saturday

Days 013-352

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

JANUARY

iii) Excitation table for JK

$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

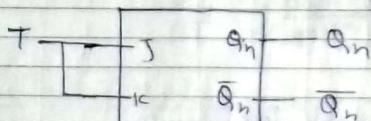
iv)  $\overline{Q_n}$   $\overline{T}$   $T$  Fa3

$\overline{Q_n}$	0	1
$Q_n$	X	X

$\overline{Q_n}$   $\overline{T}$   $T$  Fork

$Q_n$	X	X
$\overline{Q_n}$	0	1

v)



VII D to SR flip flop

i) Required flip flop:  $\rightarrow$  BSR  
Available flip flop:  $\rightarrow$  D

Wk-03  
15  
January Monday

Days 015-350

ii) Characteristic Table for BSR.

$Q_n$	S	R	$Q_{n+1}$	D
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	X	X
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	X	X

iii) Excitation table for D

$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

iv) For D

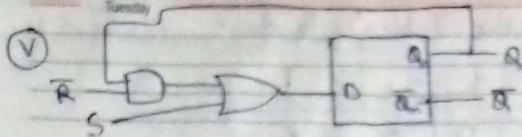
$Q_n$	SR	SR	SR	SR	SR
$Q_n$	0	0	X	1	
$Q_n$	1	0	X		

$$D = S + Q_n R$$

16

Days 518-540

2018



VIII) D to JK flip flop

i) Available = D flip flop  
Required = JK flip flop

ii) Characteristic table for JK

$Q_n$	J	K	$Q_{n+1}$	D
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	1	1
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	0

iii) Excitation table for D

$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

17

Days 517-540

January Wednesday

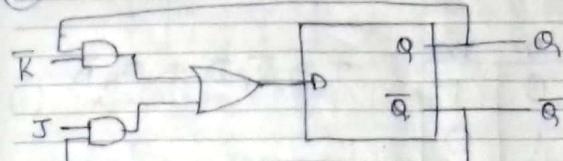
2018

VII) For D

	$S_R$	$\bar{S}_R$	$J_R$	$\bar{J}_R$	$K_R$	$\bar{K}_R$
$Q_n$	0	0	1	1	1	1
$Q_n$	1	0	0	1	1	1

$$D = \bar{J}Q_n + \bar{Q}_n\bar{K}$$

V



IX) D to T flip flop

i) Available = D flip flop  
Required = T flip flop

ii) Characteristic table for T

$Q_n$	T	$Q_{n+1}$	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

18  
January  
Thursday

Wk - 03

Days 018-347

2018

JANUARY						
M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

iii) Excitation table for D

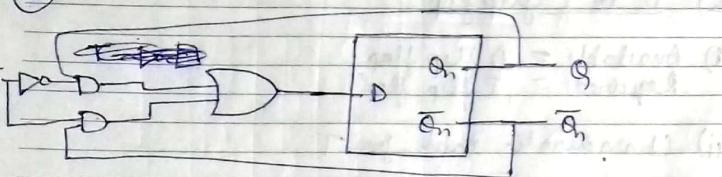
$Q_n$	$Q_{n+1}$	D
0	0	0
0	1	1
1	0	0
1	1	1

(iv) For T

$Q_n$	$\bar{Q}_n$	D
0	1	0
1	0	0

$$T = \bar{Q}_n D + Q_n \bar{D}$$

(v)



(vi) T to SR flip flop

i) Available = T flip flop.  
Required = SR flip flop.

2018  
FEBRUARY

Days 019-346

19  
January  
Friday

Wk - 03

ii) Characteristic table for SR

$Q_n$	S	R	$Q_{n+1}$	T
0	0	0	0	0
0	0	1	0	0
0	1	0	1	1
0	1	1	X	X
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	X	X

iii) Excitation table for T

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

(iv) For T

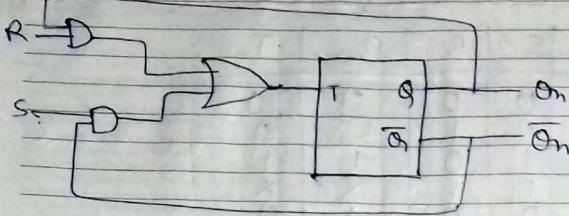
$Q_n$	SR	SR	SR	SR
0	0	X	1	0
0	1	X	0	0

$$T = S \bar{Q}_n + Q_n R$$

Wk-03  
20  
January Saturday

Days 020-345

2018						
JANUARY						
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				



### XI) T to JK flip flop.

- i) Available = T flip flop.
- Required = JK flip flop.

### ii) Characteristic table for JK

Qn	J	K	Qn+1	T
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	0	1

Sunday 21

2018						
FEBRUARY						
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

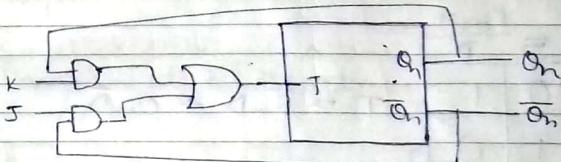
### iii) Excitation table for T.

On	On+1	T
0	0	0
0	1	1
1	0	1
1	1	0

### iv) For

On	JK	JK	JK	JK
On	0	0	1	1
On	0	1	1	0

$T = \bar{Q}_n S + Q_n K$



### XII) T to D flip flop.

- i) Available = T flip flop.
- Required = JK flip flop.

23

Wk-04

Days 023-342

January  
Tuesday

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28

JANUARY

ii) Characteristic table for D.

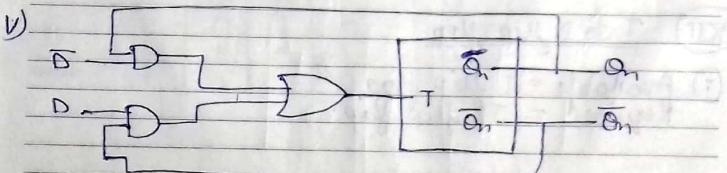
$Q_n$	D	$Q_{n+1}$	T
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

iii) Excitation table for T

$Q_n$	$Q_{n+1}$	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_n$	D	$\bar{D}$	$\bar{D}$	$F_{out}$
0	0	1		
1	1	0		

$T = \bar{Q}_n D + Q_n \bar{D}$

Topic 12

24

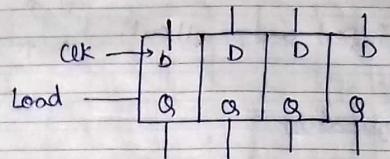
Wk-04

January  
Wednesday

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

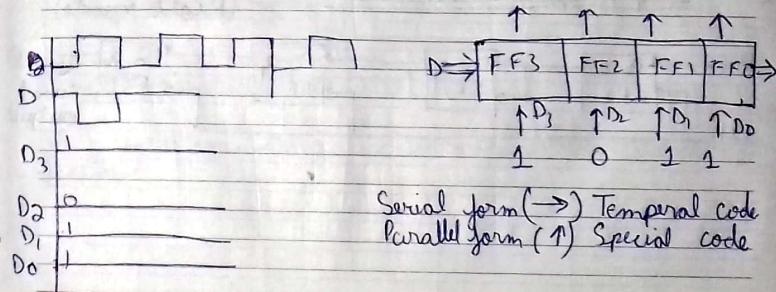
2018

- \* Registers :> Flip flop is 1-bit memory cell ( $Q_{on} 1$ ) ( $1011$ )
- To increase the storage capacity, we have to use a group of flip flop. This group of flip flop is called Registers.
- The n-bit register consist of n' numbers of flip flops and is capable of storing n-bit word.



Synch : Clock ↑ and Load ↑  
Asynch → only Load ↑

\* Serial → 1 bit at a time  
Parallel → all bits at a time.



D flip flop is used to store data.

25

January Thursday

Days 025-340

JANUARY											
M	T	W	T	F	S	S	S	S	S	S	S
1	2	3	4	5	6	7	8	9	10	11	12
13	14	15	16	17	18	19	20	21	22	23	24
25	26	27	28	29	30	31					

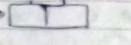
### \* Classification of register.

I Depending on I/P and O/P

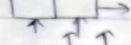
a) SISO  $\rightarrow$  (Serial in serial out)



b) SIPO  $\rightarrow$  Serial in Parallel out



c) PISO  $\rightarrow$  Parallel in serial out



d) PIPO  $\rightarrow$  (Parallel input and parallel out)



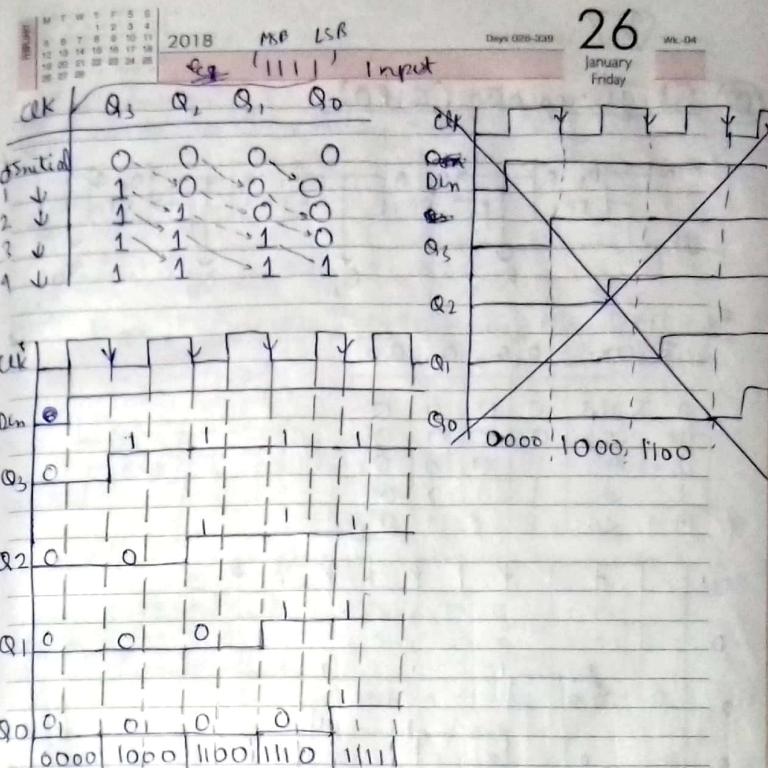
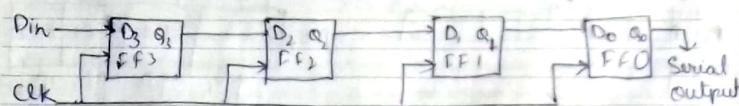
II Depending on application

a) Shift register - (shift a binary data)

b) Storage Register

① Shift register (SISO)

(Right mode)



It is used in long distance transmission of data.

Wk-04

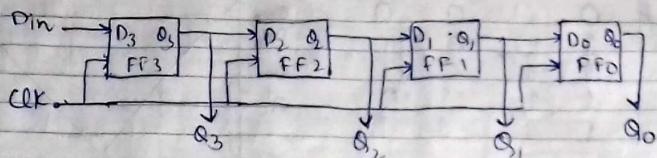
27  
January Saturday

Days 027-338

2018

JANUARY

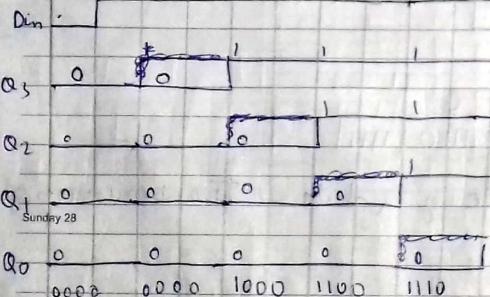
## (II) Shift register (SISO)



e.g. 1110  
at CLK      Q<sub>3</sub>, Q<sub>2</sub>, Q<sub>1</sub>, Q<sub>0</sub>

	Initial	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0 0 0 0	0	0	0	0
1 ↓	0 0 0 0	0	0	0	0
2 ↓	1 0 0 0	1	0	0	0
3 ↓	1 1 0 0	1	1	0	0
4 ↓	1 1 1 0	1	1	1	0

clk      [ ] [ ] [ ] [ ] [ ] [ ]



M T W T F S S  
1 2 3 4 5 6 7  
8 9 10 11 12 13 14  
15 16 17 18 19 20 21  
22 23 24 25 26 27 28  
29 30 31

2018

Days 028-338

29  
January Monday

Wk-05

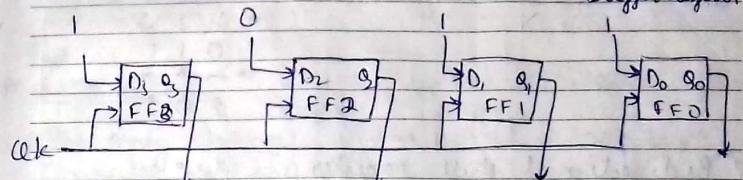
\* Application:

① Provides a time delay =  $n \tau_c = n \cdot \frac{1}{f_c}$

e.g. 4 bit data       $T = 3 \text{ sec.}$

Total time =  $4 \times 3 = 12 \text{ sec.}$

## (III) Shift register (PISO Mode) / Storage Register / Buffer Register



What value we give it will give same output.

$$\begin{aligned} & \text{at } D_3 = 0 \Rightarrow Q_{m+1} = 0 \\ & \text{at } D_3 = 1 \Rightarrow Q_{m+1} = 1 \\ & \text{at } D_3 = 0 \Rightarrow Q_{m+1} = Q_m \\ & \text{at } D_3 = X \end{aligned}$$

D<sub>1</sub>      [ ] [ ] [ ]  
D<sub>0</sub>      [ ]

1 clk pulse to store the data  
So, it is faster than SISO & SPO

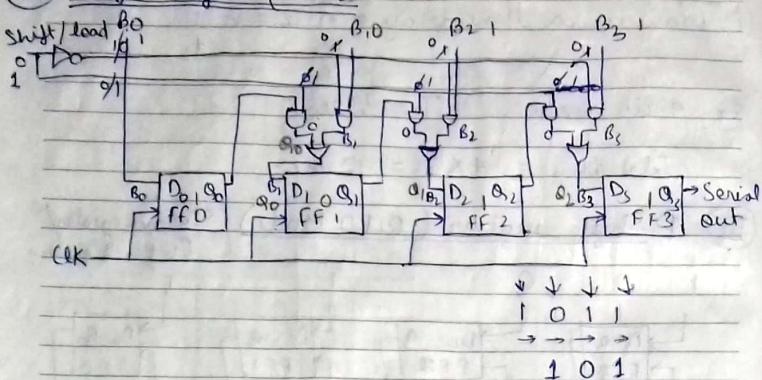
30  
Wk-05  
January  
Tuesday

Days 030-335

2018

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

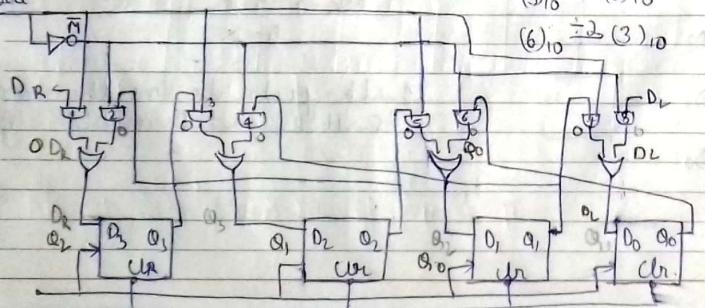
#### (IV) Shift register (PISO)



$$\begin{array}{c} \downarrow \quad \downarrow \quad \downarrow \\ 1 \quad 0 \quad 1 \\ \rightarrow \rightarrow \rightarrow \\ 1 \quad 0 \quad 1 \end{array}$$

Shift 11 to the left  
 $(110)_{10} \rightarrow (011)_{10}$

Mode:



M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

2018

Days 031-394

31  
Wk-05

January  
Wednesday

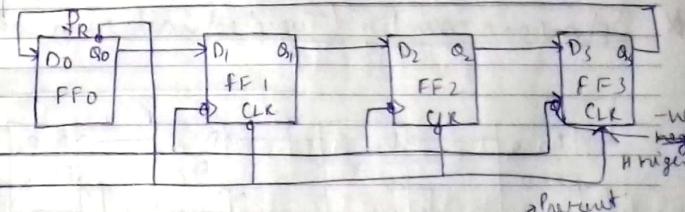
When  $M = 1$  we have shift right operation.

#### \* Unidirectional shift register

Topic no.  $\rightarrow 13$

\* Shift register counter: They are the circuit having the flip flop connected in cascade manner and counts the no. of clock pulse applied to it.

\* Ring counter: It is a typical application of shift register.  
→ The only change in the output of last ff is connected to the input of the first ff.



$\Rightarrow$  no. of states = no. of flip flop used

$$\left[ PR = 0 \quad Q_0 = 1 \atop QR = 0 \quad Q_0 = 0 \right]$$

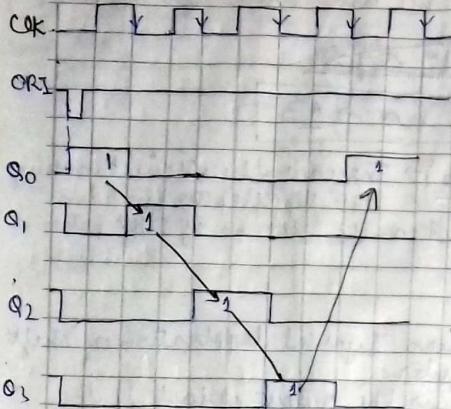
ORJ	CLK	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Count active low signal	X	1	0	0	0
1	↓	0	X	0	0
1	↓	0	0	1	0
1	↓	0	0	0	1

01  
Wk-05  
February Thursday

Days 032-333

2018

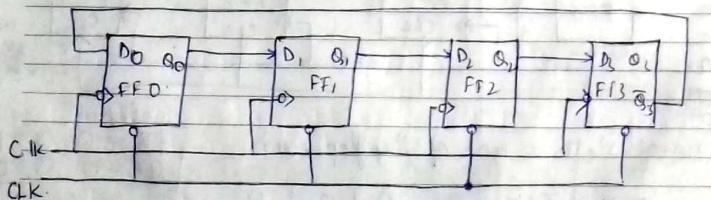
M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				



Application  
It is used in which several operations are sequentially controlled.

Eg: Resistance building the operation called sequence hold weble hold and off are to be performed sequentially we use it there.

### \* Johnson's counter (Twisted tail ring counter)



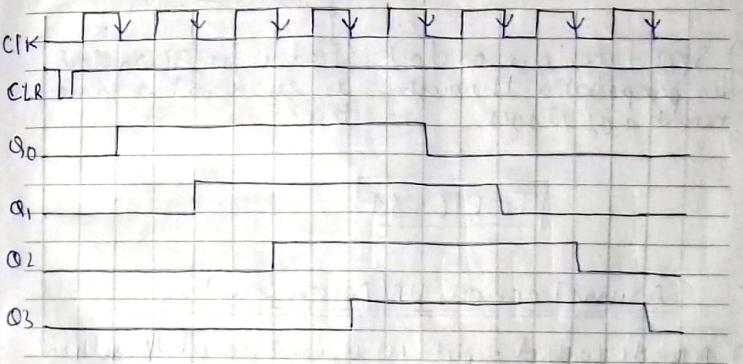
① No. of states =  $2 \times$  no. of flip flop

CLR	CLK	$Q_0$	$Q_1$	$Q_2$	$Q_3$	
X		0	0	0	0	①
	↓	1	0	0	0	②
1	↓	1	1	0	0	③
	↓	1	1	1	0	④
1	↓	1	1	1	1	⑤
	↓	0	1	1	1	⑥
1	↓	0	0	1	1	⑦
	↓	0	0	0	1	⑧
1	↓	0	0	0	0	

02  
Wk-05  
February Friday

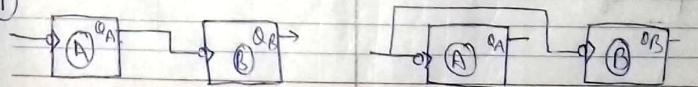
Days 033-332

2018



\* Asynchronous counter / Ripple      Synchronous counter

①



03  
Wk-05  
February Saturday

Days 034-331

2018  
M T W T F S S  
1 2 3 4  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28

- (i) Flipflops are connected in such a way that the o/p of first ff drives the clock of next ff.

There is no connection b/w o/p of first ff and clock of next ff

- (ii) FF are not clocked simultaneously

FF are clocked simultaneously

- (iii) Circuit is simple for more number of states

Circuit becomes complicated as number of states increases.

- (iv) Speed is slow as clock is propagated through number of stages

Speed is high as clock is given at a same time.

### TOPIC - 14

#### Aynchronous UP/ Down Counter

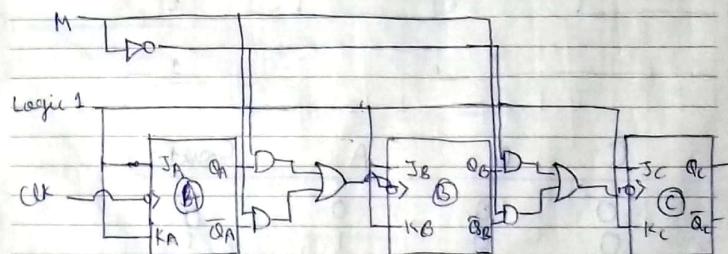
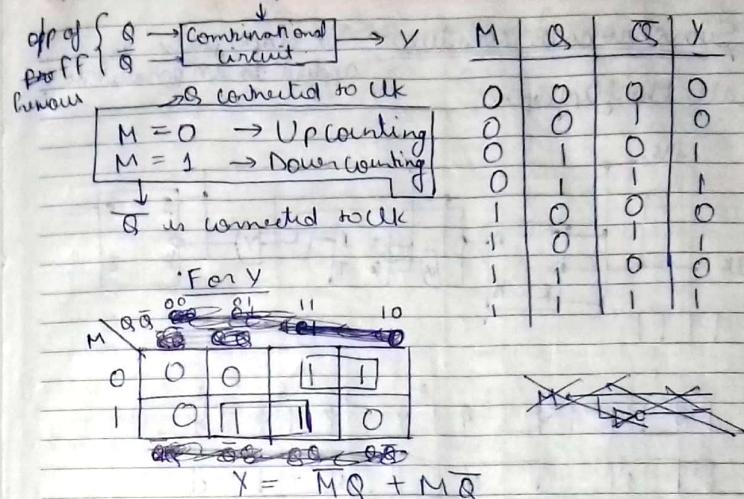
- (i) A mode control input ( $M$ ) is used to select either up or down mode.

- (ii) <sup>Sunday</sup> A combination circuit is required between each pair of ff.

05  
Wk-06  
February Monday

Days 036-329

2018  
M T W T F S S  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28 29 30 31



Wk-06  
06  
February  
Tuesday

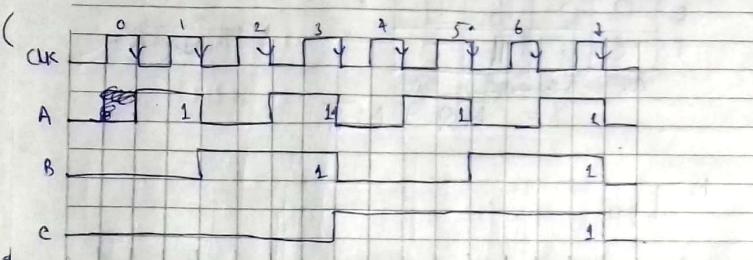
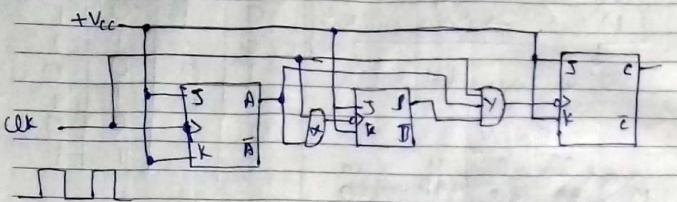
Days 037-328

2018

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

FEBRUARY

- (\*) Synchronous counter:  $\rightarrow$  The clock pulse is applied to all the flipflop.



C	B	A	Count
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
0	0	0	7

Wk-06  
07  
February  
Wednesday

$$\begin{array}{l} \text{3-bit} \\ \boxed{2^3 = 8} \end{array}$$

8 states

3 bit Synchronous Counter							
Control	Present state			Next state			Outputs
$M$	$Q_C$	$Q_B$	$Q_A$	$Q_C'$	$Q_B'$	$Q_A'$	$T_C$ $T_B$ $T_A$
0	0	0	0	0	0	1	0 0 1
0	0	0	1	0	1	0	0 1 1
0	0	1	0	0	0	1	0 0 0
0	0	1	1	1	0	0	1 1 1
0	1	0	0	1	0	1	0 0 1
0	1	0	1	1	0	0	0 1 1
0	1	1	0	1	1	1	0 0 0
0	1	1	1	0	0	0	1 1 1
1	0	0	0	1	1	1	1 1 1
1	0	0	1	0	0	0	0 0 1
1	0	1	0	0	0	1	0 1 1
1	0	1	1	0	1	0	0 0 1
1	1	0	0	0	1	1	1 1 1
1	1	0	1	1	0	0	0 0 0
1	1	1	0	1	0	1	0 1 1
1	1	1	1	1	1	0	1 0 1

For  $T_C$  :-

	$Q_B Q_A$	$\bar{Q}_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$M Q_C$	0 0	1 0	0 1	0 0
$\bar{M} Q_C$	0 0	1 0	0 1	0 0
$M \bar{Q}_C$	1 0	0 0	0 0	0 0
$\bar{M} \bar{Q}_C$	1 0	0 0	0 0	0 0

$$T_C = \bar{M} Q_B Q_A + M \bar{Q}_B \bar{Q}_A$$

08  
February Thursday

Days 039-326

2018  
FEBRUARY

2018

09  
February Friday

Wk-06

For  $T_B$

For  $T_A$

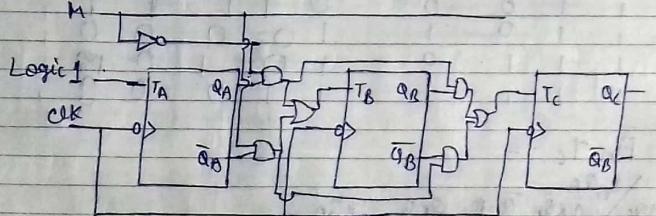
$MQ_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$M\bar{Q}_A$	0	1	1	0
$MQ_A$	0	1	1	0
$M\bar{Q}_A$	1	0	0	1
$MQ_A$	1	0	0	1

$MQ_A$	$\bar{Q}_B Q_A$	$Q_B Q_A$	$Q_B \bar{Q}_A$	$\bar{Q}_B \bar{Q}_A$
$M\bar{Q}_A$	1	1	1	1
$MQ_A$	1	1	1	1
$M\bar{Q}_A$	1	1	1	1
$MQ_A$	1	1	1	1

$$T_B = M\bar{Q}_A + M\bar{Q}_A$$

$$= M(\bar{Q}_A)$$

$$T_A = 1$$



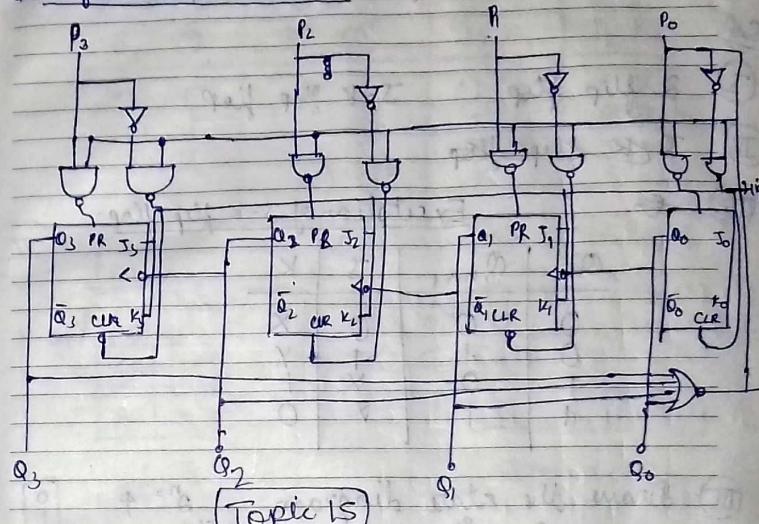
2018  
MARCH

Days 040-325

09  
February Friday

Wk-06

★ Programmable Counter



[Topic 15]

★ Design a synchronous counter

- I Decide the number of flip flop.
- II Excitation table for flip flop.
- III State diagram and circuit excitation table.
- IV Obtain simplified equations using K' map.
- V Draw the logic diagram.

Wk-06  
10  
February Saturday

Days 041-324

2018

M	T	W	T	F	S	S
5	6	7	1	2	3	4
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	1

FEBRARY

Wk-07  
12  
February Monday

Days 043-322

2018

MARCH

5

6

7

8

9

10

11

12

13

14

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16

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18

19

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21

22

23

24

25

26

27

28

29

30

31

Q Design 2-bit synchronous up counter.

Q1

I A flip flop J-K flip flop

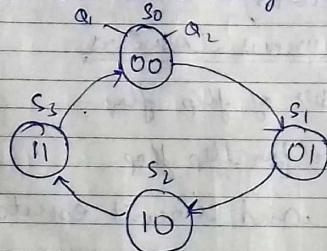
II JK flip flop

III Excitation of J-K flip flop

$Q_n$	$Q_{n+1}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

IV Draw the state diagram

$$2^n = 4 \\ \text{State} = 4-1 = 3$$



Sunday 11

Circuit excitation table

$Q_1$	$Q_2$	$Q_1^*$	$Q_2^*$	$J_1$	$K_1$	$J_2$	$K_2$
0	0	0	1	0	X	1	X
0	1	1	0	1	X	1	X
1	0	1	1	X	0	X	1
1	1	0	0	X	1	1	X

V

For  $J_1$

$Q_1$	$Q_2$	$J_1$
0	0	1
1	X	X

For  $K_1$

$Q_1$	$Q_2$	$K_1$
0	0	X
1	0	1

$$J_1 = Q_2$$

For  $J_2$

$Q_1$	$Q_2$	$J_2$
0	0	X
1	1	X

$$K_1 = Q_2$$

$$J_2 = 1$$

$Q_1$	$Q_2$	$J_2$
0	0	X
1	1	1

$$K_2 = 1$$

13

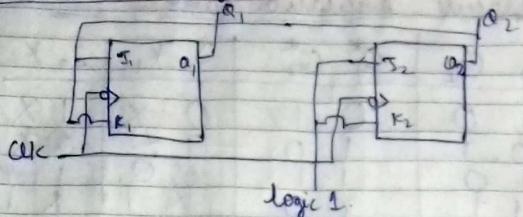
February  
Tuesday

Days 044-321

2018

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

FEBRUARY

(V) Draw circuit diagram★ Application of counters:

- Measurement of the frequency of a pulse signal.
- Measurement of the period of a pulse signal.
- The digital clock.

★ Modulus-n counter

→ 2-bit ripple Counter → MOD-4 or Modulus 4 cont.  
 → 3-bit ripple counter → MOD-8.

★ Non-sequential counter design(I) Using J-K flip flop:

0, 1, 3, 2, 1, 0

Topic → 16

14

February  
Wednesday

Days 045-320

2018

M	T	W	T	F	S	S
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31		

Present State			Next State			Excitation state					
$q_2$	$q_1$	$q_0$	$q_2$	$q_1$	$q_0$	$J_2$	$K_2$	$J_1$	$K_1$	$J_0$	$K_0$
0	0	0	0	0	0	0	0	1	0	X	X
1	0	0	0	1	0	0	0	X	1	X	0
2	0	1	1	1	0	0	1	X	X	0	X
3	1	1	0	1	1	1	X	0	X	0	X
4	1	1	1	0	0	0	X	1	X	1	X
5	0	1	0	X	X	X	X	X	X	X	X
6	1	0	0	X	X	X	X	X	X	X	X
7	1	0	1	X	X	X	X	X	X	X	X
8	0	1	0	X	X	X	X	X	X	X	X
9	1	0	0	X	X	X	X	X	X	X	X
10	1	0	1	X	X	X	X	X	X	X	X
11	1	1	1	0	0	X	1	X	1	X	1
12	1	1	1	1	1	1	X	0	X	0	X
13	0	1	0	X	X	X	X	X	X	X	X
14	1	0	0	X	X	X	X	X	X	X	X
15	1	0	1	X	X	X	X	X	X	X	X
16	1	1	0	X	X	X	X	X	X	X	X
17	1	1	1	0	0	X	1	X	1	X	1
18	0	1	0	X	X	X	X	X	X	X	X
19	1	0	0	X	X	X	X	X	X	X	X
20	1	0	1	X	X	X	X	X	X	X	X
21	1	1	0	X	X	X	X	X	X	X	X
22	1	1	1	0	0	X	1	X	1	X	1
23	0	1	0	X	X	X	X	X	X	X	X
24	1	0	0	X	X	X	X	X	X	X	X
25	1	0	1	X	X	X	X	X	X	X	X
26	1	1	0	X	X	X	X	X	X	X	X
27	1	1	1	0	0	X	1	X	1	X	1
28	0	1	0	X	X	X	X	X	X	X	X
29	1	0	0	X	X	X	X	X	X	X	X
30	1	0	1	X	X	X	X	X	X	X	X
31	1	1	0	X	X	X	X	X	X	X	X

For  $J_2$ 

$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 q_1 \bar{q}_0$	$\bar{q}_2 q_0$
0	0	1	X	0	0
X	X	X	X	X	X

 $J_2 = q_1$ For  $J_1$ 

$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 q_1 \bar{q}_0$	$\bar{q}_2 q_0$
0	1	X	X	0	0
X	X	X	X	X	X

 $J_1 = q_0$ For  $K_2$ 

$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 q_1 \bar{q}_0$	$\bar{q}_2 q_0$
X	X	X	X	X	X
X	X	X	X	X	X

 $K_2 = q_0$ For  $K_1$ 

$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_1 \bar{q}_0$	$\bar{q}_2 \bar{q}_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_2 q_1 \bar{q}_0$	$\bar{q}_2 q_0$
X	X	X	X	X	X
X	X	X	X	X	X

 $K_1 = q_2 q_0$

Wk-07

15

Dayii 046-319

February Thursday

2018

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30		

For  $Q_0$ 

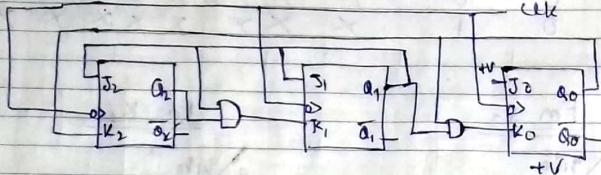
$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	X	X
$\bar{q}_2$	X	1	0	0
$q_2$	X	X	1	X

$$J_0 = 1$$

For  $K_0$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	0	1
$\bar{q}_2$	X	1	0	X
$q_2$	X	X	1	X

$$K_0 = q_1 q_0$$

(II) Using D flip flop.

0 2 1 3 5

	$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$D_2$	$D_1$	$D_0$
0	0	0	0	0	1	0	0	0	1
2	0	1	0	0	1	0	0	1	1
1	0	0	1	1	0	0	1	0	0
3	0	1	1	1	0	0	1	0	0
5	1	0	1	0	0	0	0	0	0
4	1	0	0	X	X	X	X	X	X
6	1	1	0	X	X	X	X	X	X
7	1	1	1	X	X	X	X	X	X

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30		

2018

For  $D_2$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	0	1
$\bar{q}_2$	0	0	1	0
$q_2$	X	0	X	X

$$D_2 = q_1 q_0$$

For  $D_1$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	0	1
$\bar{q}_2$	0	0	1	0
$q_2$	X	0	X	X

For  $D_1$ (II) Using D - flip flop

0, 2, 1, 3, 5

$q_n$	$q_{n+1}$	$D$
0	0	0
2	0	1
1	0	0
3	0	1
5	1	0
4	1	0
6	1	0
7	1	1

$q_2$	$q_1$	$q_0$	$q_2$	$q_1$	$q_0$	$D_2$	$D_1$	$D_0$
0	0	0	0	1	0	0	1	0
2	0	1	0	0	1	0	0	1
1	0	0	1	0	0	0	1	1
3	0	1	1	0	0	1	0	1
5	1	0	0	0	0	0	0	0
4	1	0	0	X	X	X	X	X
6	1	1	0	X	X	X	X	X
7	1	1	1	X	X	X	X	X

For  $D_2$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	0	1
$\bar{q}_2$	0	0	1	0
$q_2$	X	0	X	X

For  $D_1$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	1	X	0	0
$\bar{q}_2$	0	0	1	0
$q_2$	X	0	X	X

Wk -07

17  
February  
Saturday

Days 048-317

2018

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

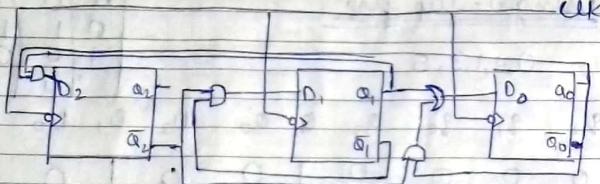
$$D_2 = Q_1 Q_0$$

$$D_1 = \bar{Q}_1 \bar{Q}_2$$

For  $D_0$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	0	1	1	1
$\bar{q}_2$	0	0	1	0
$q_1$	X	O	X	X

$$D_0 = Q_1 + Q_0 \bar{Q}_2$$

III) Using T flip flop $0, 2, 1, 3, 5$ 

Sunday 18

M T W T F S S  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28 29 30 31

2018

Days 050-315

19  
February  
Monday

Wk -08

$q_2$	$q_1$	$q_0$	$Q_2$	$Q_1$	$Q_0$	$T_2$	$T_1$	$T_0$
0	0	0	0	0	1	0	0	1000
1	0	0	0	1	1	0	1	00
2	0	1	0	0	0	1	0	101
3	0	1	1	1	0	1	1	100
4	1	0	0	X	X	X	X	X
5	1	0	1	0	0	0	0	1
6	1	1	0	X	X	X	X	X
7	1	1	1	X	X	X	X	X

For  $T_2$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	0	0	1	0
$\bar{q}_2$	X	1	X	X

$$T_2 = q_1 q_0 + q_2$$

$$T_1 = \bar{q}_2$$

For  $T_0$ 

$q_1 q_0$	$\bar{q}_1 \bar{q}_0$	$\bar{q}_1 q_0$	$q_1 \bar{q}_0$	$q_1 q_0$
$q_2$	0	0	0	1
$\bar{q}_2$	X	1	X	X

$$T_0 = q_2 + q_1 \bar{q}_0$$

Wk-08

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February  
Tuesday

Days 051-314

2018

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

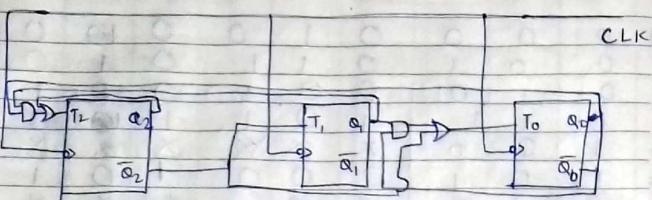
FEBRUARY

Days 052-313

2018

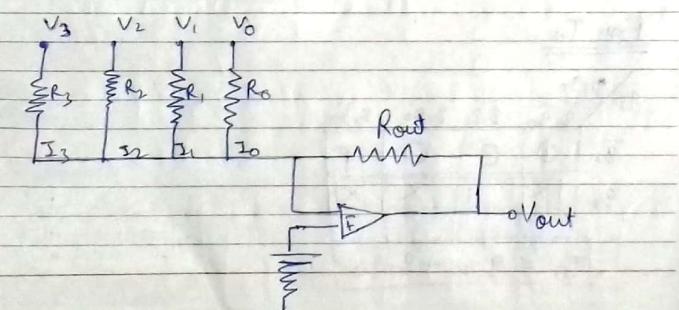
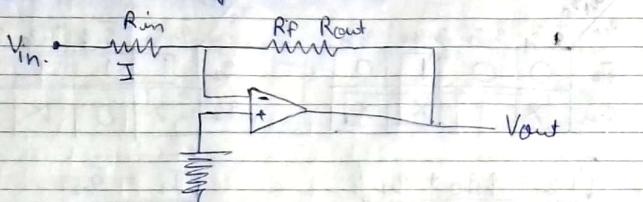
21  
February  
Wednesday

Wk-08



## TOPIC - 18

★ Digital to Analog converter:→



M	T	W	T	F	S	S
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30	31		

$$I = I_0 + I_1 + I_2 + I_3$$

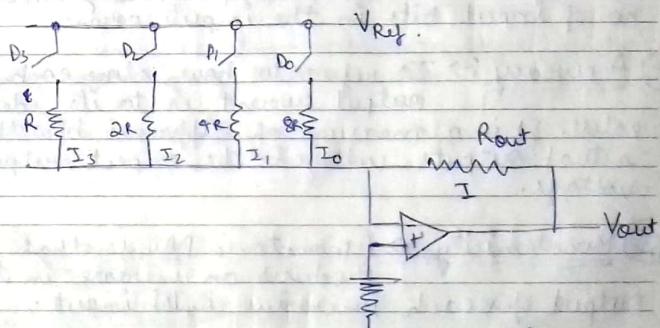
$$I_0 = \frac{R_0}{V_{ref}}$$

$$V_{out} = \left[ \frac{V_3}{R_3} + \frac{V_2}{R_2} + \frac{V_1}{R_1} + \frac{V_0}{R_0} \right] R_{out}$$

If there is a common Vref

$$\therefore V_{out} = \left[ \frac{1}{R_3} + \frac{1}{R_2} + \frac{1}{R_1} + \frac{1}{R_0} \right] V_{ref} \cdot R_{out}$$

## (I) Binary weighted resistor DAC



$$I = \frac{V_{ref}}{R} \left[ \frac{1}{2^0} + \frac{1}{2^1} + \frac{1}{2^2} + \frac{1}{2^3} \right] = 1.875 \frac{V_{ref}}{R}$$

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22  
February  
Thursday

Days 053-312

2018 | M T W T F S S  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28 | FEBRUARY

$$V_{out} = -\frac{R_f}{R} V_{ref} \left( D_3 + \frac{D_2}{2} + \frac{D_1}{4} + \frac{D_0}{8} \right)$$

### \* Specification of DAC

(I) Resolution :→ It is the ratio of the LSB implement to the maximum output

$$\text{Resolution} = \frac{1}{2^n - 1}$$

→ It is also define as the smallest implement in the voltage that can be observed by the circuit and depends primarily on the no. of input bits in the input word.

(II) Accuracy :→ It refers to how close each output current is to its ideal value. It is a measure of difference b/w the actual outputs voltage & the expect output voltage.

(III) Monotonicity :→ A monotonic DAC is that produces an increase in the output for each successive digital input.

(IV) Settling time :→ When the digital input convert the changes approximately voltage changes occurs as the switches are

MARCH | M T W T F S S  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28 29 30 31 | 2018

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23  
February  
Friday

Wk-08

broken or closed. There is a finite time required to reach the new output level. This time interval that ellapse from the input change through the time what the output can settle are close enough.

(V) Temperature sensitivity :→ For any fix digital input the analog output will vary. The overall temperature sensitivity of due to ~~due to~~ temperature sensitivity of a reference voltage and the offset voltage of an open.

### \* Drawback

(I) For a n-bit digital input n resistors are required in addition to a load resistance.

(II) The values of resistors should be perfect for the proper operation of D/A converter.

(III) Each resistor, The values are different so they handle different current.

### \* Analog to Digital Converter

→ Successive Approximation A/D converter

Wk-08

24

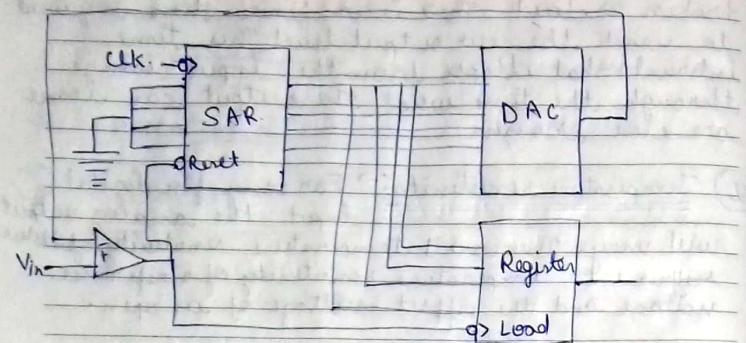
February Saturday

Days 055-310

2018

FEBRUARY

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				



Q) An 8 bit ADC at a resolution of 20 mV. what will be its digital output for an analog input of  $2.17 \text{ mV}$ .

Sel)

$$\text{Resolution} = \frac{1}{2^n - 1}$$

$$\Rightarrow 20 \text{ mV} = \frac{2.17}{2^n - 1} \Rightarrow 2^n - 1 = \frac{2.17}{20 \times 10^{-3}}$$

$$\Rightarrow 2^n - 1 = 100 \frac{2.17 \times 10^3}{20}$$

$$\Rightarrow 2^n - 1 = 2.17 \times 10050$$

$$\Rightarrow 2^n = 108$$

$$\Rightarrow 2^8 = 108 \Rightarrow (11011000)_2$$

Sunday 25

MARCH

2018

MARCH

M	T	W	T	F	S	S
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

2018

Topic :- 19.

Days 057-308

26

February Monday

Wk-09

### \* Logic families

RTL → Resistor Transistor Logic

DTL → Diode Transistor logic

DCTL → Diode Coupled Transistor logic

HTL → High threshold logic

I<sup>2</sup>L → Injection Injection logic

TTL → Transistor Transistor logic

ECL → Emitter Coupled logic

- RTL is the oldest logic family.
- DTL is low cost family that give rise to TTL.
- HTL has the most noise immunity.
- ECL has the least propagation delay.
- I<sup>2</sup>L has highest packing density.
- CMOS - has extremely low power disturbance.
- TTL - is very design logic family. It can be used for many complex functions.

### ⇒ Characteristics of digital logic families

i) Propagation delay :→ It is the time taken by the logic circuit to produce the output after receiving all the inputs.

ii) Fan in :→ It is the minimum number of inputs that can be connected to the input of a digital circuit.

iii) Fan out :→ It is the minimum number of load that can be connected to the output

27  
February  
Tuesday

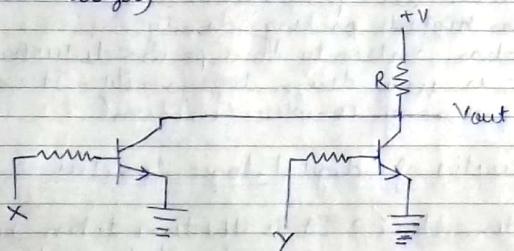
Days 058-307

2018  
M T W T F S S  
5 6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28

of the digital gate.

- ④ Noise margin : $\rightarrow$  It is the range of noise voltage that can be present ~~on~~ or may be present in a digital circuit without affecting its operation.
- ⑤ Operating temperature : $\rightarrow$  It is the range of temperature within which the digital ICs can operate.

### \* RTL (Resistor-transistor logic)



### Parameters of RTL

- ① Exhibit poor noise margin
- ② Poor fan out
- ③ Low speed operation
- ④ High propagation delay
- ⑤ High power dissipation

### \* DTL (Diode-transistor logic)

#### Parameters of DTL

- ① It has propagation delay - 30 ns
- ② Power dissipation 12 mW
- ③ Fan out is 8

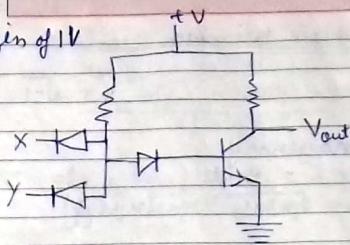


28  
February  
Wednesday

Days 059-308

2018  
M T W T F S S  
6 7 8 9 10 11  
12 13 14 15 16 17 18  
19 20 21 22 23 24 25  
26 27 28 29 30 31

iv) Noise margin of 1V



### \* TTL (Transistor-transistor logic)

S.No.	Name	Aberration	Propagation delay	Power dissipation	Speed power product
1.	Standard TTL	TTL	10	10	100
2.	Low-power TTL	L TTL	33	1	33
3.	High speed TTL	H TTL	6	22	132
4.	Schottky TTL	STTL	3	19	57
5.	Low-Power Schottky TTL	LSTTL	9.5	2	19

AUGUST	M	T	W	T	F	S	S
	1	2	3	4	5		
	6	7	8	9	10	11	12
	13	14	15	16	17	18	19
	20	21	22	23	24	25	26
	27	28	29	30	31		

# Digital Electronics

2018

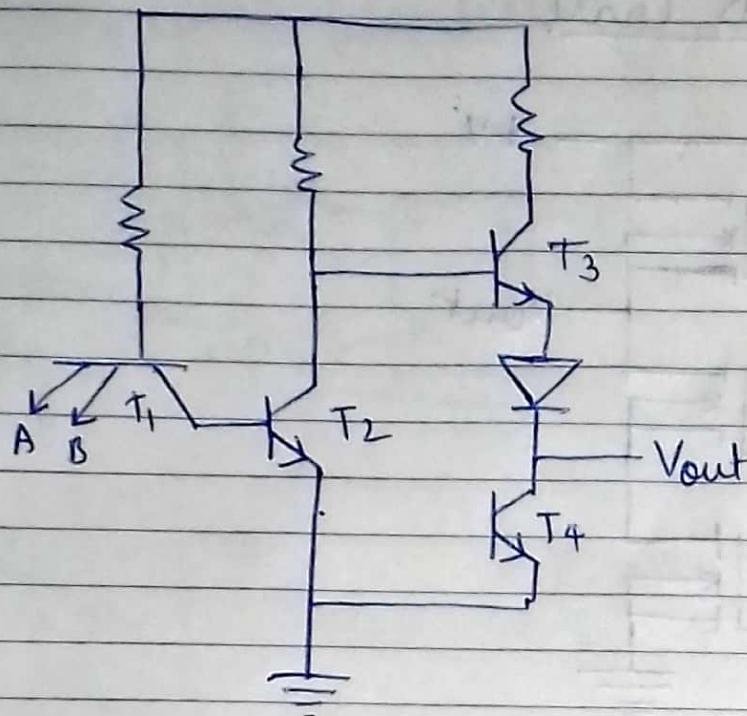
Days 183-182

02

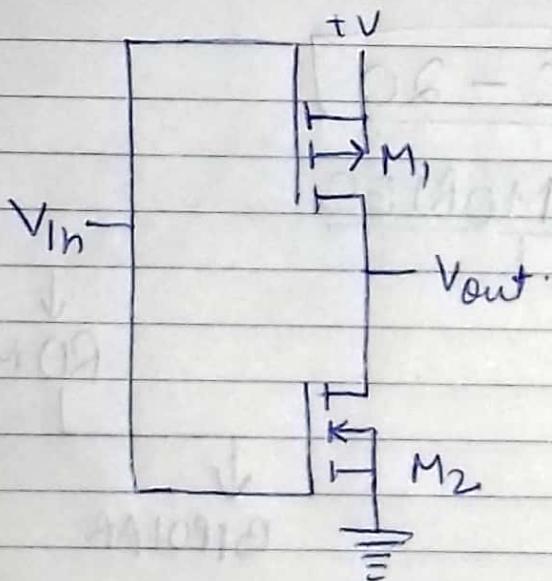
July  
Monday

Wk.-27

★ TTL



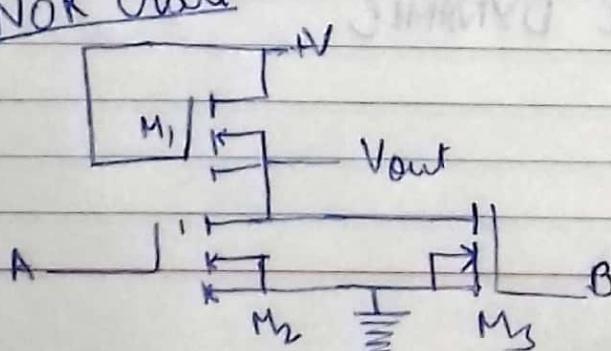
★ CMOS



CMOS consist of both PMOS and NMOS. It operates faster than circuits having only PMOS and NMOS.

★ NMOS

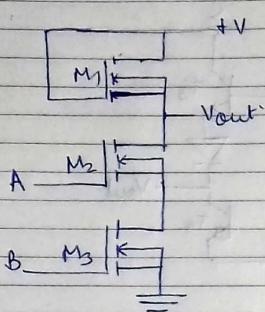
NOR Gate



Transistors M1 & M2 are connected in ||.

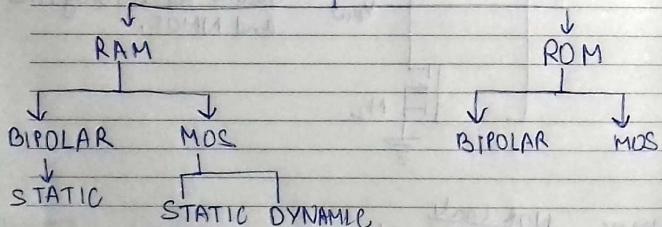
Wk-27  
03  
July  
Tuesday

Days 184-181  
2018  
NMOS



TOPIC - 20

MEMORIES



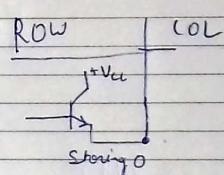
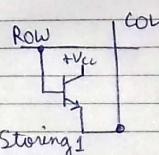
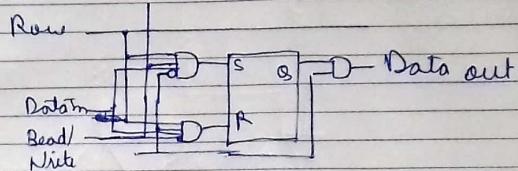
2018

AUGUST  
2018  
Days 185-180

04  
July  
Wednesday

Wk-27

Column static Ram cell.



For reading from the memory R/W is High  
For writing from the memory R/W is Low.

D