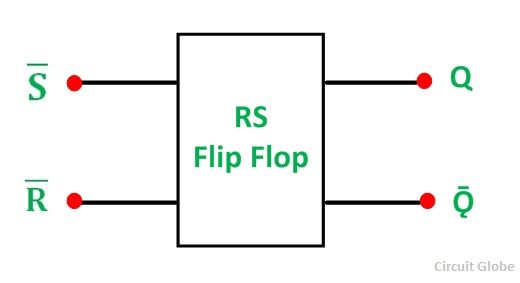
**Experiment - 4**

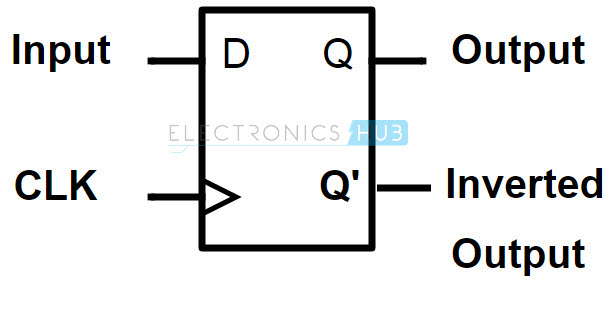
Submitted by ADITYA SINGH 2K19/EP/005

**Aim** - To verify truth tables of R-S, D and J-K Flip Flops.

**Theory**

R-S Flip Flop

It has two inputs, one is called “SET” which will set the device (output = 1) and is labelled S and another is known as “RESET” which will reset the device (output = 0) labelled as R. The RS stands for SET/RESET.

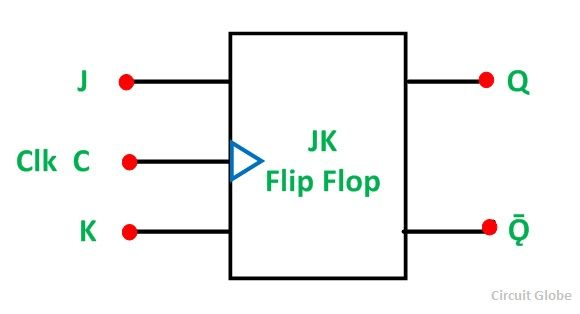


D Flip Flop

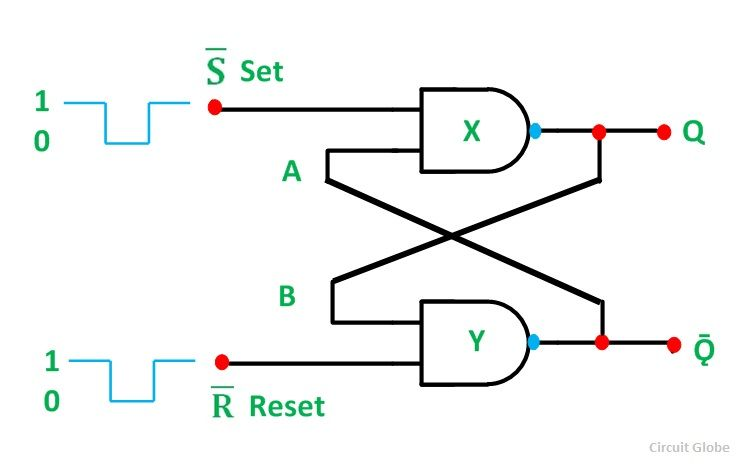
The D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level.

One of the main disadvantages of the basic SR NAND Gate Bistable circuit is that the indeterminate input condition of SET = “0” and RESET = “0” is forbidden.

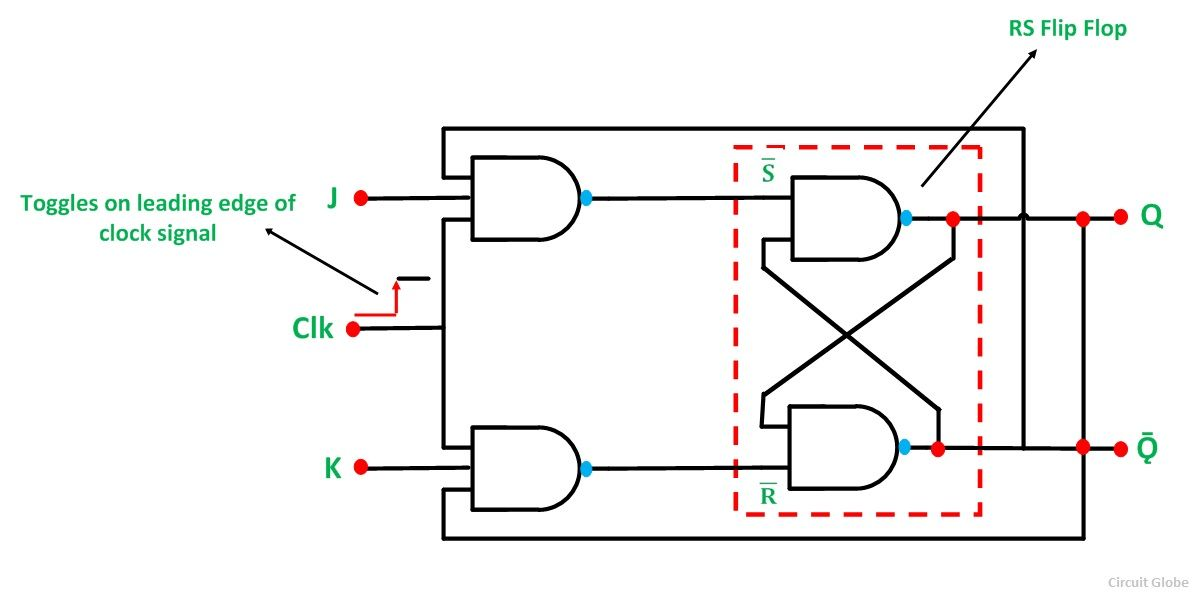
J-K Flip Flop

It is considered to be a universal flip-flop circuit. The sequential operation of the JK Flip Flop is the same as for the RS flip-flop with the same SET and RESET input.

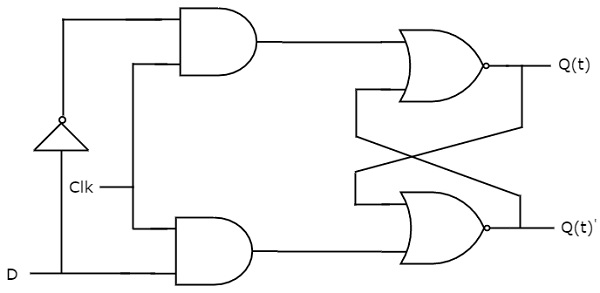
The difference is that the JK Flip Flop does not invalidate the invalid input states of the RS Latch (when S and R are both 1).

**Circuit Diagram**

1. R-S Flip Flop



1. J-K Flip Flop



1. D Flip Flop

**Truth Tables**

1. R-S Flip Flop

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **S** | **R** | **Qnext** | **Action** | **Q** | **Qnext** | **S** | **R** |
| 0 | 0 | Q | Hold state | 0 | 0 | 0 | X |
| 0 | 1 | 0 | Reset | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | Set | 1 | 0 | 0 | 1 |
| 1 | 1 | X | Not allowed | 1 | 1 | X | 0 |

1. J-K Flip Flop

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **J** | **K** | **Comment** | **Qnext** | **Q** | **Qnext** | **Comment** | **J** | **K** |
| 0 | 0 | Hold state | Q | 0 | 0 | No change | 0 | X |
| 0 | 1 | Reset | 0 | 0 | 1 | Set | 1 | X |
| 1 | 0 | Set | 1 | 1 | 0 | Reset | X | 1 |
| 1 | 1 | Toggle | Q | 1 | 1 | No change | X | 0 |

1. D Flip Flop

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  |  | | --- | --- | --- | --- | | **D** |  | **Q** | **Q** | | 0 | 0 | 0 | | 0 | 1 | 0 | | 1 | 0 | 1 | | 1 |  | 1 | 1 | |  |

**Expressions**

1. R-S

Qn+1 = S + R’Qn

1. J-K

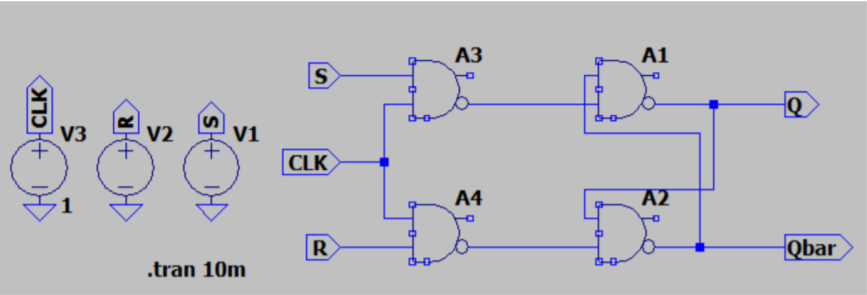
Qn+1 = JQn’ + K’Qn

1. D

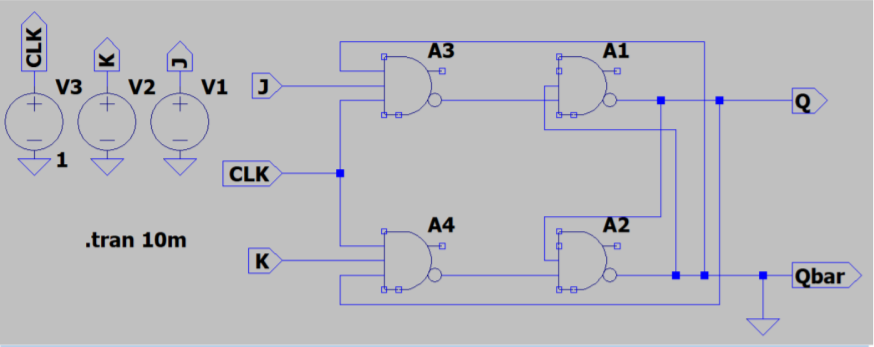
Qn+1 = D

**Design**

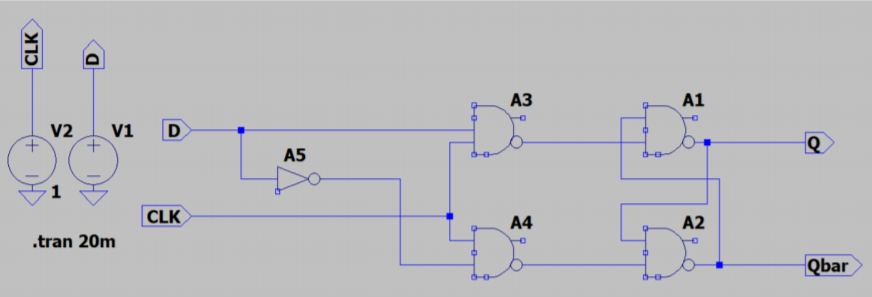
1. R-S Flip Flop



1. J-K Flip Flop

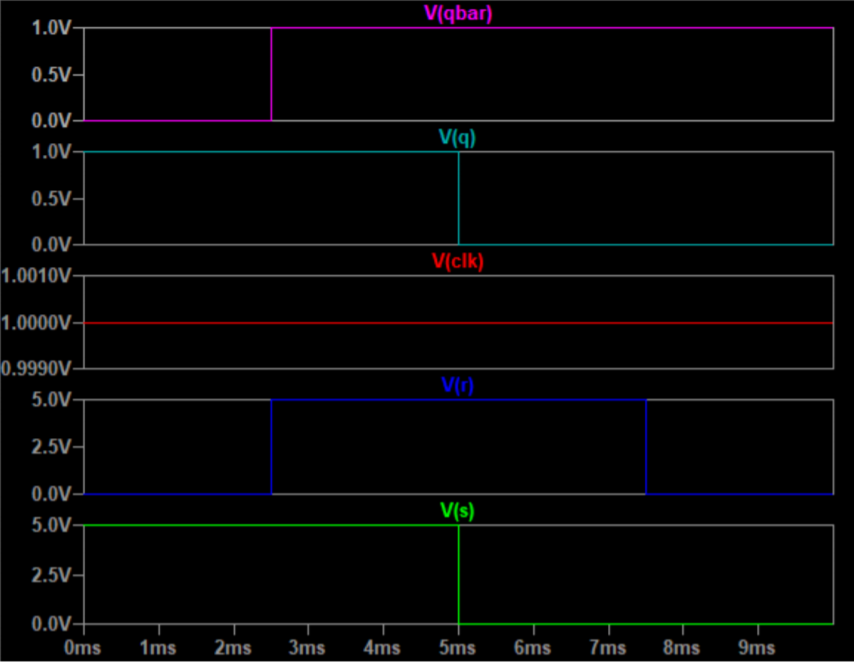


1. D Flip Flop

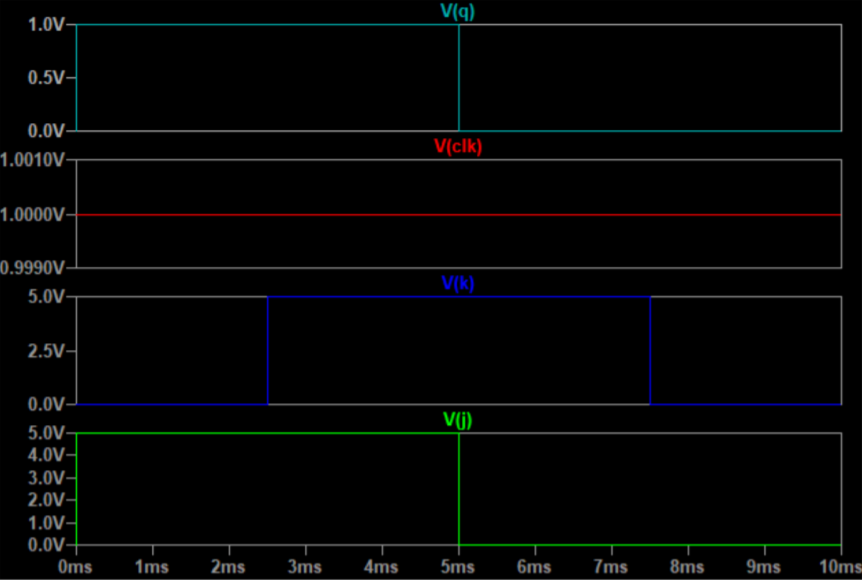


**Results**

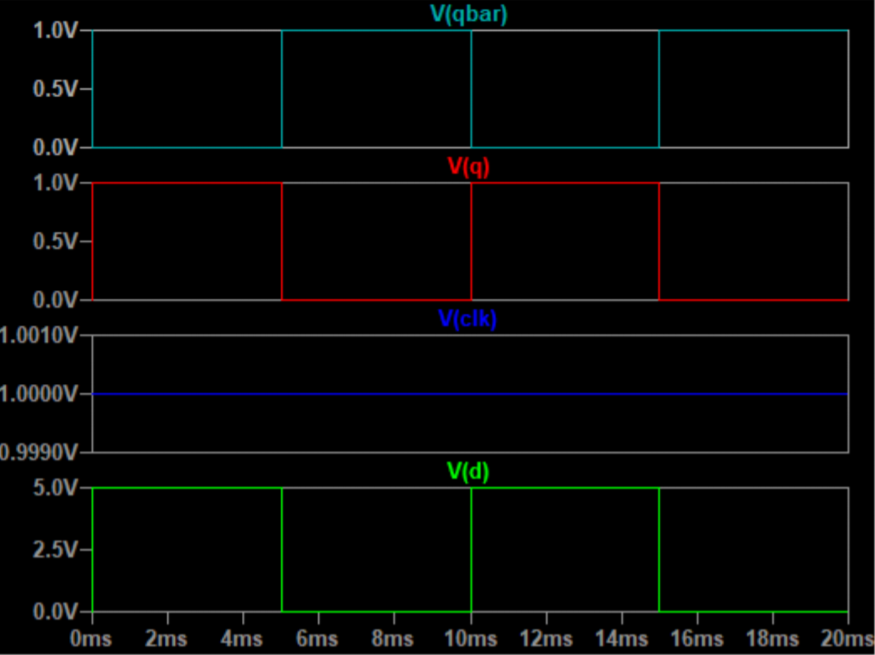
1. R-S Flip Flop



1. J-K Flip Flop



1. D Flip Flop



END