**Experiment - 5**

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**Aim** - To verify the operation of Shift Registers: SISO, SIPO, PISO and PIPO.

**Theory -**

## Serial-in to Serial-out (SISO) Shift Register

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The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.

Serial-in to Parallel-out (SIPO) Shift Register

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It looks like a serial-in, serial-out shift register with taps added to each stage output.Serial data shifts in at SI (Serial Input). After a number of clocks equal to the number of stages, the first data bit appears at SO (QD) in the above figure.

In general, there is no SO pin. The last stage (QD above) serves as SO and is cascaded to the next package if it exists.

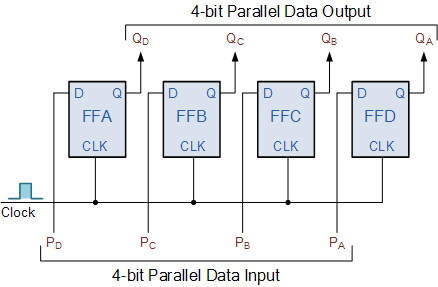
## Parallel-in to Serial-out (PISO) Shift Register

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The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins PA to PD of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at PA to PD.

This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

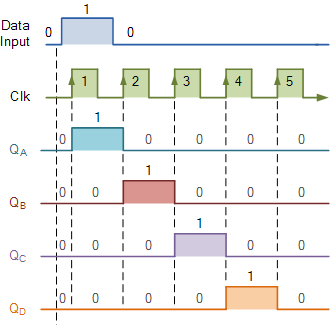
## Parallel-in to Parallel-out (PIPO) Shift Register



The final mode of operation is the Parallel-in to Parallel-out Shift Register. This type of shift register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above. The data is presented in a parallel format to the parallel input pins PA to PD and then transferred together directly to their respective output pins QA to QD by the same clock pulse. Then one clock pulse loads and unloads the register.

**Basic Data Movement Through Shift Registers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Pulse** | **QA** | **QB** | **QC** | **QD** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 0 | 0 |

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**Design**

