**Experiment - 7**

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**Aim** - To study the operation of 8-bit parity generator and checker; and operation of BCD to 7-segment display (74180, 7447).

**Theory**

### Parity Generator

It is a combinational circuit that accepts an n-1 bit stream data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is termed as a parity bit.

In an even parity bit scheme, the parity bit is ‘0’ if there are an even number of 1s in the data stream and the parity bit is ‘1’ if there are an odd number of 1s in the data stream.

In an odd parity bit scheme, the parity bit is ‘1’ if there are an even number of 1s in the data stream and the parity bit is ‘0’ if there are an odd number of 1s in the data stream.

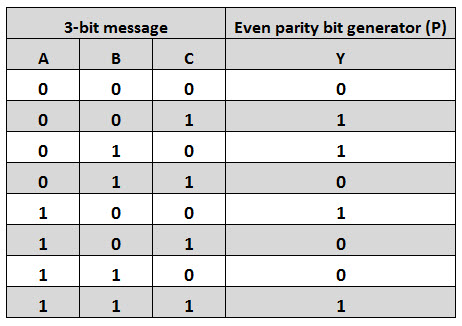
### Parity Check

It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as an even parity checker, the number of input bits must always be even.

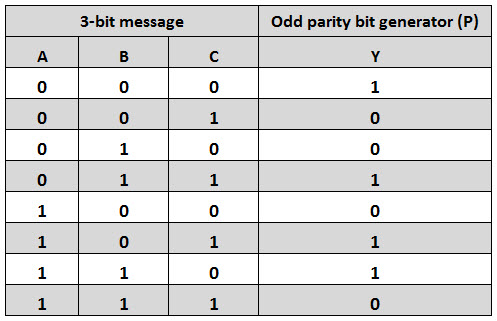
When a parity error occurs, the ‘sum even’ output goes low and ‘sum odd’ output goes high. If this logic circuit is used as an odd parity checker, the number of input bits should be odd, but if an error occurs the ‘sum odd’ output goes low and ‘sum even’ output goes high.

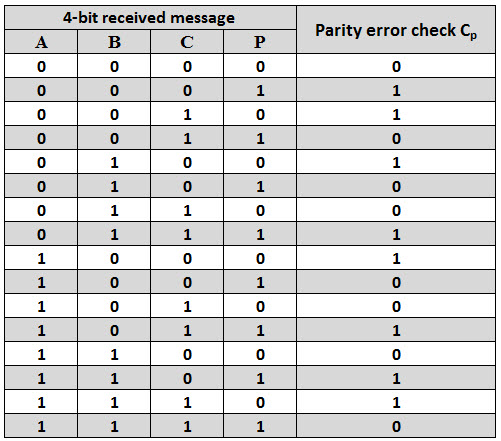
**Truth Tables**

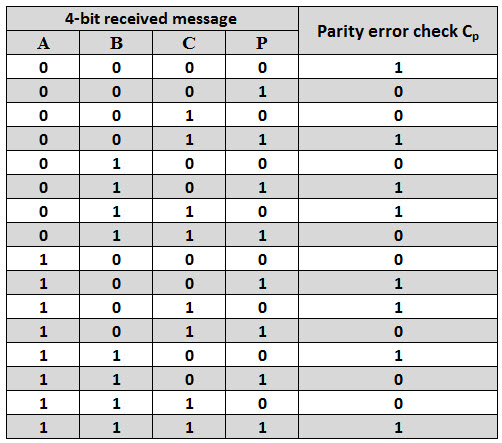
1. Even Parity Generator



1. Odd Parity Generator

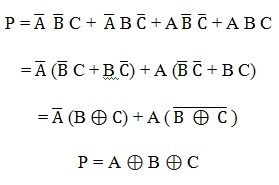
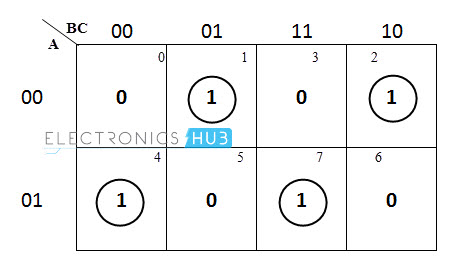


1. Even Parity Checker
2. Odd Parity Checker

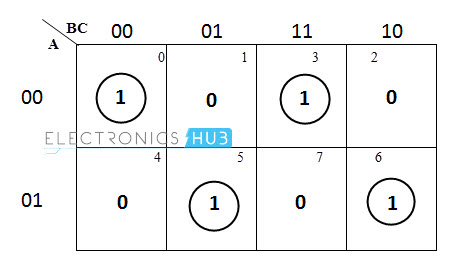


**Expressions**

1. Even Parity Generator

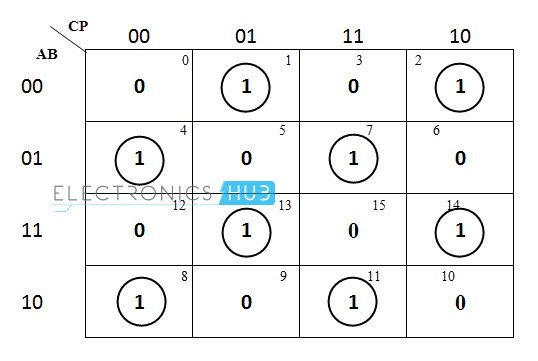


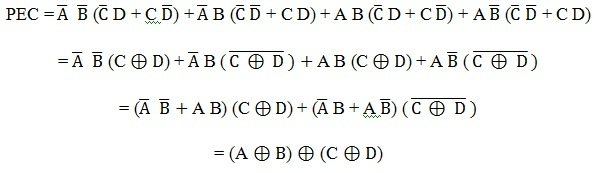
1. Odd Parity Generator



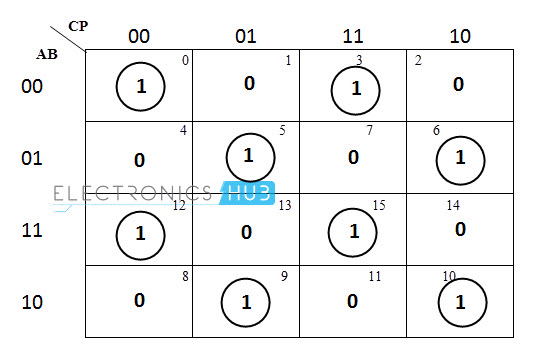
P = A ⊕ B Ex-NOR C

1. Even Parity Checker

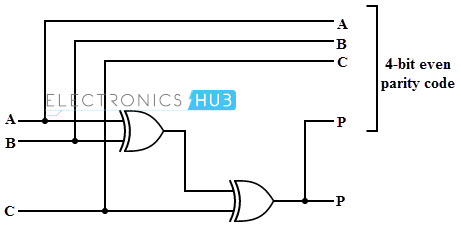


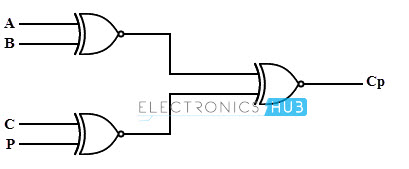


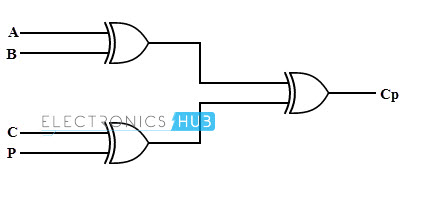
1. Odd Parity Checker



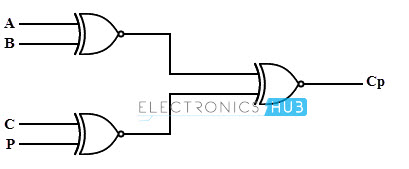
PEC = (A Ex-NOR B) Ex-NOR (C Ex-NOR D)

**Circuit Diagram**

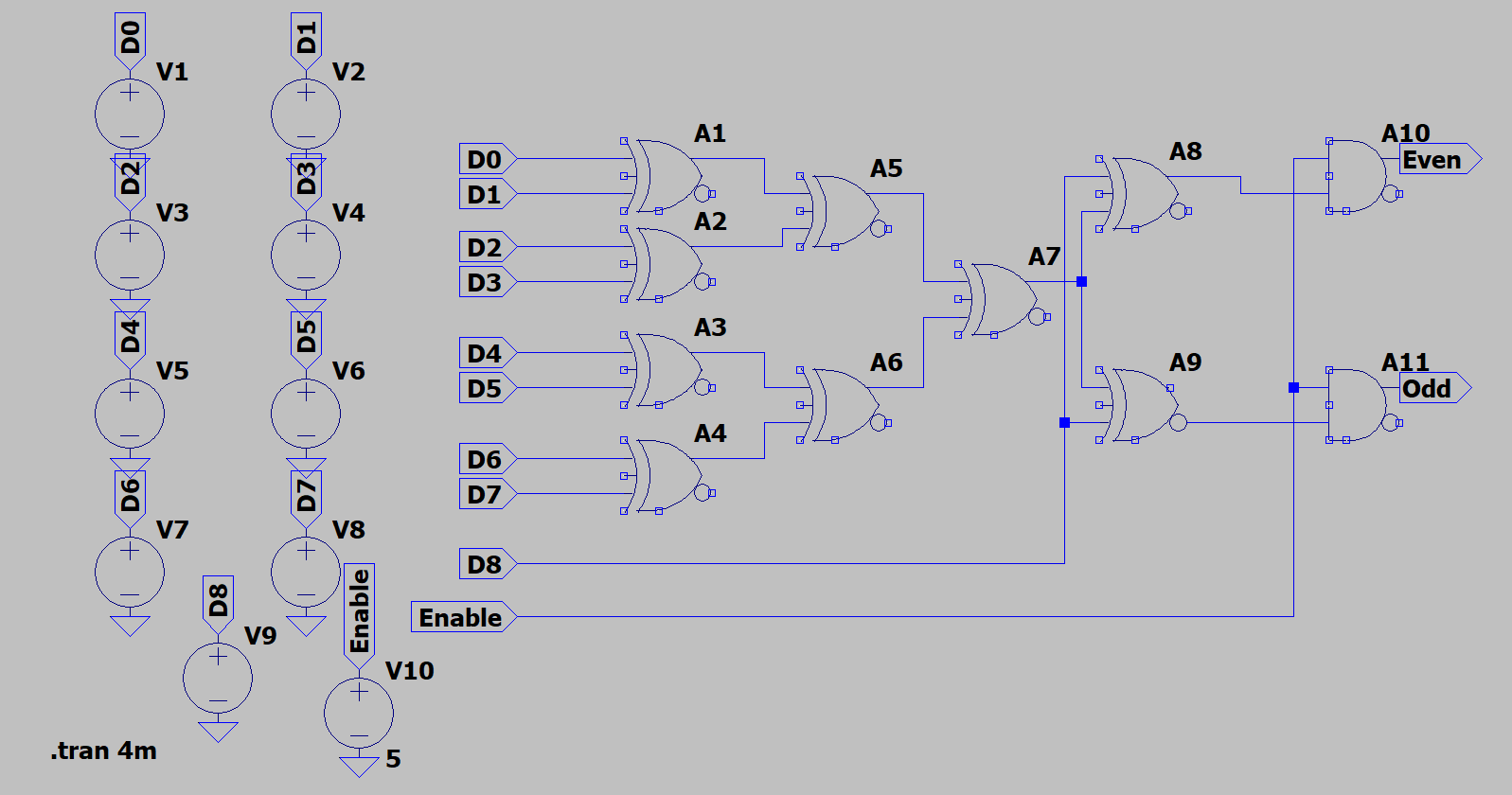
1. Even Parity Generator
2. Odd Parity Generator



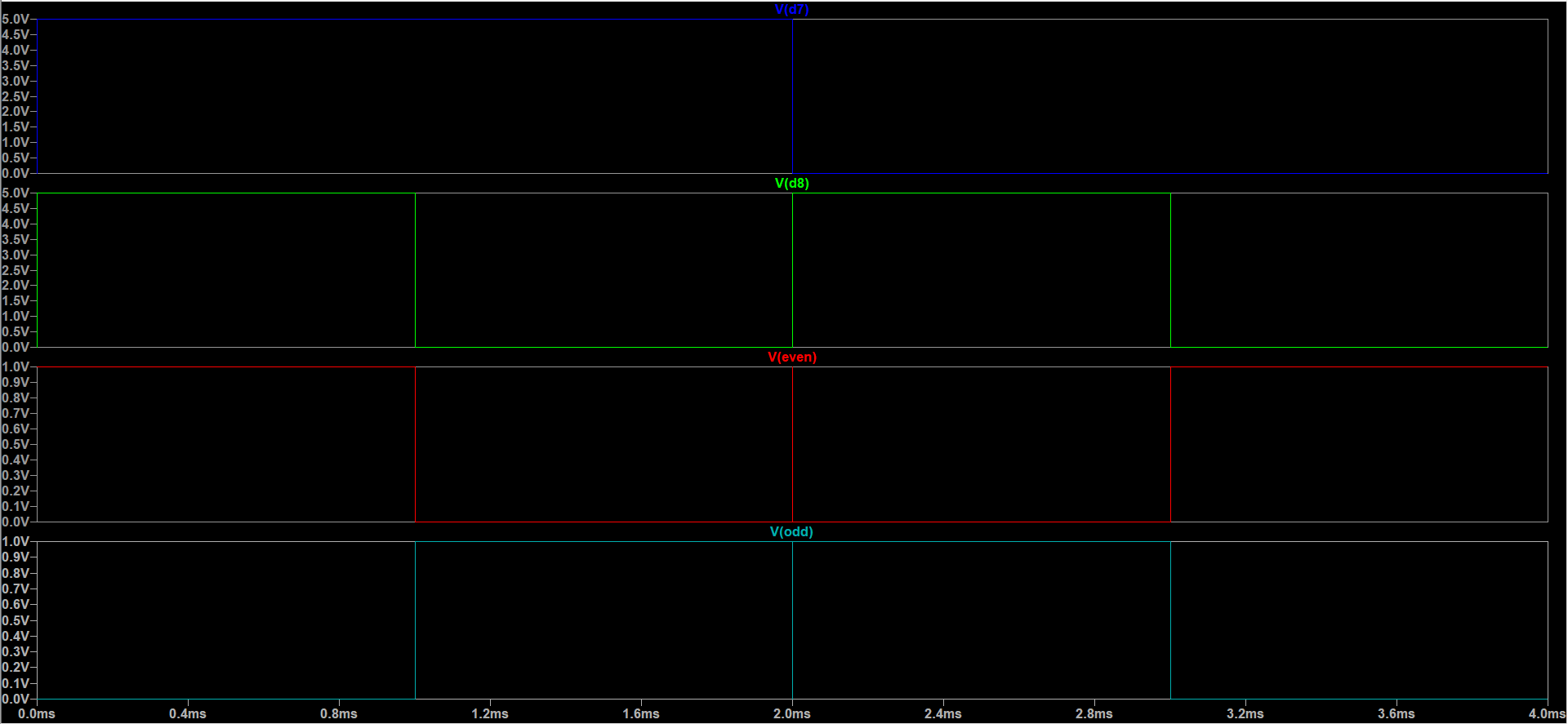
1. Even Parity Checker
2. Odd Parity Checker



**Design**



**Results**



END