8257 | DMA CONTROLLER

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8257 DMAC | PIN DIAGRAM

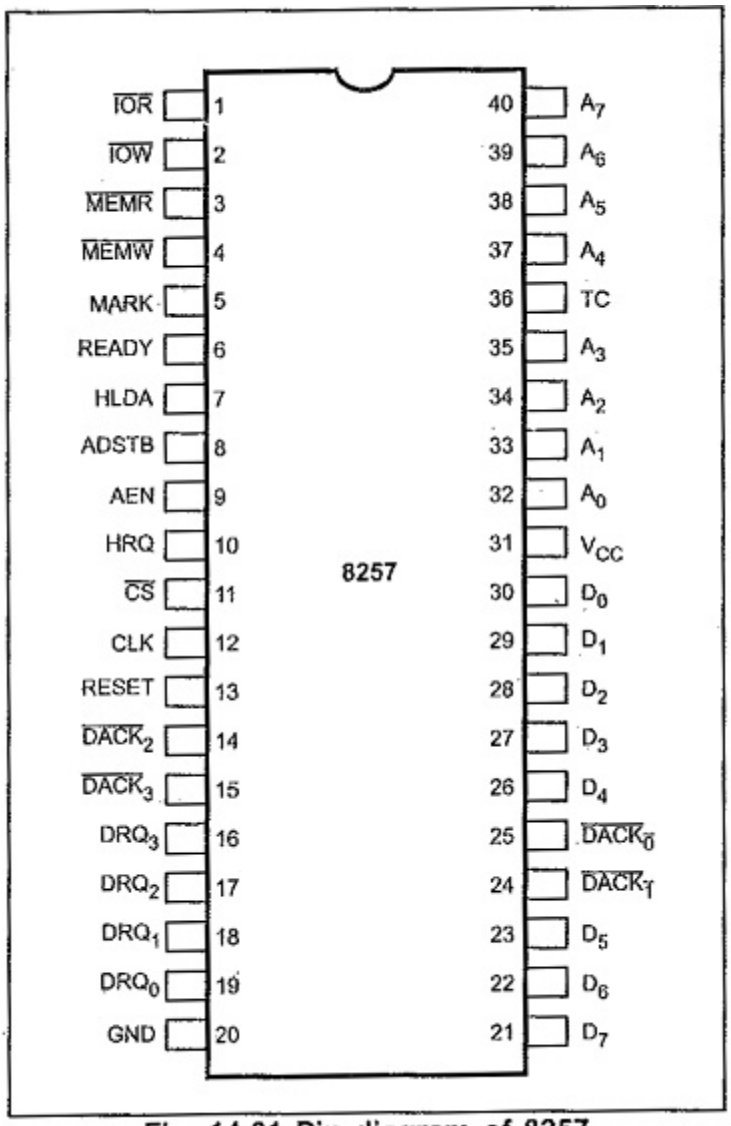


Fig. 14.61 Pin diagram of 8257

1) DREQ3 … DREQ0 (Data Request lines)

These input pins are used by the I/O device to request the DMAC for DMA Transfer.
These pins can be made active high / active low through program.
By default, they are active high.
There are 4 DREQ pins as there are 4 channels (one per channel).
At a time only one channel can perform DMA transfer.
Thus, for multiple simultaneous requests, priorities are used.
DREQ0 has the highest priority while DREQ3 has the lowest priority. (Fixed priority mode)

2) $\overline{DACK_3}$ … $\overline{DACK_0}$ (Data Acknowledgement)

These output pins are used by the DMAC to inform the I/O device that it is performing a data transfer.
This pin becomes low just before a DMA data transfer.
There are 4 DACK pins as there are 4 channels (one per channel).

3) HRQ (Hold Request)

This output pin is used by the DMAC to request the µP to release the system bus.
It is connected to the HOLD pin of the µP.

4) HLDA (Hold Acknowledge)

This input pin is used by the µP to inform the DMAC that it as released to system bus.
It is connected to the HLDA pin of the µP.

5) AEN (Address Enable)

This is an output pin from the DMAC.

When AEN = 0 (default), μP is the Bus master.
At that time the latches of the μP are enabled and the DMAC latch is disabled.

When AEN = 1, DMAC is the Bus master.
At that time the latches of the μP are disabled and the DMAC latch enabled.
This connects the DMAC's address-data lines to the system bus.

6) ADSTB (Address Strobe)

It is an output signal.
To put it simply this is the ALE issued by the DMAC.

When ADSTB = 1, the multiplexed bus (DB0-DB7) carries address (A8-A15).
When ADSTB = 0, the multiplexed bus (DB0-DB7) carries data (D0-D7).

7) DB7 – DB0 (Data Bus)

These are 8 bi-directional data lines used to connect the internal data bus of 8257 with the external (system) data bus.
When μP is the bus master, this bus is used by the μP to read/write from the DMAC.
In active cycle (which means DMAC is the bus master), this bus carries the 8 higher order bits of the 16 bit address (the other 8 bits being in the A7–A0).
During memory-to-memory transfer, this bus carries the data byte to be transferred.

8) A7 – A4 (Address bits)

These are 4 output address lines.
In active cycle, these lines carry the A7–A4 bits of the address at which the transfer is to be done. As this address is generated by the 8257, these are output lines.

9) A3 – A0 (Address bits)

These are 4 bi-directional address lines.
In idle cycle, µP sends the address A3–A0, to select one of its registers.
Since µP sends the address to 8257, these are input lines.
In active cycle, these lines carry the A3–A0 bits of the address at which the transfer is to be done. As this address is generated by the 8257, these are output lines.

10) $\overline{\text{IOR}}$, $\overline{\text{IOW}}$

These are bi-directional control lines.
During idle state, the µP issues these signals to read from or write into the 8257 (as the DMAC itself is an I/O device w.r.t. the µP).
During active state, the DMAC issues these signals to read from or write into an I/O Device.

11) $\overline{\text{MEMR}}$, $\overline{\text{MEMW}}$

These are output control lines.
During active state, the DMAC issues these signals to read from or write into the Memory.

12) Ready

Similar function as Ready pin of the μP.
It is used to synch DMAC with slower devices when DMAC is the Bus Master.
DMAC checks this signal during every DMA transfer cycle.

If Ready = 1, it means I/O device is ready.
Hence DMAC will continue with the transfer.

If Ready = 0, it means I/O device is not ready.
Hence DMAC will insert Wait states during the transfer to allow the device to become ready.

13)CLK

This is a clock-input signal for the DMAC.
It is usually connected to the system clock.

14)RESET

This is a reset-input signal for the DMAC.
This signal clears the internal registers of the DMAC and causes it to enter Idle State.

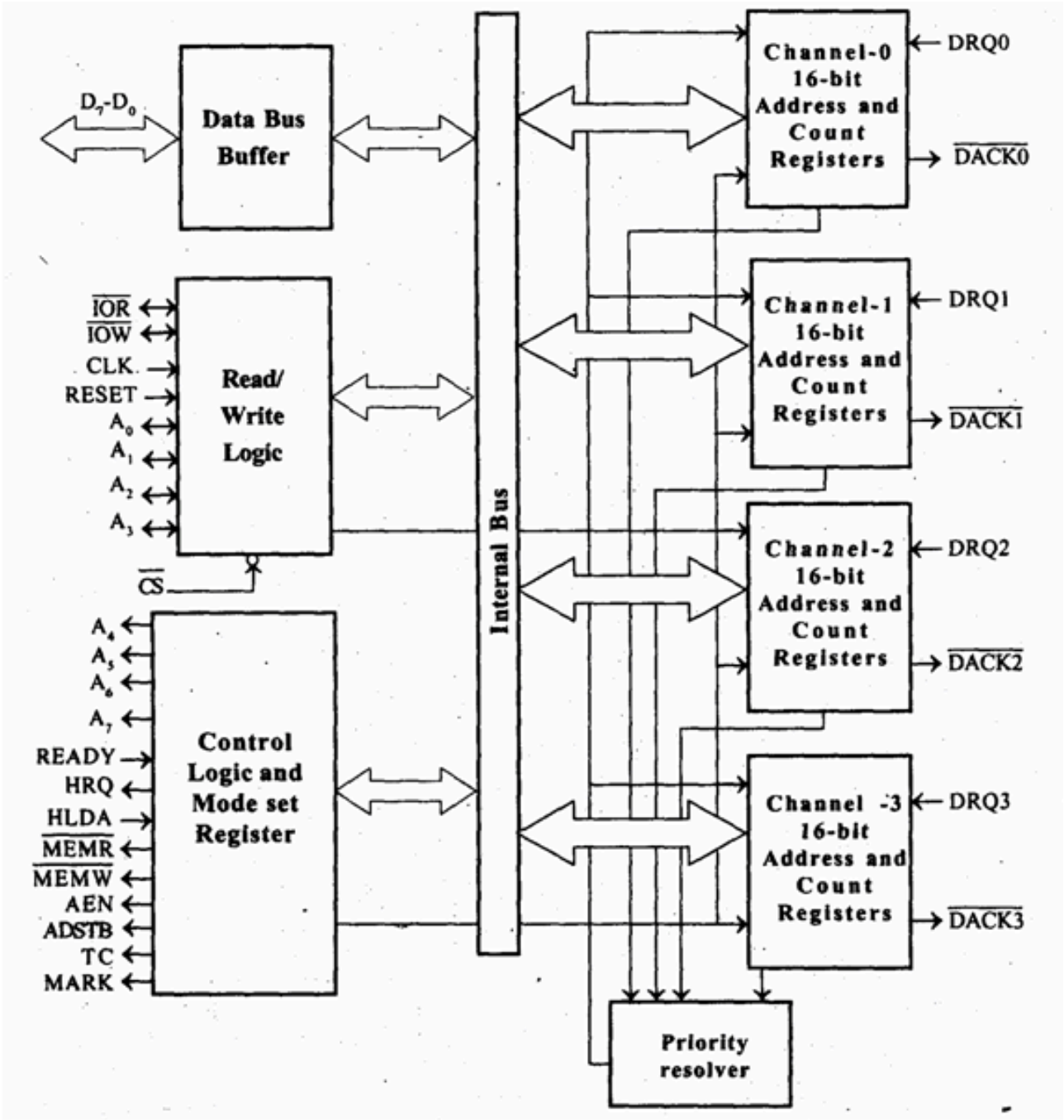
15) TC

This is an output signal from the DMAC.
It becomes 1 to indicate that terminal count is reached, that means the count has become 0 and hence the transfer has been completed.

16) Mark

This is an output signal from the DMAC.
It is a modulo 128 mark output. This means it becomes 1 on every 128^{th} cycle of the data transfer as a marker to indicate that a batch of 128 cycles has been completed.

8257 DMAC | ARCHITECTURE



The internal architecture of 8257 has the following components

1) DMA Channels (0…3)
2) Priority Resolver
3) Data Bus Buffer
4) Read Write Logic
5) Control Logic and Mode Set Register

1) DMA Channels (0…3)

A single 8257 DMAC has 4 DMA Channels (0…3)
Four I/O devices are connected on these DMA Channels, one on each.
In the default priority mode (Fixed priority), Channel 0 is the highest and 3 is the lowest priority.

Each Channel has 4 components:
Address Register, **Terminal Count Register**, **DREQ** and $\overline{\textbf{DACK}}$.

a) Address Register (16 bit)

It is used to store the 16 bit memory address for the DMA Transfer.
μP initializes this register with the starting address of the DMA Transfer.
Thereafter, as each byte is transferred the address gets incremented
(or decremented, depending upon the mode selected by the programmer)

b) Terminal Count Register (16-bit)

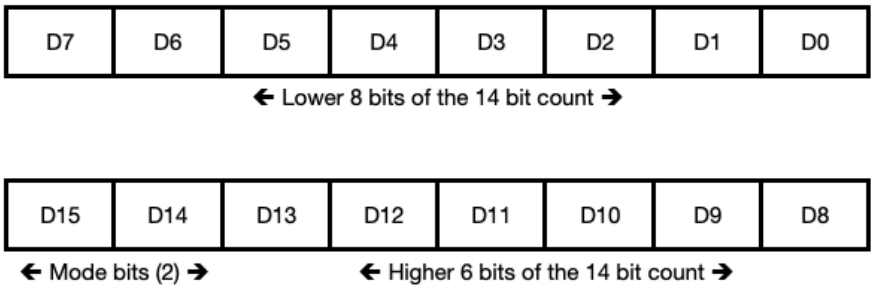
It is used to store the 14bit count of the DMA Transfer.
The remaining higher two bits are used to decide the mode of DMA operation.
μP initializes this register with the 14 bit count (N-1) of the DMA Transfer.
Thereafter, as each byte is transferred the count gets decremented.
This repeats till the count becomes 0 also called Terminal Count (TC).

The higher two bits are used to select the mode.
They can be used to give 3 different modes: DMA Verify, DMA Read, DMA Write

DMA Read

In this mode, when DMAC becomes the bus master, it transfers data from Memory to I/O. Hence in every transfer, the signals produced are $\overline{\textbf{MEMR}}$ **and** $\overline{\textbf{IOW}}$

Count Register: 16 bit (D15...D0)



Mode Bits		Mode Selected
0	0	DMA Verify Cycle
0	1	DMA Write Cycle (I/O to Memory)
1	0	DMA Read Cycle (Memory to I/O)
1	1	No action

DMA Write

In this mode, when DMAC becomes the bus master, it transfers data from I/O to Memory. Hence in every transfer, the signals produced are **$\overline{\text{IOR}}$ and $\overline{\text{MEMW}}$**

DMA Verify

In this mode, when DMAC becomes the bus master, it doesn't really transfer any data. This mode is just used to verify the DMA process.
The DMAC will issue a HOLD, will become bus master, issue the acknowledgement to the I/O device and so on. It just will not produce any read or write signals to perform any data transfer. If you are learning by Piracy, you are a THIEF!

c) DREQ

I/O device gives this signal to the DMAC to request a DMA transfer

d) $\overline{\text{DACK}}$

It is given by DMAC to the I/O device, indicating that a DMA transfer is being performed.

2) Priority Resolver

Priority is needed when several DMA channels get request (DREQ) from I/O devices "simultaneously" for data transfer. Priority resolver decides which channel will be "serviced" first, and which one will become "pending". There are two priority schemes: Fixed Priority and Rotating Priority.

Fixed Priority

This is the Default Mode.
Channel 0 is the highest priority and Channel 3 is the lowest.
Fixed priority causes Domination.
If Channel 0 and 1 keep requesting all the time the Channel 2 and 3 will starve and never get a chance. This is called Domination.
To avoid this, we can use Rotating Priority.

Rotating Priority

Here, once a channel is serviced it becomes the lowest priority.
All channels below it rise up by one position in the priority order.
As priorities move in a circular manner, it is called Rotating Priority.
It gives every channel a fair chance of being high priority and hence prevents Domination.

Before CH.0 is serviced

Highest	CH.0
	CH.1
	CH.2
Lowest	CH.3

← Active DMA request

After CH.0 is serviced

CH.1	Highest
CH.2	
CH.3	
CH.0	Lowest

3) Read Write Logic

It mainly provides the read and write signals as well as the chip select signal.

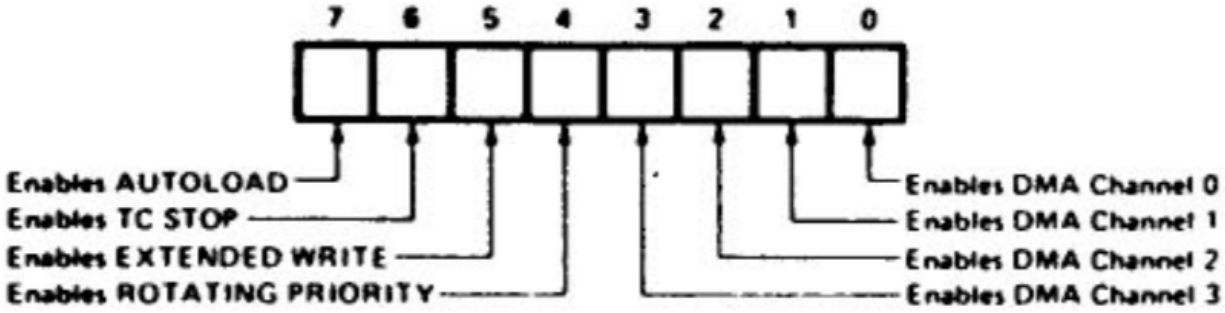
The read and write signals are connected to $\overline{\textbf{IOR}}$, $\overline{\textbf{IOW}}$ of the μP.

It also has address lines A3…A0 used for internal selection of components as explained earlier in the pin descriptions.

4) Control Logic and Mode Set Register

It generates the internal control signals for the DMAC.
It also provides external signals such as HRQ (Hold), HLDA, AEN, ADSTB, TC, MARK etc. as explained earlier. If you are learning by Piracy, you are a THIEF!
Additionally, it has the Mode Set register.

Mode Set Register



Bit 0…3: Channel Enables

1: Enable the respective DMA channel
0: Disable

Bit 4: Rotating Priority

1: Rotating Priority
0: Fixed Priority

Bit 5: Extended Write

1: Extended Write
0: Normal Write

Extended Write Mode

Here the Write control signal gets activated one T-State in advance.
This is similar to the Advanced write signals of 8086 Maximum Mode.
Once the Write signal gets activated (goes low), the I/O device has to respond by Making Ready Signal=1 to indicate that it is ready for the transfer. A slow device

may require additional time to get ready and hence this will force the DMAC to insert Wait states in between every cycle, thus making the whole operation slow. To avoid this, we use the extended write mode.
Here, the Write signal goes low one T-state in advance hence the I/O gets a little extra time to become ready. This reduces the chances of inserting Wait states and hence prevents a slightly slow I/O device from making the whole DMA operation slow.

Bit 6: TC Stop

1: Enable TC Stop mode
0: Disable

TC Stop Mode

In this mode, the DMA operation stops once terminal count is reached.
The Respective DMA channel enable bit automatically becomes 0.

Bit 7: Auto load

1: Enable Auto Load Mode
0: Disable

Auto Load Mode

This is a continuous self-reloading mode.
It is applicable only for Channel 2.
When this mode is selected the original count and address register values of Channel 2 are stored as a back up in Channel 3 registers.
After every byte is transferred, Channel 2 registers keep changing but Channel 3 registers maintain the original values.
When Channel 2 reaches TC, There is an Automatic reload of address and count information from Channel 3 registers to Channel 2 registers and the DMA transfer restarts. This mode is basically used to perform repetitive DMA transfers.

5) Data Bus Buffer

It connects the external data bus of the system with the internal data bus of the DMAC, when the DMAC Chip is selected. If you are learning by Piracy, you are a THIEF!

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