→ Write an instruction sequence to set up the 3 counters of an 8253 located at I/O address 40H as follows:
Counter 0 - Binary ctr operating in mode 0 with an initial value of 1234H.
ctr 1 - BCD ctr operating in mode 2 with an initial value of 100H
ctr 2 - Binary ctr. operating in mode 4 with an initial count of 1FFFH.

```
MOV AL, 30H          ; set up ctr 0 mode 0
OUT 43H, AL

MOV AL, 55H          ; ctr. 1
OUT 43H, AL

MOV AL, B8H          ; ctr 2
OUT 43H, AL

MOV AL, 34H          ; Load ctr 0
OUT 40H, AL
MOV AL, 12H
OUT 40H, AL

MOV AL, 00H          ; Load ctr 1
OUT 41H, AL
MOV AL, 01H
OUT 41H, AL

MOV AL, FFH          ; Load ctr 2.
OUT 42H, AL
MOV AL, 1FH
OUT 42H, AL
```

8253 Examples

Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0040H for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 1.5 MHz respectively,

1. To generate a square wave of period 1 ms.
2. To interrupt the processor after 10 ms.
3. To derive a monoshot pulse with quasistable state duration 5 ms.

Solution: Neglecting the higher order address lines (A_{16}-A_8) the interfacing circuit diagram is shown in Fig. 1.10. The 8253 is interfaced with lower order data bus (D_0-D_7), hence A_0 is used for selecting the even bank. The A_0 and A_1 of the 8253 are connected with A_1 and A_2 of the processor. The counter addresses can be decoded as given below. If A_0 is 1, the 8253 will not be selected at all.

A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	0	0	0	= 40H Counter 0
					0	1	0	= 42H Counter 0
					1	0	0	= 44H Counter 0
					1	1	0	= 46H CWR

i. For generating a square wave. 8253 should be used in mode 3.
Let us select counter 0 for this purpose. that will be operated in BCD mode (may even be operated in HEX mode). Now suitable count is to be calculated for generating 1 ms time period.

f=1.5MHz.

$T=1/1.5X10^{-6}$ =0.66μs

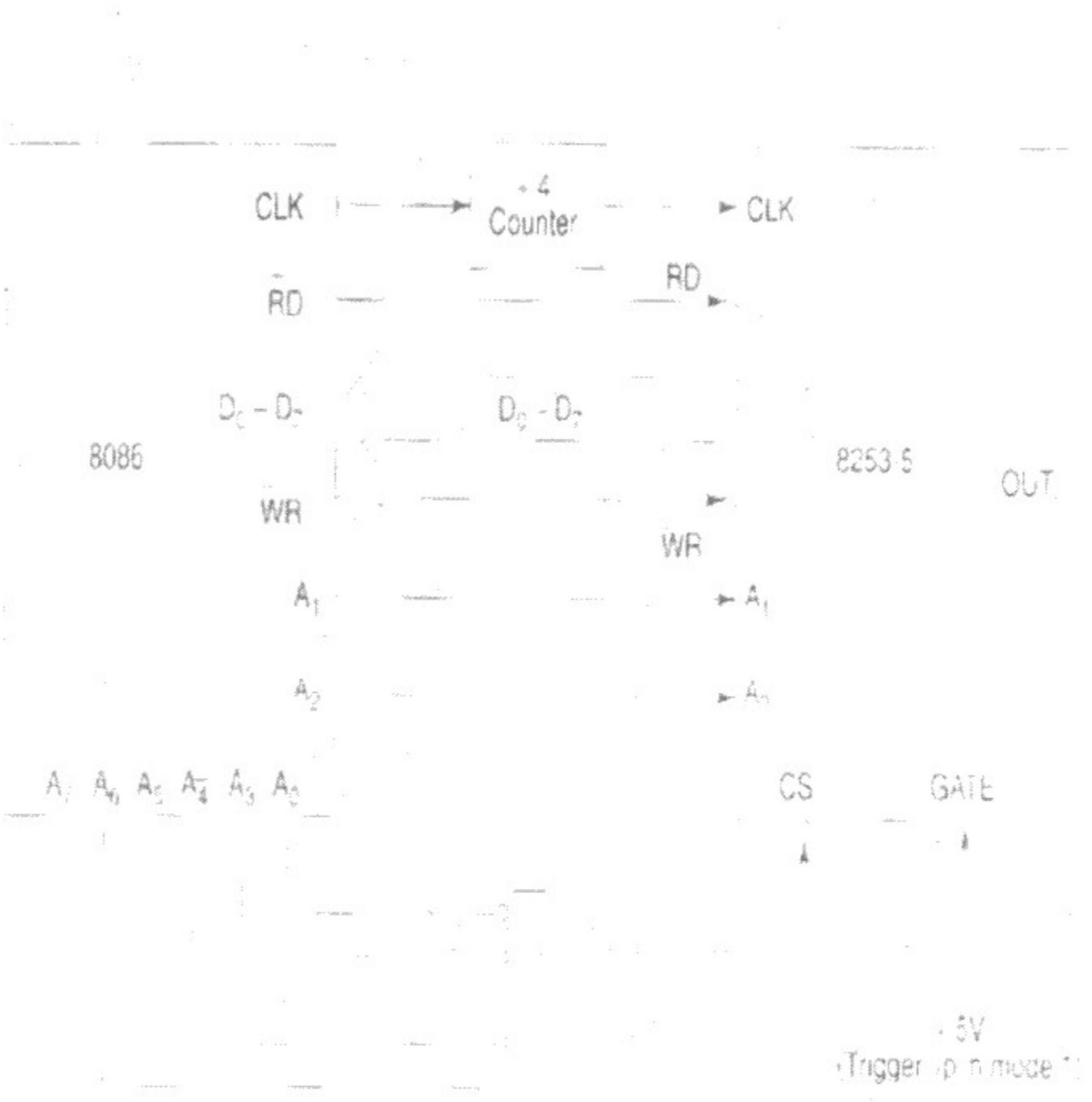
If N is the number of T states required for 1ms.

$N=1X10^{-3}/0.66x10^{-6}=1.5x10^{3}$

=1500 states

The control word is decided as below

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD	
0	0	1	1	0	1	1	1	=37H



MOV AL,37H
OUT 43H, AL
MOV AL, —
OUT 40H, AL
MOV AL, —
OUT 40H, AL

A

Fig1.10 Interfacing 8253 with 8086

Assembly language program

CODE SEGMENT

```
ASSUME CS:CODE
START:    MOV AL,70H      ;Initialise 8253 with
          OUT 46H,AL      ;Counter1 in mode0
          MOV AL,98H      ;Load 98H as LSB of count
          OUT 42H,AL      ;In count reg of counter1
          MOV AL,3AH      ;15 decimal in MSB as a
          OUT 42H,AL      ;of counter1
          MOV AH,4CH      ;Return to DOS
          INT 21H
CODE ENDS
END START
```

iii. For generating a 5ms quasistable state duration, the count required is calculated first. The counter 2 of 8253 is used in mode1, to count in binary. The OUT2 signal normally remains high after the count is loaded, till the trigger is applied. After the application of trigger signal, the output goes low in the next cycle, count down starts and whenever the count goes zero the output again goes high.Number of T states required for 05ms delay

$=5X10^{-3}/0.66x10^{-6}$

=7500 states

=1D4C H

The control word is decided as below

SC_1	SC_0	RL_1	RL_0	M_2	M_1	M_0	BCD	
								=B2H
1	0	1	1	0	0	1	0	

Assembly language program

```
CODE SEGMENT
ASSUME CS:CODE
START:      MOV AL,B2H        ;Initialise 8253 with
            OUT 46H,AL        ;Counter2 in mode1
            MOV AL,4CH        ;Load 4CH (LSB of count)
            OUT 44H,AL        ;Into count register
            MOV AL,1DH        ;Load1DH (MSB of count)
            OUT 44H,AL        ;Into count register
            MOV AH,4CH        ;Return to DOS
            INT 21H
CODE ENDS
END START
```