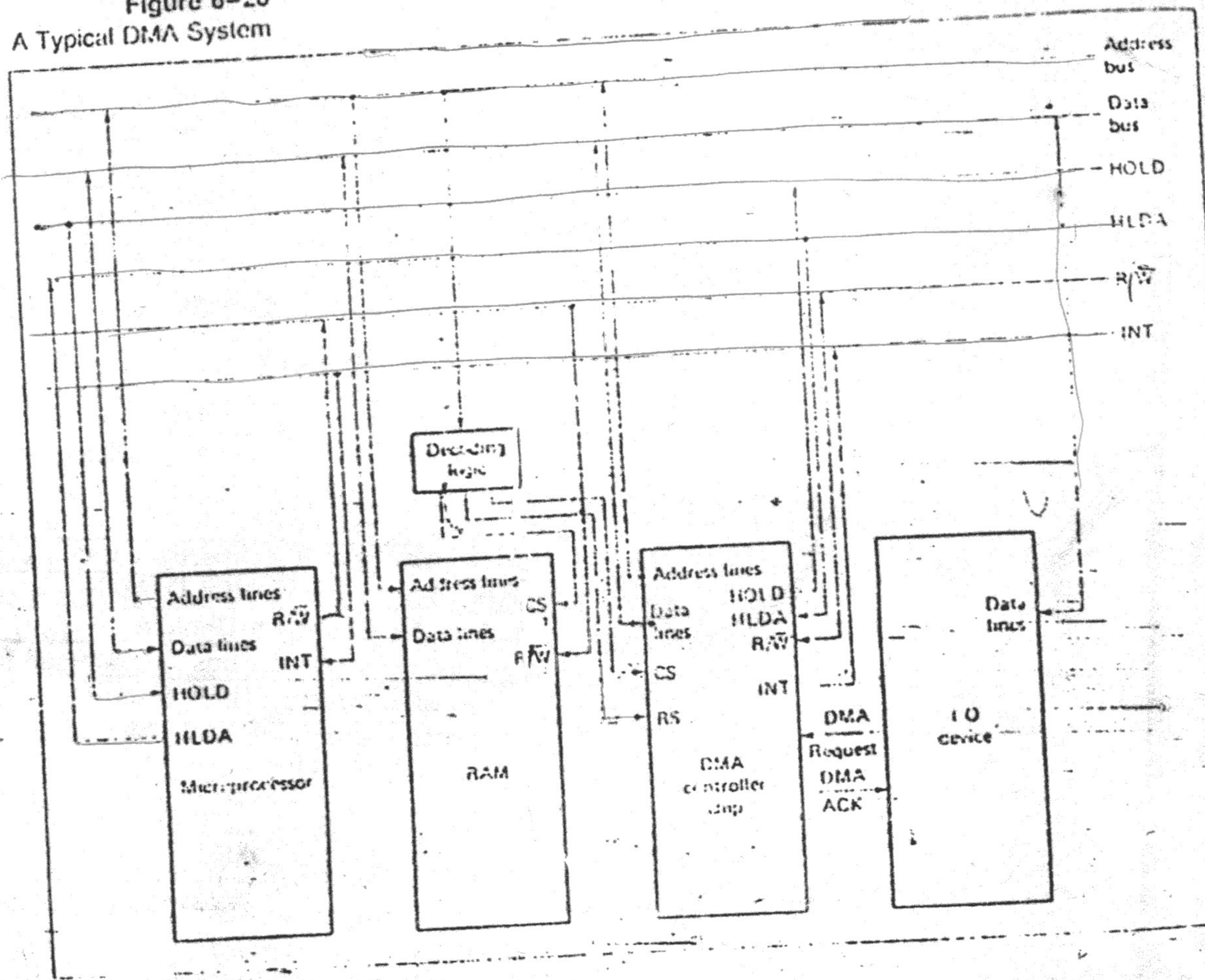


Mamta

## Chapter 6 Basic Input, Output and Interfacing

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Figure 6-20  
A Typical DMA System



### Cycle Stealing DMA

In this technique, the DMA controller transfers a byte of data between the memory and a peripheral device by stealing a clock cycle of the microprocessor. The DMA controller will complete the transfer by bypassing the microprocessor and generating proper signals to complete the transfer. Since the microprocessor is operated by an external clock, it is quite simple to stop the microprocessor momentarily. This is accomplished by not providing the clock signal to the microprocessor. An INHIBIT signal is used for this purpose. The INHIBIT is normally HIGH and is logically ANDed with the system clock to generate the microprocessor clock, as shown in Figure 6-21.

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## 11-1 BASIC DMA OPERATION

Two control signals are used to request and acknowledge a direct memory access (DMA) transfer in the microprocessor-based system. The HOLD pin is an input used to request a DMA action and the HLDA pin is an output that acknowledges the DMA action. Figure 11-1 shows the timing that is typically found on these two DMA control pins.

Whenever the HOLD input is placed at a logic 1 level, a DMA action (hold) is requested. The microprocessor responds, within a few clocks, by suspending the execution of the program and by placing its address, data, and control bus at their high-impedance states. The high-impedance state causes the microprocessor to appear as if it has been removed from its socket. This state allows external I/O devices or other microprocessors to gain access to the system buses so memory can be accessed directly.

As the timing diagram indicates, HOLD is sampled in the middle of any clocking cycle. Thus, the hold can take effect at any time during the operation of any instruction in the microprocessor. As soon as the microprocessor recognizes the hold, it stops executing software and enters hold cycles. Note that the HOLD input has a higher priority than the INTR or NMI interrupt inputs. Interrupts take effect at the end of an instruction, while a HOLD takes effect in the middle of an instruction. The only microprocessor pin that has a higher priority than a HOLD is the RESET pin. Note that the HOLD input may not be active during a RESET or the reset is not guaranteed.

The HLDA signal becomes active to indicate that the microprocessor has indeed placed its buses at their high-impedance state as can be seen in the timing diagram. Note that there are a few clock cycles between the time that HOLD changes until the time that HLDA changes. The HLDA output is a signal to the external requesting device that the microprocessor has relinquished control of its memory and I/O space. You could call the HOLD input a DMA request input and the HLDA output a DMA grant signal.

### Basic DMA Definitions

Direct memory accesses normally occur between an I/O device and memory without the use of the microprocessor. A DMA read transfers data from the memory to the I/O device. A DMA write transfers data from an I/O device to memory. In both operations, the memory and I/O are controlled simultaneously and that is why the system contains

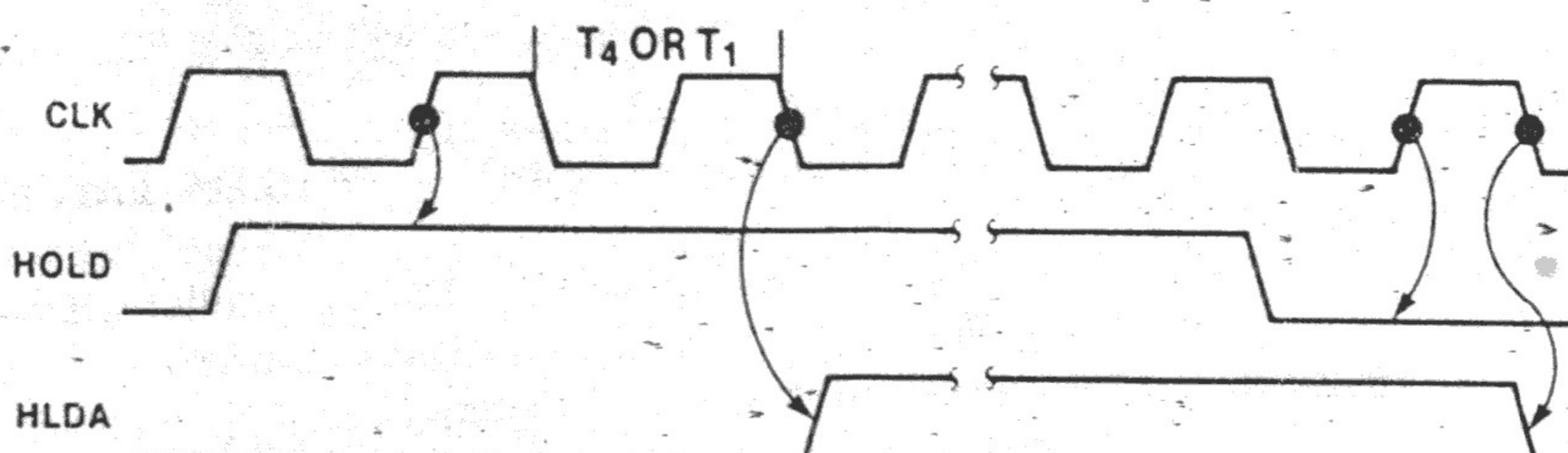


FIGURE 11-1 HOLD and HLDA timing for the 8086/8088 microprocessor.

Figure 11-3 shows the pinout and block diagram of the 8237 programmable DMA controller. Although this device may not appear as a discrete component in modern microprocessor-based systems, it does appear within system controller chip sets found in most newer systems. Although not described because of its complexity, the chip set (82357 ISP or integrated peripheral controller) and its integral set of two DMA controllers are programmed exactly as the 8237. The ISP also provides a pair of 8259A programmable interrupt controllers for the system.

The 8237 is a four-channel device that is compatible to the 8086/8088 microprocessor. The 8237 can be expanded to include any number of DMA channel inputs, although four channels seem to be adequate for many small systems. The 8237 is capable of DMA transfers at rates of up to 1.6M bytes per second. Each channel is capable of addressing a full 64K byte section of memory and can transfer up to 64K bytes with a single programming.

#### Pin Definitions

- ✓ 1. CLK (clock) is connected to the system clock signal as long as that signal is 5 MHz or less. In the 8086/8088 system, the clock must be inverted for the proper operation of the 8237.
- ✓ 2. CS (chip select) selects the 8237 during programming. The CS pin is normally connected to the output of a decoder. The decoder does not use the 8086/8088 control signal IO/M (M/IO) because it contains the new memory and I/O control signals (MEMR, MEMW, IOR, and IOW).
- ✓ 3. RESET (reset) clears the command, status, request, and temporary registers. It also clears the first/last flip-flop and sets the mask register. This input primes the 8237 so it is disabled until programmed otherwise.

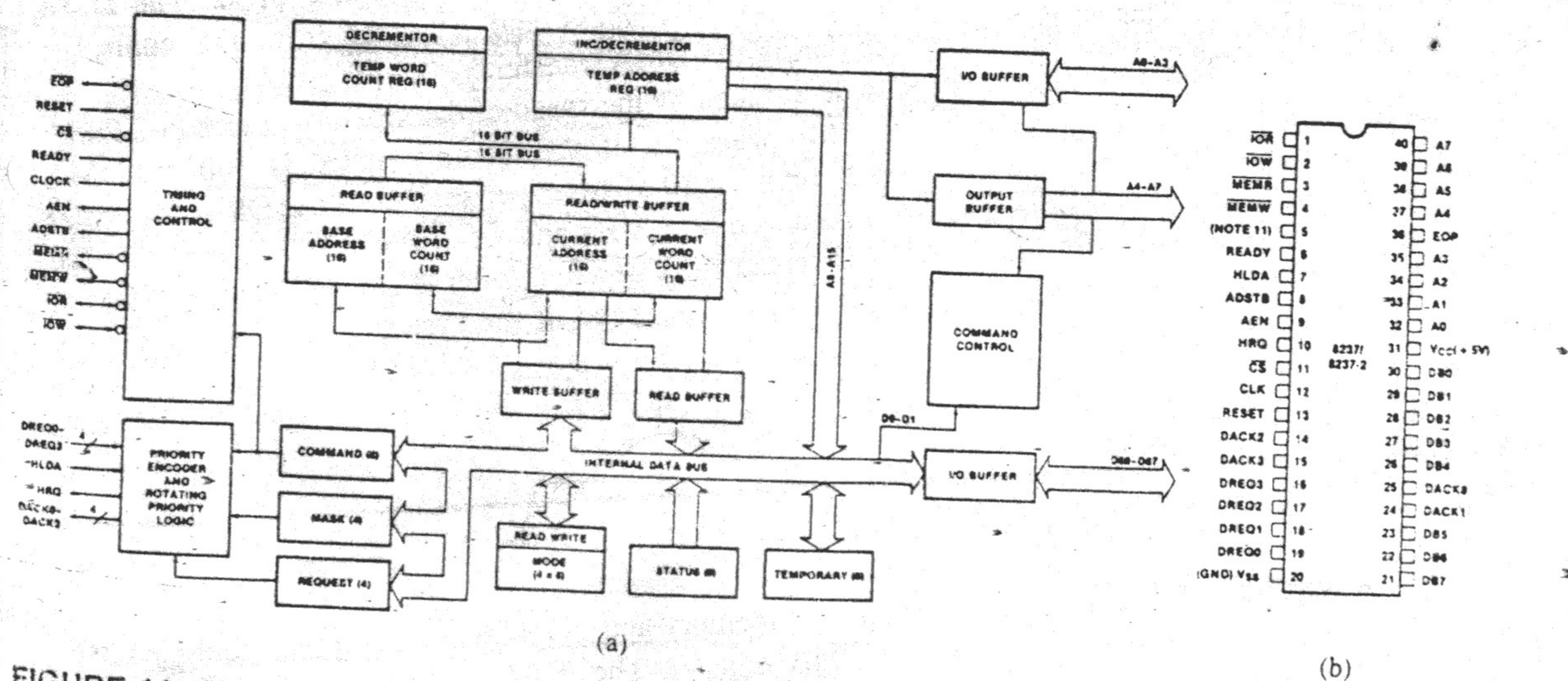


FIGURE 11-3 The 8237A-5 programmable DMA controller. (a) Block diagram, and (b) pinout. (Courtesy of Intel Corporation)

4. READY (ready) causes the 8237 to enter wait states for slower memory and/or I/O components.
5. HLDA (hold acknowledge) signals the 8237 that the microprocessor has relinquished control of the address, data, and control buses.
6. DREQ<sub>3</sub>-DREQ<sub>0</sub> (DMA request) inputs are used to request a DMA transfer for each of the four DMA channels. Because the polarity of these inputs is programmable, they are either active-high or active-low inputs.
7. DB<sub>7</sub>-DB<sub>0</sub> (data bus) pins are connected to the microprocessor data bus connections and are used during the programming of the DMA controller.
8. IOR (I/O read) is a bidirectional pin used during programming and during a DMA write cycle.
9. IOW (I/O write) is a bidirectional pin used during programming and during a DMA read cycle.
10. EOP (end-of-process) is a bidirectional signal that is used as an input to terminate a DMA process or as an output to signal the end of the DMA transfer. This input is often used to interrupt a DMA transfer at the end of a DMA cycle.
- X 11. A<sub>3</sub>-A<sub>0</sub> (address) are pins that are used to select an internal register during programming and also provide part of the DMA transfer address during a DMA action.
12. A<sub>7</sub>-A<sub>4</sub> (address) are outputs that provide part of the DMA transfer address during a DMA action.
13. HRQ (hold request) is an output that connects to the HOLD input of the microprocessor in order to request a DMA transfer.
14. DACK<sub>3</sub>-DACK<sub>0</sub> (DMA channel acknowledge) are outputs that acknowledge a channel DMA request. These outputs are programmable as either active-high or active-low signals. The DACK outputs are often used to select the DMA controlled I/O device during the DMA transfer.
15. AEN (address enable) enables the DMA address latch connected to the DB<sub>7</sub>-DB<sub>0</sub> pins on the 8237. It is also used to disable any buffers in the system connected to the microprocessor.
16. ADSTB (address strobe) functions as ALE, except that it is used by the DMA controller to latch address bits A<sub>15</sub>-A<sub>8</sub> during the DMA transfer.
17. MEMR (memory read) is an output that causes memory to read data during a DMA read cycle.
18. MEMW (memory write) is an output that causes memory to write data during a DMA write cycle.

#### *Internal Registers*

- X 1. *Current address register (CAR)* is used to hold the 16-bit memory address used for the DMA transfer. Each channel has its own current address register for this purpose. When a byte of data is transferred during a DMA operation, the CAR is either incremented or decremented, depending on how it is programmed.
- X 2. *Current word count register (CWCR)* programs a channel for the number of bytes (up to 64K) transferred during a DMA action. The number loaded into this register is one less than the number of bytes transferred. For example; if a 10 is loaded into the CWCR, then 11 bytes are transferred during the DMA action.