



Programmable Interrupt Controller

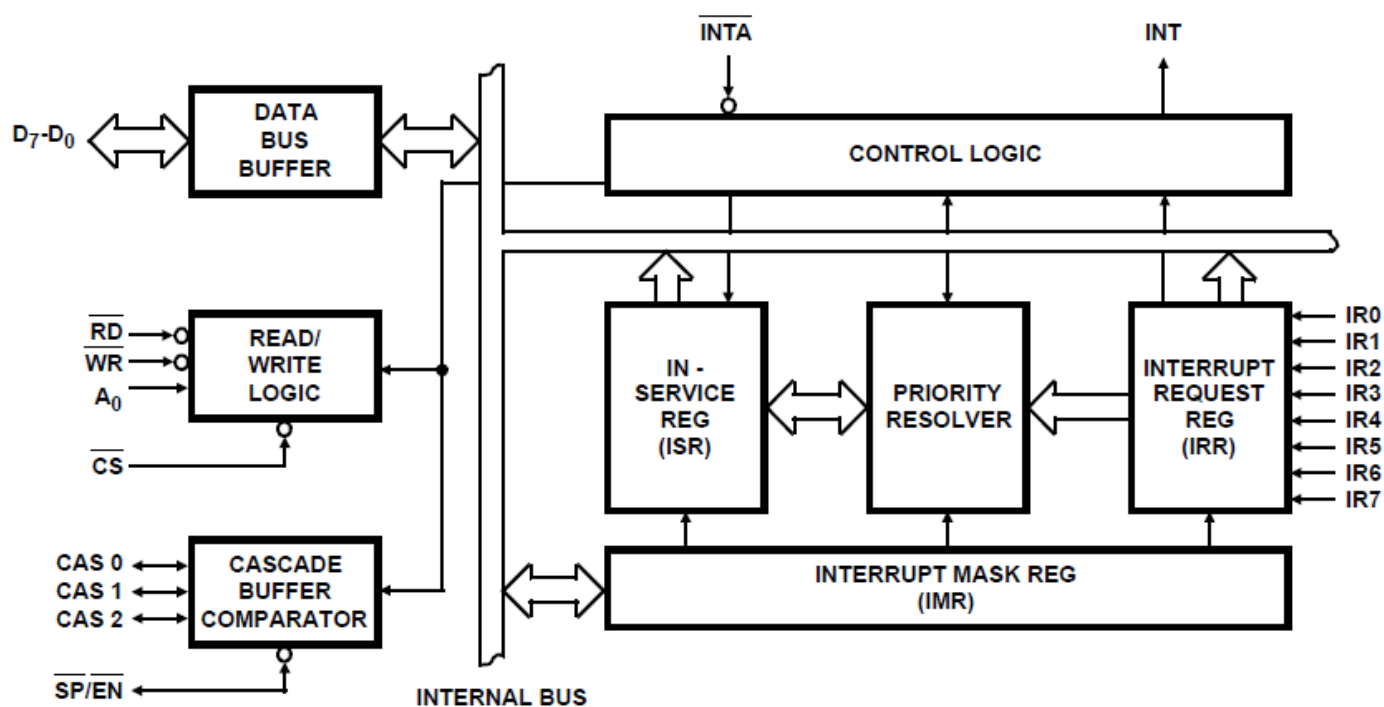
8259 | PIC

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Salient Features

- 1) PIC 8259 is a Programmable Interrupt Controller that can work with 8085, 8086 etc.
- 2) **It is used to increase the number of interrupts.**
- 3) A single 8259 provides 8 interrupts while a cascaded configuration of 1 master 8259 and 8 slave 8259s can provide up to 64 interrupts.
- 4) 8259 can handle **edge as well as level triggered** interrupts.
- 5) 8259 has a **flexible priority** structure. © For doubts contact Bharat Sir on 98204 08217
- 6) In 8259 interrupts can be **masked** individually.
- 7) The **Vector address** of the interrupts is **programmable**.
- 8) 8259 has to be **compulsorily initialized** by giving commands, to decide several properties such as Vector Numbers, Priority, Masking, Triggering etc.
- 9) In a **cascaded configuration**, each 8259 has to be **individually initialized**, master as well as each slave.

ARCHITECTURE OF 8259





1) Interrupt Request Register (IRR)

8259 has **8 interrupt** input lines **IR₇ ... IR₀**.

The IRR is an **8-bit register** having **one bit** for **each** of the **interrupt** lines.

When an **interrupt request** occurs on any of these lines, the **corresponding bit** is **set** in the Interrupt Request Register (**IRR**).

2) In-Service Register (InSR)

It is an **8-bit** register, which **stores** the **level** of the Interrupt Request, which is **currently** being **served**.

3) Interrupt Mask Register (IMR)

It is an **8-bit** register, which stores the **masking pattern** for the interrupts of 8259. It stores **one bit per interrupt level**.

4) Priority Resolver

It **examines** the **IRR**, **InSR**, and **IMR** and determines which interrupt is of **highest priority** and should be sent to the μ P.

5) Control Logic

It has **INT output** connected to the **INTR** of the μ P, to **send** the **Interrupt** to μ P.

It also has the **INTA input** signal connected to the **INTA** of the μ P, to **receive** the interrupt **acknowledge**. It is also used to control the remaining blocks.

6) Data Bus Buffer

It is a bi-directional buffer used to **interface** the internal **data bus** of 8259 with the external (system) data bus.

7) Read/Write Logic

It is used to accept the **RD** , **WR** , A₀ and CS signal.

It also holds the Initialization Command Words (ICW's) and the Operational Command Words (OCW's).

8) Cascade Buffer / Comparator

It is used in **cascaded mode** of operation.

It has two components:

i. **CAS₂, CAS₁, CAS₀ lines:**

These lines are **output for the master, input for the slave**.

The **Master sends** the **address of the slave** on these lines (hence output).

The **Slaves read** the **address** on these lines (hence input).

As there are 8 interrupt levels for the Master, there are **3 CAS lines** (**2³ = 8**).

ii. **SP / EN** (Slave Program/Master Enable): ¶For doubts contact Bharat Sir on 98204 08217

In **Buffered Mode**, it **functions** as the **EN line** and is used to **enable** the **buffer**.

In **Non buffered mode**, it **functions** as the **SP output line**.

For Master 8259 **SP** should be **high**, and **for the Slave SP** should be **low**.



INTERFACING AND WORKING OF A "SINGLE" 8259

A single 8259 can accept 8 interrupts.

Whenever a device interrupts 8259, 8259 will interrupt the μP on **INTR pin**.

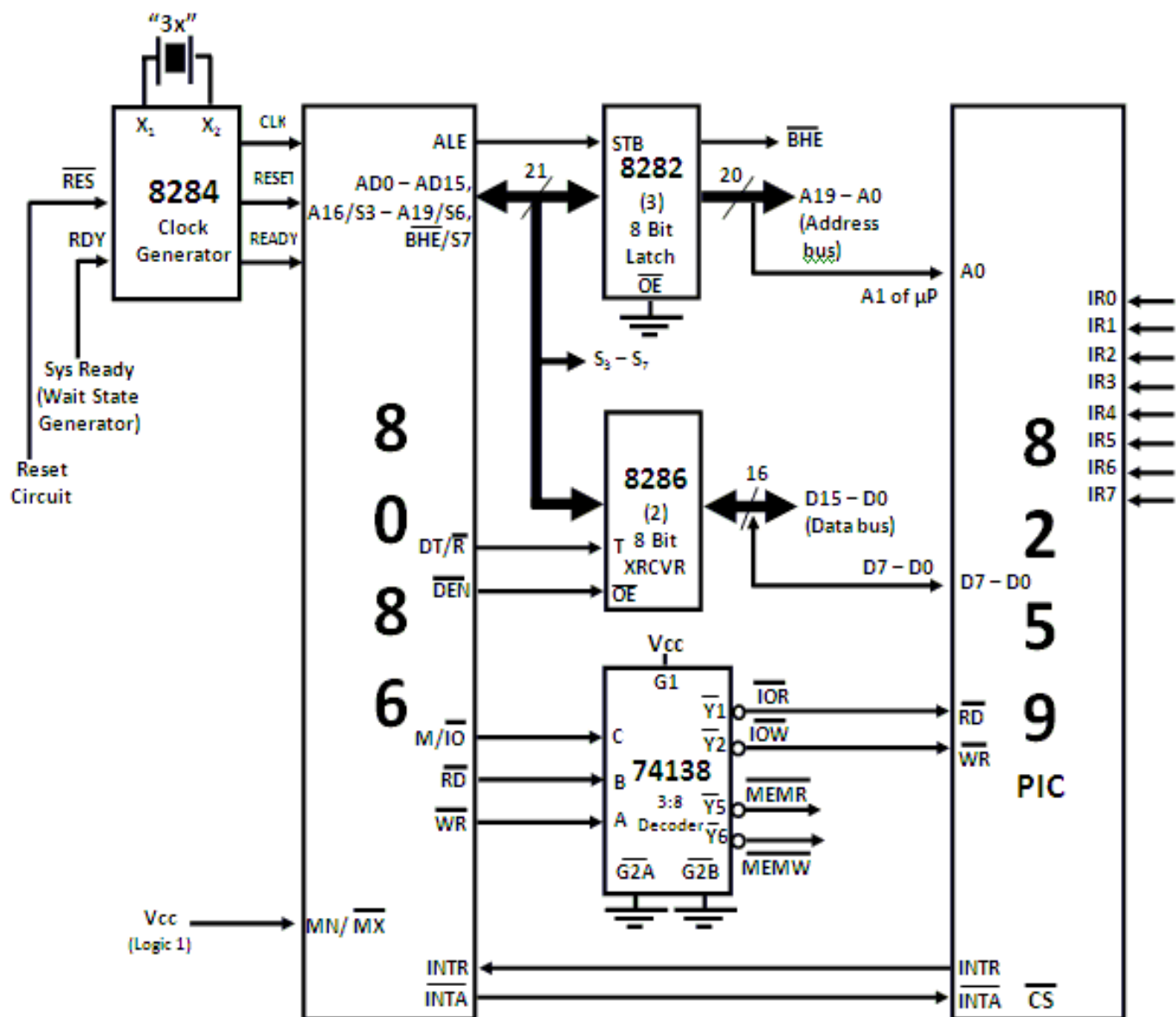
Hence, first the **INTR** signal of the μP **should be enabled** using the **STI** instruction.

8259 is initialized by giving **ICW1** and **ICW2** (compulsory) and **ICW4** (optional).

Note that **ICW3 is not given** as Single 8259 is used. OCWs are given if required.

Once 8259 is initialized, the **following sequence** of events takes place when one or more **interrupts occur** on the IR lines of the 8259.

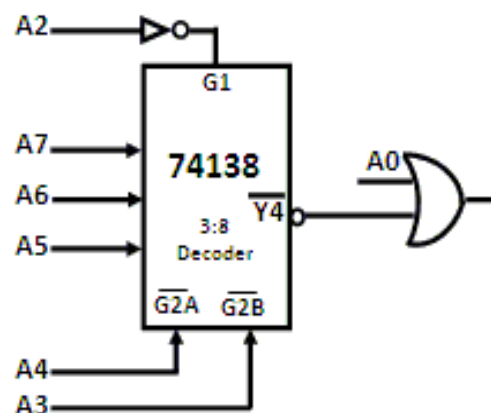
- 1) The **corresponding bit** for an interrupt is **set in IRR**.
- 2) The **Priority Resolver checks** the 3 registers:
IRR (for highest interrupt request)
IMR (for the masking Status)
InSR (for the current level serviced)
and **determines** the **highest priority** interrupt.
It **sends** the **INT** signal to the μP .
- 3) The μP **finishes** the **current instruction** and **acknowledges** the interrupt by **sending** the **first INTA pulse**.
- 4) On receiving the first **INTA** signal, the **corresponding bit** in the **InSR** is **set** (indicating that now this interrupt is in service) and the **bit** in the **IRR** is **reset** (to indicate that the request is accepted).
For doubts contact Bharat Sir on 98204 08217
8259 now prepares to send the Vector number **N** to the μP on the data bus.
- 5) The μP **sends the second INTA pulse** to 8259.
- 6) In response to the 2nd **INTA** pulse, **8259 sends the one byte Vector Number N** to μP .
- 7) Now the μP **multiplies N x 4**, to get the values of CS and IP **from the IVT**.
- 8) **In the AEOI Mode** the **InSR bit is reset** at this point, **otherwise it remains set until an appropriate EOI** command is given at the End of the ISR.
- 9) The μP **pushes** the contents of **Flag Register, CS, IP**, into the **Stack, Clears IF and TF** and **transfers program to the address** of the **ISR**.. *#Please refer Bharat Sir's Lecture Notes for this ...*
- 10) **The ISR thus begins.**



I/O Map of 8259 at 80H

| | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | |
|------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----|
| ICW1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80H |
| ICW2 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82H |

Chip Selection: A₇ to A₂
Internal Selection: A₁ to A₀
Bank Selection: A₇ to A₄





Interfacing and Working of “CASCADED” 8259

When **more than one 8259s** are connected to the μP , it is called as a **Cascaded configuration**. A Cascaded configuration **increases** the **number of interrupts** handled by the system. As the **maximum** number of **8259s** interfaced can be **9** (1 Master and 8 Slaves) the **Maximum** number of **interrupts** handled can be **64**.

The **master 8259** has $\overline{SP} / \overline{EN} = +5V$ and the **slave** has $\overline{SP} / \overline{EN} = 0V$.

Each slave's INT output is **connected** to the **IR input** of the **Master**.

The **INT** output of the **Master** is **connected** to the **INTR** input of the μP .

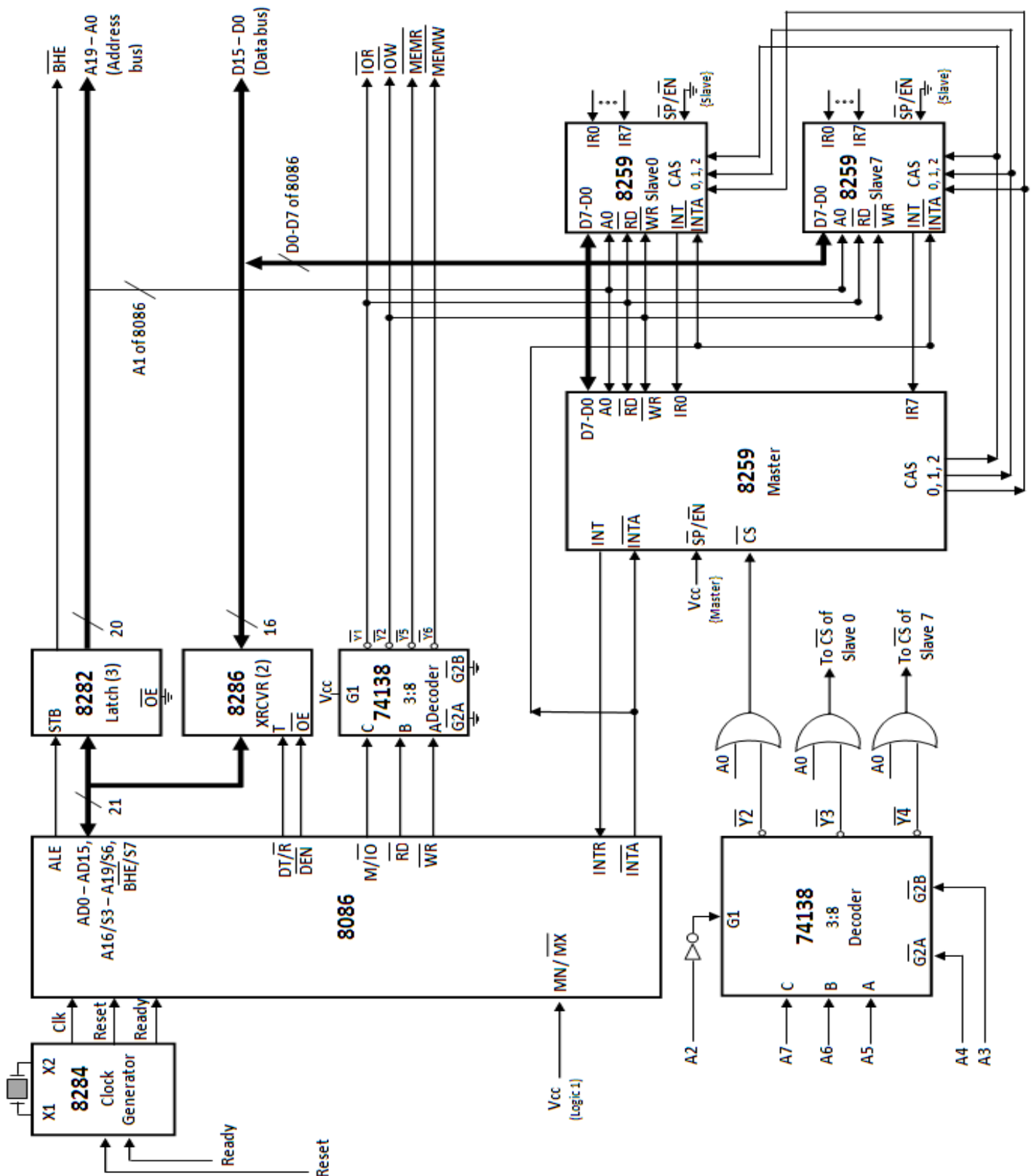
The **master addresses** the individual **slaves** through the **CAS₂, CAS₁, CAS₀** lines connected from the master to each of the slaves.

First the **INTR** signal of the μP **should be enabled** using the **STI** instruction.

Each 8259 (Master or Slave) **has its own address** and **has to be initialized separately** by giving ICWs as per requirement.

When an **interrupt request** occurs on a **SLAVE**, the events are performed:

- 1) The **slave 8259 resolves** the **priority** of the interrupt and **sends** the **interrupt** to the **master 8259**.
- 2) The **master resolves** the **priority** among its slaves and **sends** the **interrupt** to the μP .
- 3) The μP **finishes the current instruction** and **responds** to the interrupt **by sending 2 \overline{INTA} pulses**.
- 4) **In response to the first \overline{INTA} pulse** the **following events occur**:
 - i. The master **sends** the **3-bit slave identification number** on the **CAS** lines.
 - ii. The **Master sets** the **corresponding bit** in its **InSR**.
 - iii. The **Slave identifies** its number on the **CAS** lines and **sets** the **corresponding bit** in its **InSR**.
- 5) In **response to the second \overline{INTA} pulse** the **slave** places **Vector Number N** on the data bus.
- 6) **During the 2nd \overline{INTA} pulse** the **InSR bit** of the **slave** is **cleared** in **AEOI mode**, **otherwise** it is **cleared** by the **EOI command** at the end of the ISR.
- 7) The μP **pushes** the contents of **Flag Register, CS, IP**, into the **Stack, Clears IF and TF** and **transfers program** to the **address** of the **ISR**.. *#Please refer Bharat Sir's Lecture Notes for this ...*
- 8) **The ISR thus begins**.





| I/O map | | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | I/O |
|-----------------|------|----|----|----|----|----|----|----|----|-----|
| 8259 Master | ICW1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 |
| | ICW2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 |
| 8259 Slave 0 | ICW1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 60 |
| | ICW2 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 62 |
| 8259 Slave 7 | ICW1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 |
| | ICW2 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 82 |