

- write instructions to transfer data under status check I/O and interrupt I/O.
- List operating modes of the 8254 timer and write instructions to set up the timer in the various modes.

- Explain the functions of the 8259A interrupt controller and its operation in the fully nested mode.
- Explain the process of the Direct Memory Access (DMA) and the functions of various elements of the 8237.

## 15.1

### THE 8255A PROGRAMMABLE PERIPHERAL INTERFACE

The 8255A is a widely used, programmable, parallel I/O device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile, and economical (when multiple I/O ports are required), but somewhat complex. It is an important general-purpose I/O device that can be used with almost any microprocessor.

The 8255A has 24 I/O pins that can be grouped primarily in two 8-bit parallel ports: A and B, with the remaining eight bits as port C. The eight bits of port C can be used as individual bits or be grouped in two 4-bit ports:  $C_U$  (C<sub>U</sub>) and  $C_L$  (C<sub>L</sub>), as in Figure 15.1(a). The functions of these ports are defined by writing a control word in the control register.

Figure 15.1(b) shows all the functions of the 8255A, classified according to two modes: the Bit Set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into three modes: Mode 0, Mode 1, and Mode 2. In Mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby ports A and/or B use bits from port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt. In Mode 2, port A can be set up for bidirectional data transfer using handshake signals from port C, and port B can be set up either in Mode 0 or Mode 1.

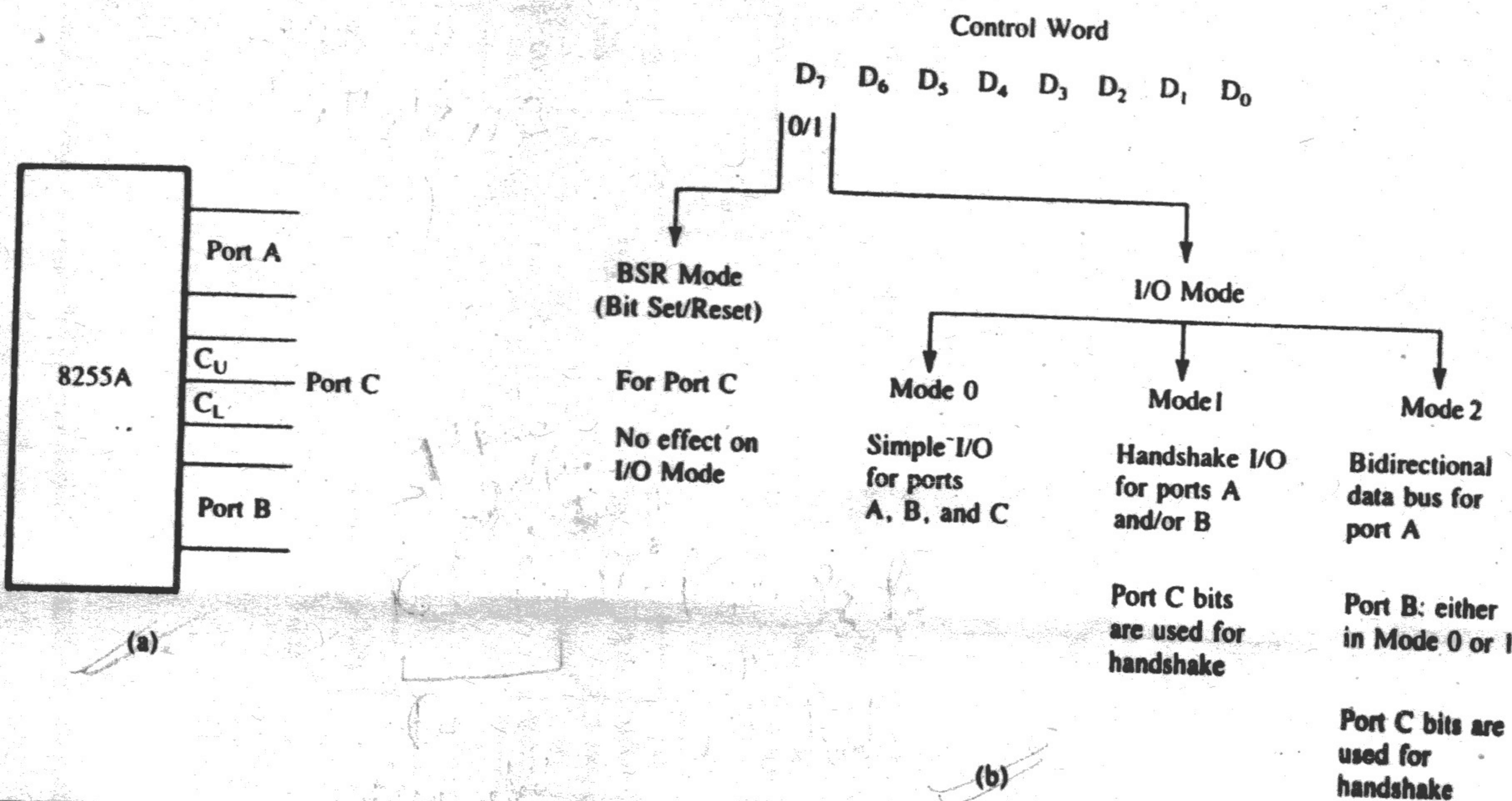
#### 15.11 Block Diagram of the 8255A

The block diagram in Figure 15.2(a) shows two 8-bit ports (A and B), two 4-bit ports ( $C_U$  and  $C_L$ ), the data bus buffer, and control logic. Figure 15.2(b) shows a simplified but expanded version of the internal structure, including a control register. This block diagram includes all the elements of a programmable device; port C performs functions similar to that of the status register in addition to providing handshake signals.

#### CONTROL LOGIC

The control section has six lines. Their functions and connections are as follows:

- RD (Read):** This control signal enables the Read operation. When the signal is low, the MPU reads data from a selected I/O port of the 8255A.
- WR (Write):** This control signal enables the Write operation. When the signal goes low, the MPU writes into a selected I/O port or the control register.



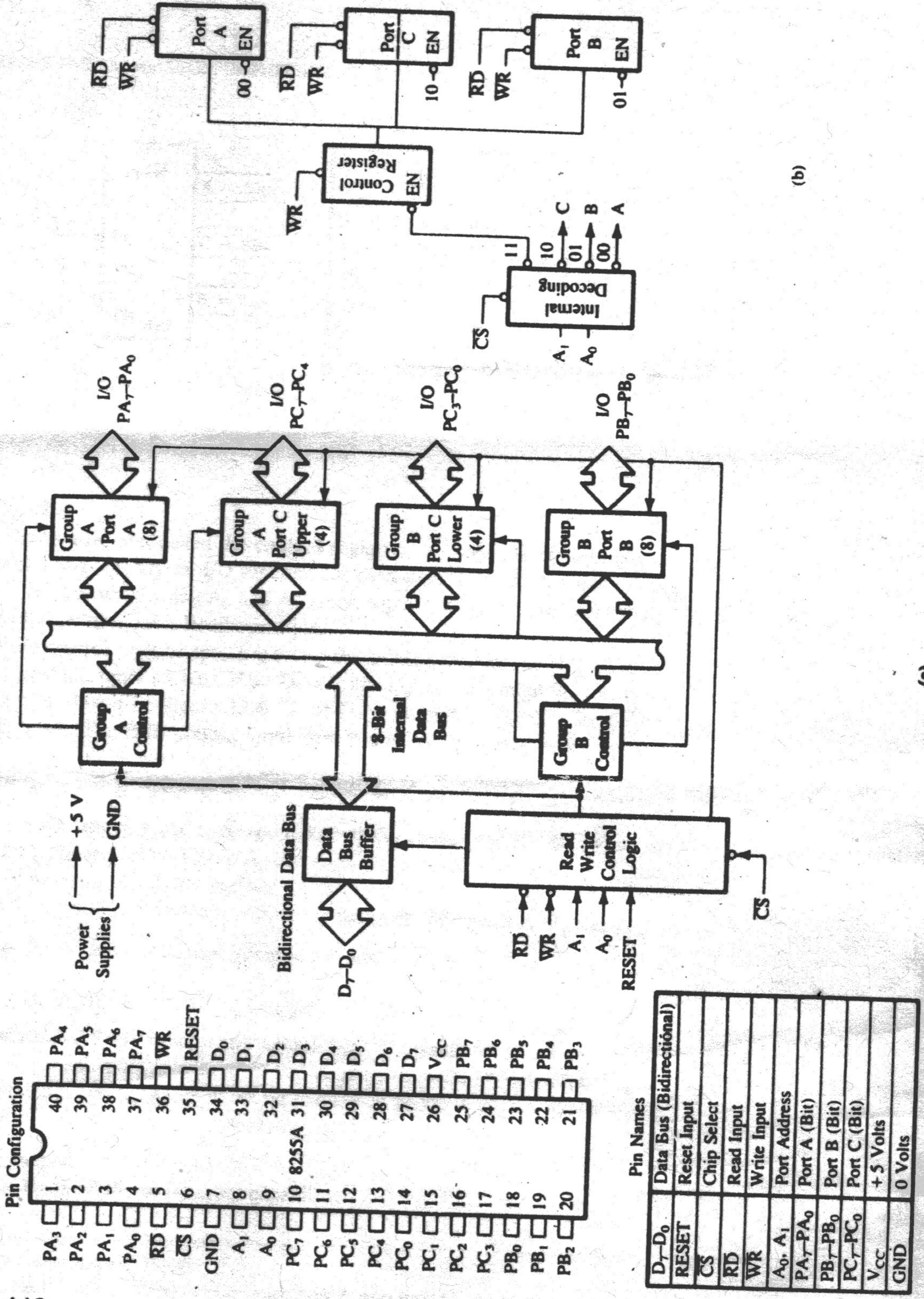
**FIGURE 15.1**  
8255A I/O Ports (a) and Their Modes (b)

- **RESET (Reset):** This is an active high signal; it clears the control register and sets all ports in the input mode.
- **CS, A<sub>0</sub>, and A<sub>1</sub>:** These are device select signals. CS is connected to a decoded address, and A<sub>0</sub> and A<sub>1</sub> are generally connected to MPU address lines A<sub>0</sub> and A<sub>1</sub>, respectively.

The CS signal is the master Chip Select, and A<sub>0</sub> and A<sub>1</sub> specify one of the I/O ports or the control register as given below:

CS	A <sub>1</sub>	A <sub>0</sub>	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255A is not selected.

As an example, the port addresses in Figure 15.3(a) are determined by the CS, A<sub>0</sub>, and A<sub>1</sub> lines. The CS line goes low when A<sub>7</sub> = 1 and A<sub>6</sub> through A<sub>2</sub> are at logic 0. When these signals are combined with A<sub>0</sub> and A<sub>1</sub>, the port addresses range from 80H to 83H, as shown in Figure 15.3(b).



**FIGURE 15.2**  
8255A Block Diagram (a) and an Expanded Version of the Control Logic and I/O Ports (b)  
SOURCE: A: Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-100.

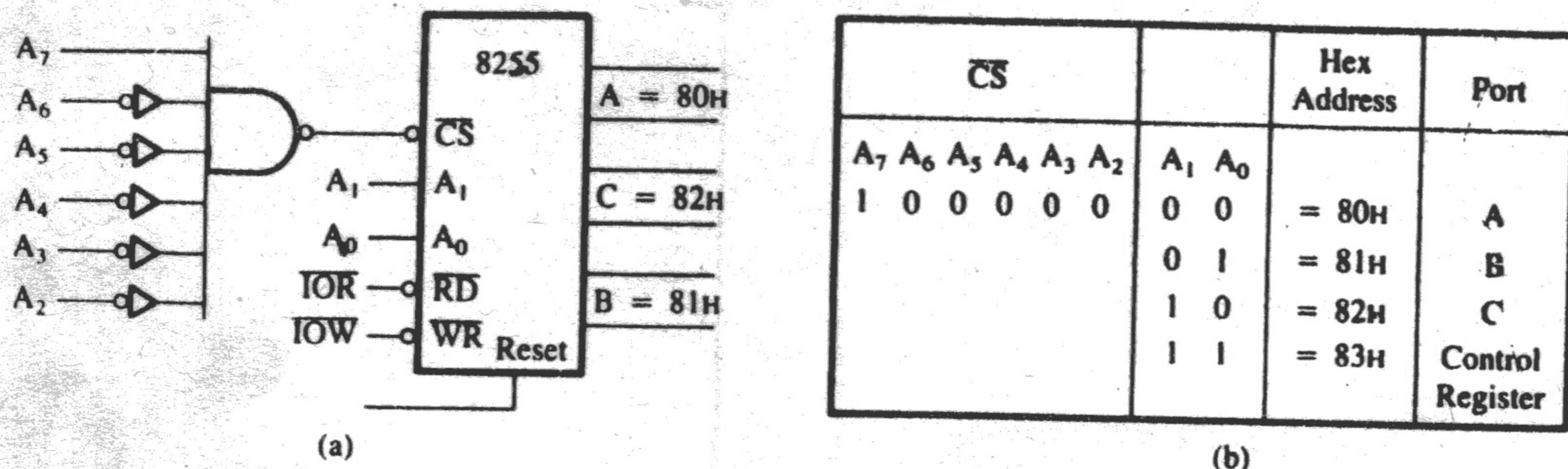


FIGURE 15.3  
8255A Chip Select Logic (a) and I/O Port Addresses (b)

### CONTROL WORD

Figure 15.2(b) shows a register called the **control register**. The contents of this register, called the **control word**, specify an I/O function for each port. This register can be accessed to write a control word when A<sub>0</sub> and A<sub>1</sub> are at logic 1, as mentioned previously. The register is not accessible for a Read operation.

Bit D<sub>7</sub> of the control register specifies either the I/O function or the Bit Set/Reset function, as classified in Figure 15.1(b). If bit D<sub>7</sub> = 1, bits D<sub>6</sub>-D<sub>0</sub> determine I/O functions in various modes, as shown in Figure 15.4. If bit D<sub>7</sub> = 0, port C operates in the Bit Set/Reset (BSR) mode. The BSR control word does not affect the functions of ports A and B (the BSR mode will be described later).

To communicate with peripherals through the 8255A, three steps are necessary:

1. Determine the addresses of ports A, B, and C and of the control register according to the Chip Select logic and address lines A<sub>0</sub> and A<sub>1</sub>.
2. Write a control word in the control register.
3. Write I/O instructions to communicate with peripherals through ports A, B, and C.

Examples of the various modes are given in the next section.

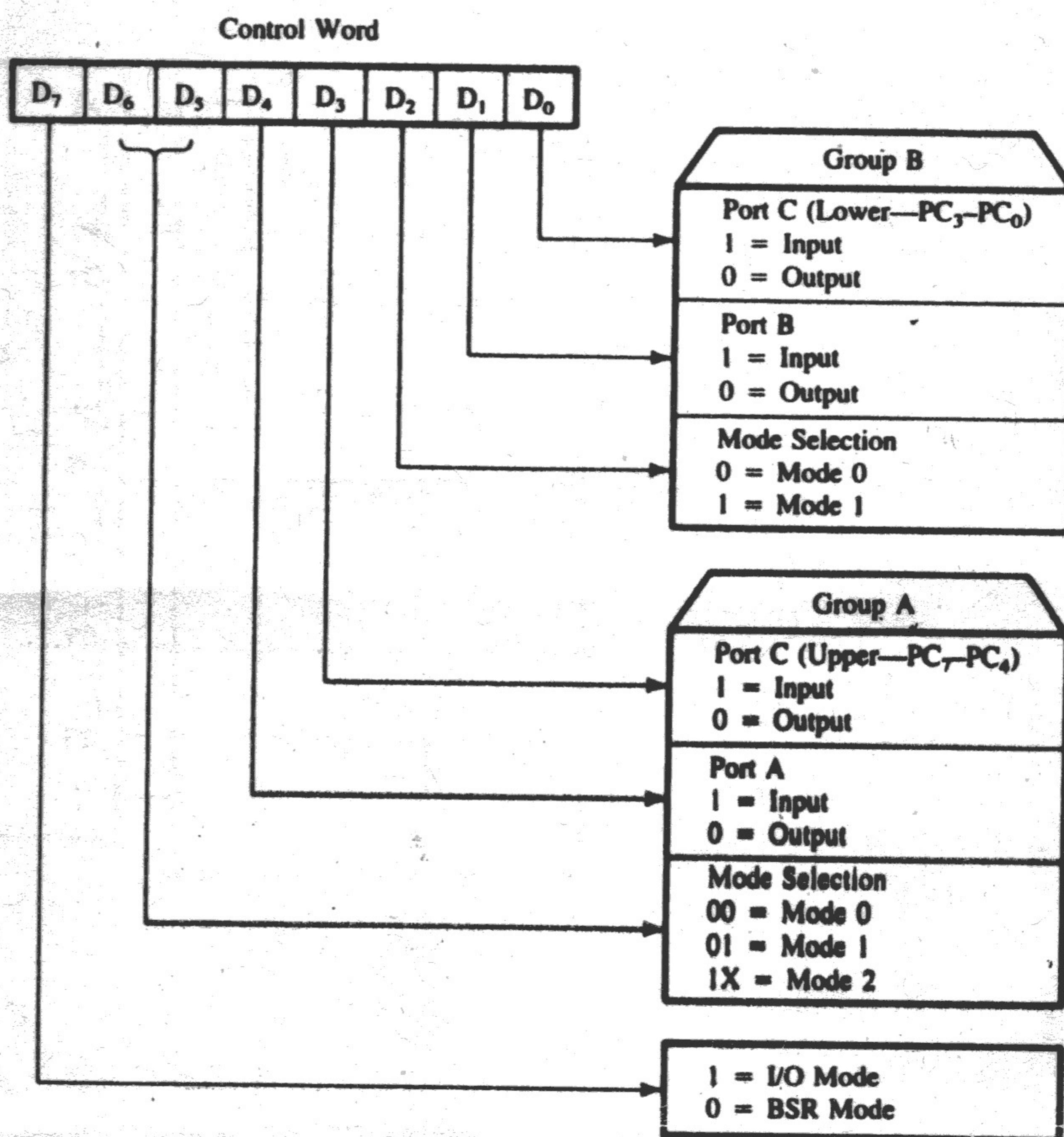
### 15.12 Mode 0: Simple Input or Output

In this mode, ports A and B are used as two simple 8-bit I/O ports and port C as two 4-bit ports. Each port (or half-port, in case of C) can be programmed to function as simply an input port or an output port. The input/output features in Mode 0 are as follows:

1. Outputs are latched.
2. Inputs are not latched.
3. Ports do not have handshake or interrupt capability.

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1. Identify the port addresses in Figure 15.5.
  2. Identify the Mode 0 control word to configure port A and port C<sub>U</sub> as output ports and port B and port C<sub>L</sub> as input ports.

Example  
15.1



**FIGURE 15.4**  
8255A Control Word Format for I/O Mode

SOURCE: Adapted from Intel Corporation, *Peripheral Components* (Santa Clara, Calif.: Author, 1993), p. 3-104.

3. Write a program to read the DIP switches and display the reading from port B at port A and from port C<sub>L</sub> at port C<sub>U</sub>.

#### Solution

1. **Port Addresses** This is a memory-mapped I/O; when the address line A<sub>15</sub> is high, the Chip Select line is enabled. Assuming all don't care lines are at logic 0, the port addresses are as follows:

Port A	=	8000H (A <sub>1</sub> = 0, A <sub>0</sub> = 0)
Port B	=	8001H (A <sub>1</sub> = 0, A <sub>0</sub> = 1)
Port C	=	8002H (A <sub>1</sub> = 1, A <sub>0</sub> = 0)
Control Register	=	8003H (A <sub>1</sub> = 1, A <sub>0</sub> = 1)

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RLC
RLC
STA 8002H ;Display data at port CU
HLT

```

**Program Description** The circuit is designed for memory-mapped I/O; therefore, the instructions are written as if all the 8255A ports are memory locations.

The ports are initialized by placing the control word 83H in the control register. The instructions STA and LDA are equivalent to the instructions OUT and IN, respectively.

In this example, the low four bits of port C are configured as input and the high four bits are configured as output; even though port C has one address for both halves C<sub>U</sub> and C<sub>L</sub> (8002H), Read and Write operations are differentiated by the control signals MEMR and MEMW. When the MPU reads port C (e.g., LDA 8002H), it receives eight bits in the accumulator. However, the high-order bits (D<sub>7</sub>-D<sub>4</sub>) must be ignored because the input data bits are in PC<sub>3</sub>-PC<sub>0</sub>. To display these bits at the upper half of port C, bits (PC<sub>3</sub>-PC<sub>0</sub>) must be shifted to PC<sub>7</sub>-PC<sub>4</sub>.

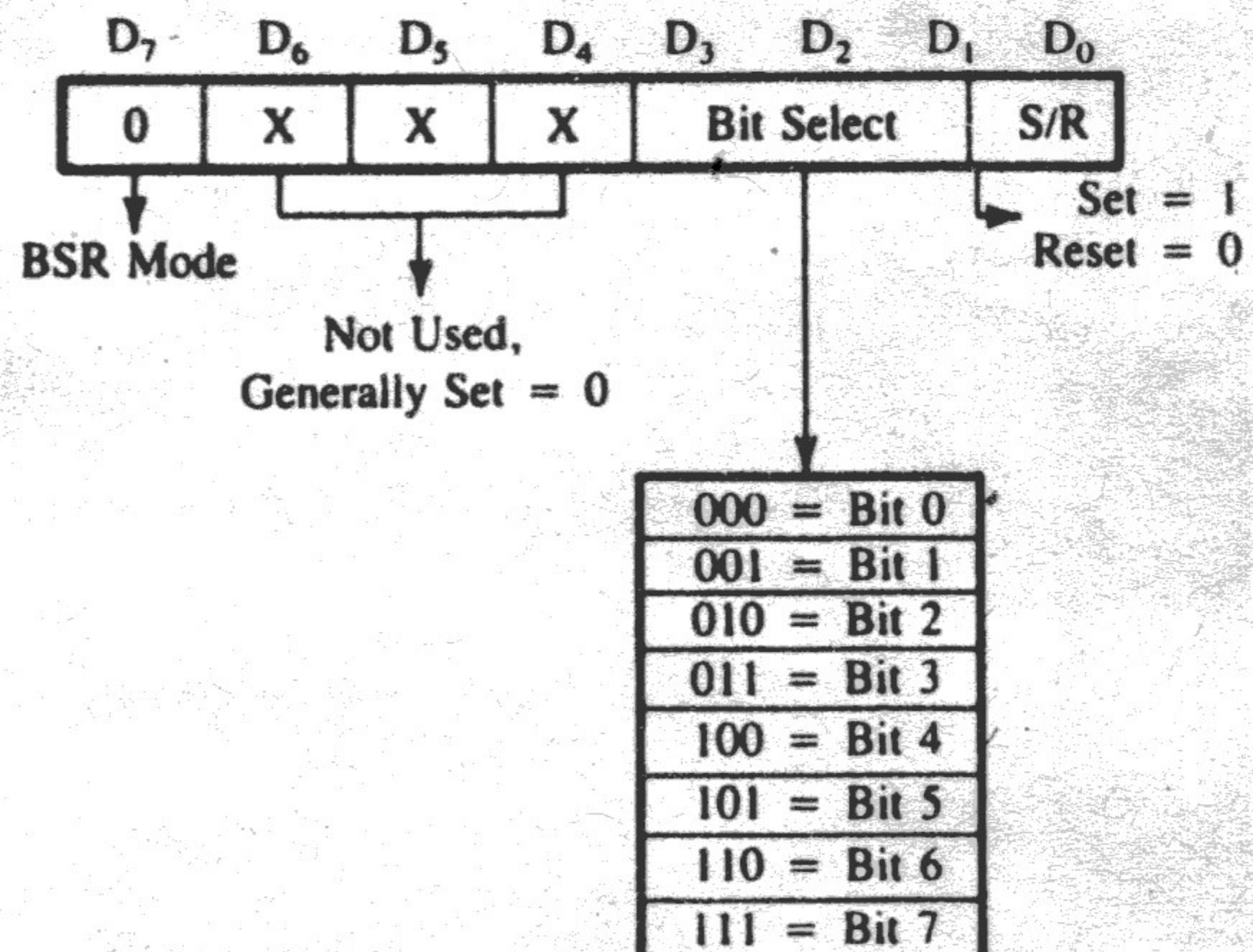
### 15.13 BSR (Bit Set/Reset) Mode

The BSR mode is concerned only with the eight bits of port C, which can be set or reset by writing an appropriate control word in the control register. A control word with bit D<sub>7</sub> = 0 is recognized as a BSR control word, and it does not alter any previously transmitted control word with bit D<sub>7</sub> = 1; thus the I/O operations of ports A and B are not affected by a BSR control word. In the BSR mode, individual bits of port C can be used for applications such as an on/off switch.

#### BSR CONTROL WORD

This control word, when written in the control register, sets or resets one bit at a time, as specified in Figure 15.6.

**FIGURE 15.6**  
8255A Control Word Format in the  
BSR Mode



Write a BSR control word subroutine to set bits PC<sub>7</sub> and PC<sub>3</sub> and reset them after 10 ms.  
Use the schematic in Figure 15.3 and assume that a delay subroutine is available.

**Example  
15.2**

### BSR CONTROL WORDS

	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	=	
To set bit PC <sub>7</sub>	=	0	0	0	0	1	1	1	=	0FH
To reset bit PC <sub>7</sub>	=	0	0	0	0	1	1	0	=	0EH
To set bit PC <sub>3</sub>	=	0	0	0	0	0	1	1	=	07H
To reset bit PC <sub>3</sub>	=	0	0	0	0	0	1	1	=	06H

### PORT ADDRESS

Control register address = 83H; refer to Figure 15.3(b).

### Solution

### SUBROUTINE

BSR:	MVI A,0FH	;Load byte in accumulator to set PC <sub>7</sub>
	OUT 83H	;Set PC <sub>7</sub> = 1
	MVI A,07H	;Load byte in accumulator to set PC <sub>3</sub>
	OUT 83H	;Set PC <sub>3</sub> = 1
	CALL DELAY	;This is a 10-ms delay
	MVI A,06H	;Load accumulator with the byte to reset PC <sub>3</sub>
	OUT 83H	;Reset PC <sub>3</sub>
	MVI A,0EH	;Load accumulator with the byte to reset PC <sub>7</sub>
	OUT 83H	;Reset PC <sub>7</sub>
	RET	

From an analysis of the above routine, the following points can be noted:

1. To set/reset bits in port C, a control word is written in the control register and not in port C.
2. A BSR control word affects only one bit in port C.
3. The BSR control word does not affect the I/O mode.

### 15.14 Illustration: Interfacing A/D Converter Using the 8255A in Mode 0 and BSR Mode

#### PROBLEM STATEMENT

Design an interfacing circuit to read data from an A/D converter, using the 8255A in the memory-mapped I/O.

1. Set up port A to read data.
2. Set up bit PC<sub>0</sub> to start conversion and bit PC<sub>7</sub> to read the ready status of the converter.