PRIORITY MODES OF 8259

Fully Nested Mode (FNM)

It is the **default mode** of 8259.
It is a **fixed priority** mode.
IR_0 has the **highest** priority and **IR_7** has the **lowest** priority.
It is preferred for **"Single"** 8259.

Special Fully Nested Mode (SFNM)

This mode can be **used for** the **Master 8259 in** a **cascaded** configuration.
Its **priority structure** is fixed and is the **same as FNM** (IR_0 highest and IR_7 lowest).
Additionally, in SFNM, the **Master would recognize a higher priority interrupt from a slave,** *whose another interrupt is currently being serviced*. This is **possible only in SFNM**.

Rotating Priority Modes

There are **two** rotating priority modes:
Automatic Rotation and Specific Rotation

Automatic Rotation Mode

This is a rotating priority mode.
It is **preferred** when **several interrupt** sources are of **equal priority**.
In this mode, **after** a device receives **service**, it **gets** the **lowest priority**.
All other priorities rotate subsequently.
Eg: If IR_2 is has just been serviced, it will get the lowest priority.

Specific Rotation Mode

It is **also** a **rotating** priority mode, **but here** the **user can select** any **IR level for lowest priority**, and thus fix all other priorities.

Special Mask Mode (SMM)

Usually 8259 **prevents interrupt requests lower or equal** to the interrupt, which is **currently** in service.
In SMM 8259 **permits interrupts** of **all levels** (lower or higher) **except** the one **currently** in service.
As we are specially masking the current interrupt, it is called Special Mask Mode.
This mode is preferred when we don't want priority

Poll Mode

Here the **INT line** of 8259 is **not used** hence 8259 cannot interrupt the **µp**.
Instead, the **µP will give Poll command** to 8259 using OCW3.
In **return**, **8259 provides** a **Poll Word** to the µP.
The Poll Word **indicates** the **highest priority interrupt**, which requires service.

Poll Word

I	x	x	x	x	W_2	W_1	W_0

1= Valid Interrupt
0 = No valid interrupt

Level No of the highest priority interrupt to be serviced

W_2	W_1	W_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Thereafter the **µP services the interrupt**. **For doubts contact Bharat Sir on 98204 08217**
Advantage: The µP's program is not disturbed. It can be used when the ISR is common for several Interrupts. It can be used to increase the total number of interrupts beyond 64.
Drawback: If the polling interval is too large, the interrupts will be serviced after long intervals. If the polling interval is small, lot of time may be wasted in unnecessary polls.

Buffered Mode

In this mode $\overline{\textbf{SP}}$ / $\overline{\textbf{EN}}$ becomes **low** during $\overline{\textbf{INTA}}$ cycle.
This signal is used to enable the buffer.

EOI – (End Of Interrupt)

When the **µP responds** to an interrupt request by **sending the first** $\overline{\textbf{INTA}}$ signal, the **8259 sets** the **corresponding bit** in the In Service Register (**InSR**).
This **begins** the **service** of the interrupt.
When this bit in the In Service Register is **cleared**, **it is called** as **End of Interrupt (EOI)**.

EOI Modes:

1) Normal EOI Mode:

Here an EOI Command is necessary. The EOI Command is given by the programmer at the end of the ISR. It causes 8259 to clear the bit from In Service Register. There are two types of EOI Commands:

Non Specific EOI Command:

Here the programmer doesn't specify the Bit number to be cleared. 8259 automatically clears the highest priority bit from In Service Register.

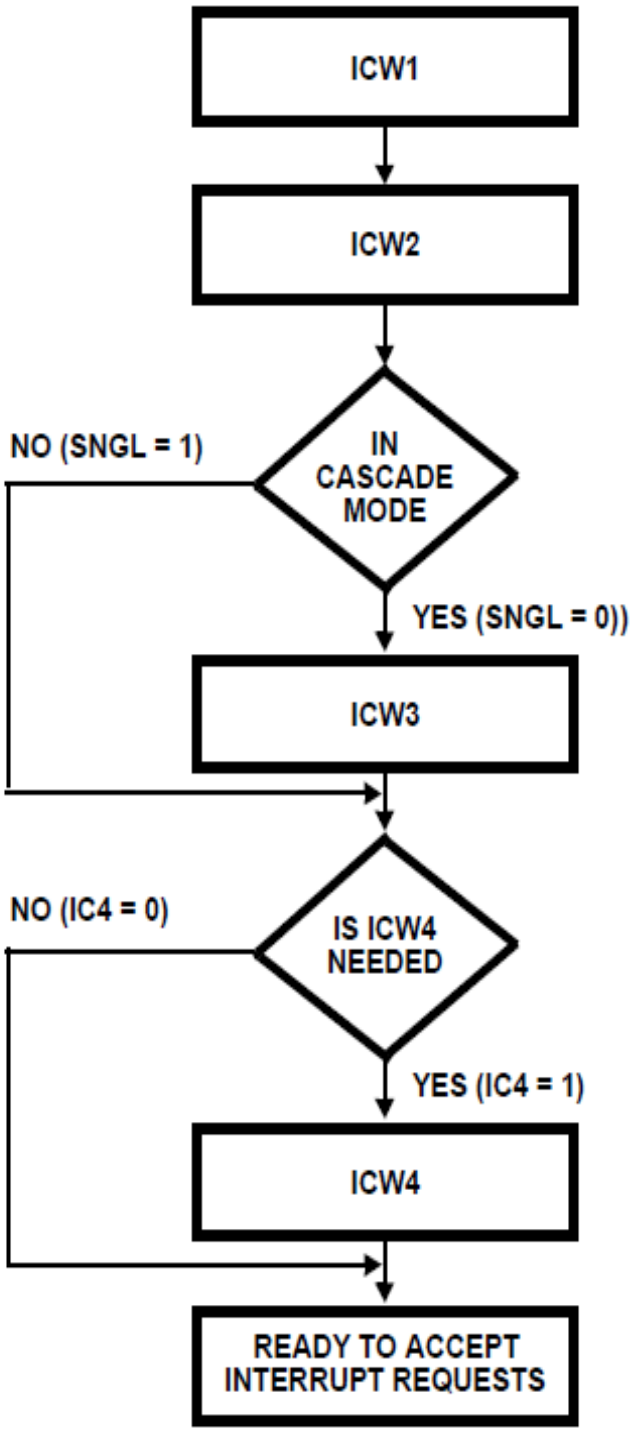
Specific EOI Command:

Here the programmer specifies the Bit number to be cleared from In Service Register.

2) Auto EOI Mode (AEOI):

In AEOI mode the EI command is not needed. Instead, 8259 will itself clear the corresponding bit from In Service Register at the end of the 2nd $\overline{\textbf{INTA}}$ pulse.

Initialization of 8259



As seen above there are **two types** of **commands**, **Initialization Command Words (ICWs)** and **Operational Command Words (OCWs).**

ICWs

ICWs have to be **given during** the **initialization** of 8259 (i.e. **before** the µP can start **using 8259**).
For doubts contact Bharat Sir on 98204 08217
ICW1 and **ICW2** are **compulsory**.
If Cascaded, **ICW3** has to be given.
Whether **ICW4** is **required** or not, is **specified in the ICW1**.
If ICW4 is **required**, it has to be **written**.
It is **important** that the ICWs are **written in** the **above sequence only**.
None of the ICWs can be individually repeated, but the entire initialization can be repeated if required.

OCWs

OCWs are **given during** the **operation** of 8259 (i.e. **after** the µP has **started using** 8259).
OCWs are **not compulsory**.
OCWs **do not** have to be given in a specific order.
OCWs can be individually repeated.

They are mainly used to alter the **masking** status and the **operation modes** of 8259.

ICW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LTIM	ADI	SNGL	IC4

1 = ICW4 needed
0 = No ICW4 needed

1 = Single
0 = Cascade Mode

CALL address interval
1 = Interval of 4
0 = Interval of 8

1 = Level triggered mode
0 = Edge triggered mode

A_7 - A_5 of Interrupt vector address
(MCS-80/85 mode only)

ICW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	A_{15} / T_7	A_{14} / T_6	A_{13} / T_5	A_{12} / T_4	A_{11} / T_3	A_{10}	A_9	A_8

A_{15} - A_8 of interrupt vector address
(MCS80/85 mode)

T_7 - T_3 of interrupt vector address
(8086/8088 mode)

ICW3 (MASTER DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

1 = IR input has a slave
0 = IR input does not have a slave

ICW3 (SLAVE DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

SLAVE ID (NOTE)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW4

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	SFNM	BUF	M/S	AEOI	µPM

1 = 8086/8088 mode
0 = MCS-80/85 mode

1 = Auto EOI
0 = Normal EOI

0	X	- Non buffered mode
1	0	- Buffered mode slave
1	1	- Buffered mode master

1 = Special fully nested moded
0 = Not special fully nested mode

OCW1

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0

Interrupt Mask
1 = Mask set
0 = Mask reset

OCW2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	R	SL	EOI	0	0	L_2	L_1	L_0

IR LEVEL TO BE ACTED UPON

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

0	0	1	Non-specific EOI command	End of interrupt
0	1	1	† Specific EOI command	
1	0	1	Rotate on non-specific EOI command	Automatic rotation
1	0	0	Rotate in automatic EOI mode (set)	
0	0	0	Rotate in automatic EOI mode (clear)	
1	1	1	† Rotate on specific EOI command	
1	1	0	† Set priority command	Specific rotation
0	1	0	No operation	

† L_0 - L_2 are used

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	ESMM	SMM	0	1	P	RR	RIS

READ REGISTER COMMAND

0	1	0	1
0	0	1	1
No Action		Read IR reg on next RD pulse	Read IS reg on next RD pulse

1 = Poll command
0 = No poll command

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
No Action		Reset special mask	Set special mask

8259 PROGRAMMING

Normally in the exam you are asked to initialize a **single 8259** for some given specifications. **For doubts contact Bharat Sir on 98204 08217**
Remember that **in any case ICW1, ICW2 and ICW4 will be required.**
If the system is **cascaded** then **ICW3** is required.
For a **cascaded system** remember that **every 8259 has to be initialized,** i.e. the entire procedure has to be **repeated for each 8259.**
If **masking** is asked then **OCW1** is required.
If **rotating priority** is asked then **OCW2** is required.
Finally, if **SMM or Polling** is asked then **OCW3** is required.

Q 1) WAP to initialize Single 8259 as follows
Edge triggered,
Single,
Auto EOI Mode,
Buffered Mode,
Mask IR3, IR4, IR5, IR6,
Vector number of IR0 is 40H.
Assume 8259 is at Port Address 80H.

Soln:

```
     Code SEGMENT
          ASSUME CS: Code

   Start: MOV AL, 13H
          OUT  80H, AL        // ICW1 = 0001 0011 = 13H

          MOV  AL, 40H
          OUT  82H, AL        // ICW2 = 0100 0000 = 40H

          MOV  AL, 0BH
          OUT  82H, AL        // ICW4 = 0000 1011 = 0BH

          MOV  AL, 78H
          OUT  82H, AL        // OCW1 = 0111 1000 = 78H

          INT  03H

     Code ENDS

          END Start
```

Q 2) **WAP to initialize Cascaded 8259.**
One Master, two slaves connected on IR2 and IR3 of master.
Master: Port address 80H. Vector Number of IR6 is 46H. Edge triggered. AEOI Mode. SFNM. Keyboard Interrupt connected on IR4.
Slave2: Port address 84H. Vector Number of IR0 is 50H. Level triggered. Normal EOI Mode. Printer Interrupt on IR0. Card Reader Interrupt on IR1.
Slave3: Port address 90H. Vector Number of IR6 is 76H. Edge triggered. AEOI Mode. External Interrupts connected on IR0, IR1, IR2 and IR7.
For all the above 8259's, mask the unwanted interrupts.
Also show the decoding for the above circuit.

Soln: **For doubts contact Bharat Sir on 98204 08217**

```
Code   SEGMENT
       ASSUME CS: Code
Start: MOV  AL, 11H     // MASTER 8259
       OUT  80H, AL          // ICW1 = 0001 0001 = 11H
       MOV  AL, 40H
       OUT  82H, AL          // ICW2 = 0100 0000 = 40H
       MOV  AL, 0CH
       OUT  82H, AL          // ICW3 = 0000 1100 = 0CH
       MOV  AL, 1FH
       OUT  82H, AL          // ICW4 = 0001 1111 = 1FH
       MOV  AL, E3H
       OUT  82H, AL          // OCW1 = 1110 0011 = E3H

       MOV  AL, 19H     // SLAVE at IR2
       OUT  84H, AL          // ICW1 = 0001 1001 = 19H
       MOV  AL, 50H
       OUT  86H, AL          // ICW2 = 0101 0000 = 50H
       MOV  AL, 02H
       OUT  86H, AL          // ICW3 = 0000 0010 = 02H
       MOV  AL, 09H
       OUT  86H, AL          // ICW4 = 0000 1001 = 09H
       MOV  AL, FCH
       OUT  86H, AL          // OCW1 = 1111 1100 = FCH

       MOV  AL, 11H     // SLAVE at IR3
       OUT  90H, AL          // ICW1 = 0001 0001 = 11H
       MOV  AL, 70H
       OUT  92H, AL          // ICW2 = 0111 0000 = 70H
       MOV  AL, 03H
       OUT  92H, AL          // ICW3 = 0000 0011 = 03H
       MOV  AL, 0BH
       OUT  92H, AL          // ICW4 = 0000 1011 = 0BH
       MOV  AL, 78H
       OUT  92H, AL          // OCW1 = 0111 1000 = 78H

       INT 03H
Code   ENDS
END    Start
```