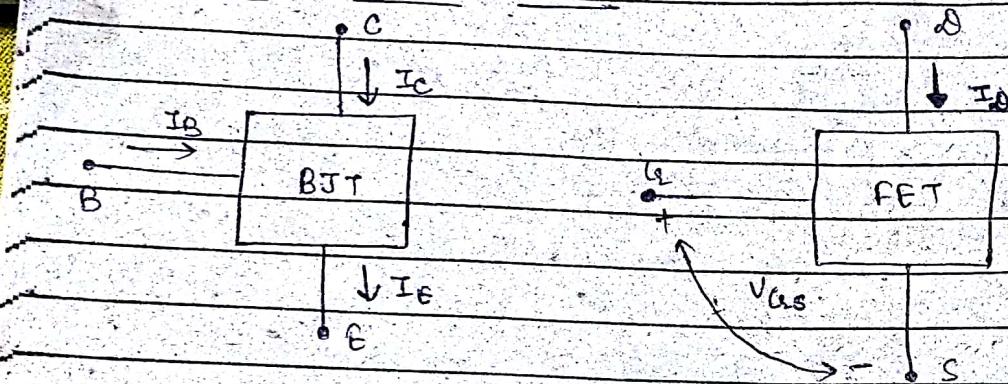


FET (b)

Field-Effect Transistor :-

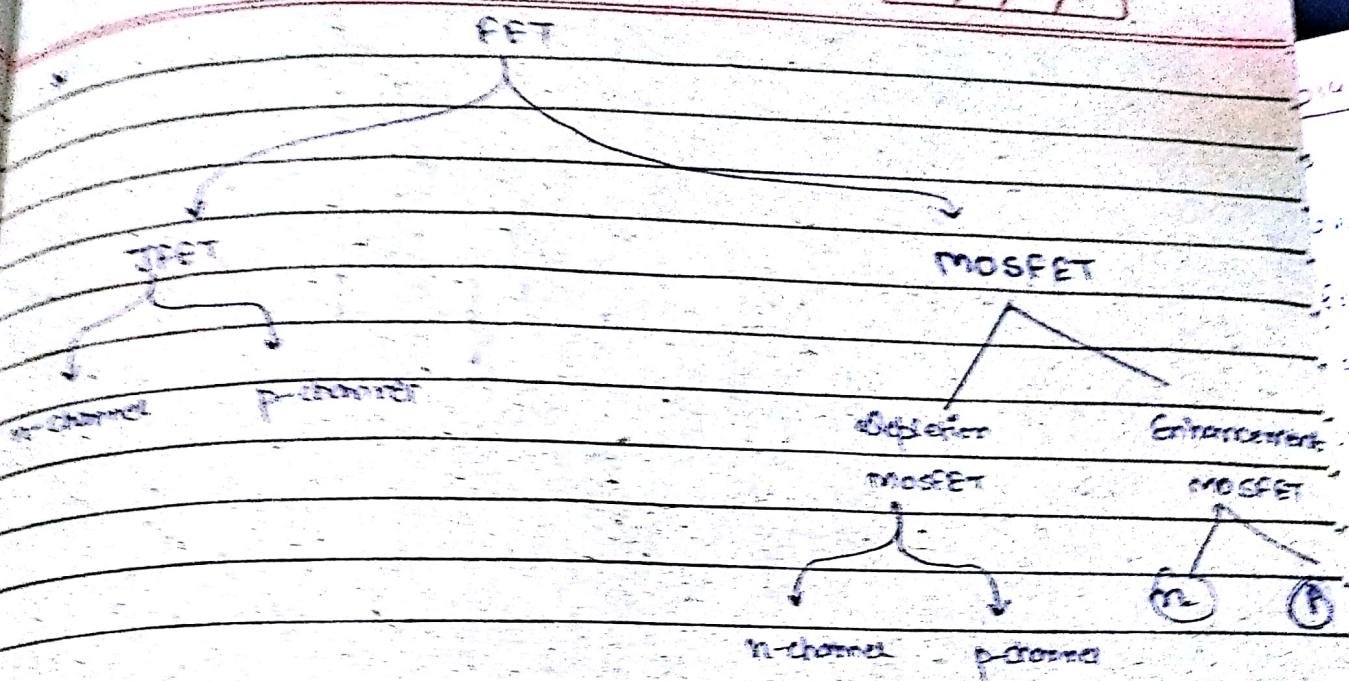
* App. of FET \approx App. of BJT

* BJT is current controlled device whereas FET is a voltage controlled device.

$$\begin{array}{l} \xrightarrow{\text{BJT}} \left. I_C = f(I_B) \right\} \quad \text{out} = f(\text{input}) \\ \xrightarrow{\text{FET}} \left. I_D = f(V_{GS}) \right. \end{array}$$

* BJT \rightarrow BipolarFET \rightarrow Unipolar either e- or holes

* FET can be used for amplification and also for switching.



due to charges, there is an E which controls conduction path of output. (Field - Effect)

- + FET have high I/O impedance
- + More temp. stable
- + Area occupied or size is lesser
- + BJT are more sensitive.

Construction & working of JFET :-

n-channel

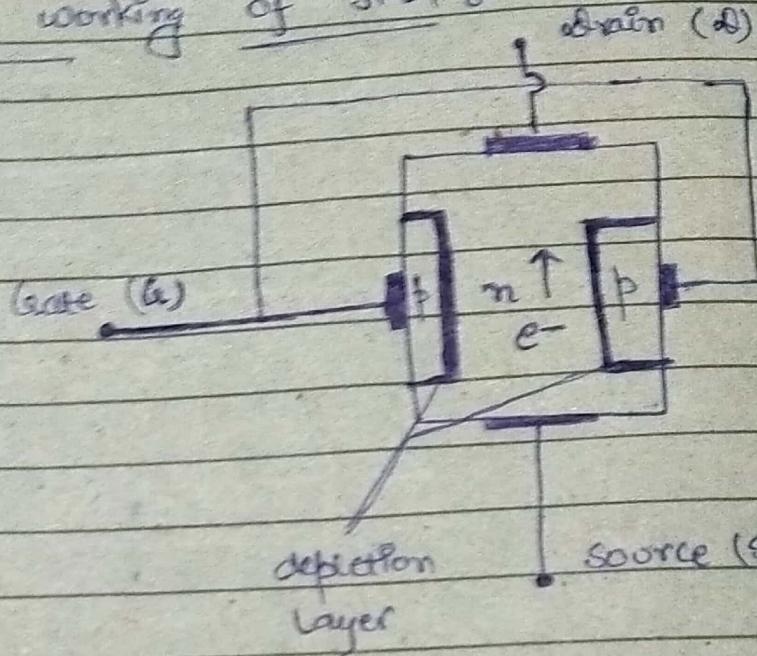
2 = pn zone



2 depletion region

water tap

JFET



water \longrightarrow e⁻

cause of water flow \longrightarrow App voltage

Working of

Case I. $V_{GS} = 0V$

V_{GS}

+ve

Valve Knob - Gate

Case II. $V_{GS} < 0V$

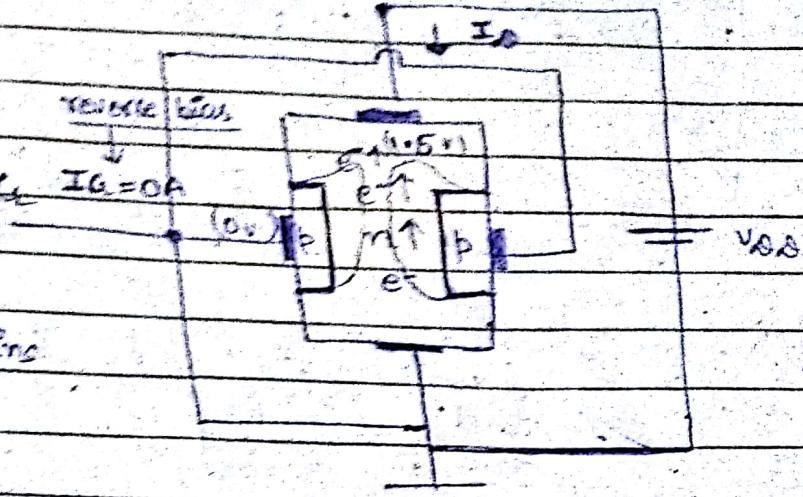
Sink - Drain

Spigot - Source

Case I.

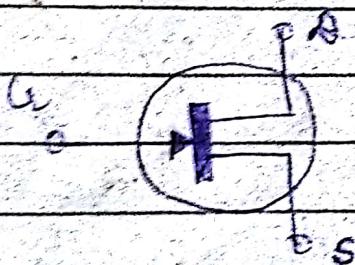
due to V_{DS} ,
depletion layer ~~resistance~~
will change
it expands
from the drain

Side but remains
almost same at
the bottom.



At gate side, 0 V is there but opposite side
1.5 V is there. So, PN junction is getting
reverse biased, that's why depletion layer ↑.

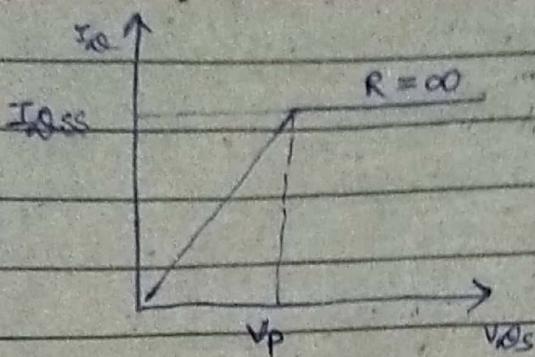
Symbol:



* Pinch-off voltage $\theta - (V_p)$ $V_{DS} \uparrow = I_D \uparrow$

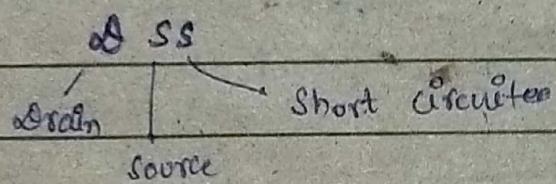
→ the voltage at which depletion layer touches
each other :

ii) ^{of f} _{Numerical} states



$I_{DSS} \rightarrow$ max drain current
when ($V_{DS} = 0V$)

$$\text{if } [V_{DS} > |V_P|]$$



* JFET as a Current Source :-

→ when $V_{DS} > V_P$, depletion region don't \uparrow at the top but it will \uparrow along the length of the n-channel. & constant current flows through the ckt.

→ $I_D = I_{DSS}$ when $V_{DS} < V_{DS\max}$

$$V_{DS} > V_{DS\max}$$

↓
a very large drain current flows i.e. breakdown

* Case II. $V_{GS} < 0$

Case I : $V_{GS} = 0 \text{ V}$

$$V_{DS} > |V_p|$$

$$\text{f } V_{DS} = V_{DD} > 0 \text{ V}, I_D = I_{DSS}$$

Case II' $V_{GS} < 0 \text{ V}$

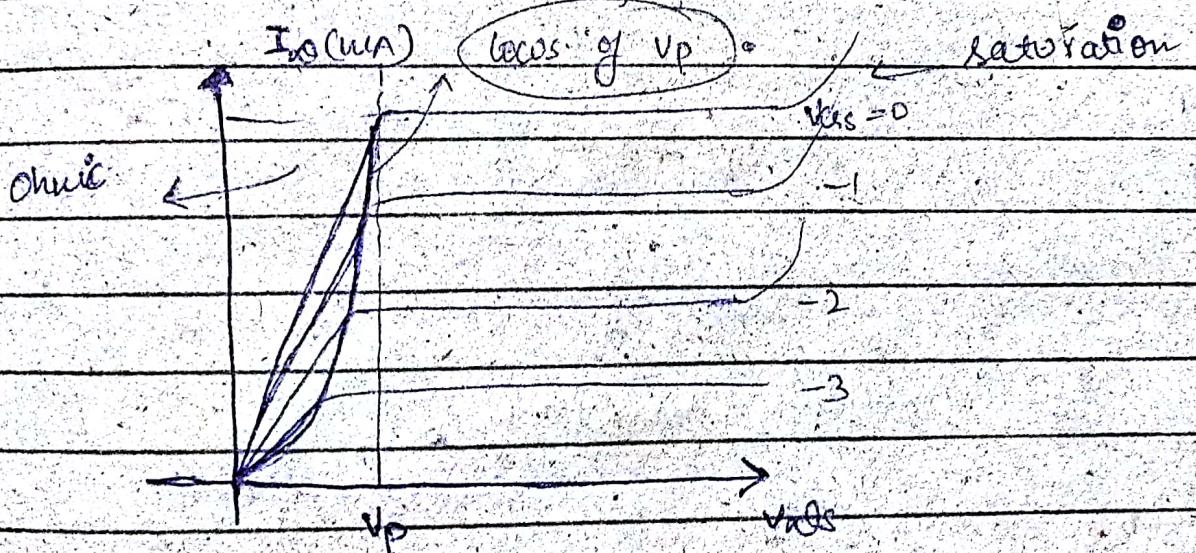
$$\text{f } V_{DS} = V_{DD} < V_{DS}$$

Obtain the Saturation at lower value of V_{DS} so that constant current I_D flows.

* Output or Drain characteristics of JFET :-

↳ n-Channel

I_D v/s V_{DS} for diff. (V_{GS})



* JFET as voltage-controlled resistors :-

Ohmic region = Voltage controlled ~~resistor~~ resistor region

JFET can be used as VCR in ohmic mode :-

as $V_{GS} \downarrow$, slope = \downarrow

$$R = 1/\text{slope} \rightarrow \text{So, } R \uparrow$$

$$R = \frac{I_d}{\text{slope}} = \frac{I_d}{(1 - \frac{V_{GS}}{V_p})^2}$$

* Transfer CT of JFET :-

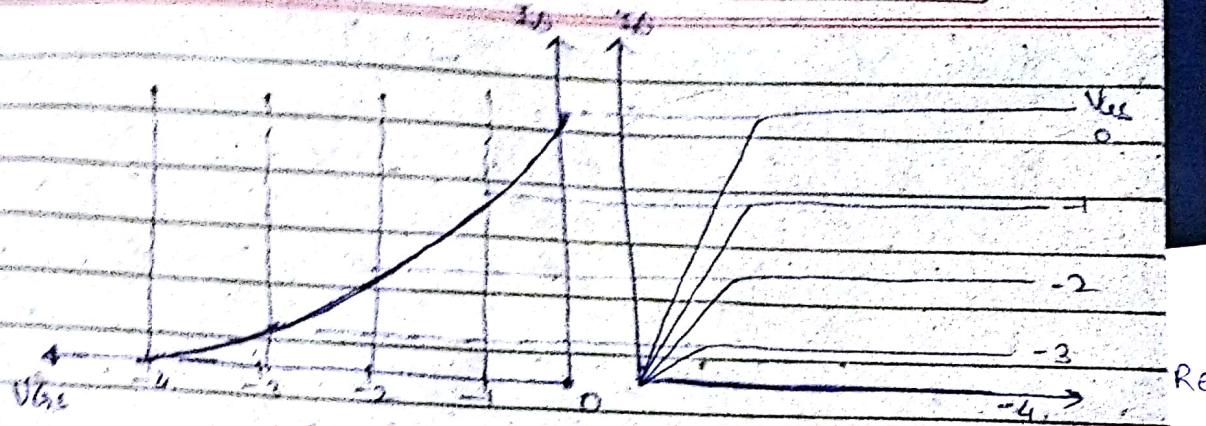
I_d v/s V_{GS} keeping V_{DS} constant.

$$I_d = I_{DSS} \left(1 - \frac{V_{GS}}{V_p}\right)^2$$

2 ways to obtain transfer CT

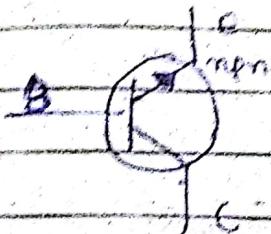
i) Using above eqn

ii) Using o/p or drain characteristics.

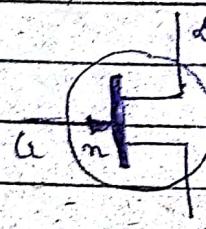


* BJT v/s JFET

1.



2.



2. $I_C = f(I_B) = \beta I_B$

Correct

2. $I_D = f(V_{GS}) = I_{DSS} (1 - \frac{V_{GS}}{V_P})^2$

3. Controlled device

3. Voltage controlled device

4. Bipolar

4. Unipolar

5. $I_C \approx I_E$

5. $I_D = I_S$

6. $V_{BE} = 0.7V$ (s)

6. $I_{CE} = 0A$

7. Good fanout

7. Bad fanout

3. b) density of

9.

- | | |
|-----------------------------------|--|
| 8. Linear Amp | 9. Non-linear Amp |
| 9. Power consumption ↑ | 9. Power consomp ↓ |
| 10. $Z_i \downarrow$ | 10. $Z_i \uparrow$ |
| 11. Thermal stability Bad | 11. Good |
| 12. Gain ↑ | 12. Gain ↓ |
| 13. Sensitivity $\Theta \uparrow$ | 13. Sens $\Theta \downarrow$ |
| 14. Noise level ↑ | 14. NC ↓ |
| 15. Size ↑ | 15. Size ↓ |
| * Transconductance | $g_m = \frac{\partial i_o}{\partial v_{de}}$ |