Construction and working of Enchancement -Type MOSFET

MOSFET → Active device

Any type of device has ability to control the flow of electron is Known as active device

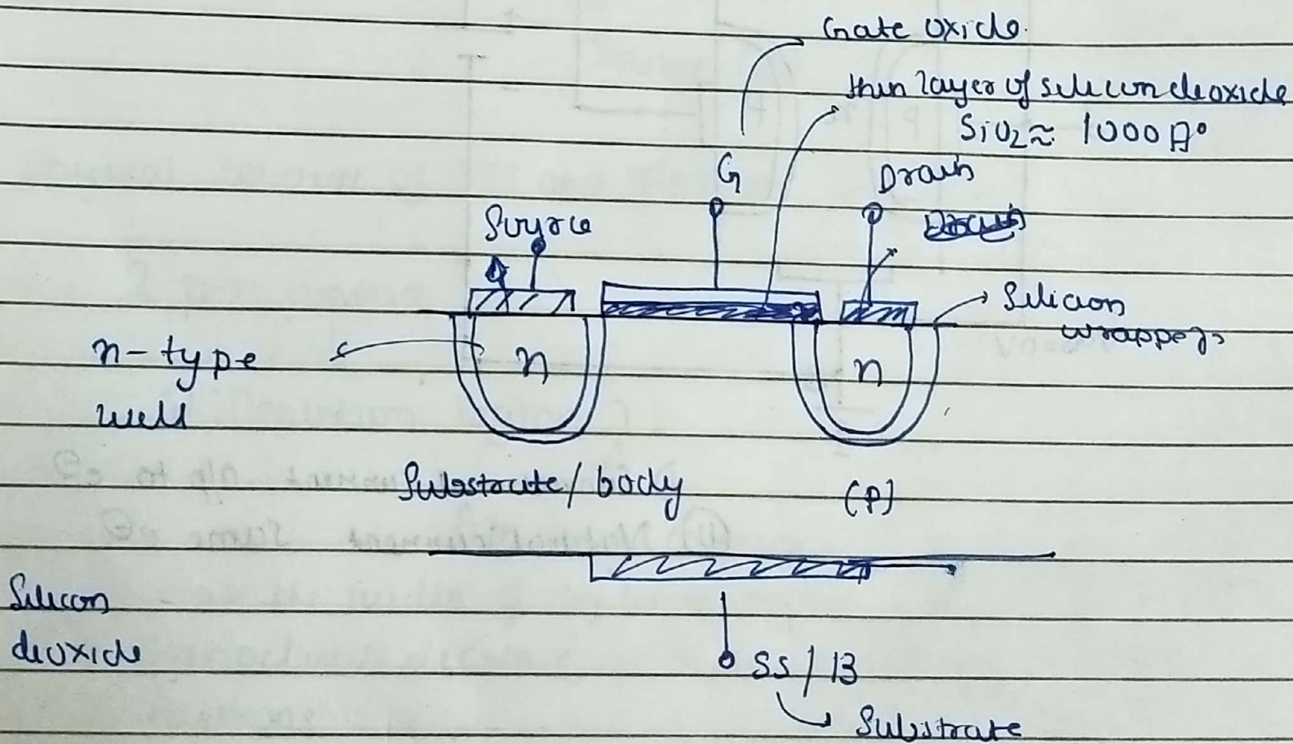
ex → BJT, JFET

Passive device

ex → Diode, Capacitors, Transformer etc

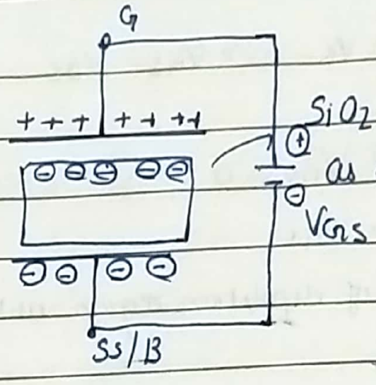
1) Depletion type MOSFET → n-channel, p-channel
Ch ✓ D and S

2) Enchancement Type MOSFET → $\boxed{\text{n-channel}}$, p-channel
Ch X D and S.



The majority charge carrier → holes.
minority charge carrier → $e^{\ominus}$
mobile C.C = Inmobile ions.

We have Gate more positive



SiO_2 acting as dielectric.

Inversion:

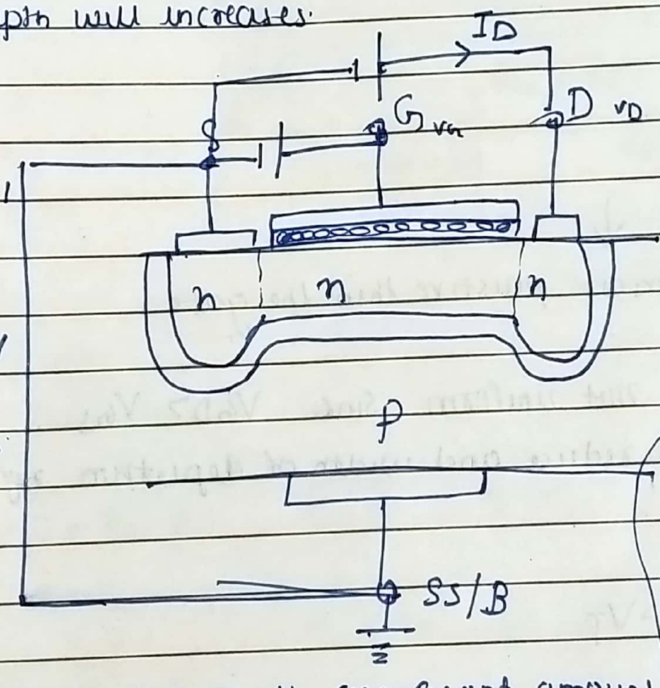
We change n-type to p-type ~~haven~~ by making gate terminal positive

So channel is formed.

$V_{GS} > 0$, Inversion will happen ptype-ntype So conductive channel is formed between source and drain

Ch. width / depth ↑

The more the positive on Gate terminal, So the channel width and depth will increases.



$V_{SSS} = 0V$

$V_{GSS} \rightarrow V_{GS}$

↑ V_{GS}

⇓

Width of channel increase

$V_{GS} >$ particular voltage then Channel width is sufficient to allow the flow of current I_D

Threshold voltage V_T

$V_T \rightarrow$ The voltage which result, significant amount of current to flow from source to Drain is known as threshold voltage.

$V_{GS} > V_T$, I_D ↑

We did not want to many biasing source

$V_G - V_{GS} + V_{DS} = V_D$

$V_{GD} = V_G - V_D = V_{GS} - V_{DS}$

$V_{GD} = V_G - V_D = V_{GS} - V_{DS}$

Case 1 = $V_{DS} = 0\,V$

$V_{GD} = V_{GS}$

width of depletion region will be uniform

$V_T = 1V$

$V_{GS} = 2V = V_{GD}$

Excess voltage $= V_{GS} - V_T = 1V$

$Ch_1 \rightarrow 1V$

$V_{GS} = 4V = V_{GD}$

$CH_3 \rightarrow 3V$

Case 2 = $V_{GS} = 3V = V_{GD}$

$CH_2 \rightarrow 3 - 1 = 2V$

$CH_1 < CH_2 < CH_3$

Case 2: $V_{DS} > 0V$

$V_{GD} = V_{GS} - V_{DS}$ ↓

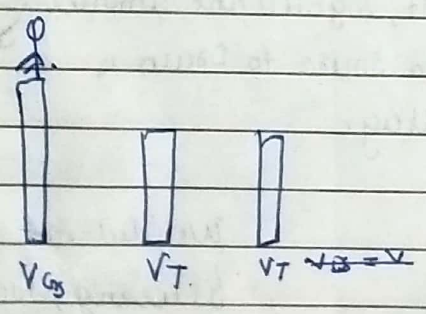
Drain is becoming more positive than the gate

Depletion region is not uniform since $V_{GD} > V_{GS}$.

width of channel will reduce and width of depletion region will increase

Case 3: $V_{DS} = V_{GS} - V_T$

$V_{GD} = V_T$



So the channel will be become very narrow and width will be almost zero, it will happen only near closing

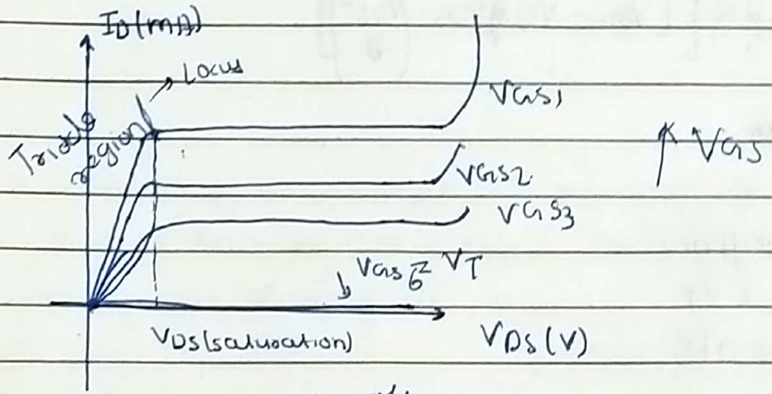
This condition is known as pinch off

Drain characteristics of Enhancement-Type MOSFET

Output characteristics

O/P i → I_D control variable → V_{GS}
O/P V → V_{DS}

Dr ch → I_D vs V_{DS} for various levels of V_{GS}



cutt-off region

V_T and K $V_{DS}(saturation) = V_{GS_1} - V_T$

Case I: $V_{GS} > V_T$
Veff $= V_{GS_1} - V_T$

$V_{DS} = 0 \Rightarrow V_D = V_S$ $V_{DS} \uparrow \rightarrow I_D \uparrow$

$V_{DS} = V_{DS\,saturation} \Rightarrow I_D =$ constant | pin off

$V_{DS} + V_{GD} - V_{GS} = 0$
$V_{GD} = V_{GS} - V_{DS}$
$V_{GD} = V_T$

Case II $V_{GS_2} < V_{GS}\,1$ $\uparrow V_{GS} \Rightarrow$ channel width ↑
$\delta_2 < \delta_1$ conductivity ↑
$R_2 > R_1$ slope2 < slope1 resistance ↓

Saturation — Regions

$V_{DS} \geq V_{GS} - V_T$

$I_D = K(V_{GS} - V_T)^2$

↳ constant depends upon w/l

$K = \dfrac{I_D}{(V_{GS} - V_T)^2}$ A/V^2

Triode Region

$V_{DS} < V_{GS} - V_T$

$I_D = 2K\left[(V_{GS} - V_T)V_{DS} - \left(\dfrac{V_{DS}^2}{2}\right)\right]$

drain

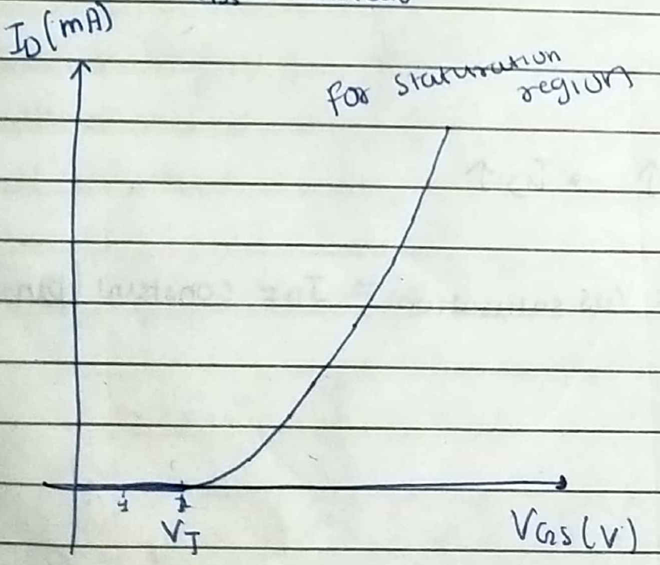
Cutt off regions

$V_{GS} < V_T$

$I_D = 0A$

Transfer characterists of Enchancement Type MOSFET

$V_{DS} \rightarrow$ constant

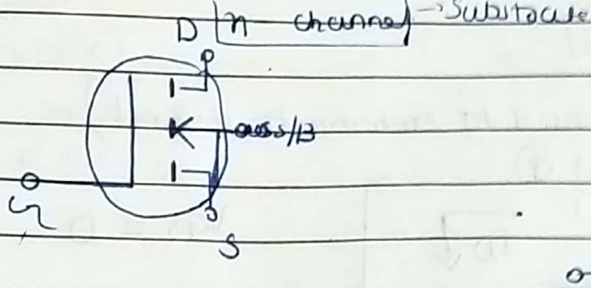


$V_{DS} \geq V_{GS} - V_T$

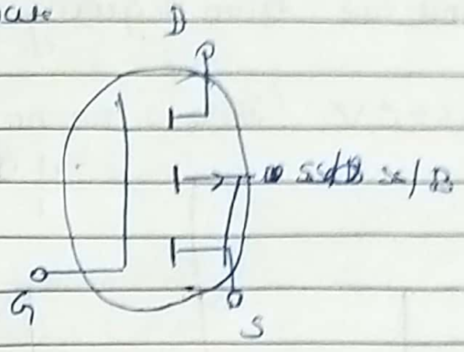
In saturation

$I_D = K(V_{GS} - V_T)^2$

$SiO_2 \rightarrow$ to insulate the Gate from drain, source and substrate so that gate current will become Zero. Due to this input impedance will be higher Hence the Gain will be higher



n- Channel



P- Channel

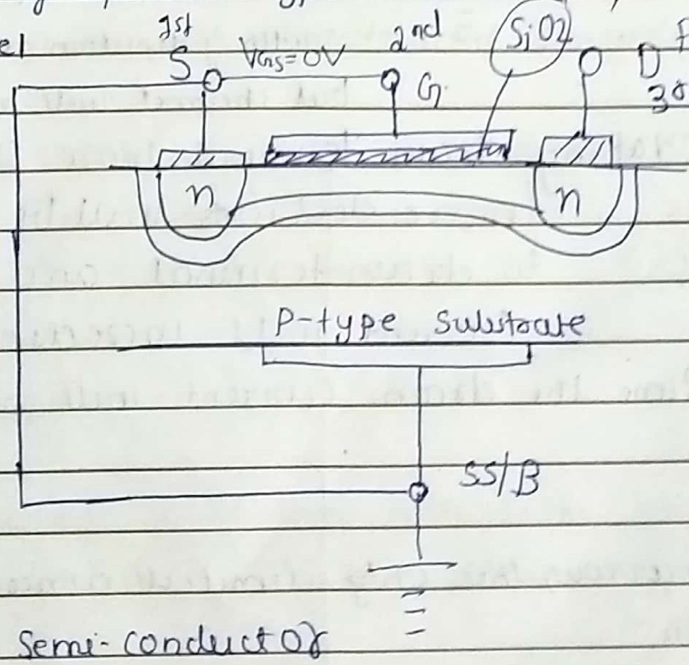
ii) Region for arrow

Arrow indicates the direction of drain current for n-channel, drain current goes into MOSFET through drain region and for p channel drain current coming out of the drain region

Construction of Depletion-Type MOSFET

Input Impedance is high, channel is present from begining

n-channel



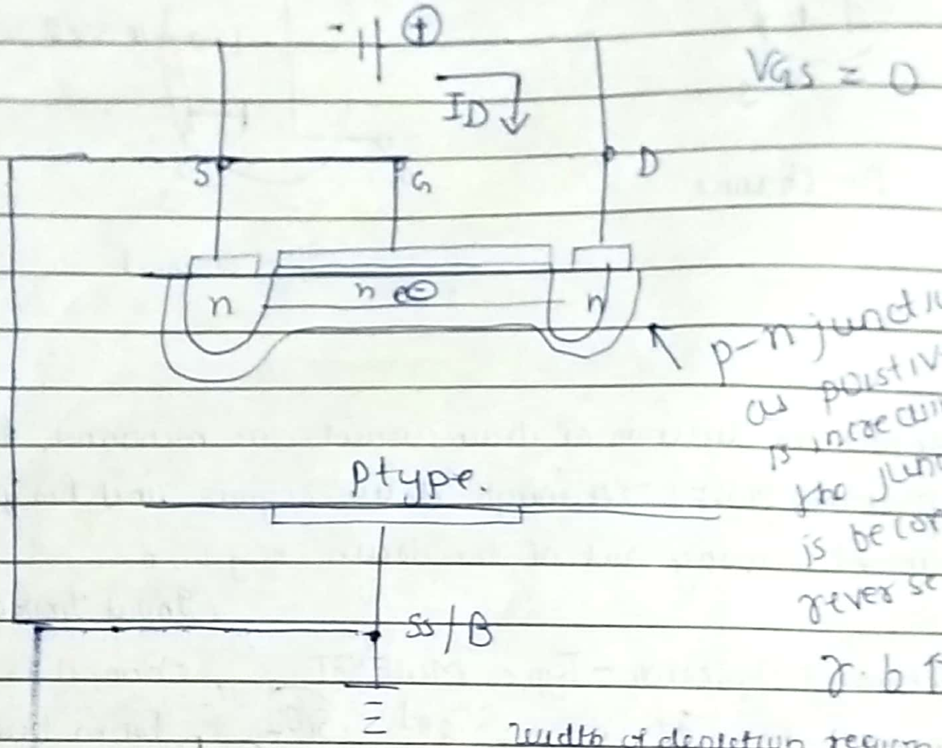
Metal oxide Semi-conductor

Working of Depletion-Type MOSFET

× n-Channel JFET

Channel are from begining

$V_{GS} = 0V$ (There is no need to enchance the channel)



as positive is increasing the junction is becoming reverse bias.

r.b ↑

width of depletion region ↑
but channel will become narrow

↑ V_{DS} | Making drain terminal more positive
(more electrons will be attracted to drain terminal and drain current will increase)

$V_{DS} = V_D - V_S$

$V_{DS} \uparrow$ =

But after some time the drain current will become constant.

The channel become narrow, then only limited amount of electrons will pass

$I_D \rightarrow$ constant

I_{DSS}

n - channel

JFET

$I_{DSS} \rightarrow$ Maximum

$V_{GS} = 0$

$V_{GS} > 0$ ✗ cannot be made

$V_{GS} \leq 0$

D-MOSFET

$I_{DSS} \rightarrow$ is Not maximum current

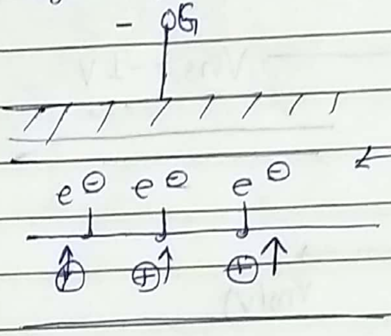
$V_{GS} = 0$

if $V_{GS} > 0$

$V_{GS} \rightarrow$ +ve, 0, −ve

Case II

$V_{GS} = -1V \rightarrow$ negative potential at gate will repel the electrons



The electrons at n-channel will push the electrons in p-substrate and holes of p channel are attracted towards n-channel

recombination take place and available electrons for conduction will decrease. Due to less electrons present in n-channel the current I_D will also decrease.

Case III

$V_{GS} = 1V$

The positive potential at the gate; attract the minority charge carrier (e^-) from p-substrate, collision will occur between accelerating particle,

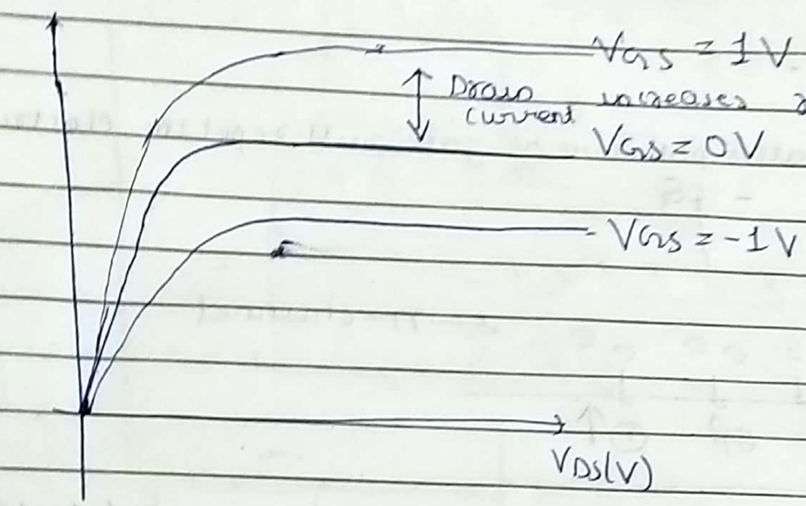
$I_D \uparrow$ rapidly

Drain and Transfer characteristics of Depletion-Type MOSFET

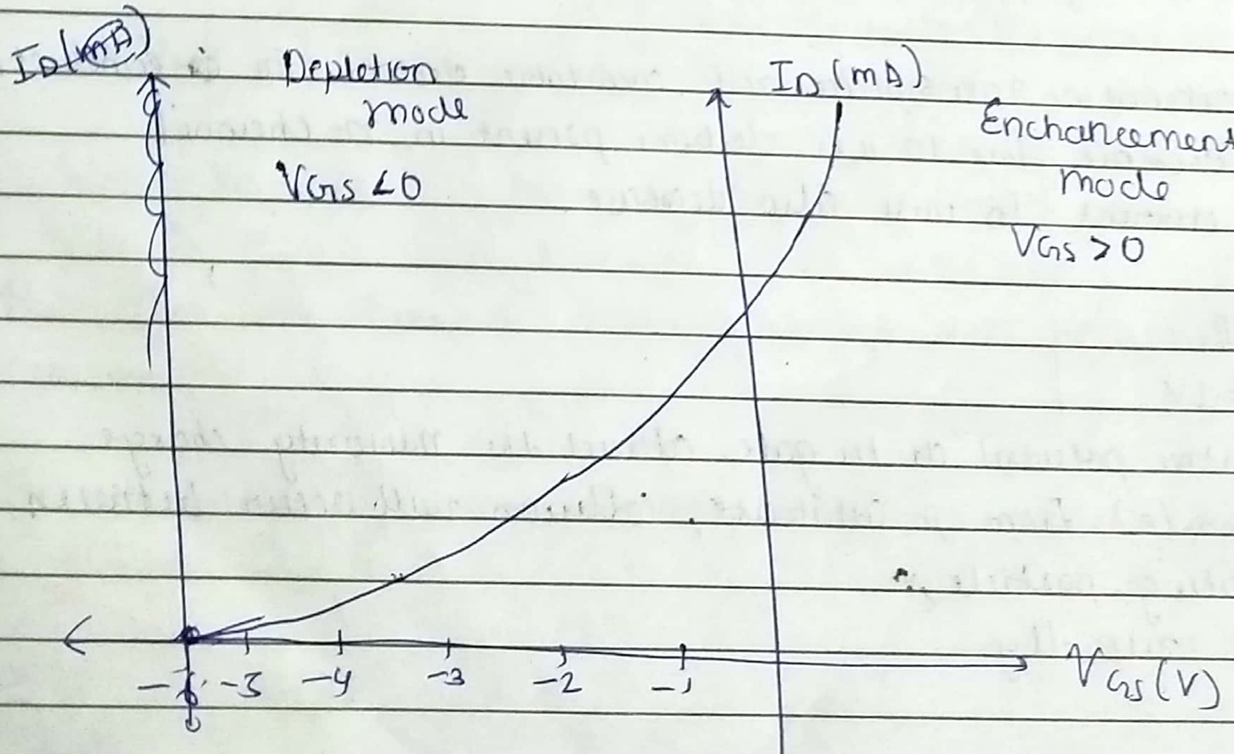
O/P I_D Vs $V_{DS} \rightarrow$ O/P
for various $V_{GS} \rightarrow$ I/P voltage

→ O/P I_D Vs V_{GS} I/P
for fixed V_{DS}

Drain characteristis



① $V_{GS} = 0\,V \Rightarrow V_D - V_S = 0 \quad V_D = V_S$



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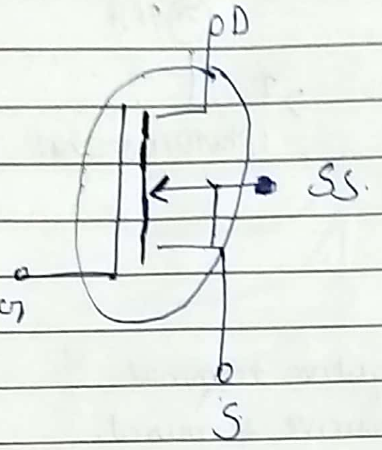
we call it enhancement mode in D-MOSFET, bcoz as positive Vgs applied through gate, the width of n-channel between source and drain increases due to flow of electron from p-type substrate into n-type channel. Hence drain current also increased due to the width of n-channel thus the drain current enhances so we called it enhancement mode



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