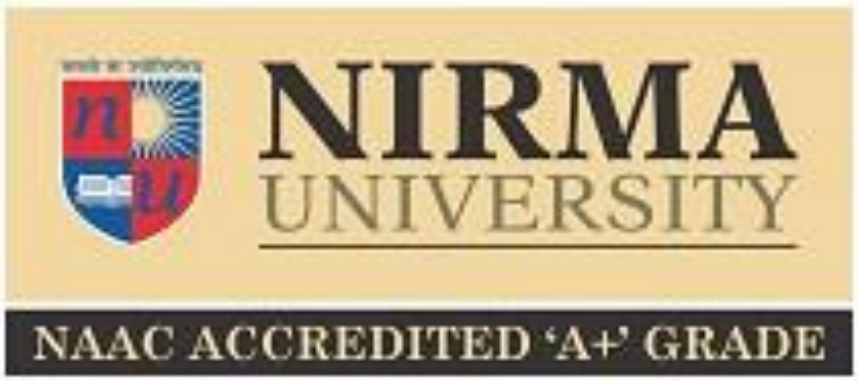
2CS401 :

COMPUTER ARCHITECTURE

INNOVATIVE ASSIGNMENT

SEMESTER IV



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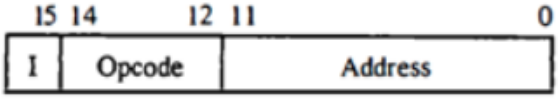
Implementation of 5 new instructions in our computer :-

In our implementation of 5 new instructions for our computer, the instructions are stored in RAM.

RAM contains 2^12=4096 memory words (Each having 12 address bits). Each memory word contains 16 bits. Size of RAM is 4096 X 16.

Micro-operations are stored in ROM. Each memory word in ROM is of 12 bits, Total of 2^7=128 memory words are defined in the ROM. Size of ROM is 128 X 12.

Instruction format is defined as:-



Operation codes of new instructions are defined as:-

Opcode	Operation	Specification
000	NOR	AC←(AC +DR)’
001	NOTDR	DR←DR’
010	MUL	AC←(AC*DR)
011	XOR	AC←(AC^DR)
100	COPY	AC←DR
101	CLRDR	DR←0

Mapping procedure:-

3-bits of opcode are mapped to make a 7-bit address

CAR(0,1,2,6)←0 , CAR(3,4,5)←opcode

Each memory word in ROM is of 12-bits defined as:-

Destination	Source-2	Source-1	Operation bits
A(9-11)	A(6-8)	A(3-5)	A(0-2)

Operation bits:-

A(0-2)	Operation
000	NOR
001	NOT
010	MUL
011	XOR
100	COPY

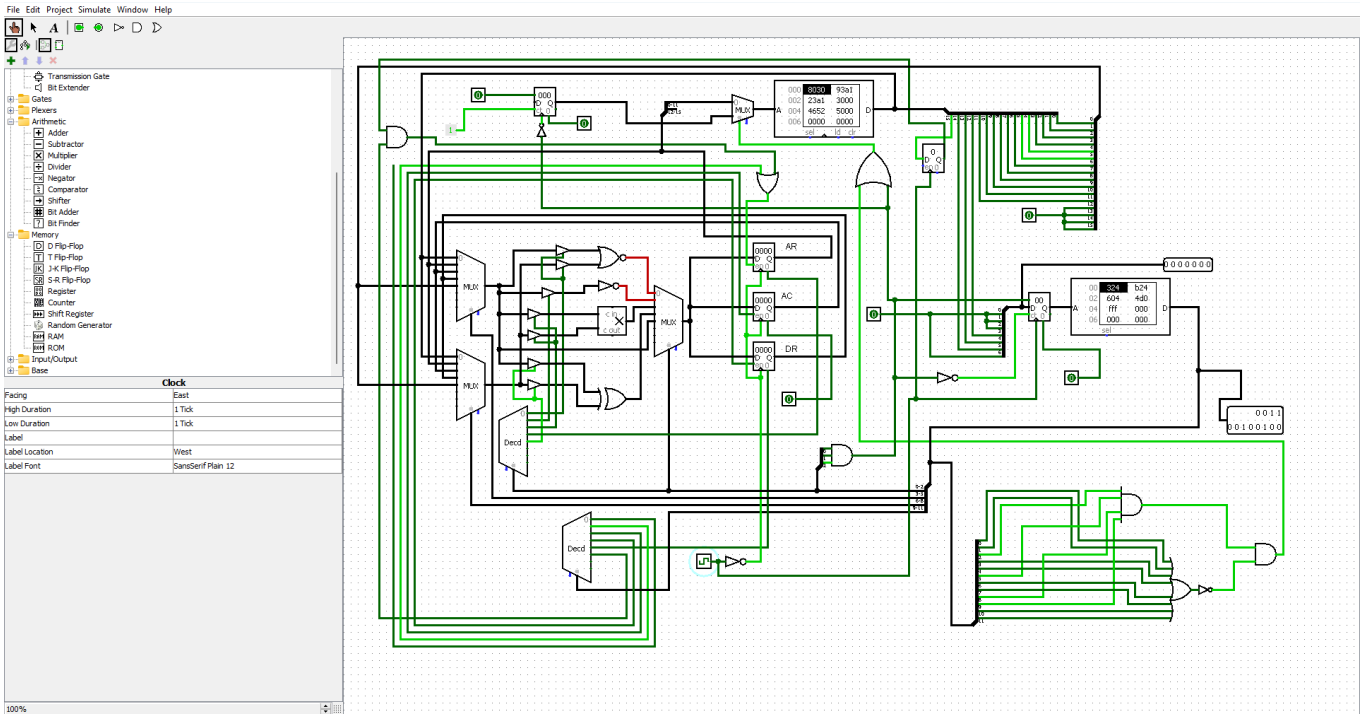
Source bits:-

A(3-5), A(6-8)	Source
000	Memory
001	AR
010	AC
011	DR
100	Memory(0-12)

Destination bits:-

A(9-11)	Destination
000	NOP
001	AR
010	AC
011	DR
100	CLRDR
101	AR (For INDR)

Screenshots:-


File Edit Project Simulate Window Help
Transmission Gate
Bit Extender
Gates
Plexers
Arithmetic
Adder
Subtractor
Multiplier
Divider
Negator
Comparator
Shifter
Bit Adder
Bit Finder
Memory
D Flip-Flop
T Flip-Flop
J-K Flip-Flop
S-R Flip-Flop
Register
Counter
Shift Register
Random Generator
RAM
ROM
Input/Output
Base
Clock
Facing East
High Duration 1 Tick
Low Duration 1 Tick
Label
Label Location West
Label Font SansSerif Plain 12
100%
AR
AC
DR
MUX
Decd